The future TPCs' signal processing, compression and read-out

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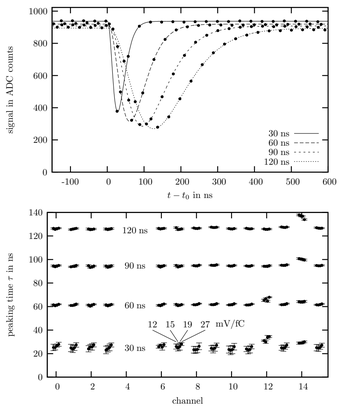
Analog signal processing

The analog signal processing is based on a programmable charge sensitive shaping amplifier. Besides converting the charge signal into a voltage signal that can be sampled by an ADC it also shapes the signal. This step is essential, as raw TPC signals have very high bandwidth, extending typically Nyquist frequencies by large factors.



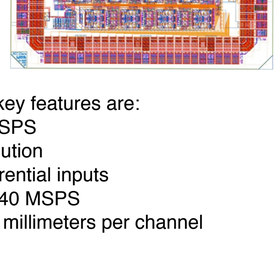
The amplifier circuit was developed at CERN and is highly programmable. Its main features are:

- programmable peaking time (30, 60, 90 or 120 ns)
- programmable amplification gain (12, 15, 19 or 27 mV/fC)
- programmable polarity (allowing it to be used for both wire chambers and GEMs)

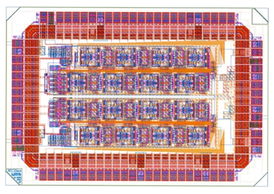
Measurements of a 16 channel silicon prototype are shown here for different settings indicating the circuits performance.

Analog to digital conversion

A CERN custom developed high performance, low power pipelined ADC is used to digitise the signal. Depicted here is a layout of the ADC as it is submitted to MOSIS. A first silicon prototype will soon be available, allowing for a full characterisation.



courtesy of H. Franca-Santos



courtesy of H. Franca-Santos

The estimated key features are:

- up to 40 MSPS
- 10 bit resolution
- 2 Vpp differential inputs
- 33 mW @ 40 MSPS
- 0.7 square millimeters per channel

Digital signal conditioning

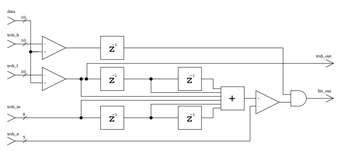
Digital signal conditioning is essential. But the only reason to do it on-chip is the necessity to perform zero-suppression. Now, a typical signal from a TPC is superimposed with various systematic and non-systemic "noise". Examples being the high current jump upon a trigger signal that triggers all detectors to start processing or signal induced by opening the gating grid in wire chambers. Further the detector response function can have parts that extend over long periodes (e.g. "ion tails"). Lastly the chip itself is subject to manufacturing process uncertainties and system-level variations (e.g. temperature) leading to varying operation points (i.e. baseline values).
The digital signal conditioning circuit tackles all the mentioned complications by:

- correcting the baseline (BC1) by
  - subtracting a trigger related pattern
  - subtracting a preprogrammed baseline value
  - subtracting a self-calculated baseline value
- using a fourth order digital filter (DS) to
  - remove long tails
  - shape the signal
- remove still remaining baseline shifts (BC2)

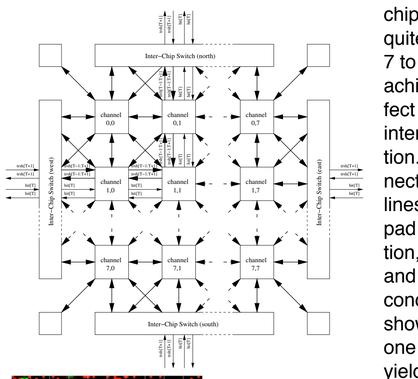
This way of processing the signal is utilised in the ALTRO chip (used for the ALCIE-TPC) and showed to preserve its relevant characteristics (charge and time information) while allowing the zero-suppression to cut away redundant signal very efficiently.

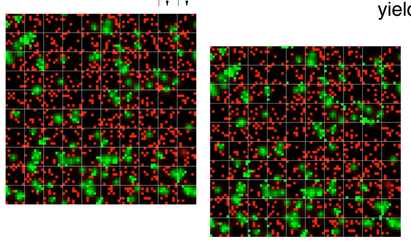
Three-dimensional zero-suppression

The S-ALTRO chip features a three-dimensional approach to zero-suppression. This allows for a) a much better noise rejection, while b) keeping the important features of the signal. I.e. it reduces the errors of first and second kind, in other words the errors of accepting of noise and rejection of real signal.
The method foreseen is a double thresholding scheme: To be detected as a pulse, a signal has to have a center pad above a "high threshold" and more then a "number threshold" of adjacent pads above a "low threshold" (compare figure). Surrounding pads are those within the cube of 3x3x3 pixels in spacial and time coordinates.



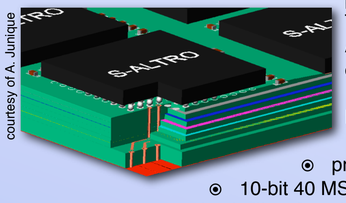
As a single chip "only" hosts 64 channels, the ratio of inner channels to those on the chip boundary is quite bad (28 to 36 or 7 to 9). In order to achieve the desired effect one has to introduce inter-chip communication. As this interconnection requires 2 lines per border pad and direction, induced noise and pin-count are of concern. But simulation shows that transmitting only one signal per border yields to similar good results. This is depicted in the figures on the left for a grid of 10x10 chips. The left picture shows the case of full interconnection, while the right shows, the "border-only" type.





The "S-ALTRO" chip

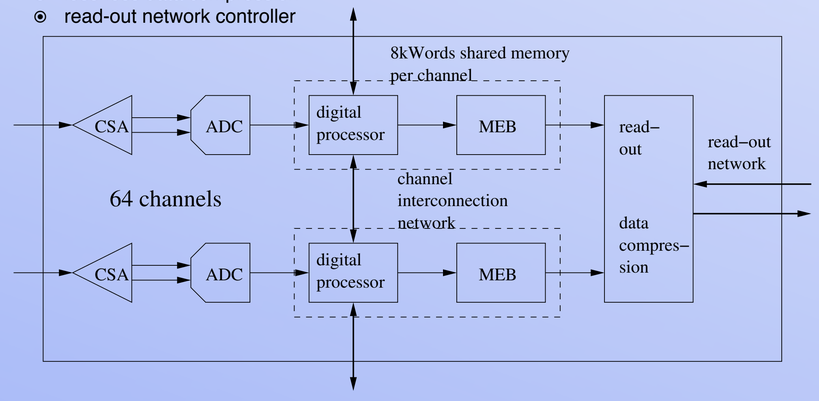
Future experiments aim at very high spacial resolution, requiring pad sizes of the order of a few square millimeters (state-the-art is 4 times 7.5 square millimeters for the ALICE-TPC). Besides leading to an increasing data rate, has this severe implications on real-estate and power consumption/cooling. Especially the latter points rule out the existing chipset based solutions. A single chip including the analog and digital signal processing is needed to fulfill the required packing density. This led to the development of a new chip – working title "S-ALTRO". The chip is supposed to be mounted directly on the endplate, as depicted.



courtesy of A. Junique

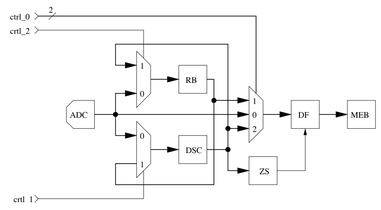
Its main features are:

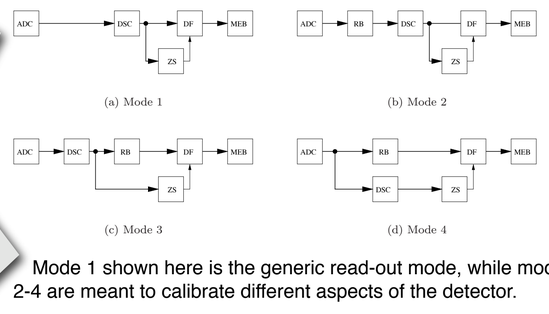
- 64 complete channels
- programmable charge sensitive amplifier
- 10-bit 40 MSPS ADCs
- a ring buffer, that allows to position the acquisition window freely with respect to the trigger (as in modern oscilloscopes) to allow to acquire data before the trigger
- 8k multi acquisition memory per channel (dynamically allocated)
- forth order digital signal processor
- three dimensional zero-suppression
- loss-less data compression
- read-out network controller



Dynamic data path

Besides the normal operation of a TPC of gathering physics data, the read-out has also to deal with the specific needs of detector calibration. The most basic way to do this is to disable the zero-suppression and digital data processing and to save the raw data. Albeit being a solution it is certainly not elegant, as it asks for a huge data volume. Typical calibrations only need channels, which have a pulse inside. This is the selective read-out. Sometimes one wants to investigate the signal before the trigger was issued. The S-ALTRO features a dynamic data path routing as depicted to benefit the most form its building blocks and to cope with the mentioned needs.



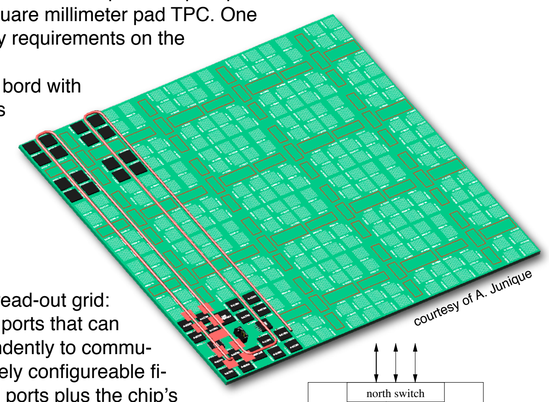


Mode 1 shown here is the generic read-out mode, while modes 2-4 are meant to calibrate different aspects of the detector.

Read-out Network

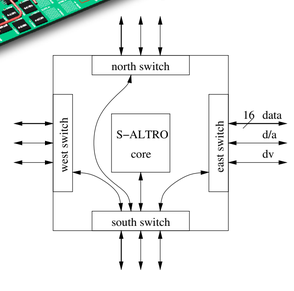
The picture shows a possible packplane design for a 4 square millimeter pad TPC. One can infer that the key requirements on the read-out network are:

- fault tolerance (a bord with hundreds of chips may not fail because of a single chip)
- low power consumption
- little noise induction
- no extra components



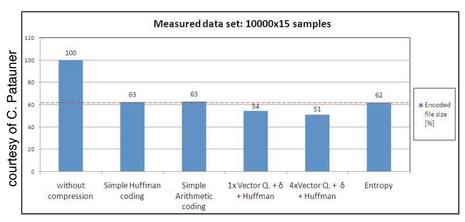
courtesy of A. Junique

The solution proposed is a read-out grid: Each chip has four external ports that can be used completely independently to communicate. This is done by a freely configureable five-port switch (four external ports plus the chip's core).
The developed protocol allows any kind of data routing using any topology of the read-out network. It is steered by the read-out controller nodes to minimize the intelligence needed to be included on-chip.
Clearly, a grid is pretty redundant, such that, combined with a dynamic routing, single chip failures will not have an impact on the system level. Even more, depending on the read-out nodes intelligence, it can choose data paths such that the overall read-out time is minimised (evacuation theory).



Loss-less data compression

It turns out, that even after the digital signal conditioner and the zero-suppression did their job and truncated the signal to its essential part (the well formed pulses), the signal it is still redundant. This is due to the nature of the signal generation process and its underlying statistics (pulse shape, height and time distribution).
As datavolume is directly related to read-out time and dead time, one cannot afford such redundancy. On the other hand, the extra logic needed to compress the data cannot be afforded on a channel basis. It is therefore put directly in front of the read-out controller and serves the whole chip at once.
Different methods of loss-less data compression are studied to compress the signal. The results for real data as acquired by the ALICE-TPC are shown here. Roughly 50% is redundancy.



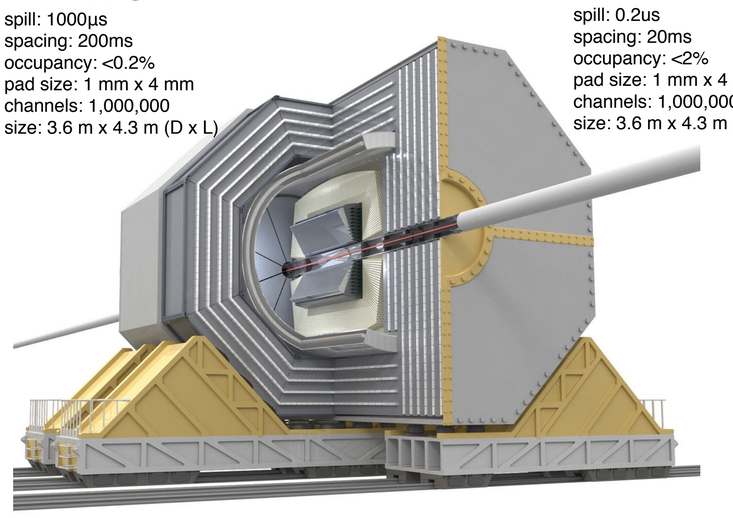
courtesy of C. Patauner

Target applications' characteristics

ILC or CLIC

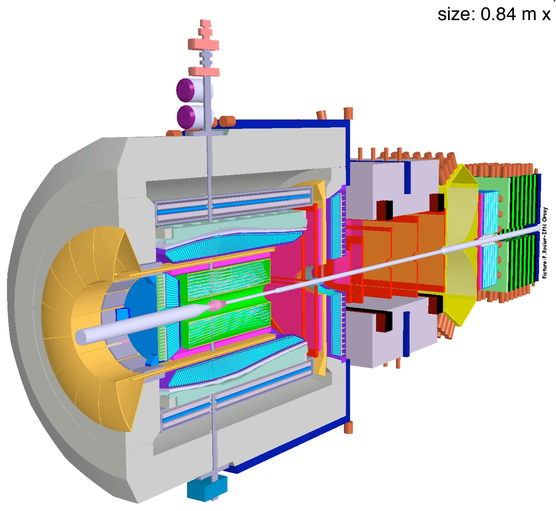
spill: 1000µs
spacing: 200ms
occupancy: <0.2%
pad size: 1 mm x 4 mm
channels: 1,000,000
size: 3.6 m x 4.3 m (D x L)

spill: 0.2us
spacing: 20ms
occupancy: <2%
pad size: 1 mm x 4 mm
channels: 1,000,000
size: 3.6 m x 4.3 m (D x L)



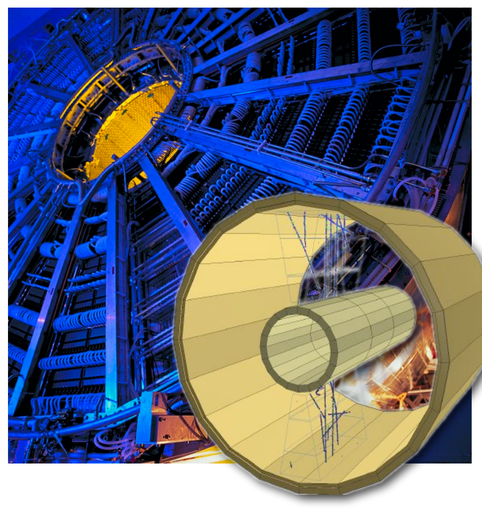
PANDA

interaction rate: 20 MHz
occupancy: 10%
pad size: 2 mm x 2 mm
channels: 100,000
size: 0.84 m x 1.5 m (D x L)



ALICE

event-rate: 1kHz
occupancy: <10%
pad size: 7.5 mm x 4 mm
channels: 500,000
size: 5 m x 5 m (D x L)



cosmic tracks in the ALICE-TPC