EIROforum School of Instrumentation CERN, 11-15 May 2009

Quality control for electronics exposed to Radiation in the ATLAS experiment at CERN and in ITER

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M.Dentan ESI 2009 Quality Control for Electronics Exposed to Radiations in ATLAS and in ITER **1/38** china eu india ianan korea russia usa

Outline

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	- •Radiation hardness assurance

Radiation issues

2 families: cumulated effects, and instantaneous (single event effects)

Cumulated effects

- • Total Ionizing Dose (TID)
	- ¾Energy deposited in the electronics by radiation in the form of ionisation.
	- ¾Unit: Gray (Gy), $1 \text{ Gy} = 100 \text{ rad} = 1 \text{ joule } k\text{ Gy}$.
	- \blacktriangleright Affects all electronics devices
- • Non-Ionizing Energy Loss (NIEL)
	- ¾Displacement damage, mainly due to hadrons (n, p, π , ...)
	- \blacktriangleright Unit : particles / cm**²**
	- \blacktriangleright Energy dependent \rightarrow normalized to 1 MeV neutrons equivalent / cm².
	- \blacktriangleright Bipolar JT, LEDs, lasers, CCDs, optocouplers, photo-BJTs,… are affected
	- \blacktriangleright CMOS are not affected (majority carriers)

Radiation issues (2)

Single Event Effects (SEE)

- • Destructive effects:
	- ¾SEL (Single Event Latch-up)
	- \blacktriangleright SEB (Single Event Burnout
	- \blacktriangleright SEGR (Single Event Gate Rupture
	- ¾…

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- Transient effects: upsets
	- \triangleright SEU : Single Event Upset (logic)
	- \blacktriangleright SET : Single Event Transient (linear)
- • SEEs are *instantaneous* effect
	- \blacktriangleright May occur just after the beam is switched on

Radiation issues : TID (total ionizing dose)

• Mechanism : charge trapping in oxides and interfaces => threshold voltage (Vt) shift, leakage current, noise, … Example: leakage current and Vt shift induced in NMOS by total dose

Radiation issues : NIEL (Non-Ionizing Energy Loss)

- • Mechanism : bulk defects in semiconductors \Rightarrow decrease of BJT gain β , noise, ...
- •Cumulated damage => delayed effect

Example: dependance of BJT gain decrease on base thickness

Radiation issues : SEE (Single Event Effects)

Contact de Drain

Power MOSFET (VDMOS) = 15000 cells in parallel Triggering of the parasitic bipolar transistor \longrightarrow Burnout

LHC experiments

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This information is private

confidential.

LHC experiment: ATLAS

- International collaboration, about 1900 people from ~150 institutions from 34 partner countries (incl. EU, US, Japan, Russia, Israel, Brazil, …)
- 300 millions Euros among which 75 millions Euros for electronics
- One of the two largest detector of the LHC experiments
- 15 main systems, each of them containing electronics

Radiation constraints (10 years)

Simulations tools : FLUKA and G3-CALOR

Front-end electronics (readout and pre-treatment) and some of the power supplies cannot be installed remotly (away from radiation), and cannot be shielded (it must be as transparent as possible to avoid shadows or parasitic images on particle detectors)

Man

ATLAS policy on radiation tolerant electronics

- • Goal: reliability of the experiment with respect to radiation
	- - Estimated lifetime of components must cover foreseen lifetime of LHC experiments, or at least a large fraction of it.
	- -Rates of transient or destructive SEE must be acceptable.
	- -Safety systems must remain always functionnal.
- • Mandatory for each sub-system of the experiment
	- - Particular attention was paid to the identification of critical elements and to their possible failure modes.
- • Coherent approach
	- Same rules for every system
	- Based on recognized test methods
		- -E.g. US-DOD MIL-STD-883E ; ESA SCC basic spec. No 22900 and 25100
	- Simple, efficient and cost-effective

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Main procedure

Content:

- **Strategy for electronics procurement (ASICs, COTS)**
- **Radiation Tolerance Criteria**
- **Radiation Test Methods**
- **Lists of radiation facilities**
- **Standard test report form**

• **(…)**

Organisation

Tutorial course

-**To establish a basic knowledge on radiation effects on electronics**

-**Part 1 : Radiation effects on electronic components**

- ¾Radiation effects on materials (semiconductors, insulators, etc.)
- \blacktriangleright Radiation units
- \blacktriangleright Radiation effects on electronic devices

Part 2 : Radiation effects on electronic circuits

- ¾Cumulated radiation effects on digital and analog circuits
- \triangleright Single event effects on digital and analogue circuits
- ¾Examples of mitigation technics
- - **Course given in 2000 to the LHC partners at CERN** and to several ATLAS Partner Institutes

-**Updated version given in 2006 at JET to EFDA Associations :**

- ¾http://www.jet.efda.org/seminars/2006/060323dentan.pdf (part 1)
- \blacktriangleright http://www.jet.efda.org/seminars/2006/060720dentan.pdf (part 2)

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Radiation Tolerance Criteria

TRT

LAR

TILE

MUON

Table of raw simulated radiation levels

Table of safety factors

SYSTEM SUB-SYSTEM

ATLAS electronics

*** ASIC = Application Specific Integrated Circuit**

ATLAS electronics (2)

Technologies used for rad-hard ASICs

¾ DMILL CMOS-NPN-PJFET SOI technology (radiation-hard)

- Developed by CEA and produced by ATMEL for LHC and other applications
- > 10 Mrads and > 3.10¹⁴ n/cm²; reduced SEE sensitivity

≥ 0.25 µm CMOS bulk technology (standard)

- •Thin gate oxide => almost no Vt shift
- Radiation tolerant layout (closed gate structure, etc.) => no leakage current
- > several 10 Mrads and > several 10¹⁴ n/cm² with radiation tolerant layout

Principle of closed gate structure

Procurement strategy

- • Whenever possible:
	- -Remove electronics from radiation and purchase standard electronics.
	- Otherwise, apply following strategy:
- • Radiation tolerant COTS:
	- 1. Determine **radiation level** in the application (tables of simulated radiation levels)
	- 2.Calculate the **Radiation Tolerance Criteria** (using ATLAS safety factors)
	- 3. **Pre-select** generic components (radiation tests)
	- 4.**Purchase** batches of pre-selected generic components
	- 5. **Qualify** batches of components (radiation tests)
		- *- Radiation tests can be made on individual components or on boards*
		- *- Special agreements with vendors may allow purchasing qualified batches only*
- • Radiation-hard ASICs:
	- 1.Determine the **radiation level** in the application
	- 2.Calculate the **Radiation Tolerance Criteria**
	- 3. **Select** a radiation hard technology (DMILL or CMOS 0.25 μm + rad-tol layout)
	- 4.**Develop** prototype ASIC and qualify the design (radiation test)
	- 5. **Qualify** batches of components (radiation tests)
	- 6. **Purchase** qualified batches

ATLAS standard radiation test methods

TID test method for qualification of batches of CMOS components

Radiation tests must be normalized:

- to be relevant ;
- to allow comparizons ;
- to allow predictions ;
- to allow sharing results.

Only components passing Radiation Tolerance Criteria with normalized tests were installed in ATLAS

- **RCT** = Radiation Tolerance Criteria (a)
- Alternatively, use appropriate safety factor and skip this step (b)

ATLAS standard radiation test methods (2)

NIEL test method for qualification of batches of components

(a) RCT = Radiation Tolerance Criteria

SEE test method for qualification of batches of components

(b) - 60 MeV < E < 200 MeV to seek soft SEEs -200 MeV < E < 500 MeV to seek hard or destructive SEEs

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Recommended irradiation sources for tests

- •• Radiation sources must be calibrated
- \bullet Radiation levels must be specified in normalized units

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Radiation Tolerant Components Database

- -Developed by ATLAS
- -Accessible on internet.
- - Standard test results recorded and shared by the four LHC experiments.
	- => savings, efficiency improvement

Only normalized test results were recorded in the database

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Example of result : ASIC « ABCD »

Technology: DMILL Function: front-end ASIC for ATLAS silicon detector

Separate TID, NIEL and SEE tests.

TID test on every production lot using X-ray machine

NIEL tests in two different facilities

(0.8 MeV neutrons from Prospero at CEA-Valduc, and TRIGA reactor neutrons at Univ. of Ljubljana), to distinguish thermal neutrons effects from standard NIEL effects.

SEE tests performed on batch samples with the SPS 24GeV protons/pions beam at CERN

ABCD chip (pixel silicon detectors) TID test results on power consumption

10 Mrads in 300 mn + annealing.

Blue: analog current. Red: digital current. After full annealing: ~ +10% on Idd

Example of result : small system « ELMB »

Technology: COTS Function: local monitoring

TID and SEU tests on 12 units using 60 MeV proton beam (CYCLONE, Louvain-La-Neuve, Belgium) Target : 1E11p/cm**²** & 140 Gy

SEU test results on ELMB parts, with equivalent cross section for every component

MIC 5203-5.0BM4 LDO Voltage Regulator NIEL tests on 12 units using 1MeV neutrons in Prospero **Dutput Voltage Change** (CEA Valduc, France) 3 Target : 5E12 n/cm**²** 0.05 ± 0.0 1 $nF+12$ 2 $nF+12$ $3.0F₂$ 4 NE+12 $5.0F + 12.$ B D F + 12 Fluence (n/cm2) Voltage change at the output of a "COTS" voltage regulator (bipolar technology => neutron sensitive)

Example of result : power supplies

Generally very sensitive to radiation.

Especially developed for LHC by industrial companies.

Batches of power devices tested separately (neutrons, SEGR, SEB) and selected according to the results.

Global acceptance criteria for power supplies includes :

- TID tests up to 140 Gy,
- NIEL tests up to 2.10**¹²** 1 MeV equivalent neutrons / cm**²**
- -SEE tests up to 1.10**¹¹** hadrons / cm**²** at energy > 20 MeV

First results were very disappointing. A lot of effort was required to achieve the required radiation tolerance.

Example of result : power supplies (cont.)

To reduce SEB cross section, devices are generally used at $Vds = 1/2$ to $1/3$ of nominal Vds

4 channels low voltage DC unit, irradiated with 250 MeV protons up to 2.10**¹¹** p / cm**²**

The main difficulties of power supplies developments were the SEGR or SEB sensitivity of power devices and the SEU sensitivity of the control part of the power unit.

Summary (1/2)

Radiation can corrupt, damage or destroy electronics. A course explaying these effects was given to ATLAS and the other LHC collaboration to build a common basic knowledge in this field.

ATLAS simulated radiation levels reach up to 1 MGy, 4.10**¹⁴** n/cm**²** (1MeV eq.) and 4.10**¹⁴** p/cm**²**.

Special electronics is needed to resist to these radiation levels:

- Rad-hard ASICs (DMILL rad-hard technology, or standard 0.25 μm CMOS + rad-tol layout) For low radiation constrainst locations:

- Qualified COTS (Components Of The Shelf) used with radiation-tolerant architecture

This electronics was developed and qualified on the basis of the **ATLAS Policy on Radiation Tolerant Electronics,** which specifies :

- -The procurement strategy for COTS and radiation-hard ASICs
- The applicable Radiation Tolerance Criteria
- The applicable Radiation Test Methods
- Etc.

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Appliyng this policy was essential to ensure the robustness of the electronics against the foreseen radiation constrainst and thus the reliability and safety of the whole experiment.

Standard test results were recorded in a databased shared by the four ATLAS experiments.

This information is private and confidential. © February 13, 2008 Each system was reviewed against radiation tolerance. Formal acceptance was mandatory before installation in ATLAS.

Summary (2/2)

The Future

LHC beams at full energy and reduced luminosity are scheduled automn 2009.

They will allow testing the robustness of the electronics against actual ATLAS radiation constrainst: SEU (immediately), then TID and NIEL (after cumulated irradiation).

The actual radiation levels will be measured using a large number of radiation sensors (electronic devices) installed in many locations of ATLAS. These measurements will allow correcting the simulated radiation levels and thus improving the predicted lifetimes and SEE rates of the electronics.

A close monitoring of the electronics will be performed during the 10 years of operation foreseen for ATLAS. Results will be compared to those obtained during qualification tests, and corrective actions will be decided if needed. Some of the electronics (inner detectors) will have to be replaced during that period.

The ITER Project

- • ITER is a joint international R&D project that aims to demonstrate scientific and technical feasibility of fusion power.
- • ITER Partners are China, India, E.U., Japan, Korea, Russian Federation, and U.S.A.

The ITER Tokamak

Example 25
 Example 26
 Example 26 Upper, equatorial, and lower ports

ITER Tokamak Building

Radiation Hardness Assurance

- • Radiation constraints in ITER – preliminary figures
	- **During operation, outside the vacuum vessel**, the simulated dose rate is around **2.5 mGy/s**. Assuming that the lethal dose for standard electronics is [~]**100 Gy**, this **corresponds to** ~ **100 shots of 400 seconds each**.
	- **During maintenance, outside the vacuum vessel**, the simulated dose rate can be as high as 3 mGy/h. This corresponds to **100 Gy in 3.8 years**.
	- **During maintenance, inside the vacuum vessel**, the simulated level is **several hundred Gy/h**, well above the lethal dose of standard electronics.

The ITER approach

- ITER is currently developing a policy inspired from the ATLAS approach.
- This policy will apply to any electronics exposed to radiation in ITER, including « visible » electronics (crates, etc.) and « hidden » electronics (in electromechanical systems such as motors, etc).
- - As for ATLAS, this policy should be coherent, based on recognized test methods, efficient and cost effective.
- Once developed, the implementation of this policy will require a substantial learning period in the ITER community.

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THANK YOU !

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