

Progress towards electron-beam feedback at the nanometre level, for linear colliders and FELs, at the KEK/ATF2

Feedback On Nanosecond Timescales (FONT)

Philip Burrows

Neven Blaskovic, Talitha Bromwich, Glenn Christian, Colin Perry,

Rebecca Ramjiawan

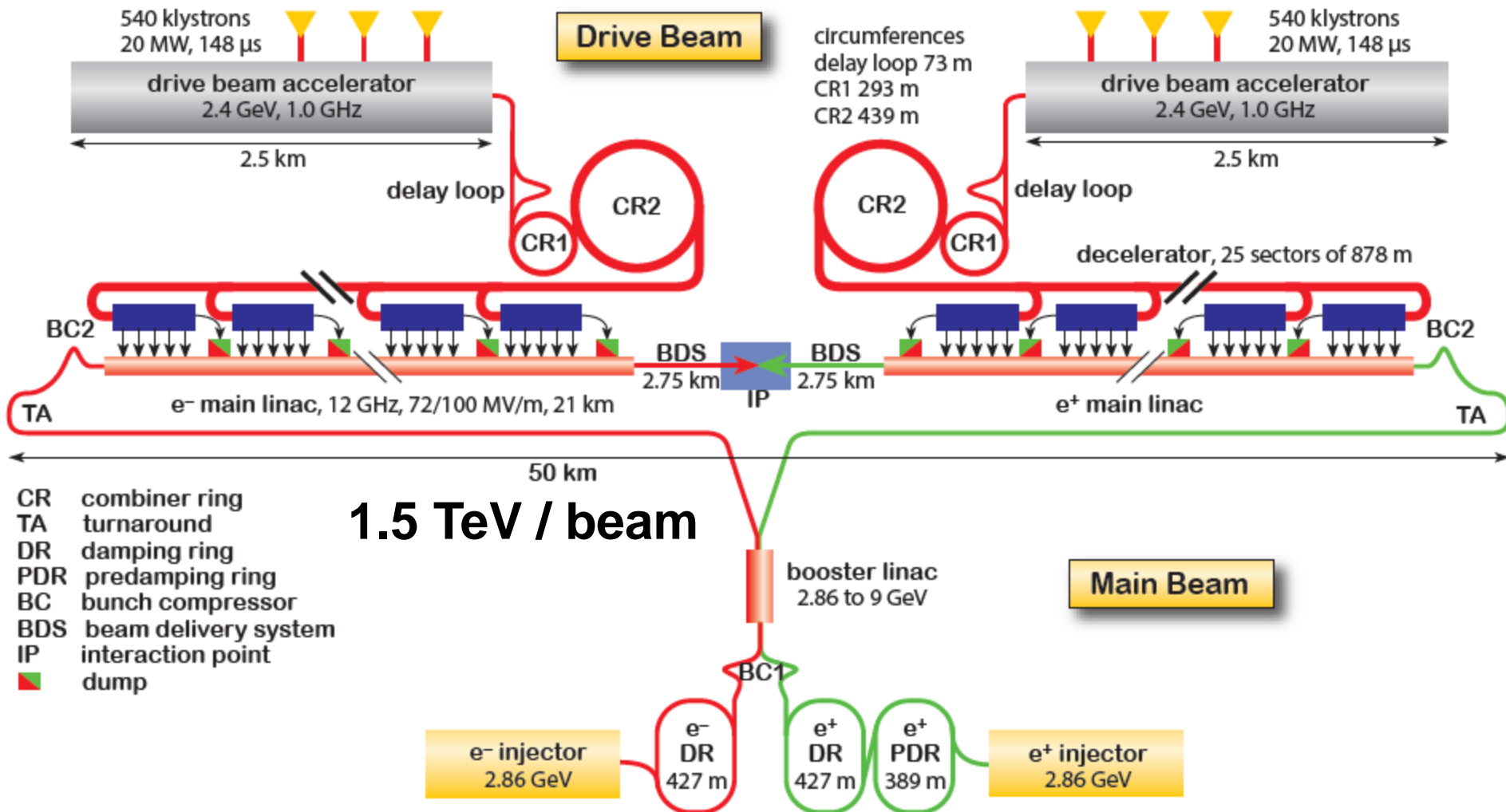
John Adams Institute, Oxford University

in collaboration with: KEK, KNU, LAL

Outline

- **ILC + CLIC luminosity requirements**
- **Interaction-point beam collision feedbacks**
- **Feedback system prototyping at ATF/ATF2**
- **Summary**

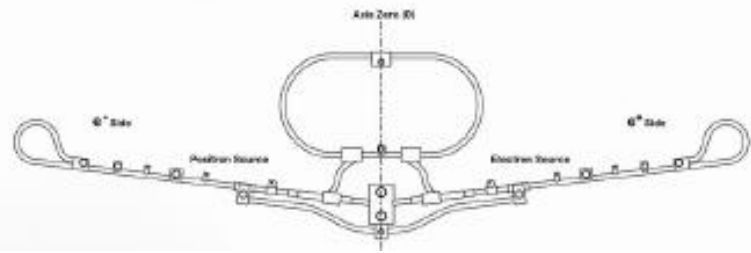
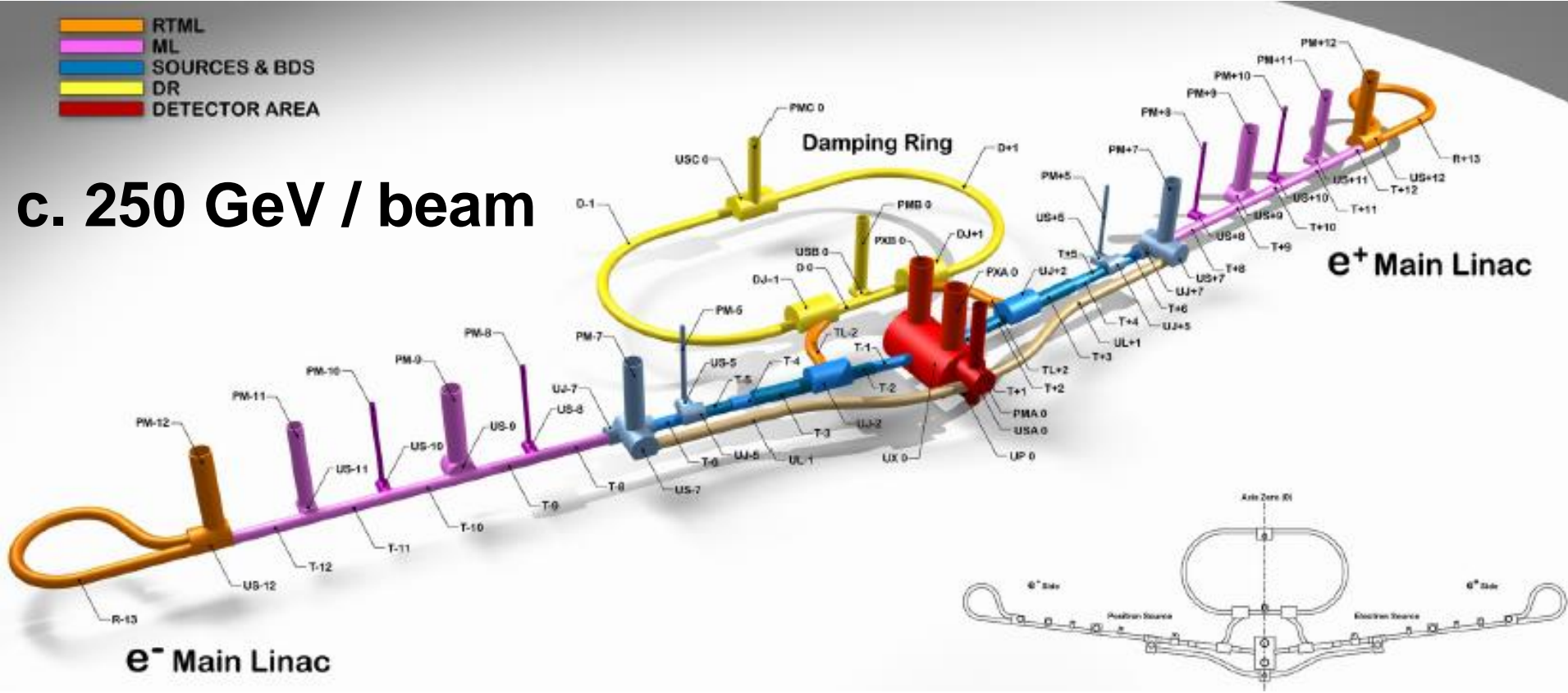
Compact Linear Collider (CLIC)



International Linear Collider (ILC)

- RTML
- ML
- SOURCES & BDS
- DR
- DETECTOR AREA

c. 250 GeV / beam



31 km

LC beam parameters

	ILC 500	CLIC 3 TeV	
Electrons/bunch	2	0.37	10**10
Bunches/train	1312	312	
Bunch separation	554	0.5	ns
Train length	727	0.156	us
Train repetition rate	5	50	Hz
Horizontal IP beam size	474	40	nm
Vertical IP beam size	6	1	nm
Longitudinal IP beam size	300	44	um
Luminosity	2	6	10**34

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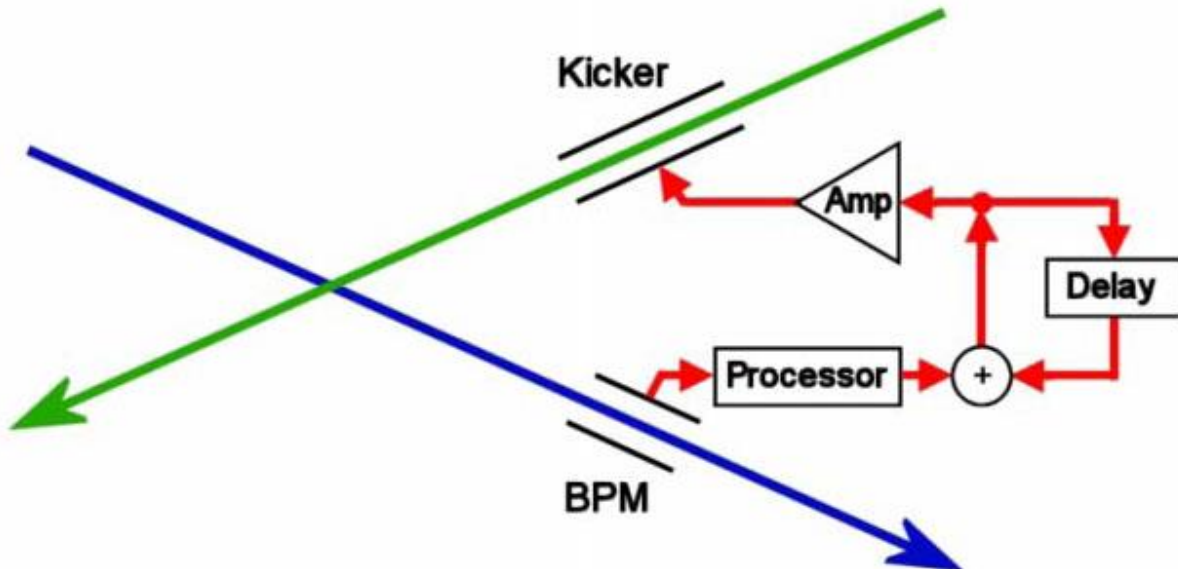
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LC IP beam feedback concept

Last line of defence
against relative
beam misalignment

Measure vertical
position of outgoing
beam and hence
beam-beam kick
angle

Use fast amplifier and
kicker to correct
vertical position of
beam incoming to IR



FONT – Feedback On Nanosecond Timescales:

Robert Apsimon, Neven Blaskovic Kraljevic, Douglas Bett, Ryan Bodenstein, Talitha Bromwich, Philip Burrows, Glenn Christian, Christine Clarke, Ben Constance, Michael Davis, Tony Hartin, Young Im Kim, Simon Jolly, Steve Molloy, Gavin Neson, Colin Perry, Rebecca Ramjiawan, Javier Resta Lopez, Christina Swinson

General considerations

Time structure of bunch train:

ILC (500 GeV): c. 1300 bunches w. c. 500 ns separation

CLIC (3 TeV): c. 300 bunches w. c. 0.5 ns separation

Feedback latency:

ILC: O(100ns) latency budget allows **digital** approach

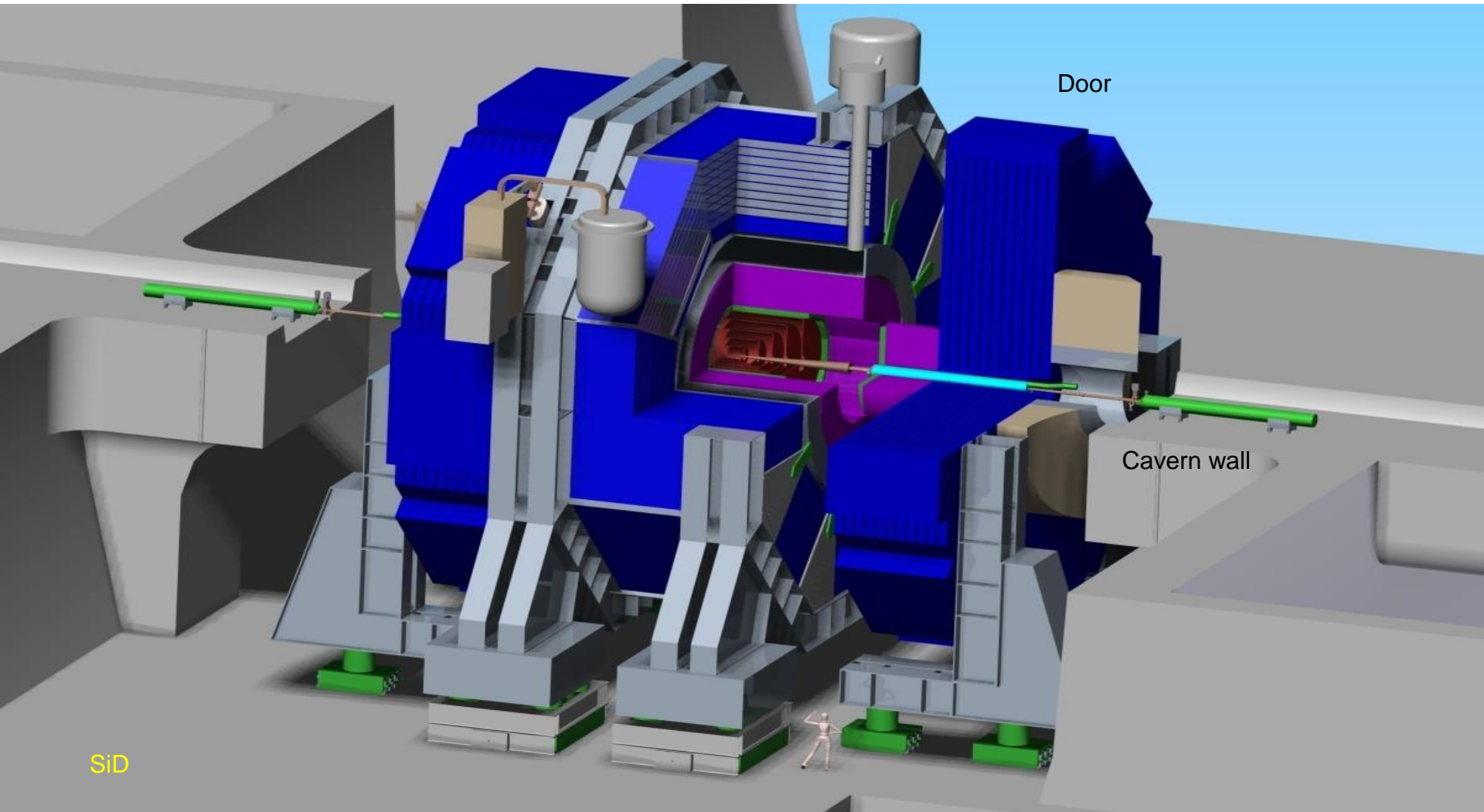
CLIC: O(10ns) latency requires **analogue** approach

Recall speed of light: $c = 30 \text{ cm / ns}$:

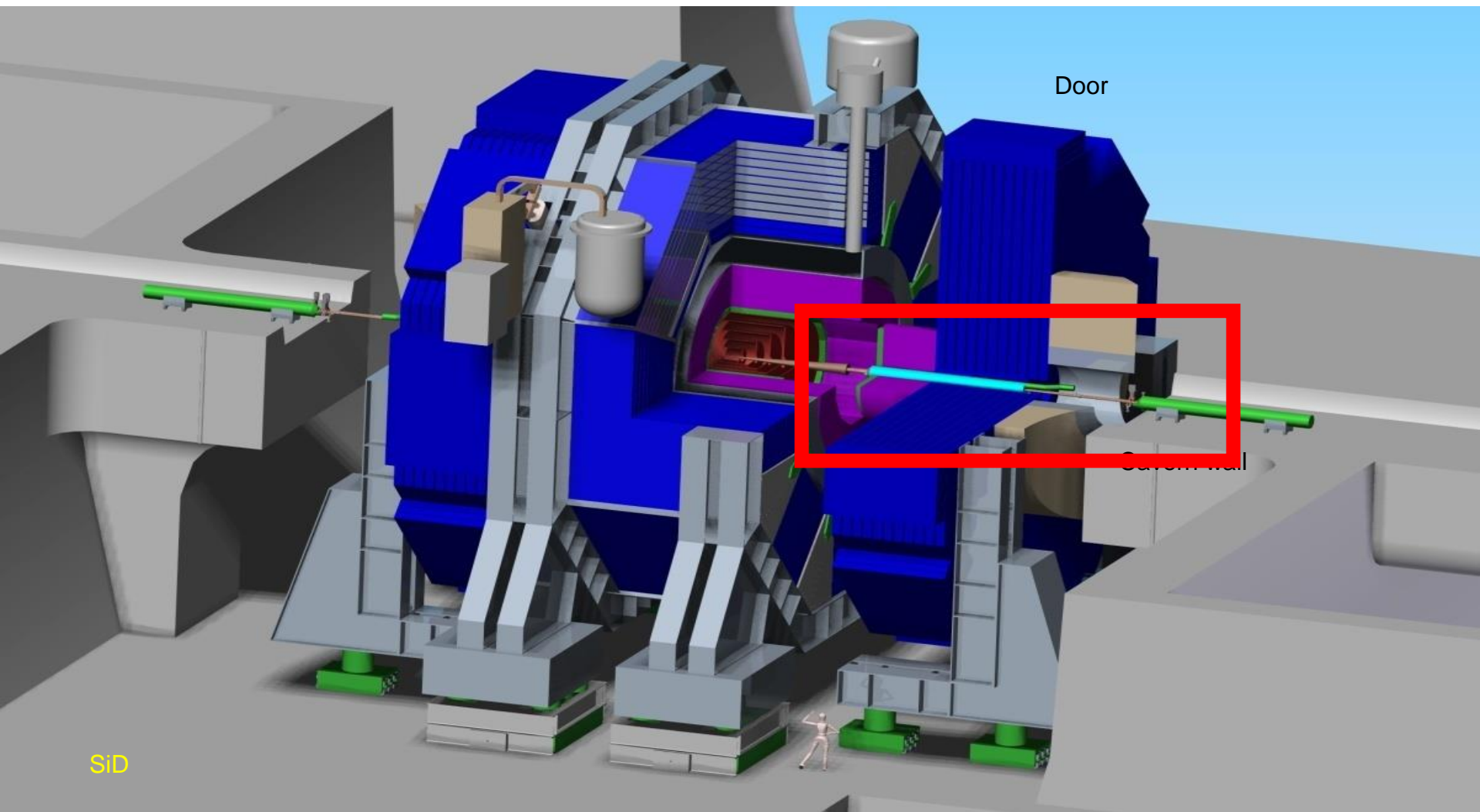
FB hardware should be close to IP (especially for CLIC!)

Two systems, one on each side of IP, allow for redundancy

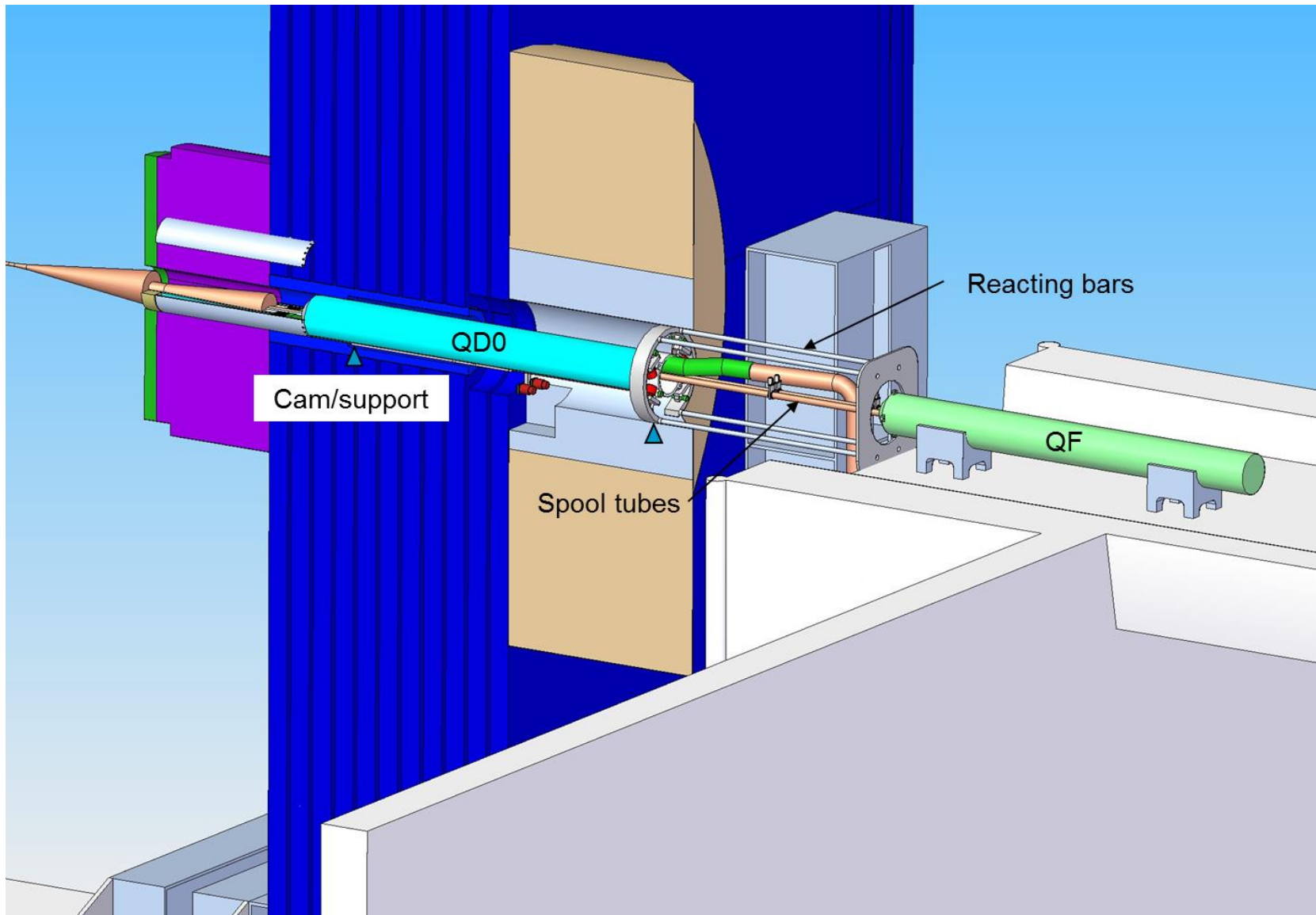
ILC IR: SiD for illustration



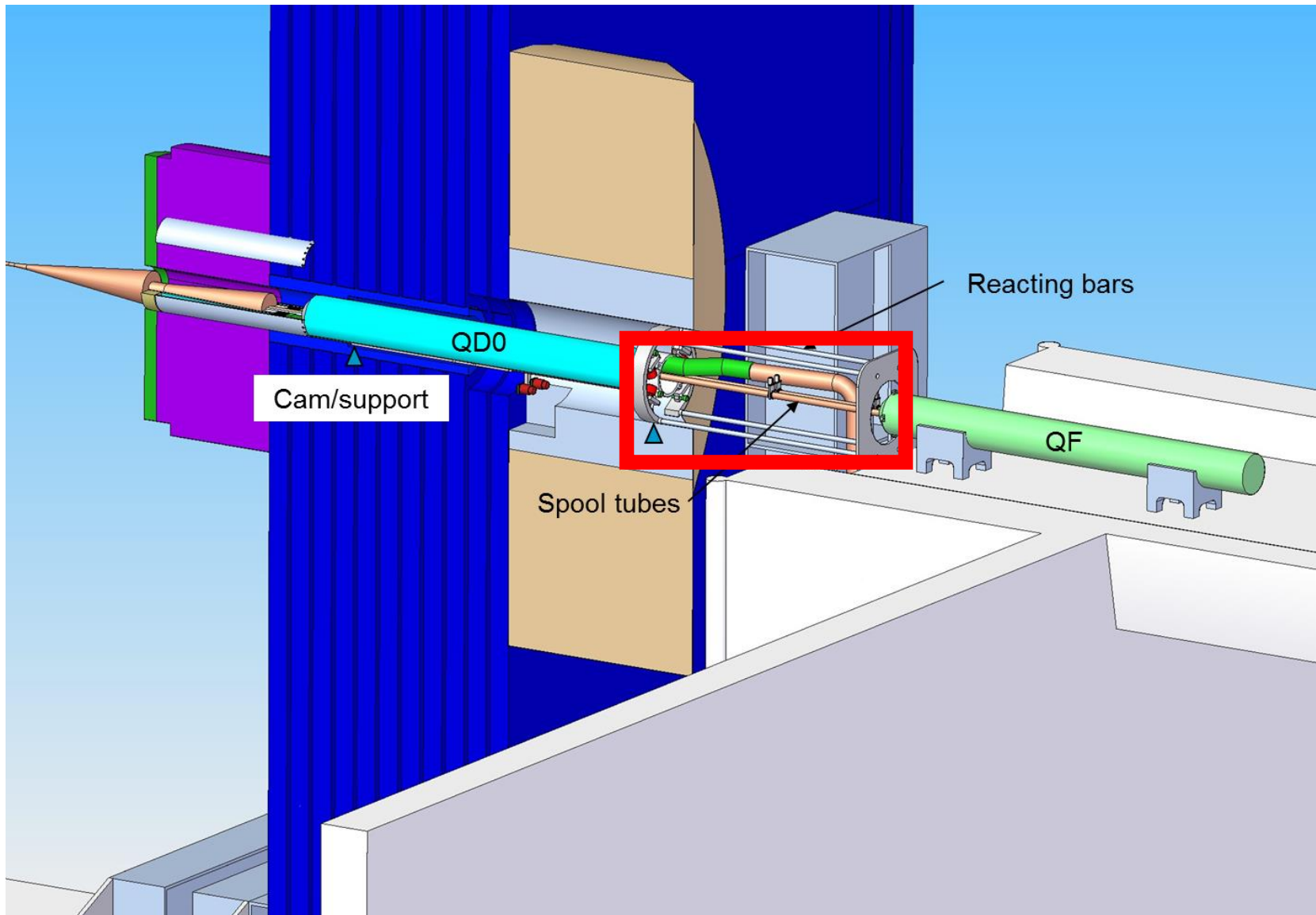
ILC IR: SiD for illustration



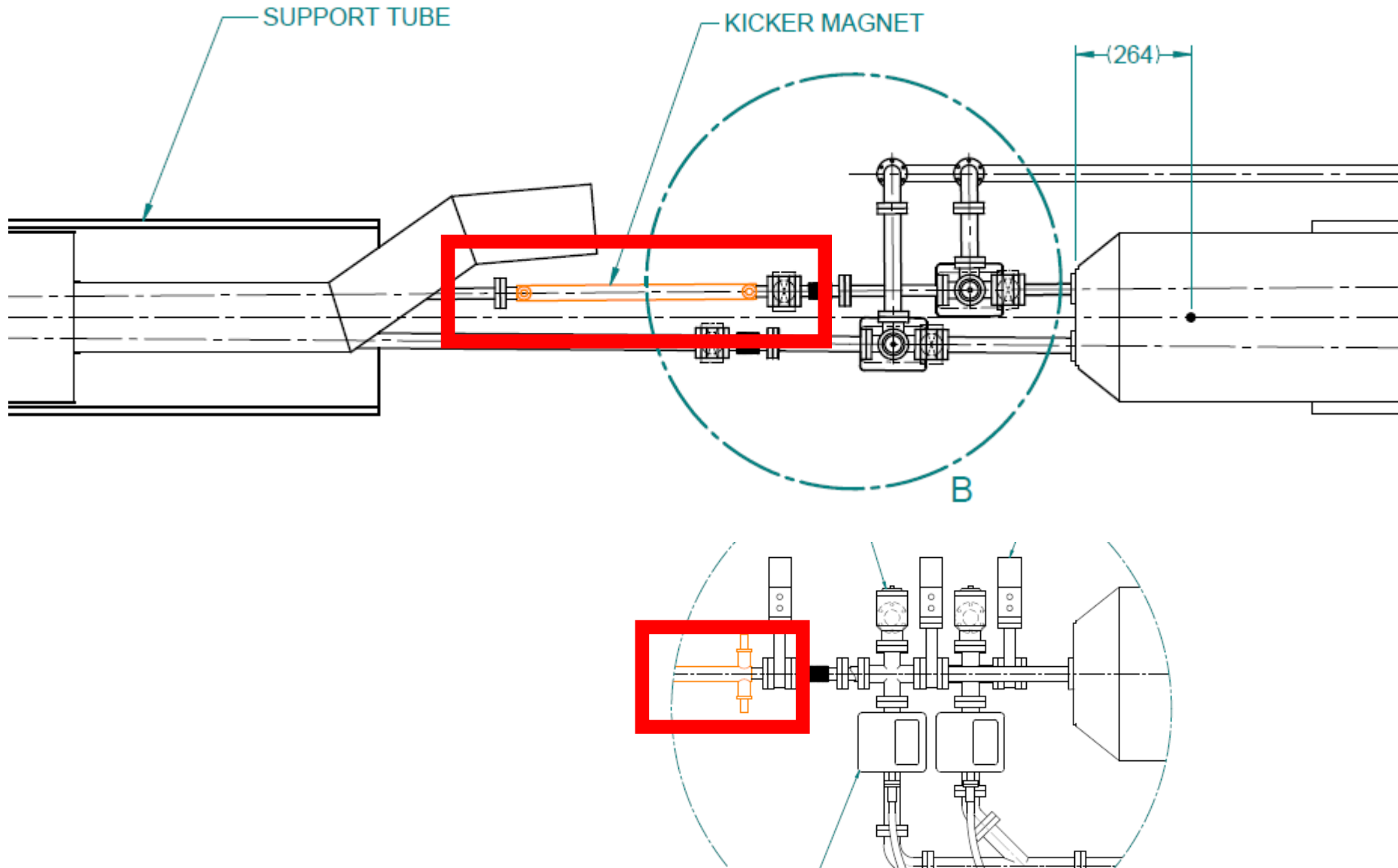
Final Doublet Region (SiD)



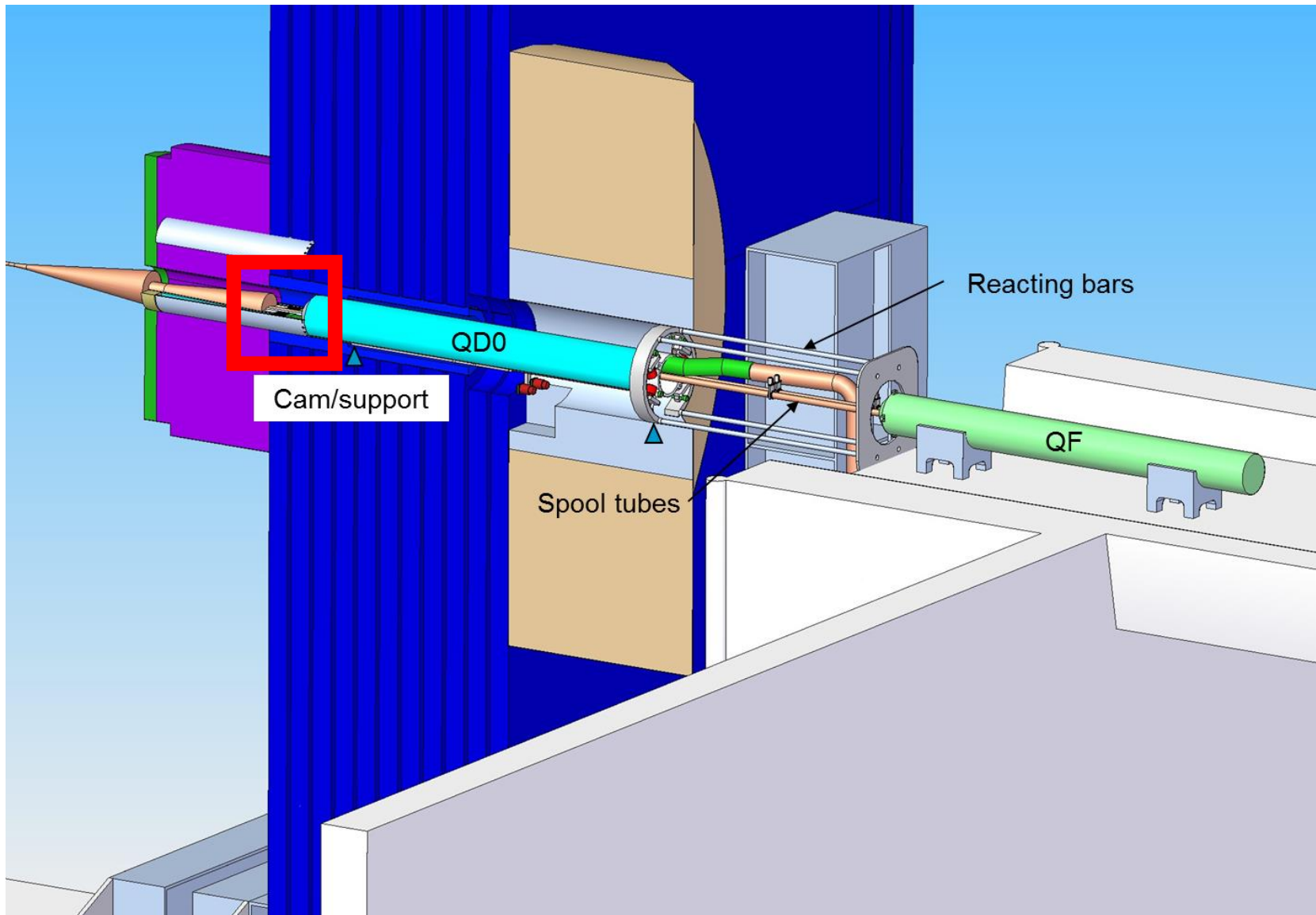
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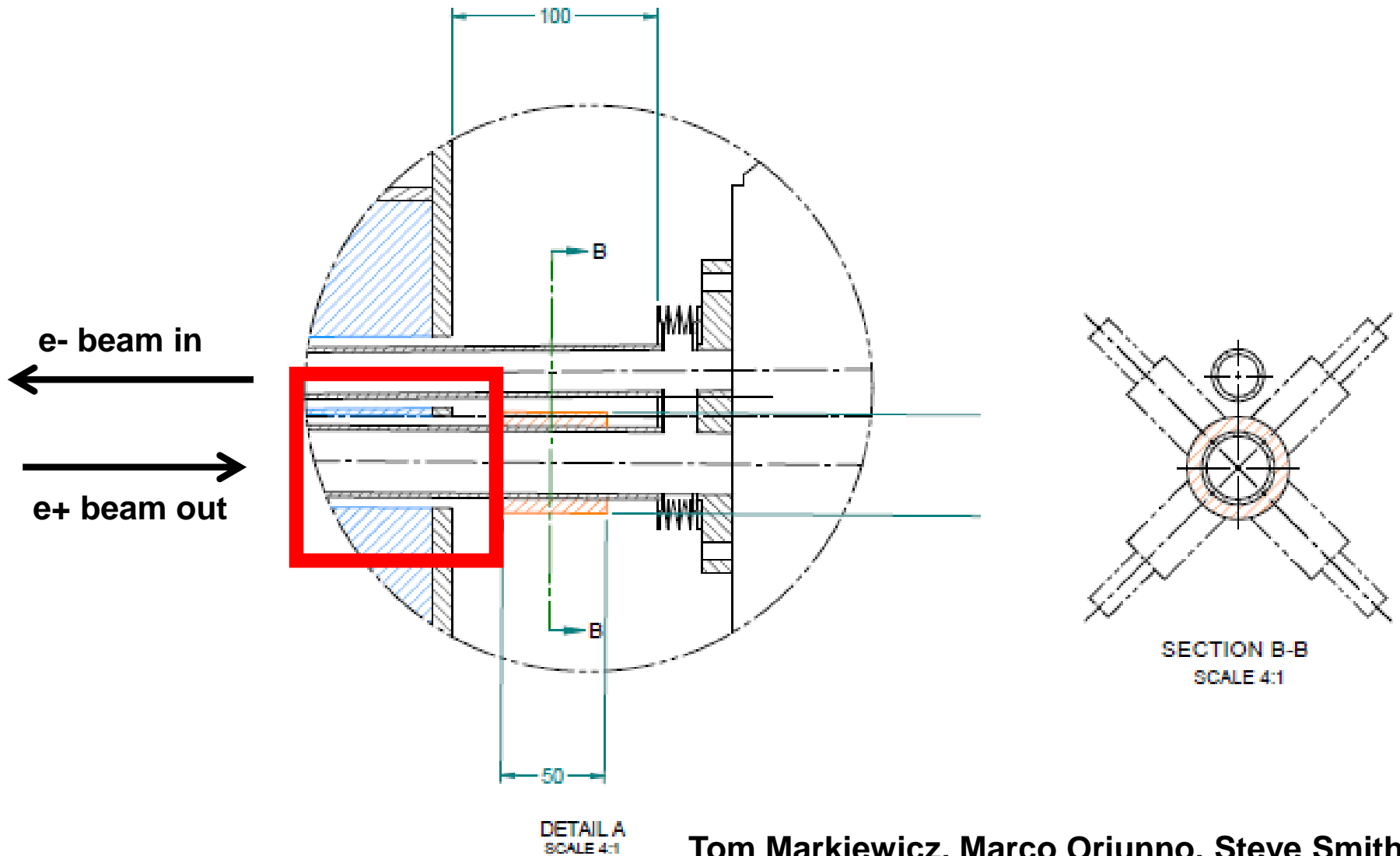
IP kicker detail (SiD)



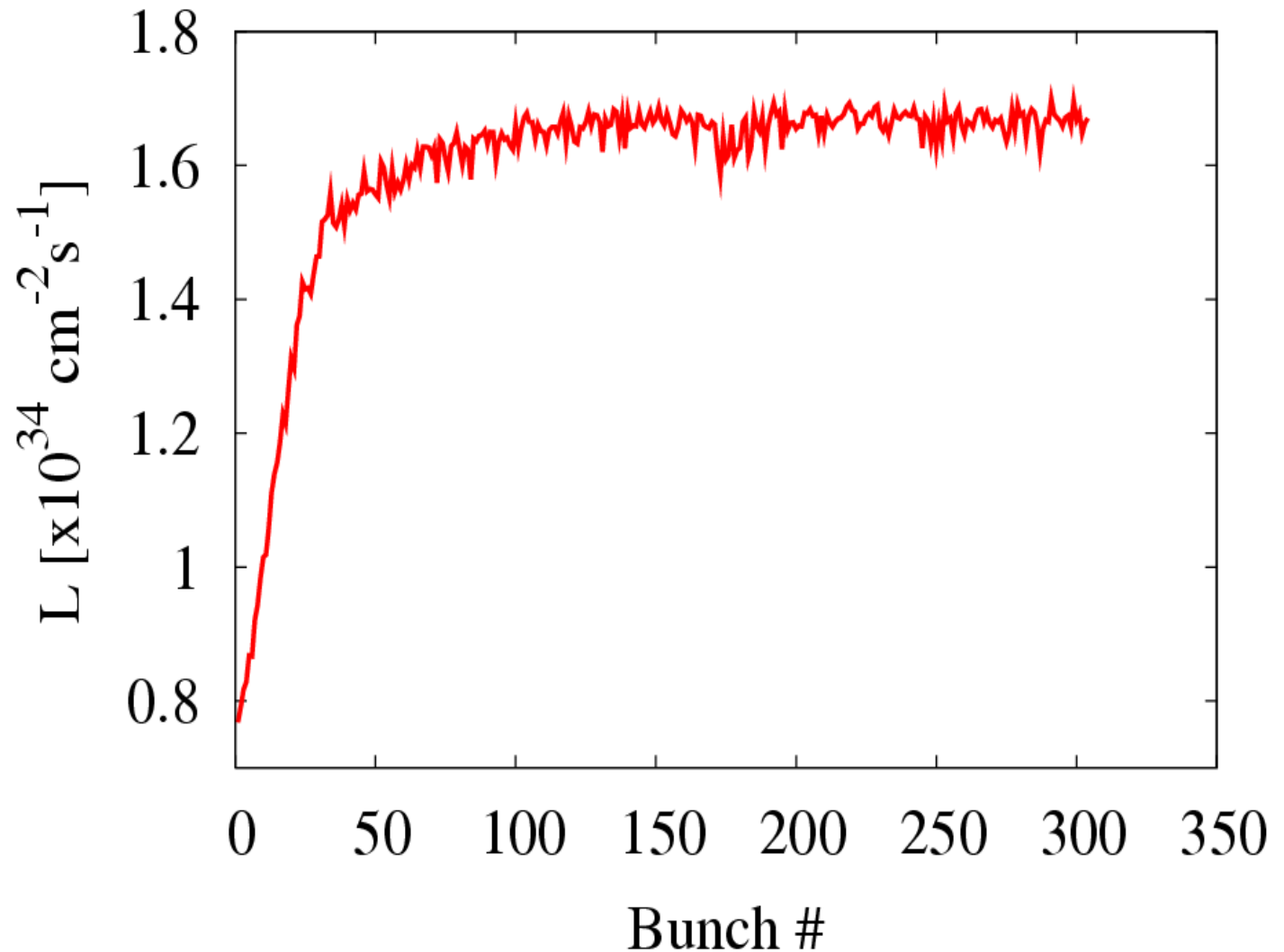
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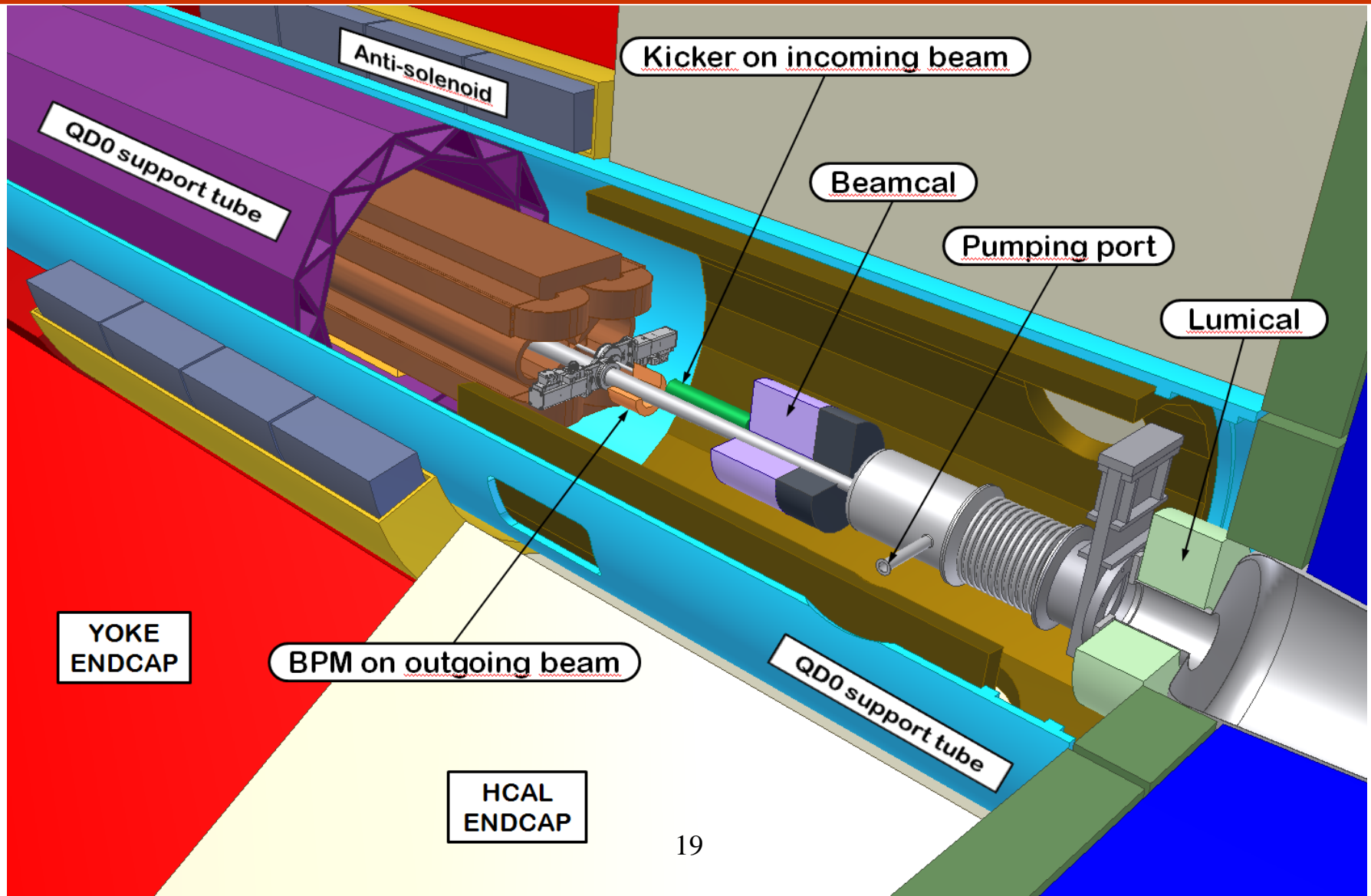
IP FB BPM detail (SiD)



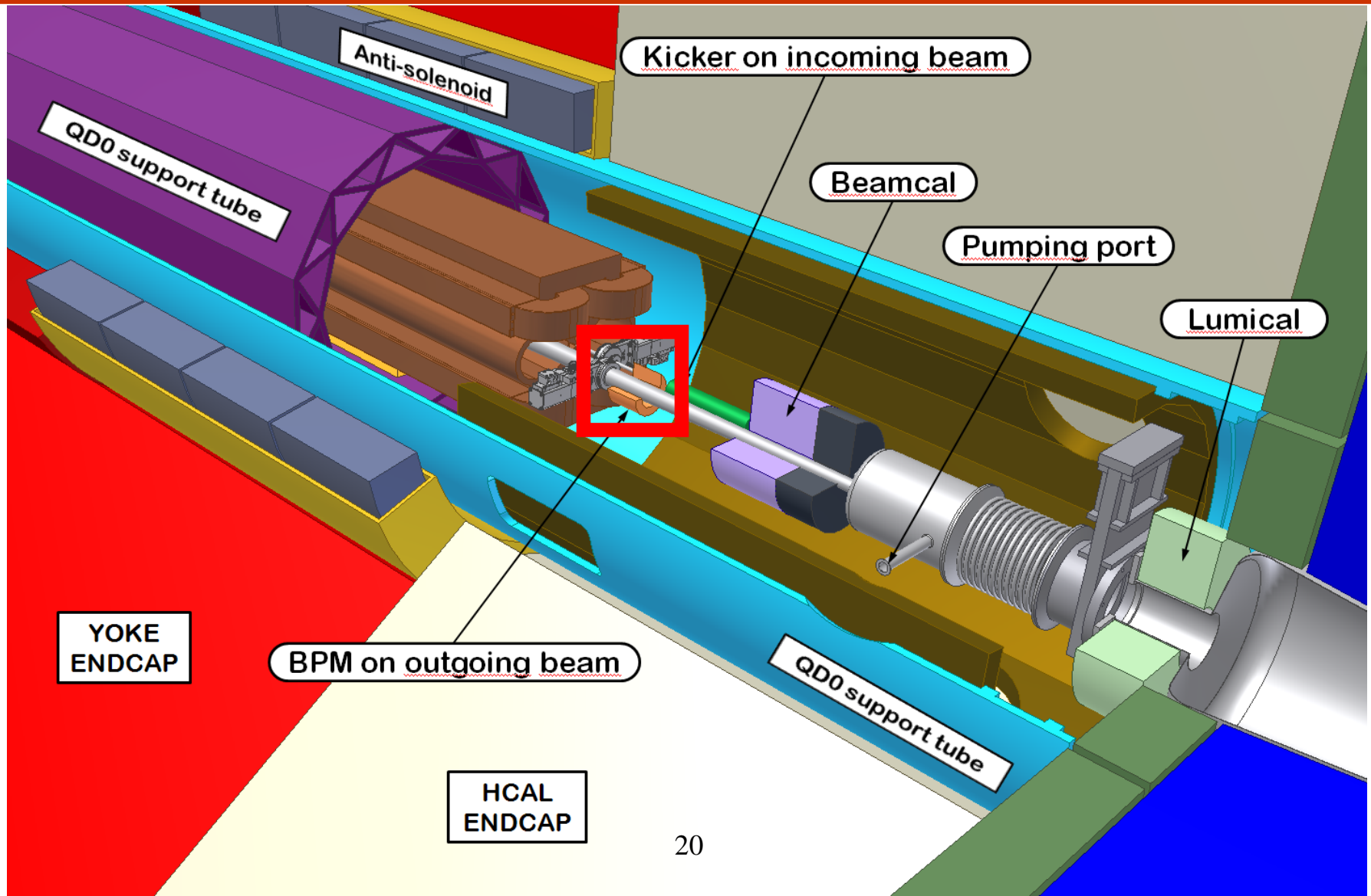
ILC IP FB performance (TDR)



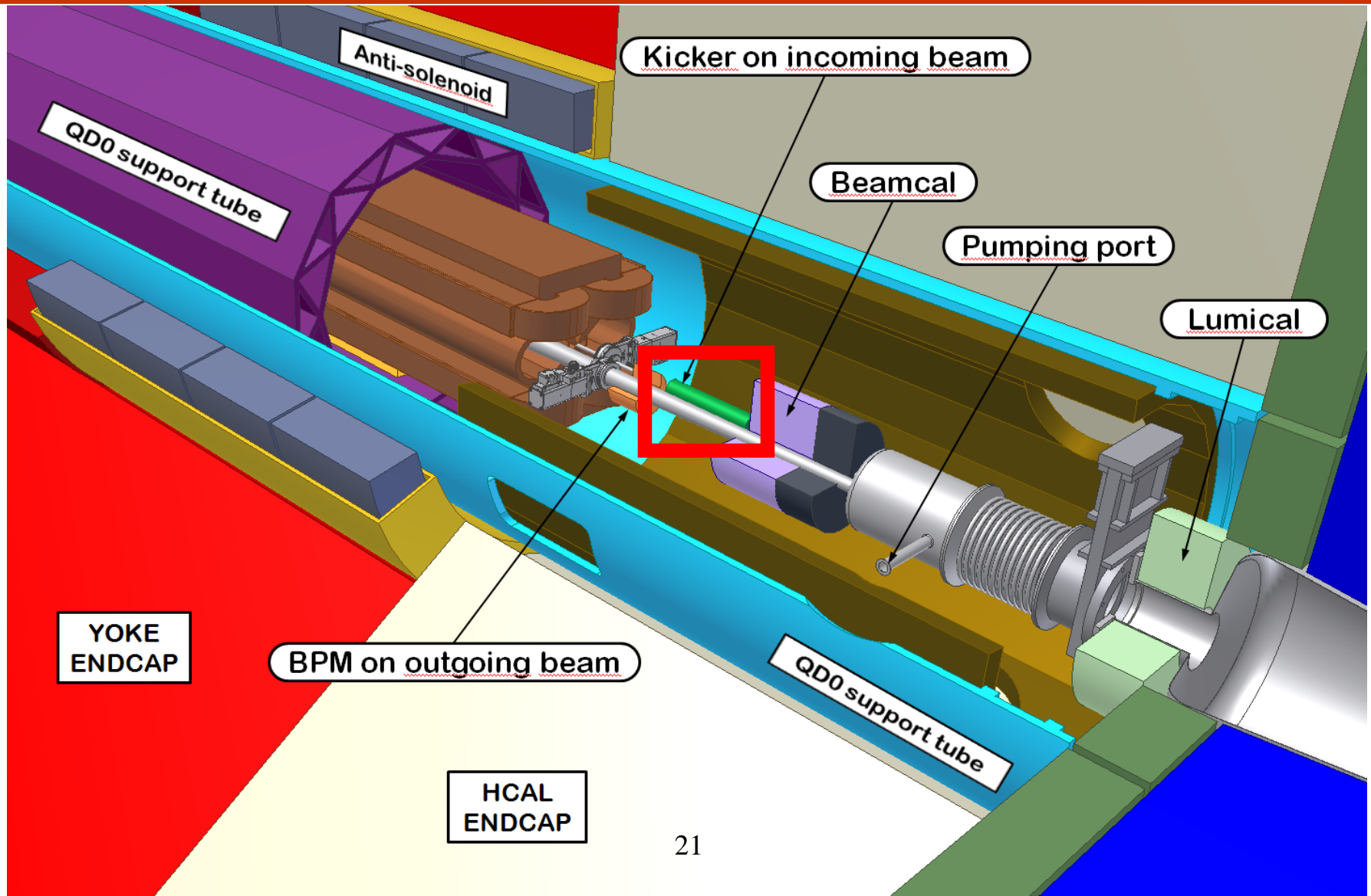
CLIC Final Doublet Region (CDR)



CLIC Final Doublet Region (CDR)

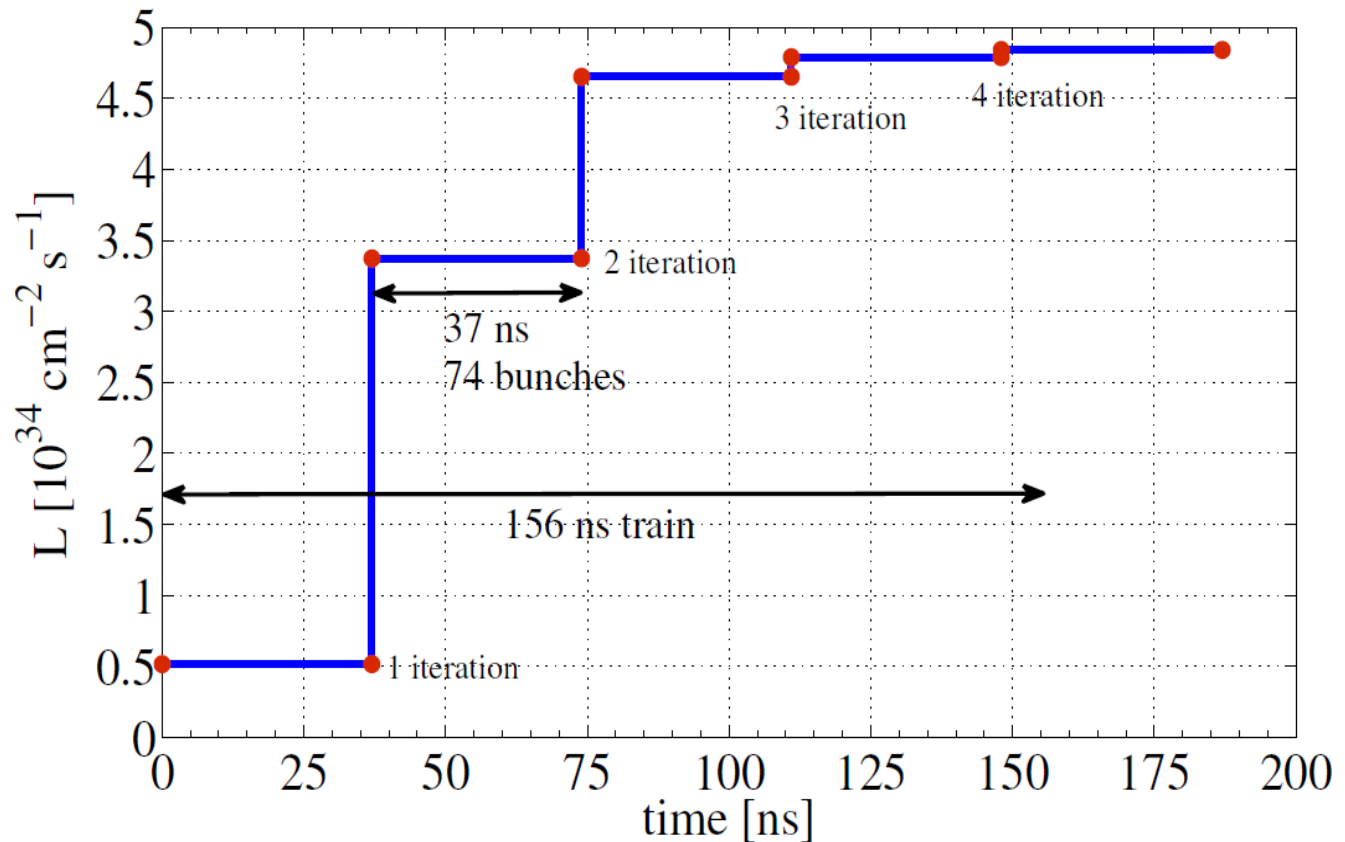


CLIC Final Doublet Region (CDR)

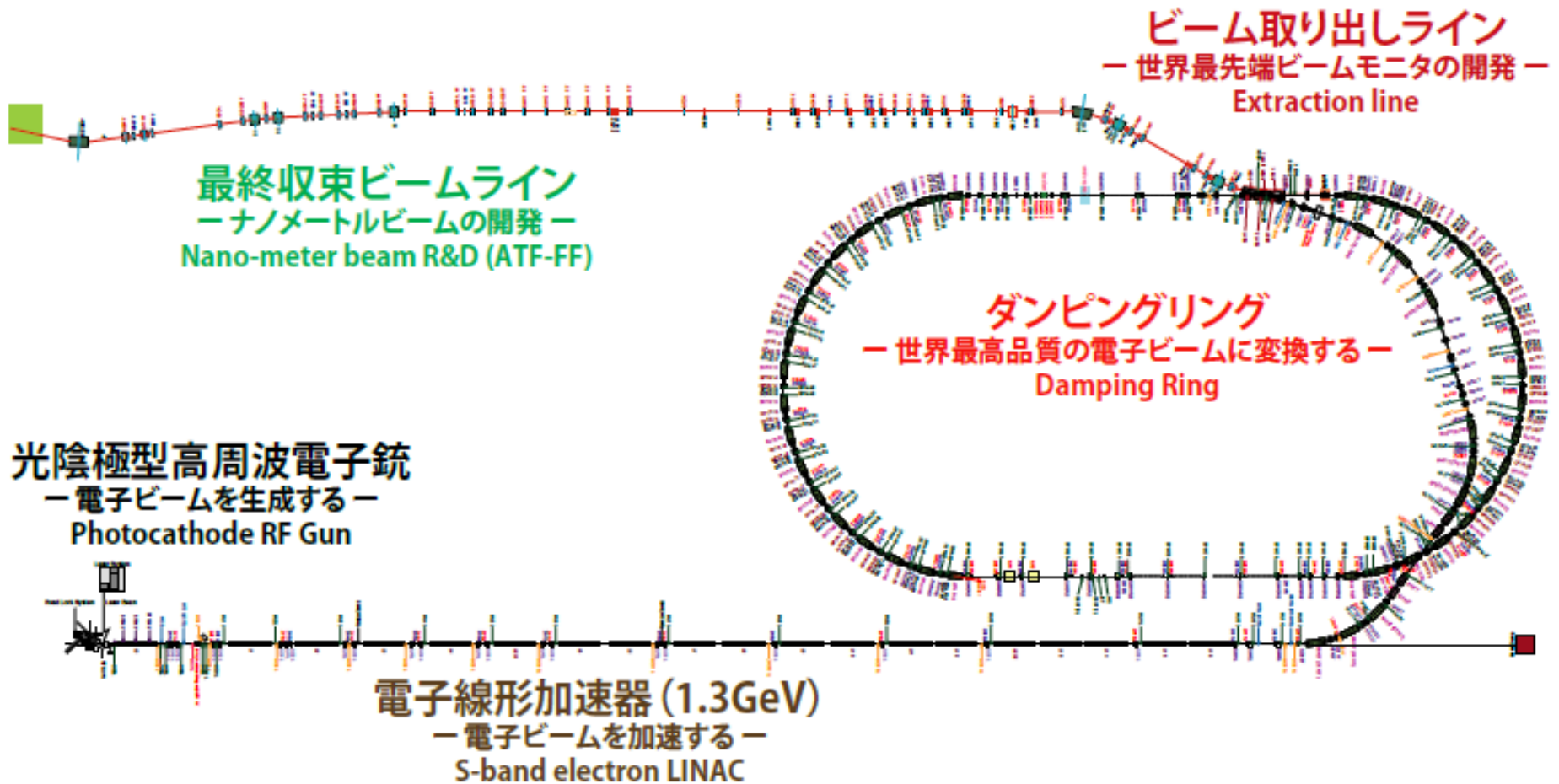


CLIC IP FB performance (CDR)

Single random seed of GM C

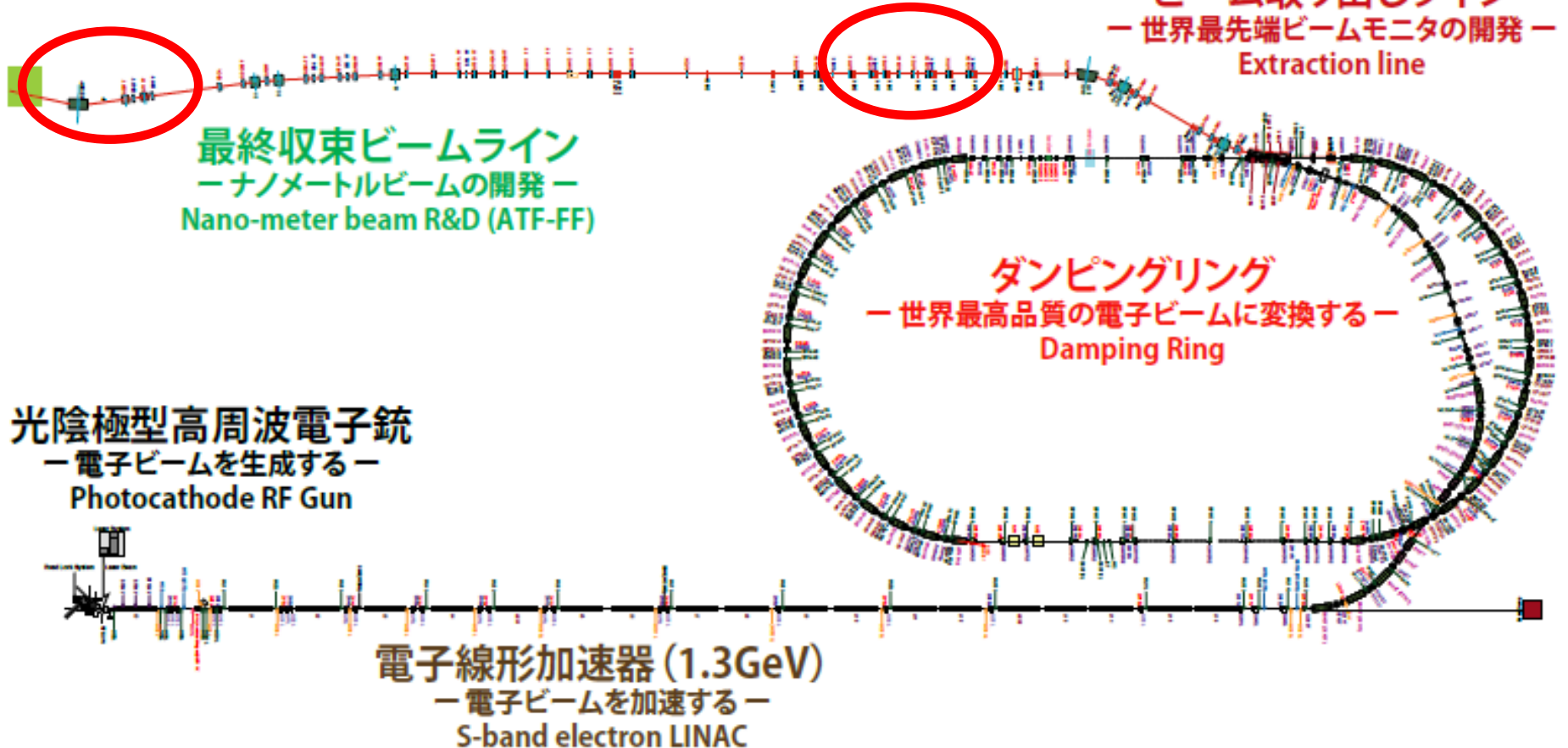


ATF2/KEK

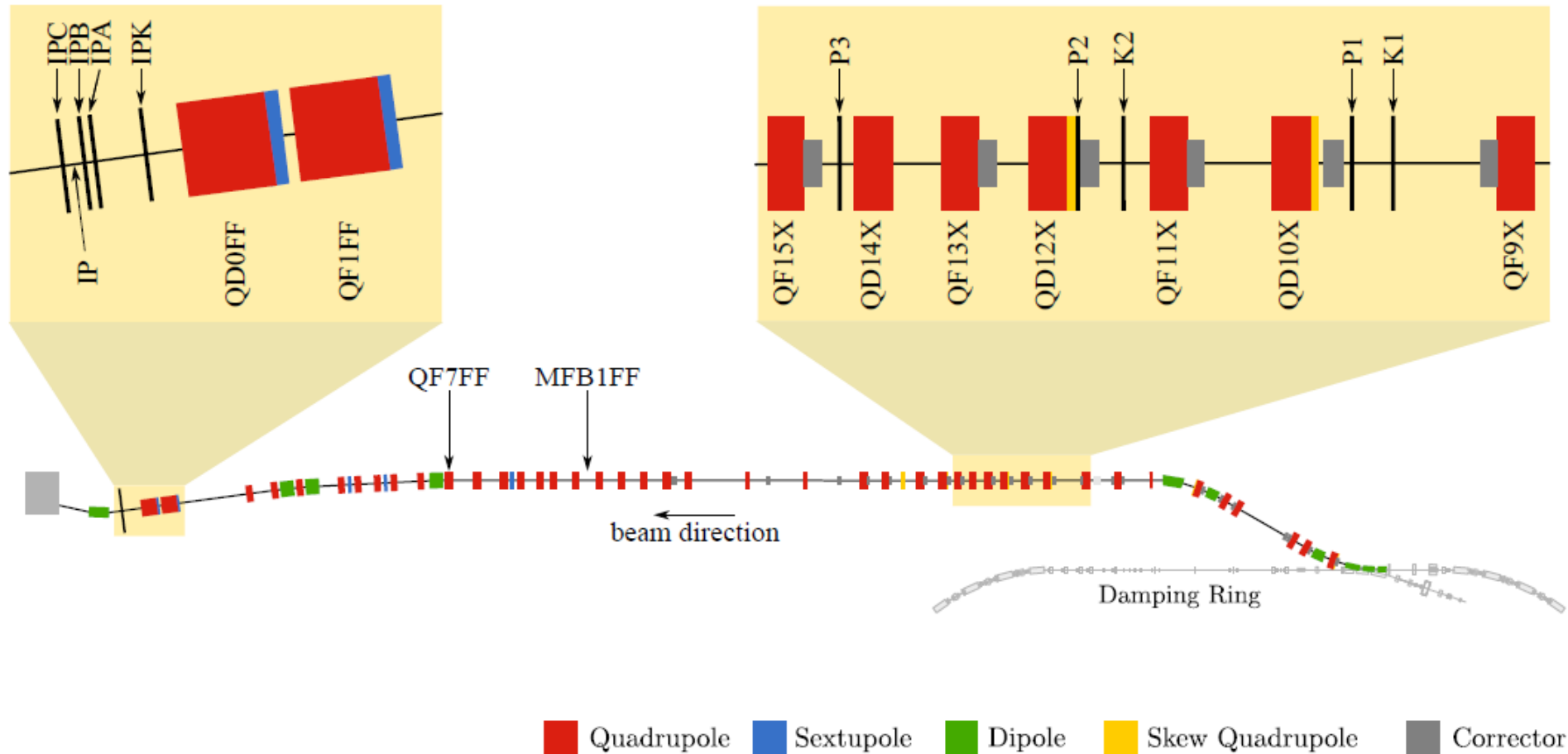


FONT5 'intra-train' feedbacks

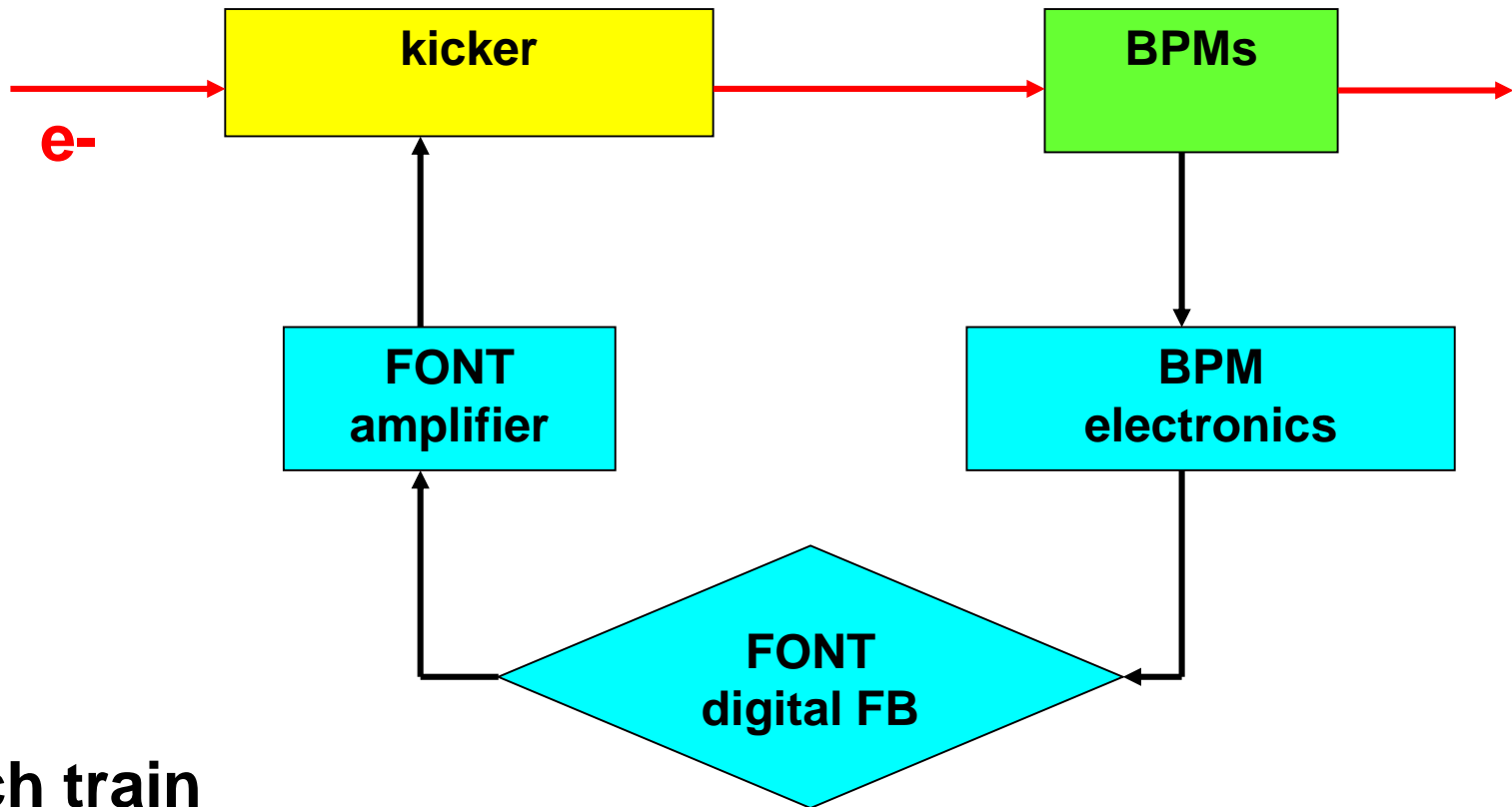
ATF2 extraction line



FONT5 'intra-train' feedbacks



ILC-style IPFB loop schematic



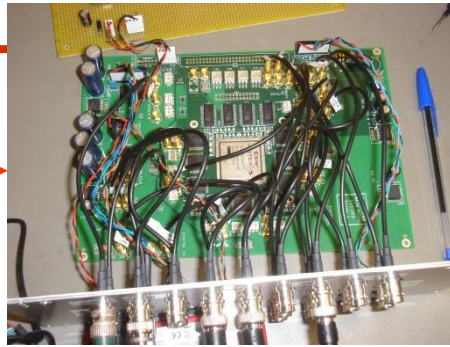
ATF2:

- 3-bunch train
- Bunch interval 154ns
- Measure bunch-1 vertical position
- Correct bunch-2 and bunch-3 positions

Upstream FONT5 System



**Analogue Front-end
BPM processor**



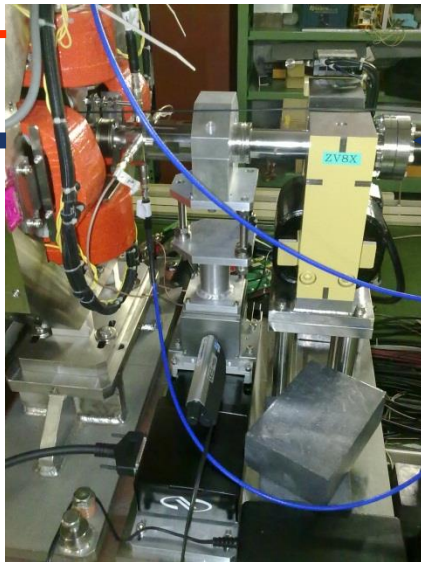
**FPGA-based digital
processor**



Kicker drive amplifier

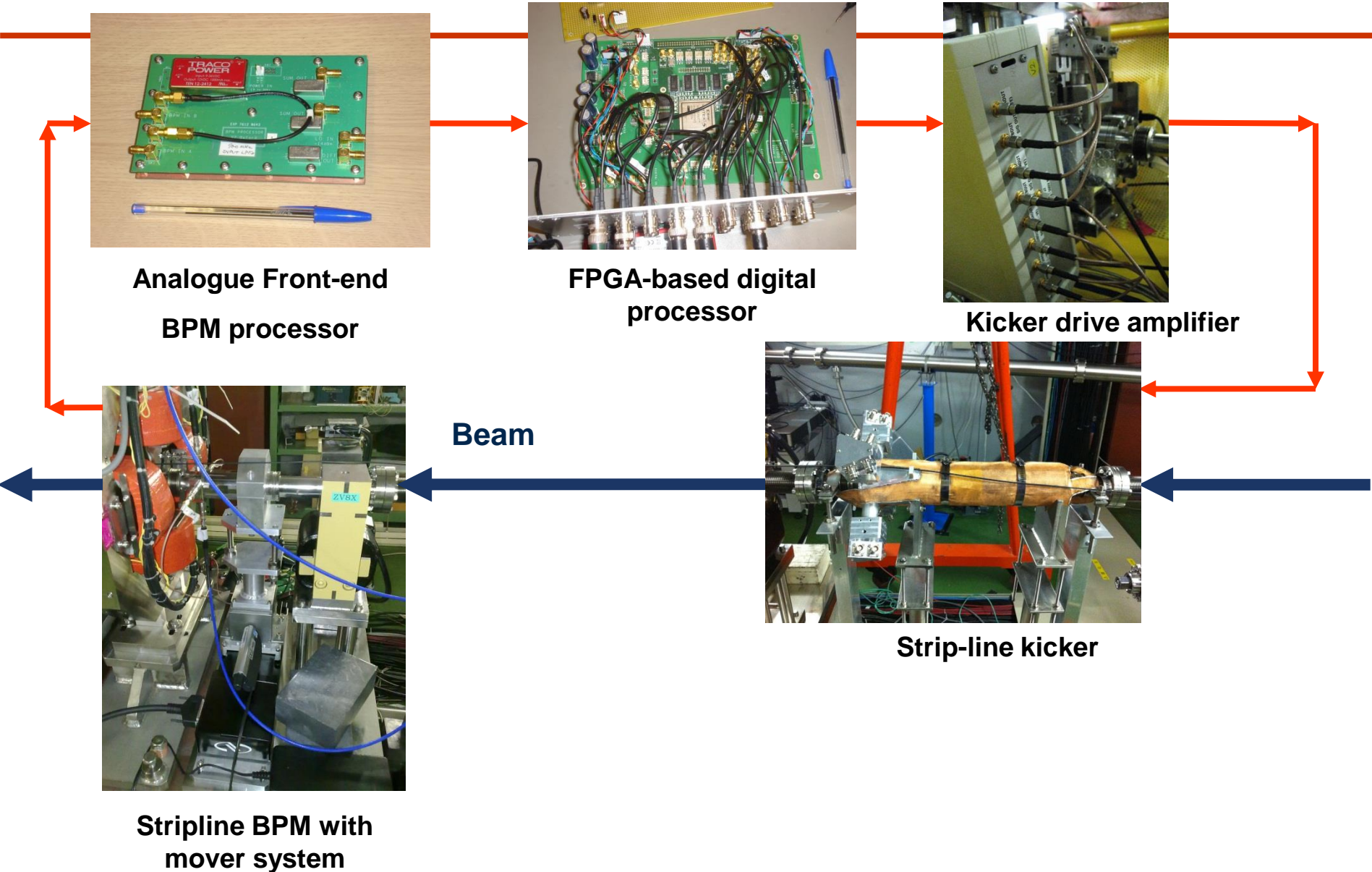


Strip-line kicker

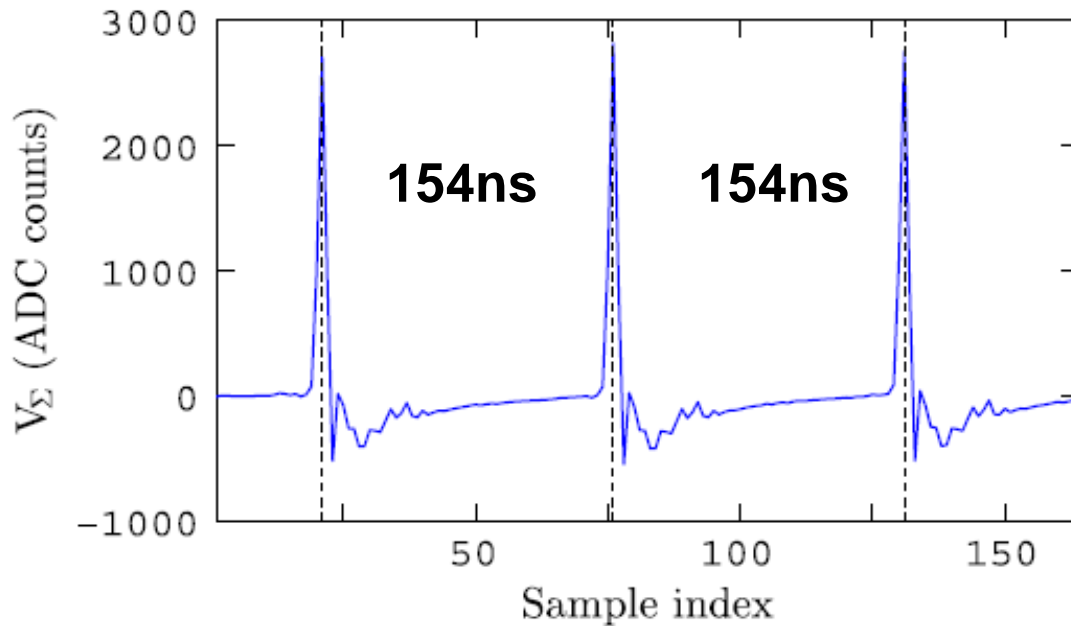
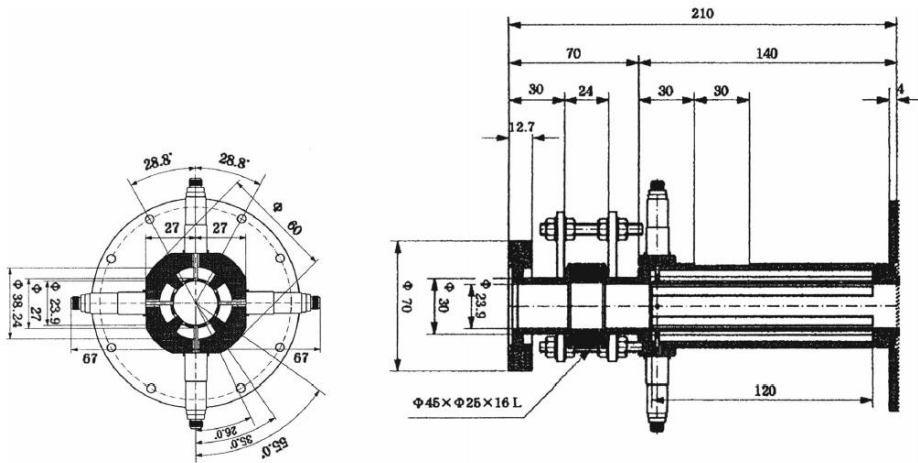


**Stripline BPM with
mover system**

Beam

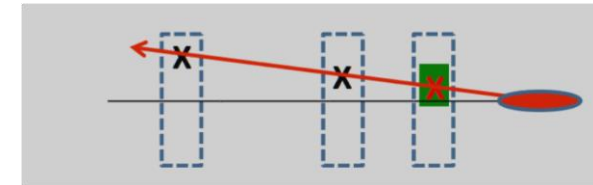
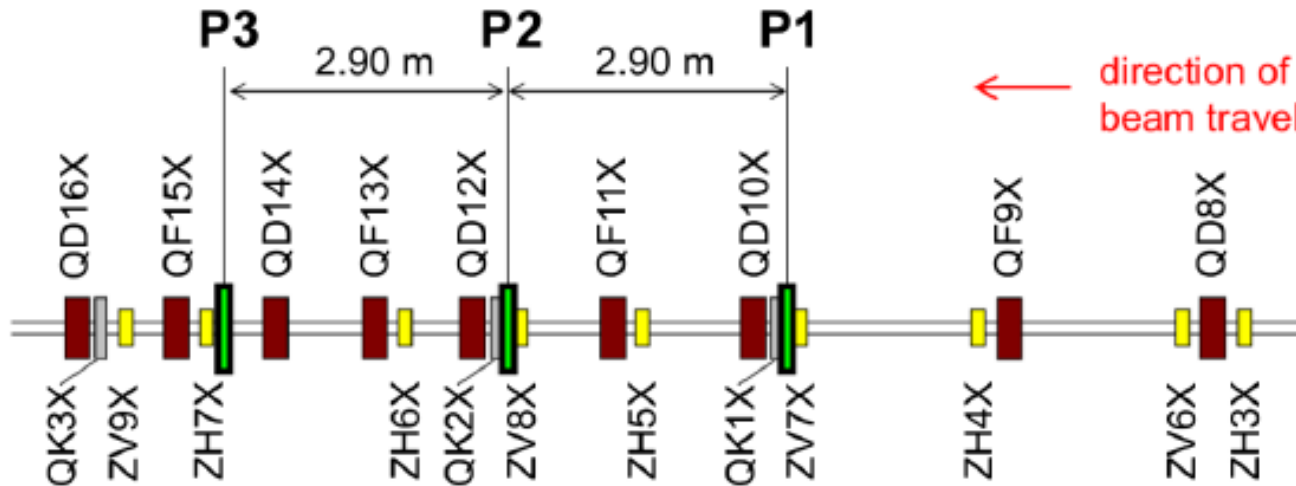


Stripline BPMs

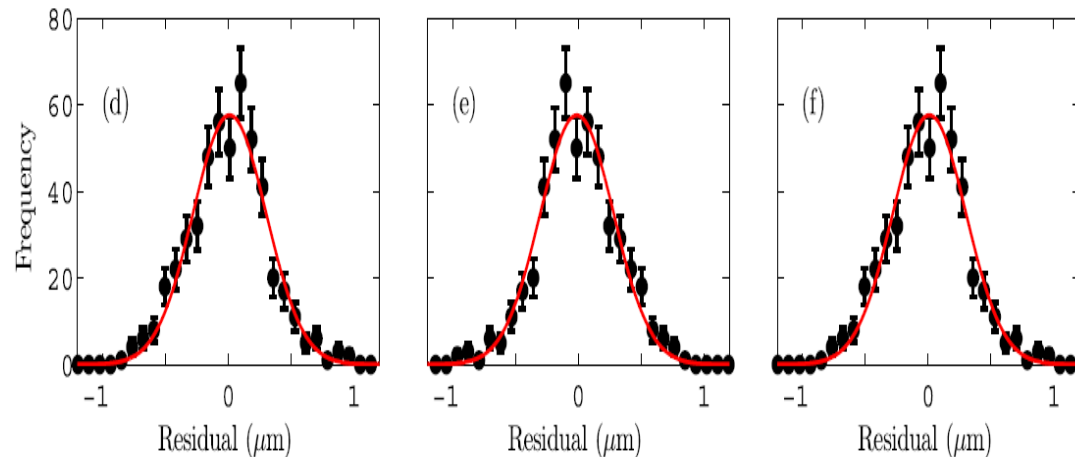


Excellent temporal resolution

BPM spatial resolution



**Resolution = 291 +/- 10 nm (Q ~ 1nC),
 → meets ILC + CLIC requirements**



PHYSICAL REVIEW SPECIAL TOPICS - ACCELERATORS AND BEAMS 18, 032803 (2015)

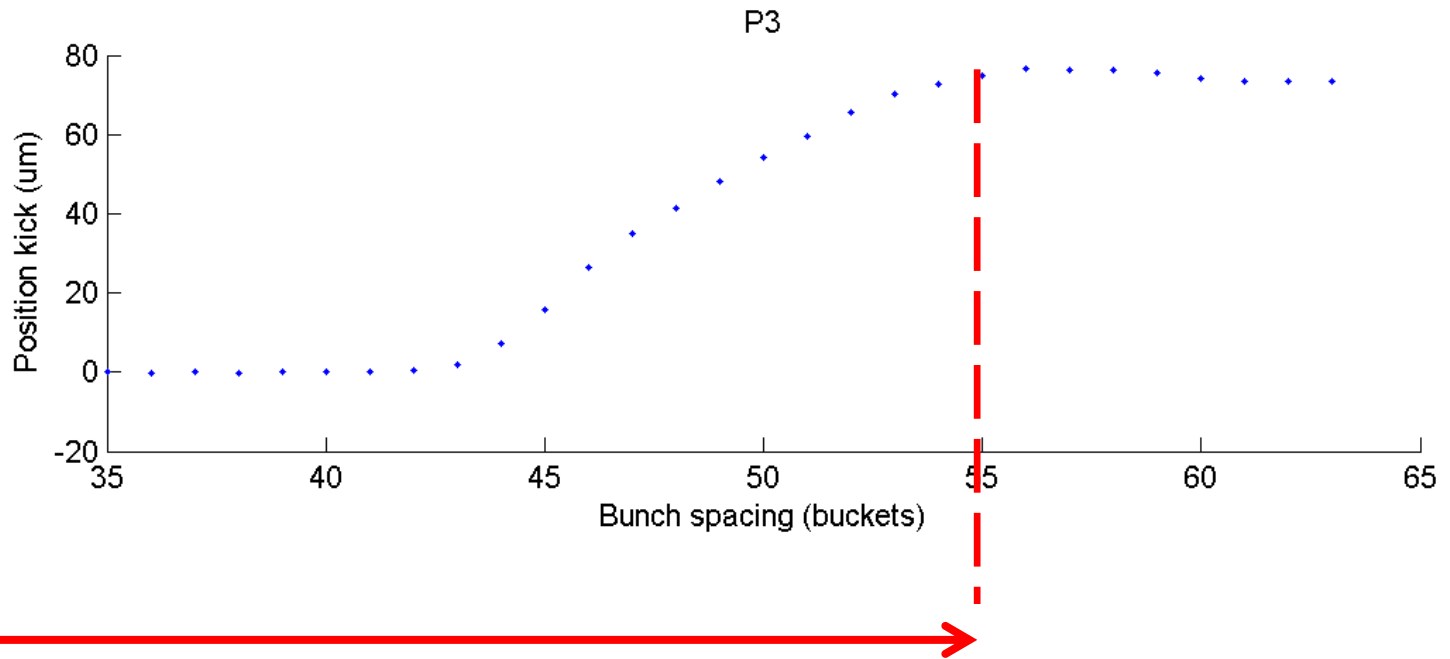
Design and performance of a high resolution, low latency stripline beam position monitor system

R. J. Apsimon,^{*} D. R. Bett,[†] N. Blaskovic Kraljevic, P. N. Burrows, G. B. Christian,[‡]
 C. I. Clarke,[§] B. D. Constance, H. Dabiri Khah, M. R. Davis, C. Perry,
 J. Resta López,^{||} and C. J. Swinson[¶]

John Adams Institute for Accelerator Science at University of Oxford, Denys Wilkinson Building,
 Keble Road, Oxford OX1 3RH, United Kingdom

FB system latency

**Kick to
bunch 2**

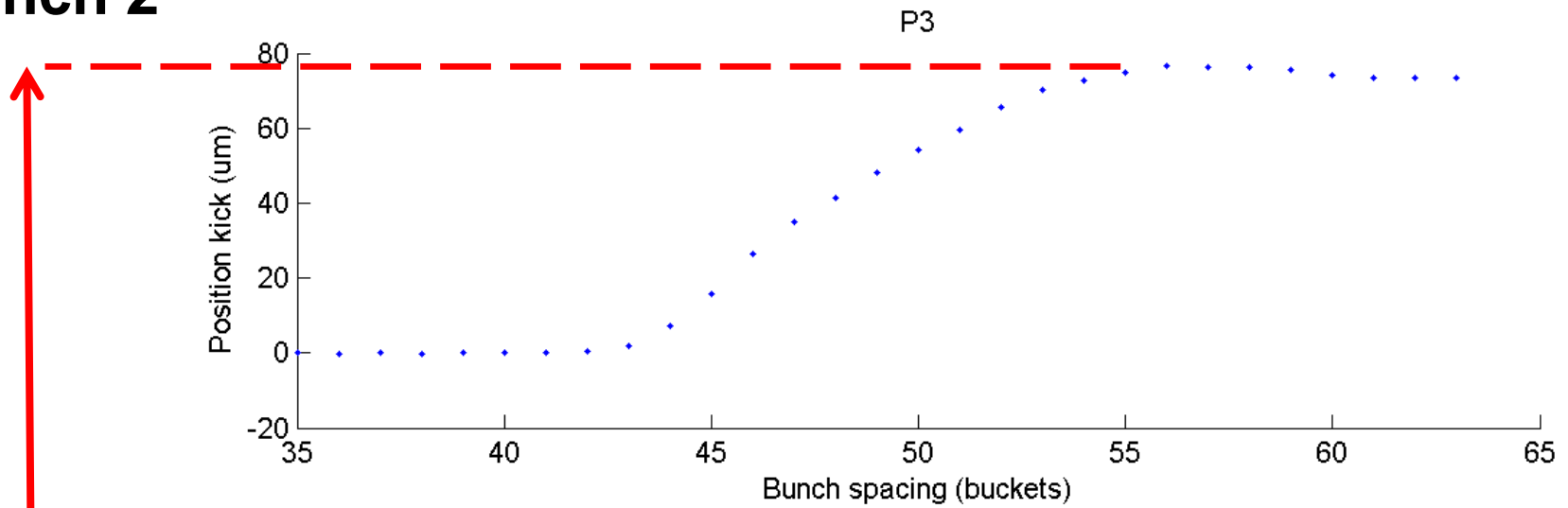


Latency: <math><154\text{ ns}</math>

→ meets ILC requirements

FB system dynamic range

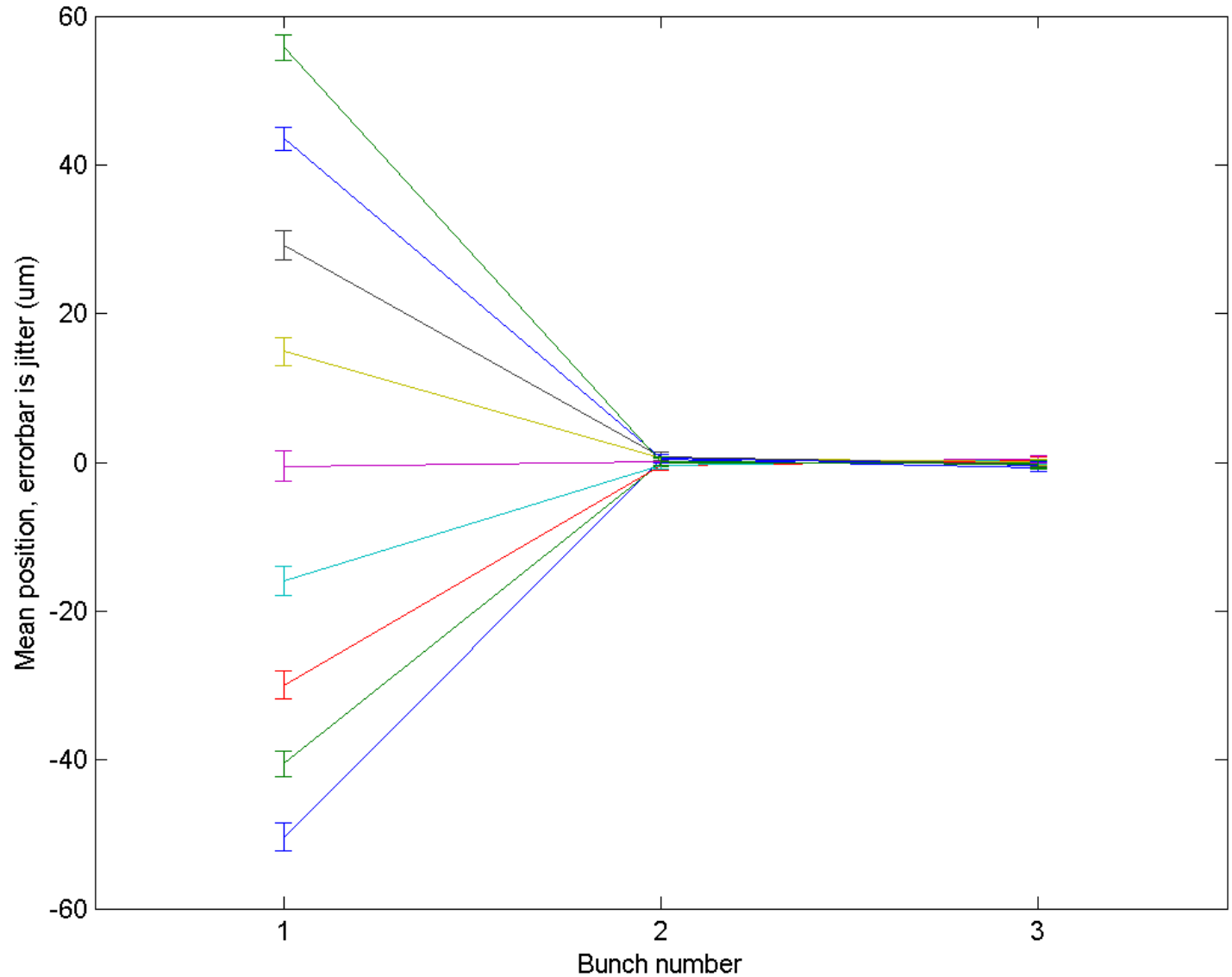
**Kick to
bunch 2**



Max. kick = 75 um (1.3 GeV)
= 400 nm (ILC 250 GeV beam)
= 66 σ_y (ILC 250)
→ meets ILC requirement of 50 σ_y

Trajectory scan

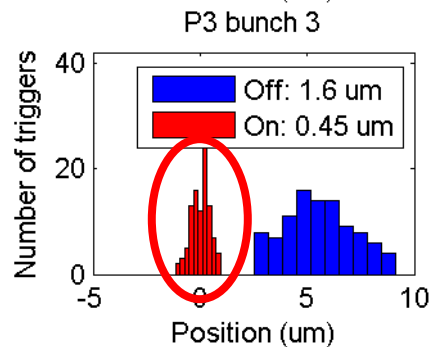
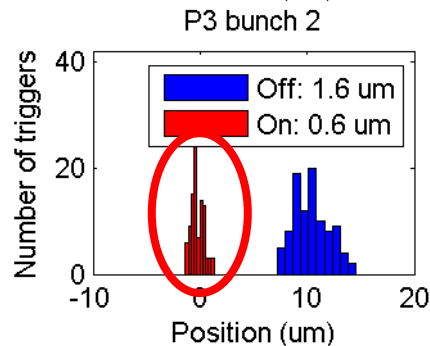
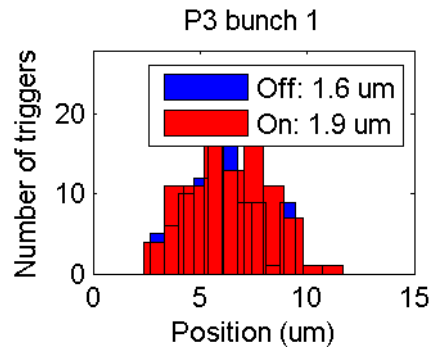
vertical
beam
position



Operational jitter correction

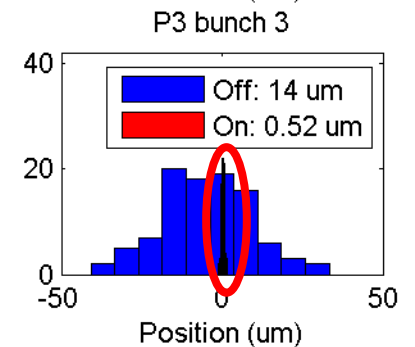
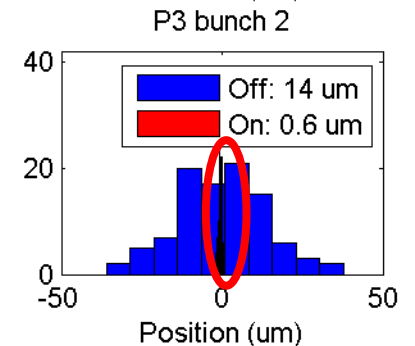
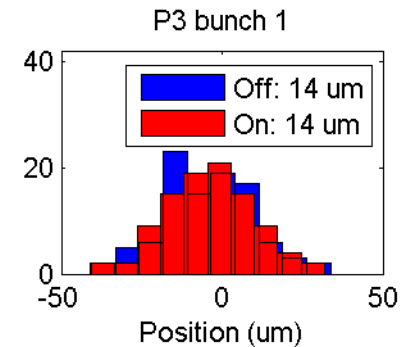
Normal operations:

2um jitter
→ 500nm



Deliberately enhanced jitter:

14um jitter
→ 500nm



Summary

- **Advanced designs for intra-train beam feedbacks for ILC and CLIC**
- **Simulations show excellent potential to meet ILC + CLIC design luminosities**
- **Prototypes tested at ATF with multi-bunch beam**
- **Digital FB meets ILC requirements in terms of:**
 - BPM resolution**
 - system latency**
 - beam-correction dynamic range**
- **Routinely stabilise 1.3 GeV beam to sub-um level**
- **Applicable to single-pass e- beamlines eg. FELs**

Summary – not presented

- Tested all-analogue FB system that meets CLIC IP FB requirements for latency + drive
- ATF2 coupled-loop FB system for $y + y'$ correction
 - **extrapolated performance ~ 4 nm at IP**
- Single-beam ATF2 IP FB based on cavity BPMs
 - **direct beam stabilisation < 70nm at IP**

Issue at ATF2 is how to measure directly the beam position at nm level ...

... not relevant for ILC+CLIC because beam-beam deflection provides $O(100\mu\text{m})$ signal input to IP FB

Backup slides

CLIC prototype: FONT3 at KEK/ATF



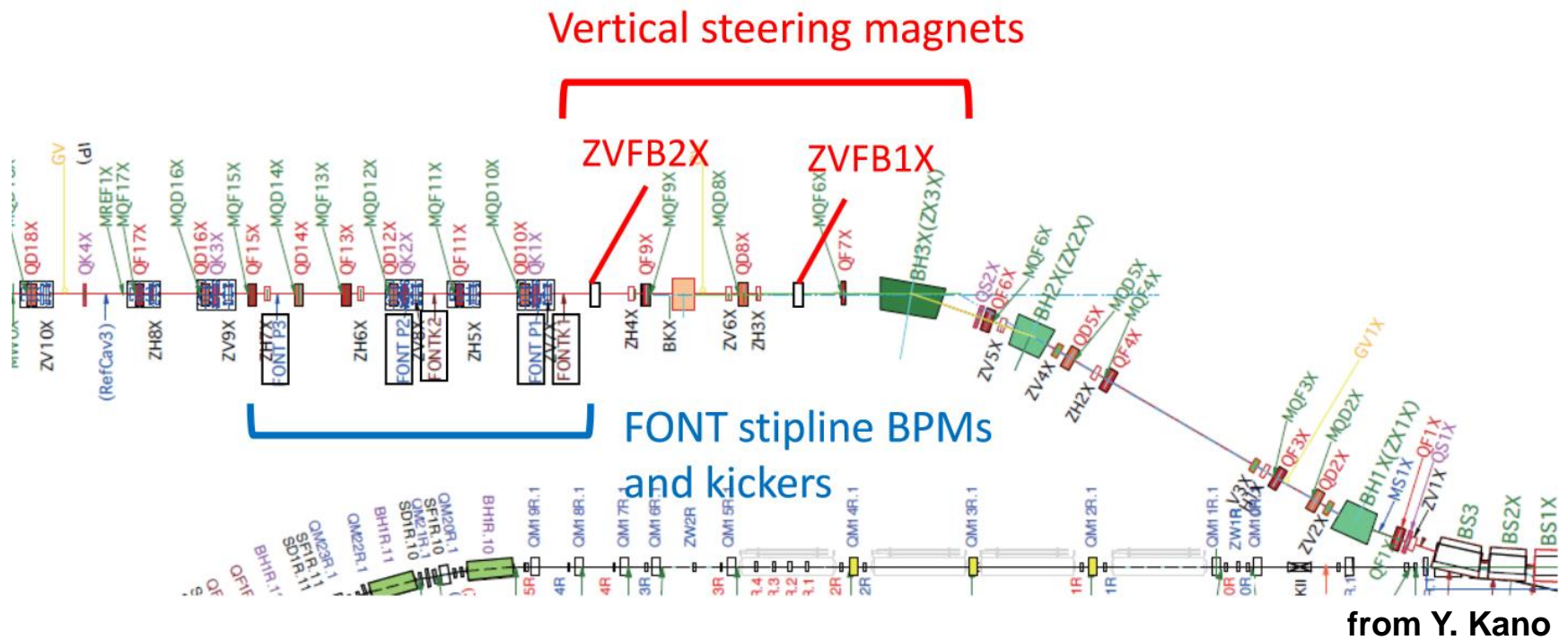
Electronics latency ~ 13ns
Drive power > 50nm
@ CLIC

ATF2 design parameters

Parameter		Design value
Energy	(GeV)	1.3
Intensity	(electrons/bunch)	1×10^{10}
Repetition rate	(Hz)	3.12
Horizontal emittance	ϵ_x (m rad)	2×10^{-9}
Vertical emittance	ϵ_y (m rad)	1.2×10^{-11}
Horizontal IP beam size	\hat{x}^* (m)	2.8×10^{-6}
Vertical IP beam size	\hat{y}^* (m)	3.7×10^{-8}
Horizontal IP beta function	β_x^* (m)	4×10^{-3}
Vertical IP beta function	β_y^* (m)	1×10^{-4}
RMS energy spread	(%)	0.08

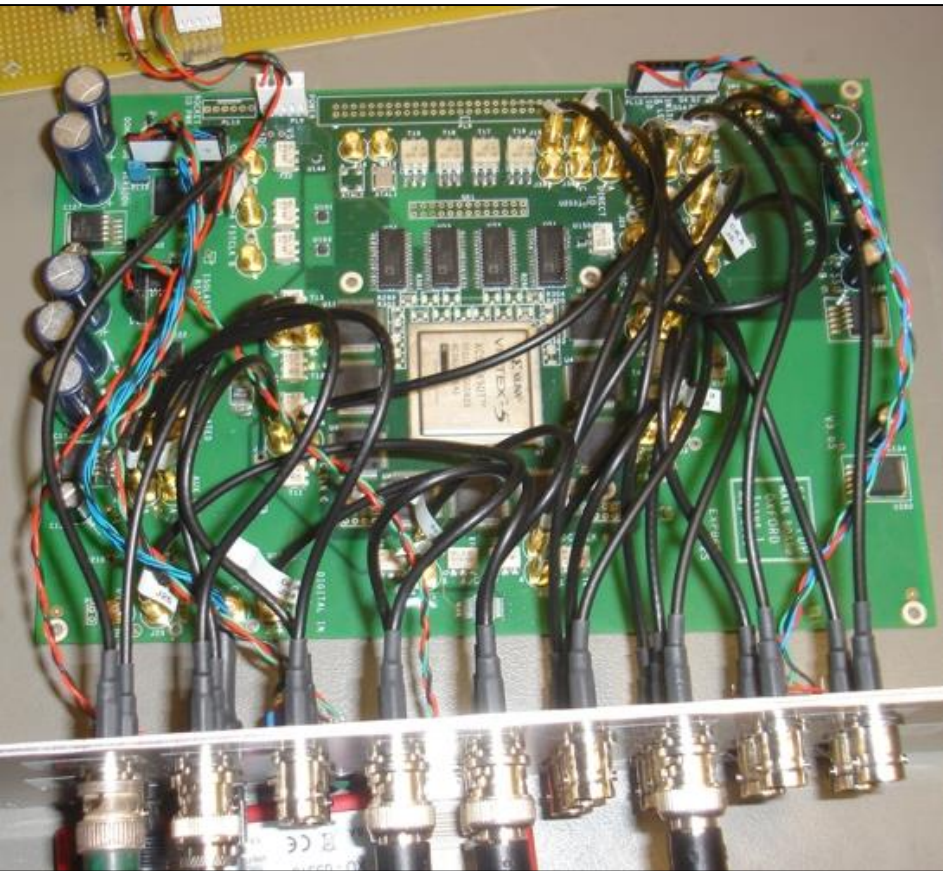
Random jitter source

Random jitter introduced pulse-to-pulse using ZVFB1X & ZVFB2X



from Y. Kano

FONT5 digital FB board



Xilinx Virtex5 FPGA

**9 ADC input channels
(TI ADS5474)**

**4 DAC output channels
(AD9744)**

**Clocked at up to 400 MHz
(phase-locked to beam)**

FONT4 drive amplifier

- FONT4 amplifier, outline design done in JAI/Oxford
- Production design + fabrication by TMD Technologies
- Specifications:

+ - 15A (kicker terminated with 50 Ohm)

+ - 30A (kicker shorted at far end)

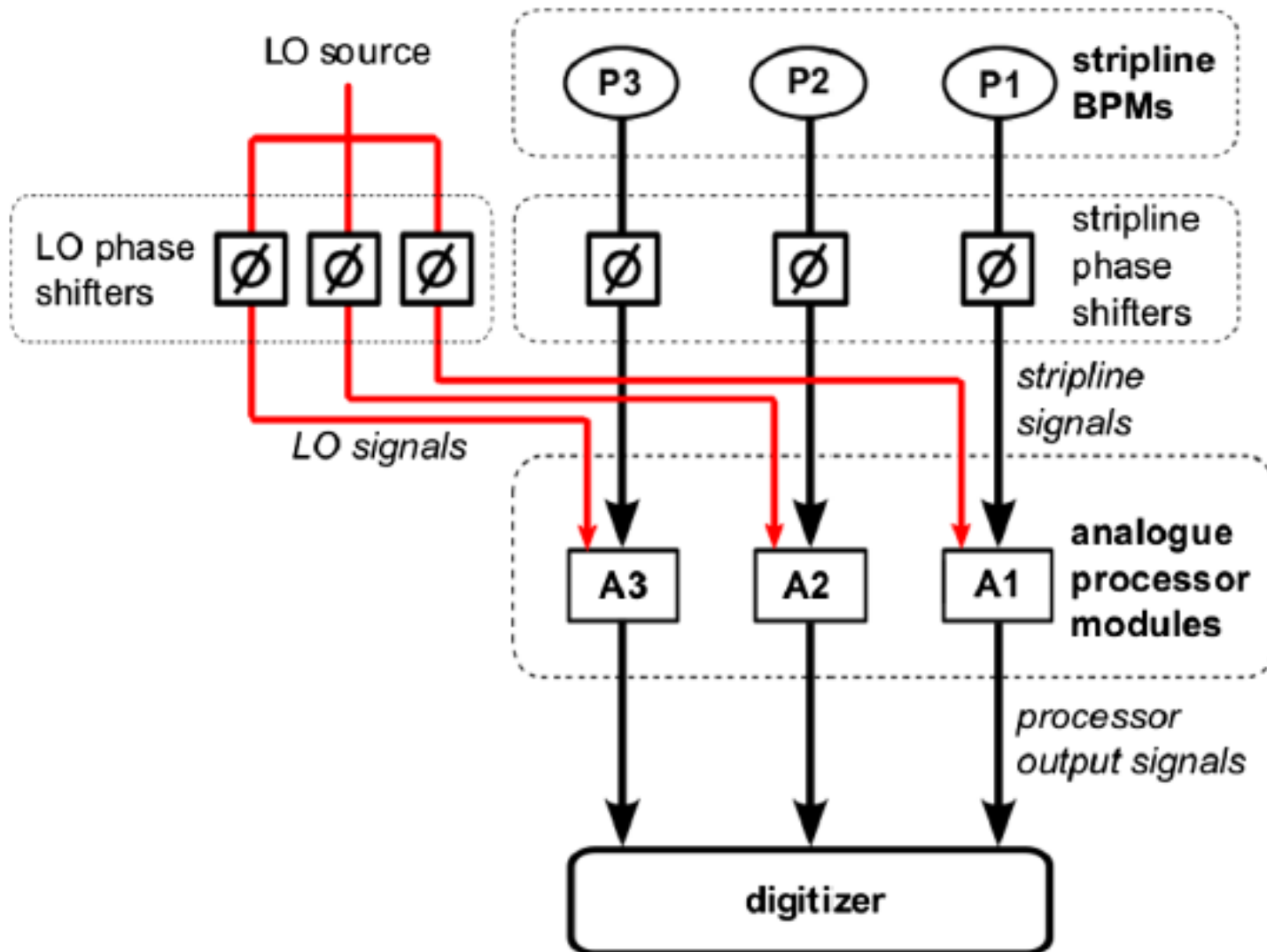
35ns risetime (to 90%)

pulse length 10 us

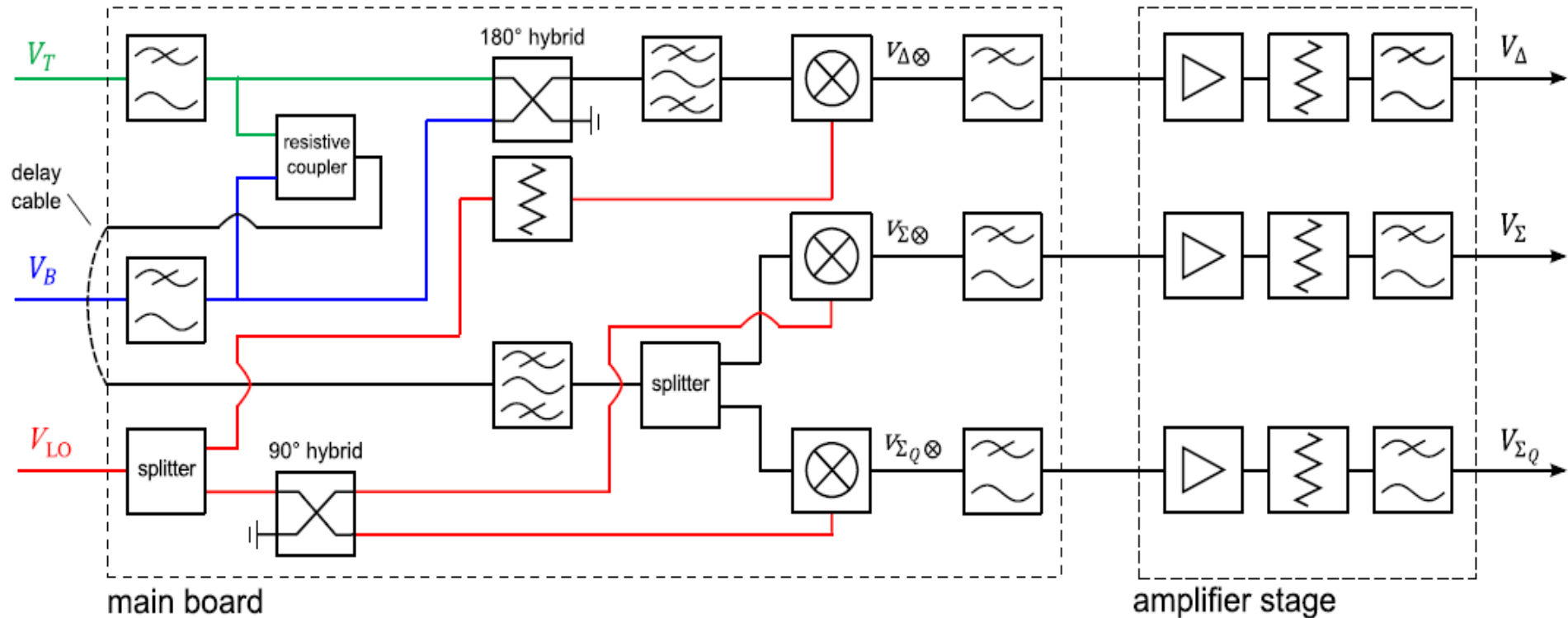
repetition rate 10 Hz



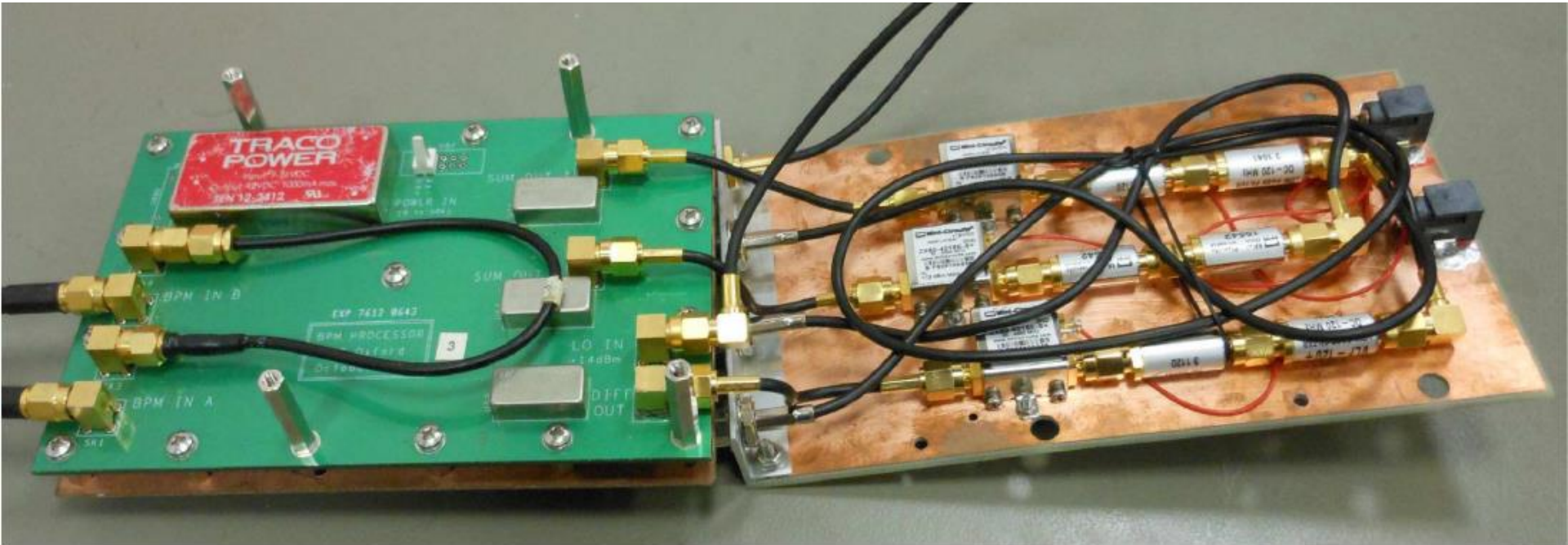
BPM readout



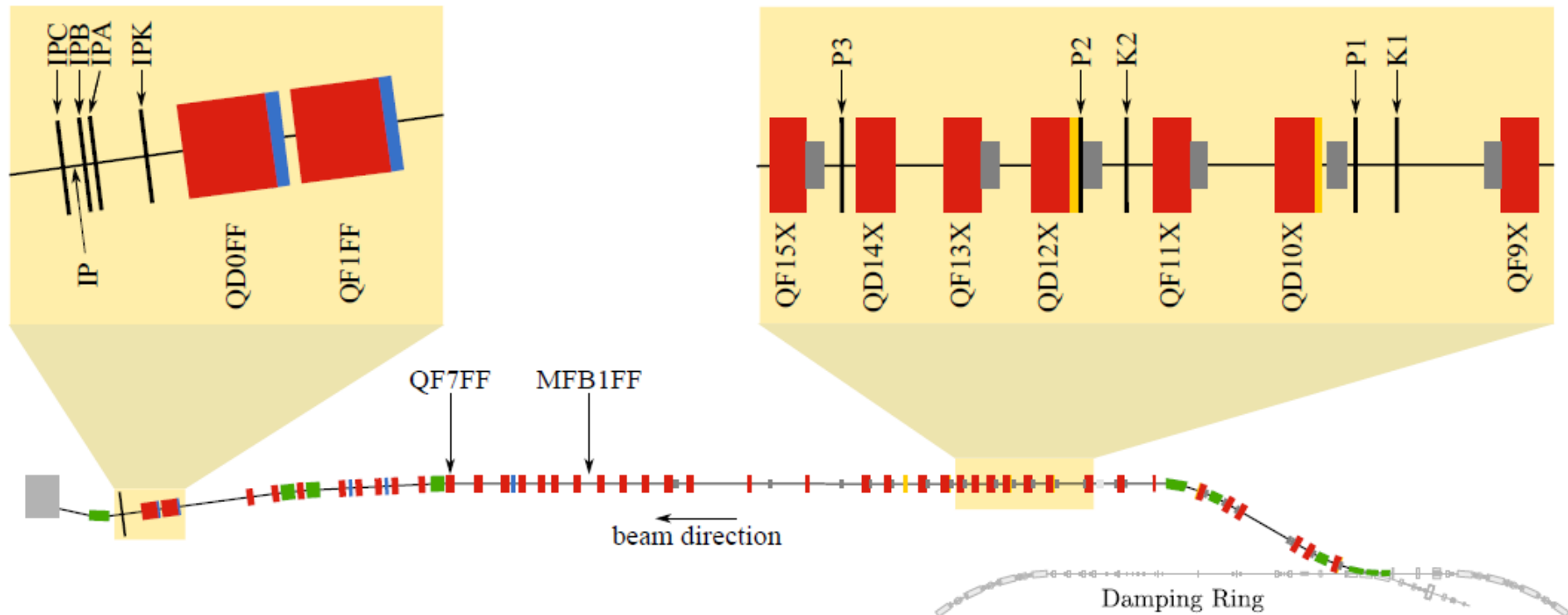
BPM signal processing



BPM signal processor



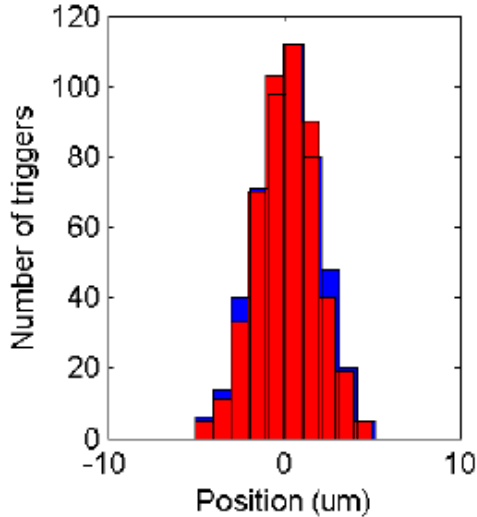
Stabilising beam near IP



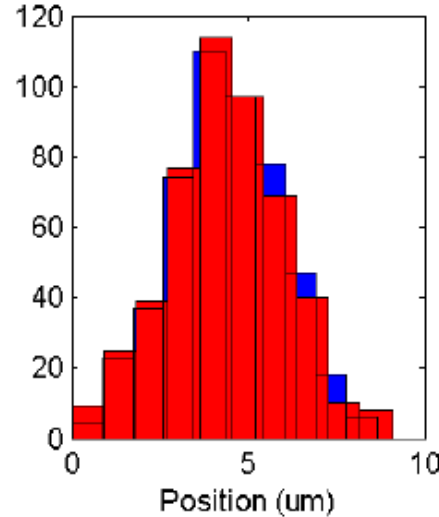
- 1. Upstream FB:** monitor beam at IP
- 2. Feed-forward:** from upstream BPMs → IP kicker
- 3. Local IP FB:** using IPBPM signal and IP kicker

FONT5 system performance

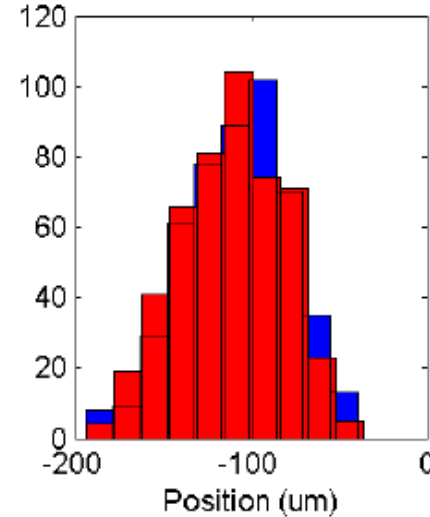
(a) P2 bunch 1



(b) P3 bunch 1



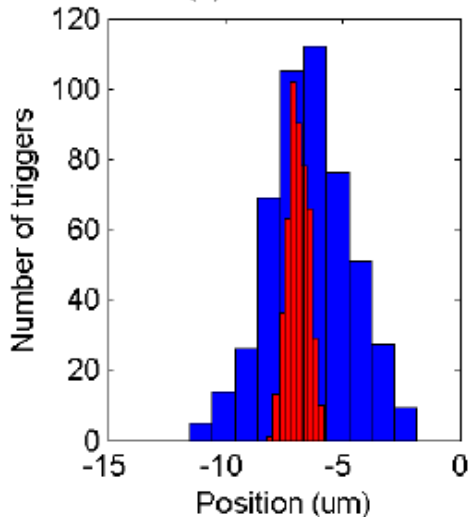
(c) MFB1FF bunch 1



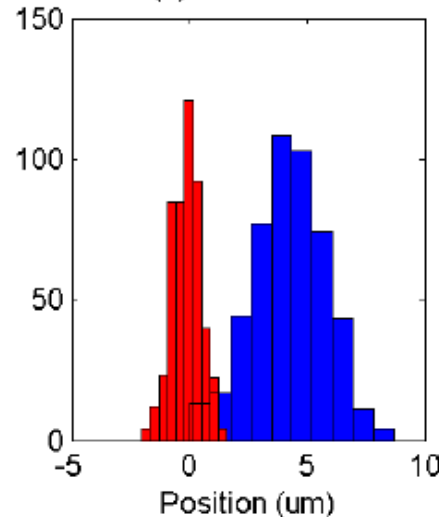
**Bunch 1:
input to FB**

FB off
FB on

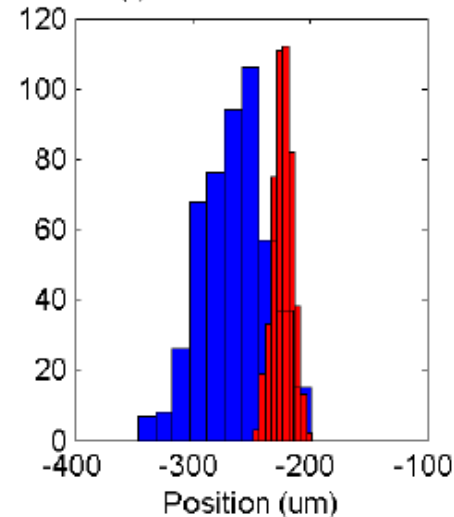
(d) P2 bunch 2



(e) P3 bunch 2



(f) MFB1FF bunch 2



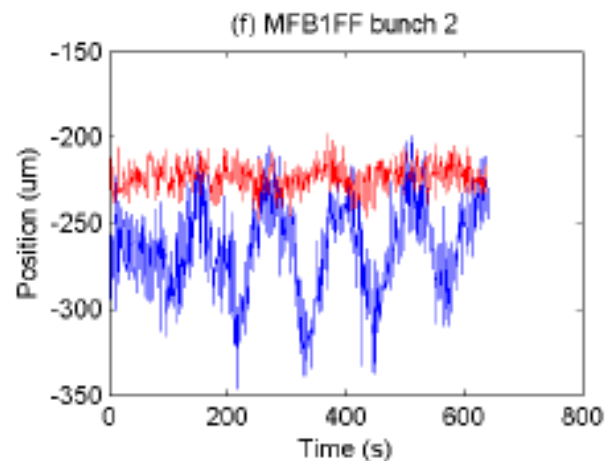
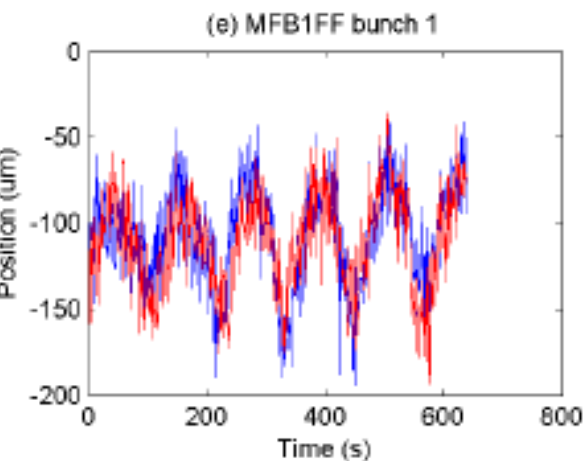
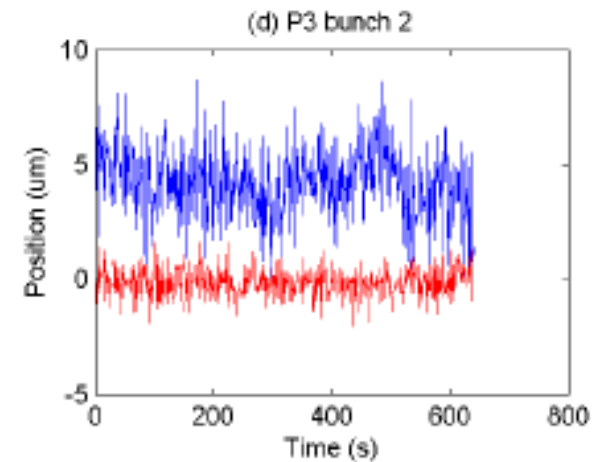
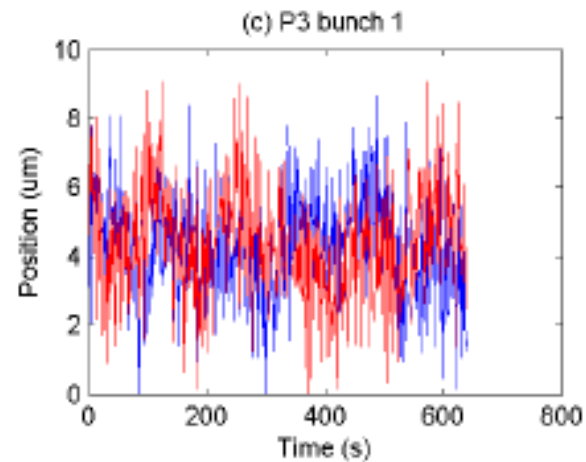
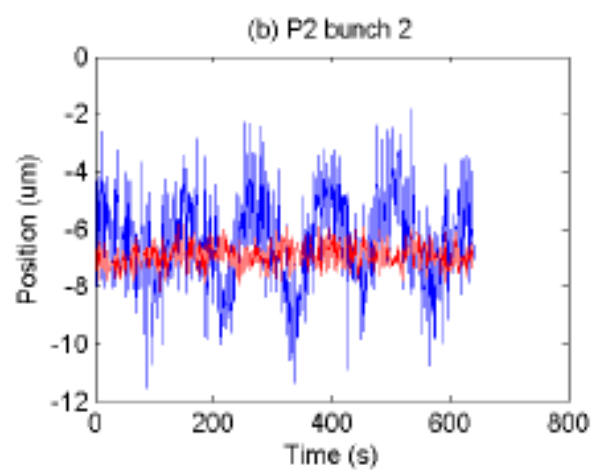
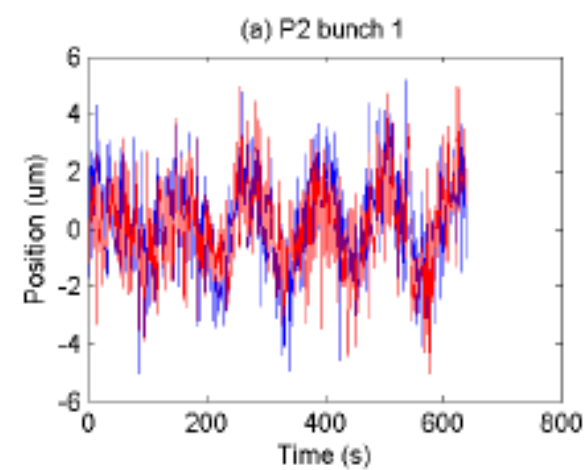
**Bunch 2:
corrected**

FB off
FB on

Time sequence

**Bunch 2:
corrected**

FB off
FB on



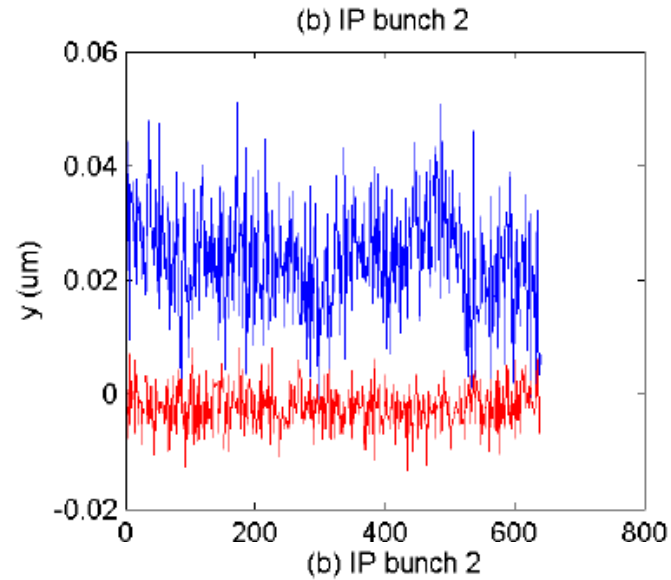
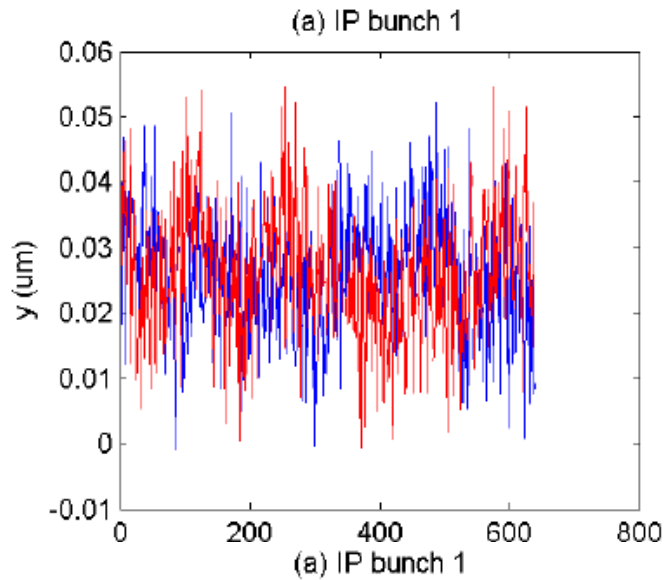
Jitter reduction

BPM	Position jitter (μm)			
	Bunch 1		Bunch 2	
	Feedback off	Feedback on	Feedback off	Feedback on
P2	1.80 ± 0.06	1.70 ± 0.05	1.74 ± 0.06	0.44 ± 0.01
P3	1.56 ± 0.05	1.66 ± 0.05	1.55 ± 0.05	0.61 ± 0.02
MFB1FF	29.9 ± 1.0	29.4 ± 0.9	27.5 ± 0.9	8.3 ± 0.3

Factor ~ 3.5 improvement

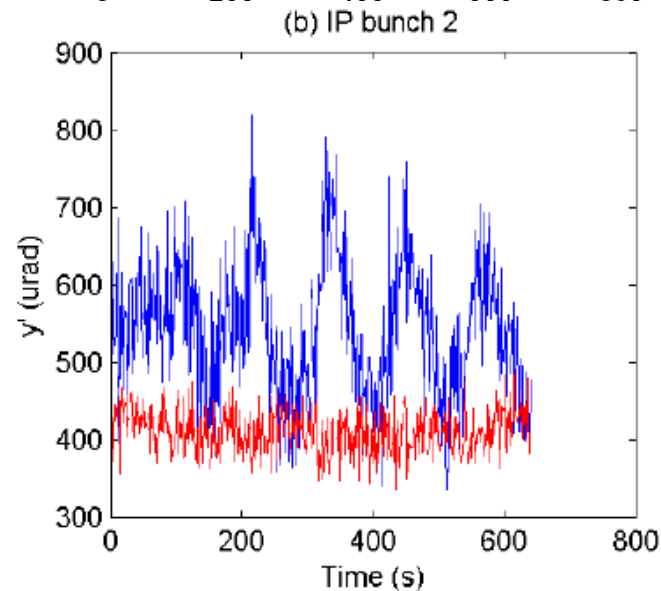
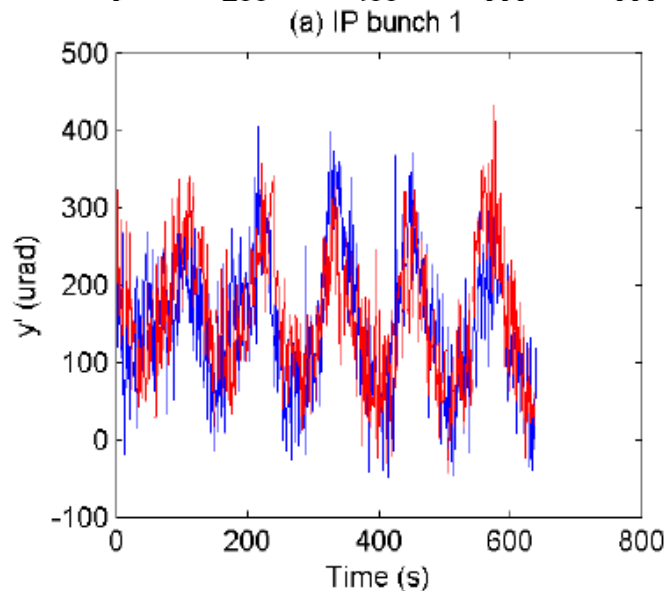
Predicted jitter reduction at IP

y



FB off
FB on

y'



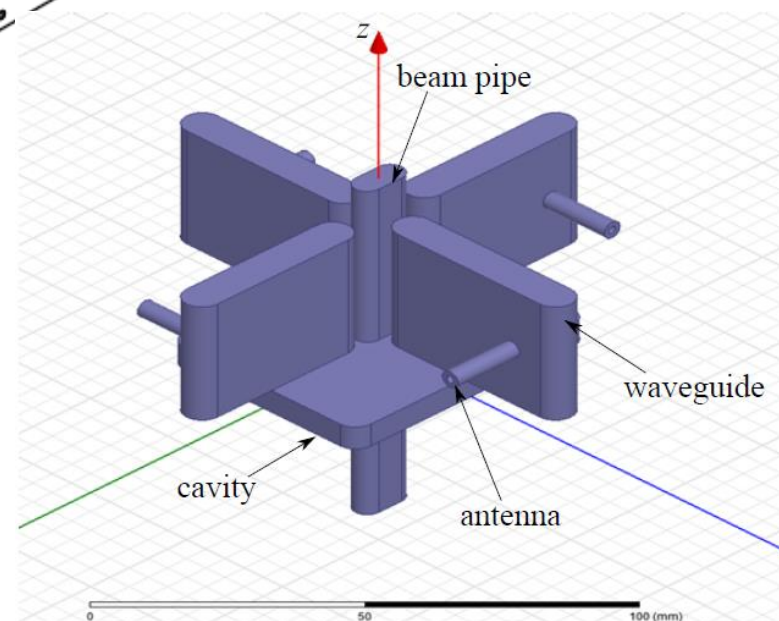
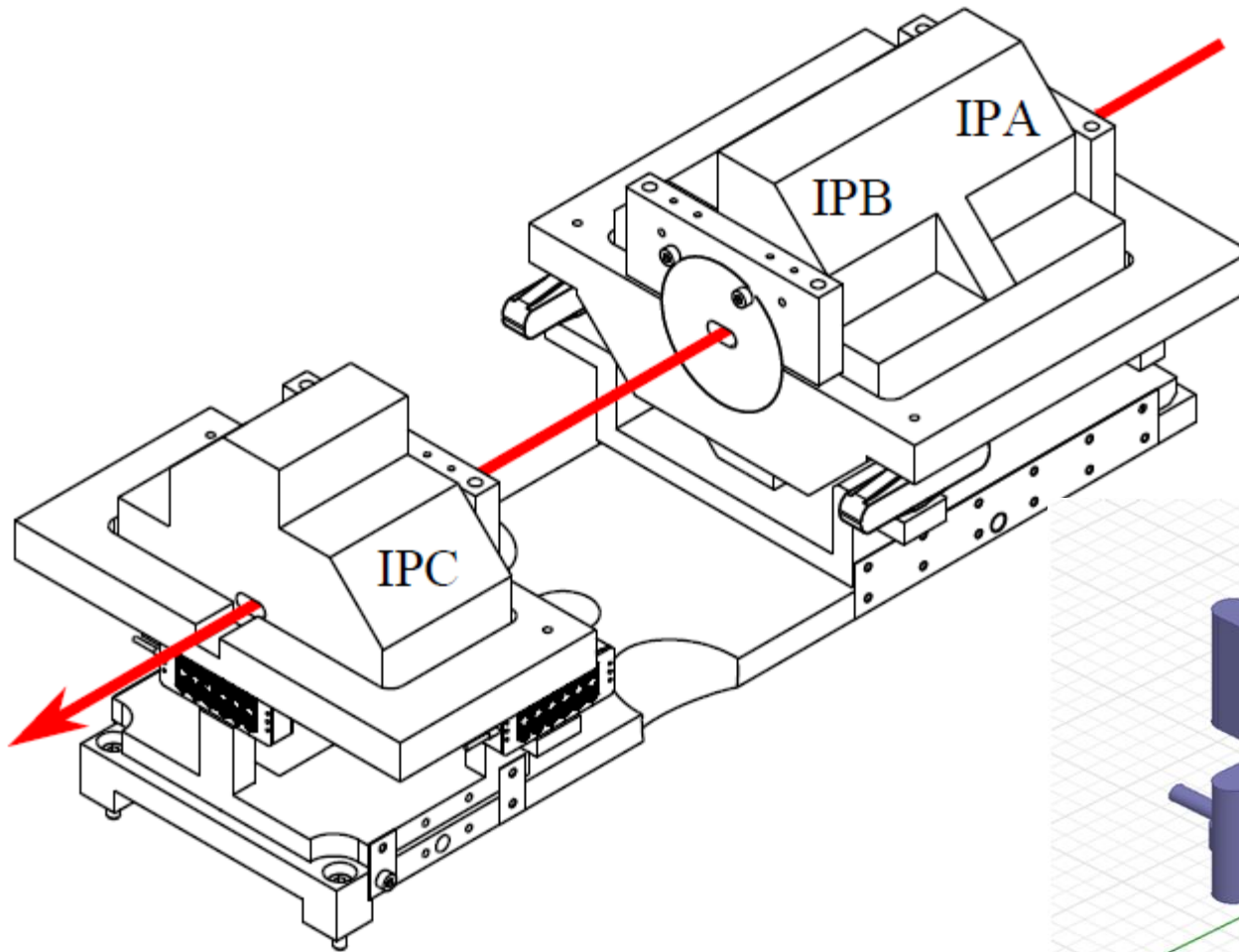
Predicted jitter reduction at IP

Bunch	Position y jitter (nm)		Angle y' jitter (urad)	
	Feedback off	Feedback on	Feedback off	Feedback on
1	9.5 ± 0.3	10.1 ± 0.3	89 ± 3	87 ± 3
2	9.4 ± 0.3	3.6 ± 0.1	87 ± 3	28 ± 1

**Predict position stabilised
at few nanometre level...**

How to measure it?!

IP cavity BPM system

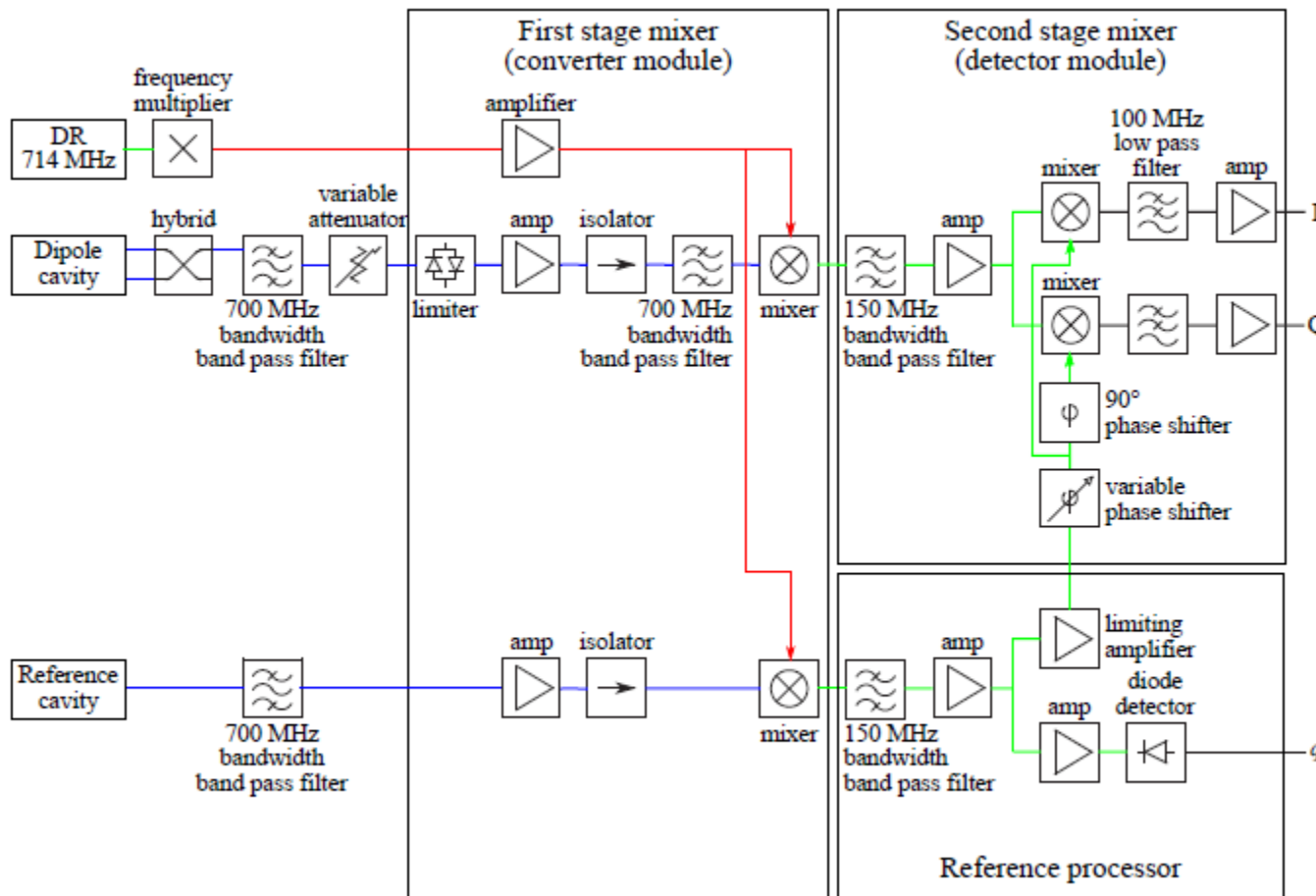


Low-Q cavity BPMs

Design parameters

Parameter			Dipole cavities		Reference cavities	
			<i>x</i> port	<i>y</i> port	<i>x</i> cavity	<i>y</i> cavity
Resonant frequency	f_{mn}	(GHz)	5.712	6.426	5.711	6.415
Internal quality factor	$(Q_0)_{mn}$		4959	4670	1201	1229
Decay time	τ_{mn}	(ns)	18.72	17.23	33.16	30.03

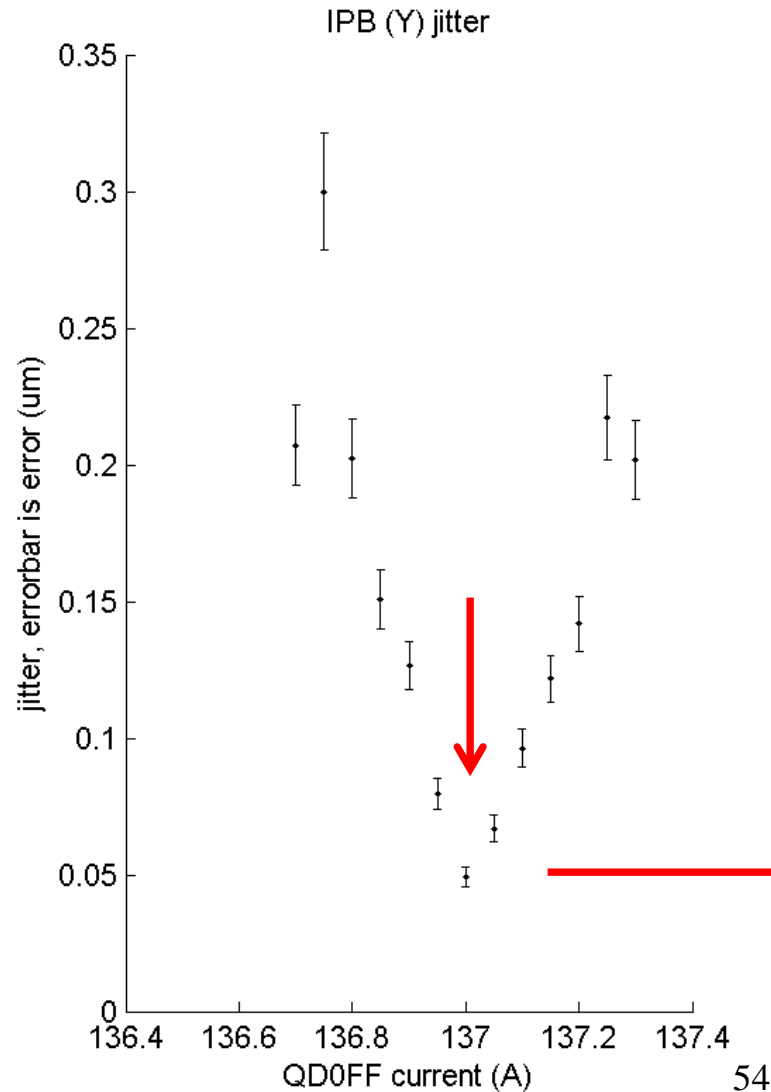
Cavity BPM signal processing



I → **I'**
Q → **Q'**

bunch charge

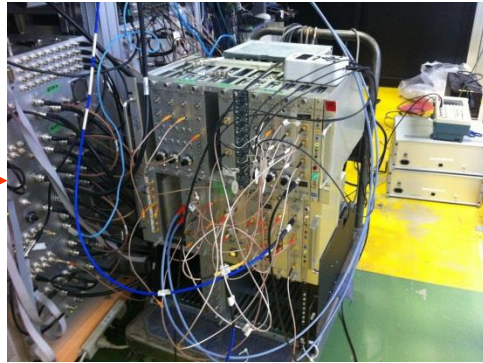
Jitter vs. QD0FF setting (waist scan)



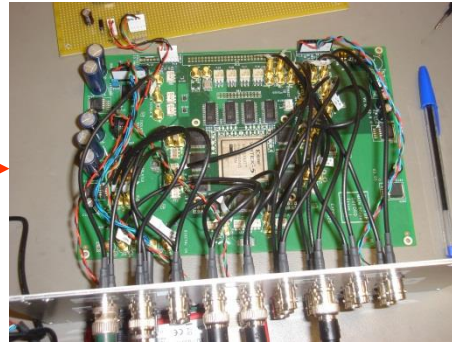
**minimum
jitter:**

**49 nm
(integration)**

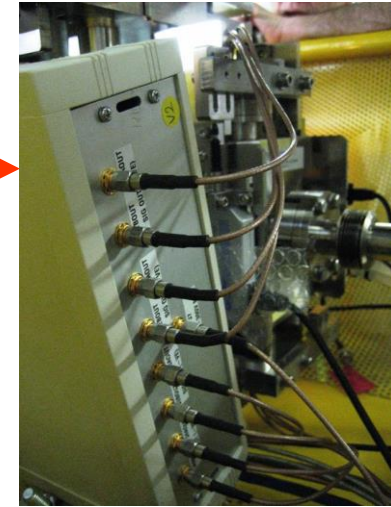
Interaction Point FONT System



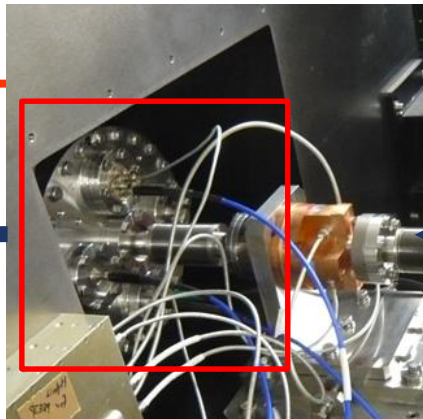
**Analogue Front-end
BPM processor**



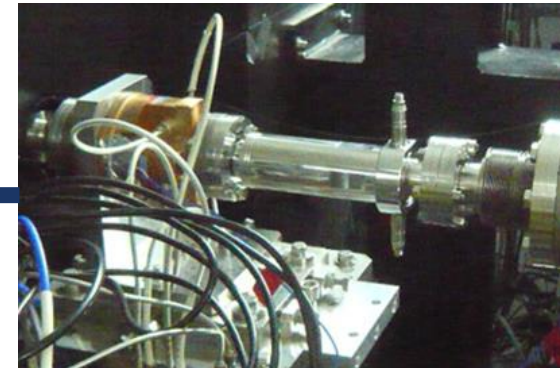
**FPGA-based digital
processor**



Kicker drive amplifier

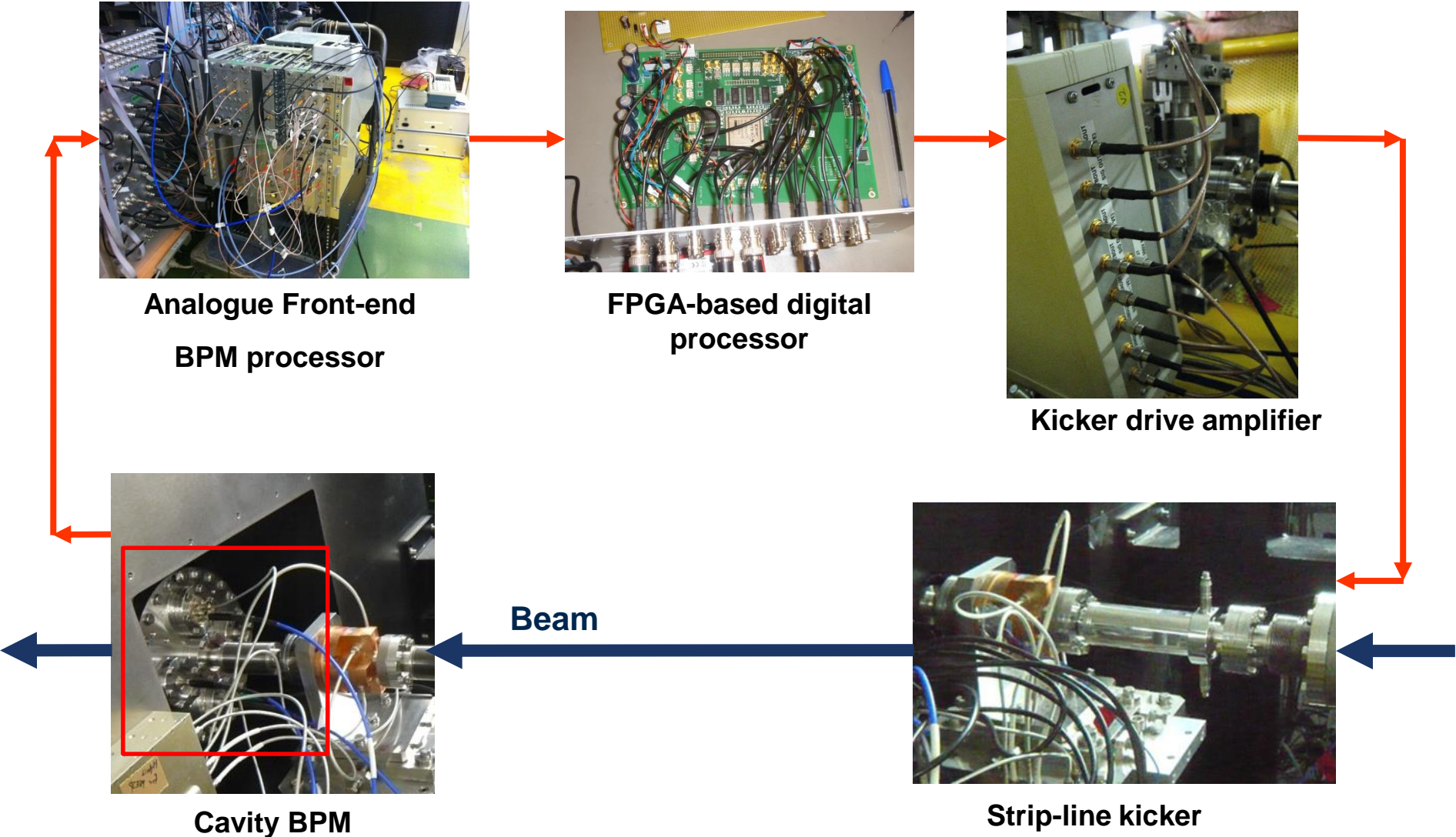


Cavity BPM



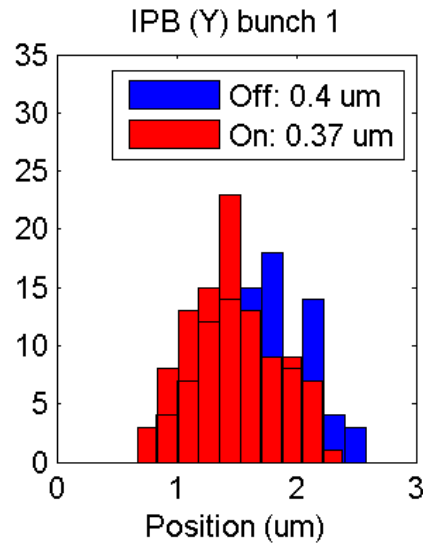
Strip-line kicker

Beam

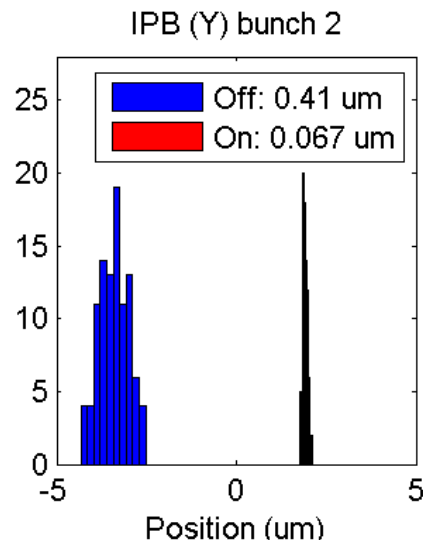


IPFB results

**Bunch 1:
not corrected,
jitter ~ 400nm**



**Bunch 2:
corrected,
jitter ~ 67nm**



Corrected jitter 67nm

→ resolution 47nm

IPFB results: time sequence

