Silicon Pixel R&D for CLIC

38th International Conference
on High Energy Physics (ICHEP 2016)

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Chicago

Dominik Dannheim (CERN)
on behalf of the
CLIC detector and physics (CLICdp) collaboration

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AIDA 2020

CERN

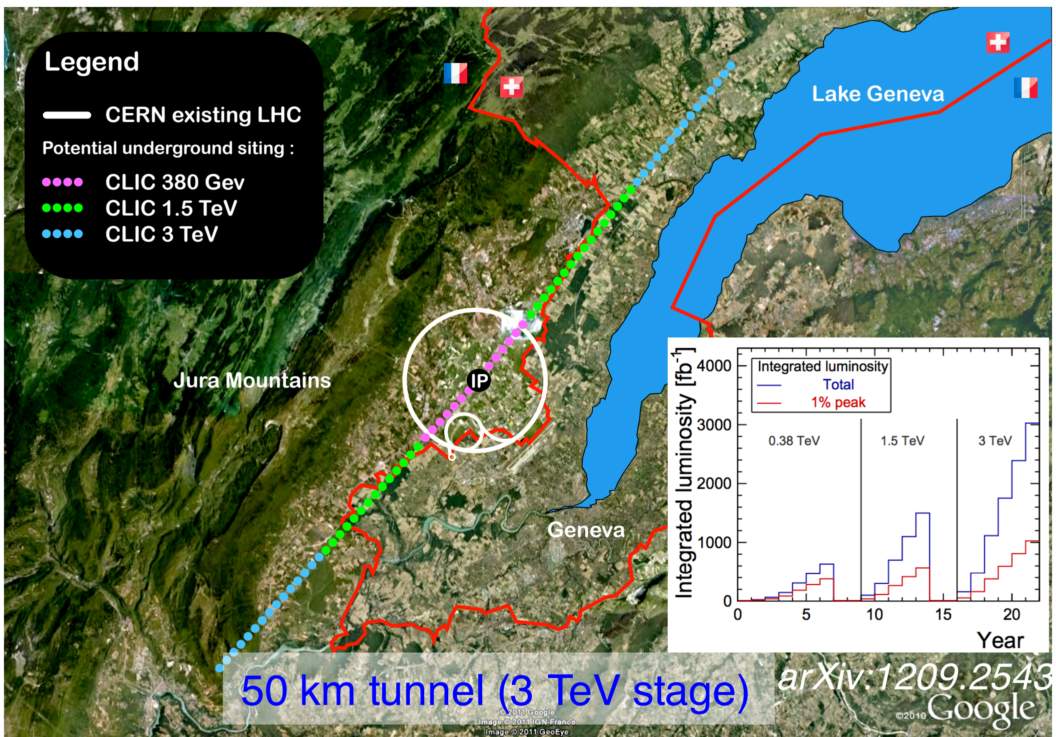
Outline

- CLIC vertex- and tracking detector requirements
- Hybrid pixel-detector assemblies with:
  - thin planar sensors
  - small-pitch planar sensors
  - small-pitch active sensors
- Integrated CMOS pixel sensors
- Summary / Conclusions

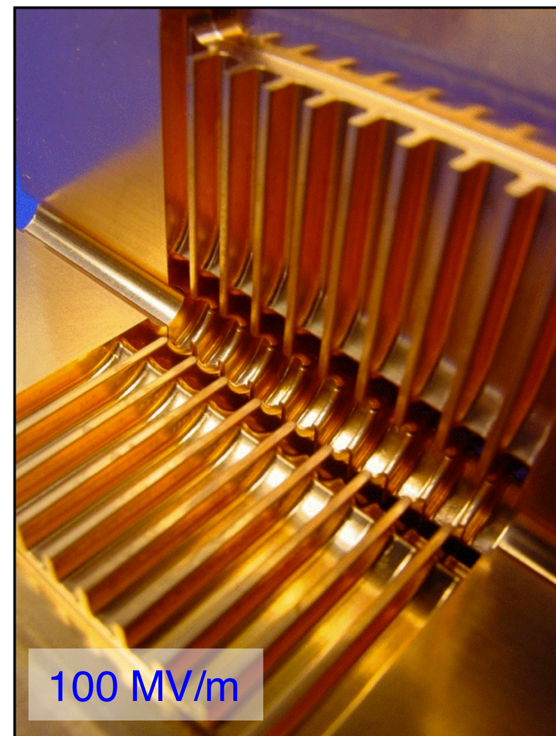
CLIC

- CLIC (Compact LInear Collider): linear e^+e^- collider concept for post HL-LHC phase
- $\sqrt{s}$ from few hundred GeV up to 3 TeV (two-beam acceleration with ~100 MV/m)
- Physics goals:
  - Precision measurements of SM processes (Higgs, top)
  - Precision measurements of new physics potentially discovered at 14 TeV LHC
  - Search for new physics: unique sensitivity to particles with electroweak charge

Possible staged CLIC implementation near CERN

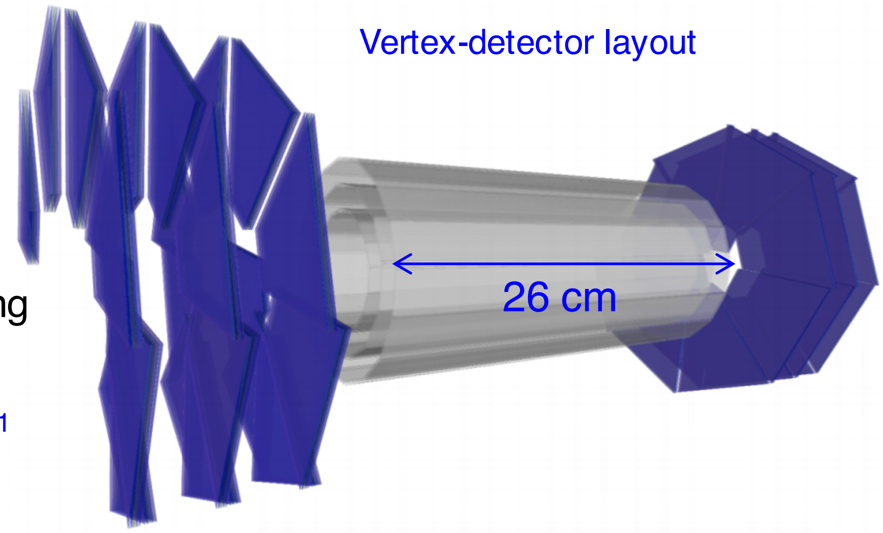


CLIC accelerating structure

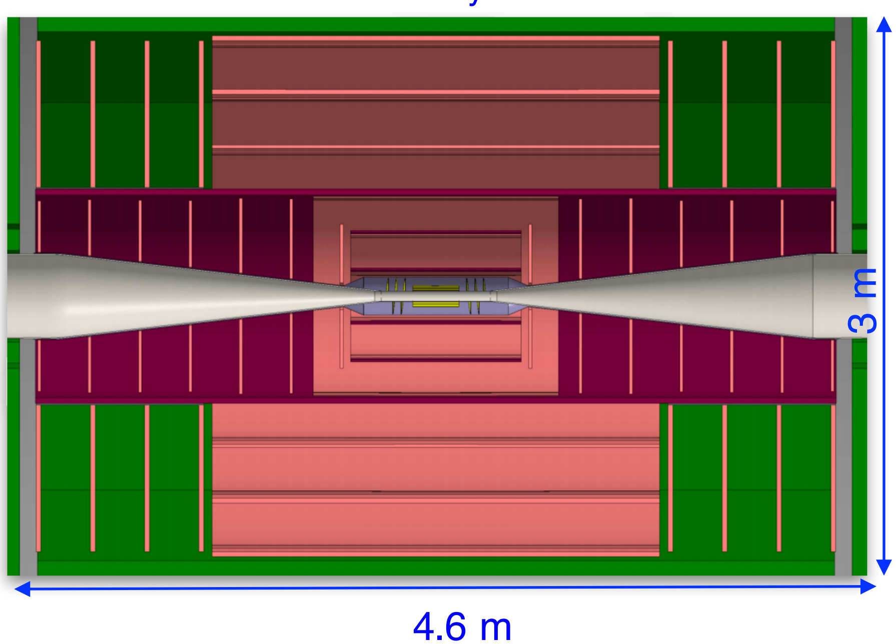


CLIC vertex-detector and tracker requirements

Vertex detector:
- efficient tagging of heavy quarks through precise determination of displaced vertices:
  - → good single point resolution: σ_{SP}~3 μm
    - → small pixels <~25x25 μm², analog readout
  - → low material budget: X ≲ 0.2% X_0 / layer
    - → low-power ASICs (~50 mW/cm²) + gas-flow cooling



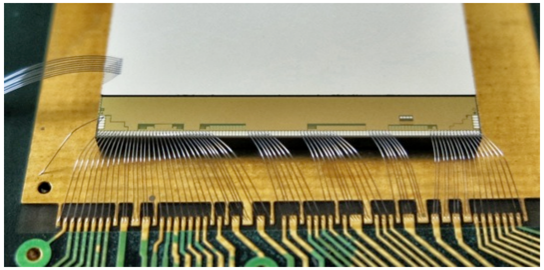
Tracker:
- Good momentum resolution: $\sigma(p_T) / p_T^2 \sim 2 \times 10^{-5}$ GeV^{-1}
  - → 7 μm single-point resolution (≲50 μm pitch)
  - → many layers, large outer radius (~90 m² surface)
  - → ~1-2% X0 per layer
    - → low-mass supports + services



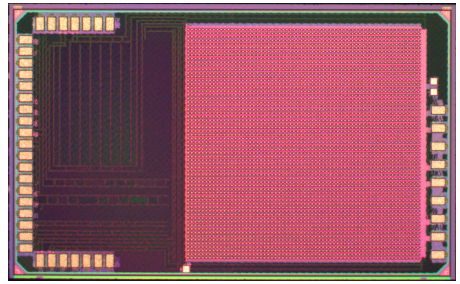
Both:
- 20 ms gaps between bunch trains
  - → trigger-less readout, pulsed powering
- few % maximum occupancy from beam backgrounds
  - → sets inner radius and limits cell sizes
  - → time stamping with ~10 ns accuracy
    - → depleted sensors (high resistivity / high voltage)
- moderate radiation exposure (~10⁴ below LHC!):
  - NIEL: < 10^{11} $n_{eq}/cm^2/y$
  - TID: < 1 kGy / year

Vertex and tracker technology R&D

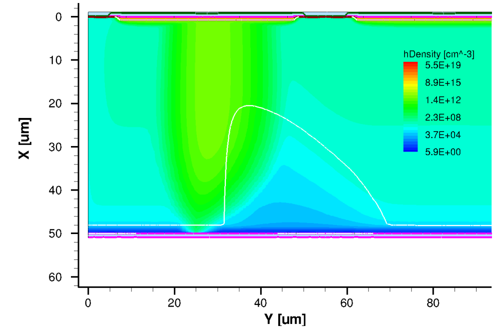
Sensors



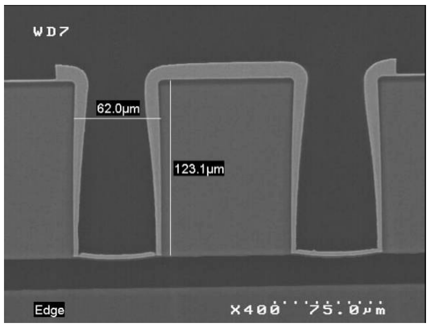
Readout ASICs



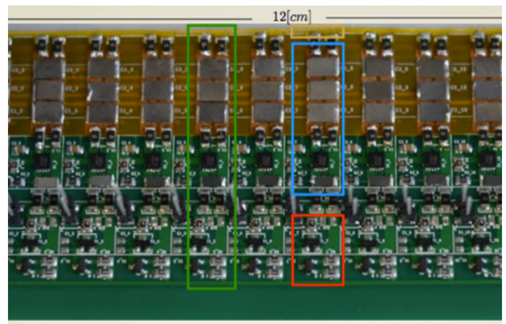
Simulations



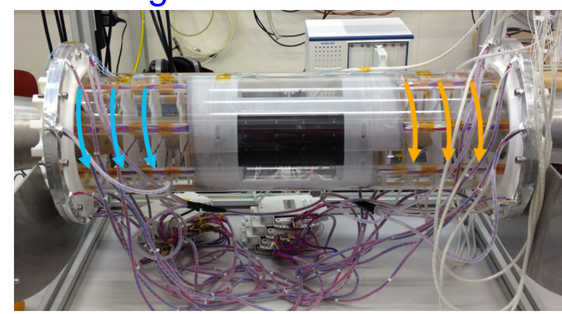
Interconnects



Powering

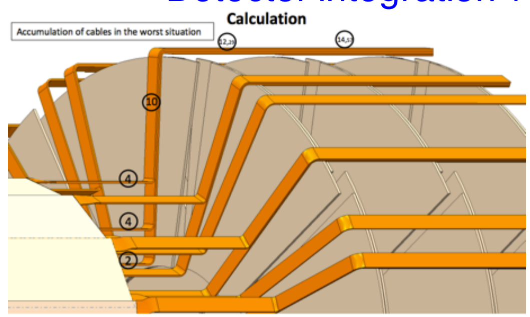


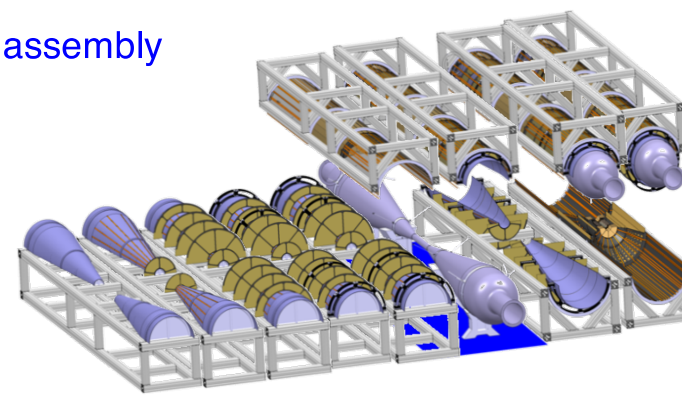
Cooling



Light-weight supports

Detector integration + assembly





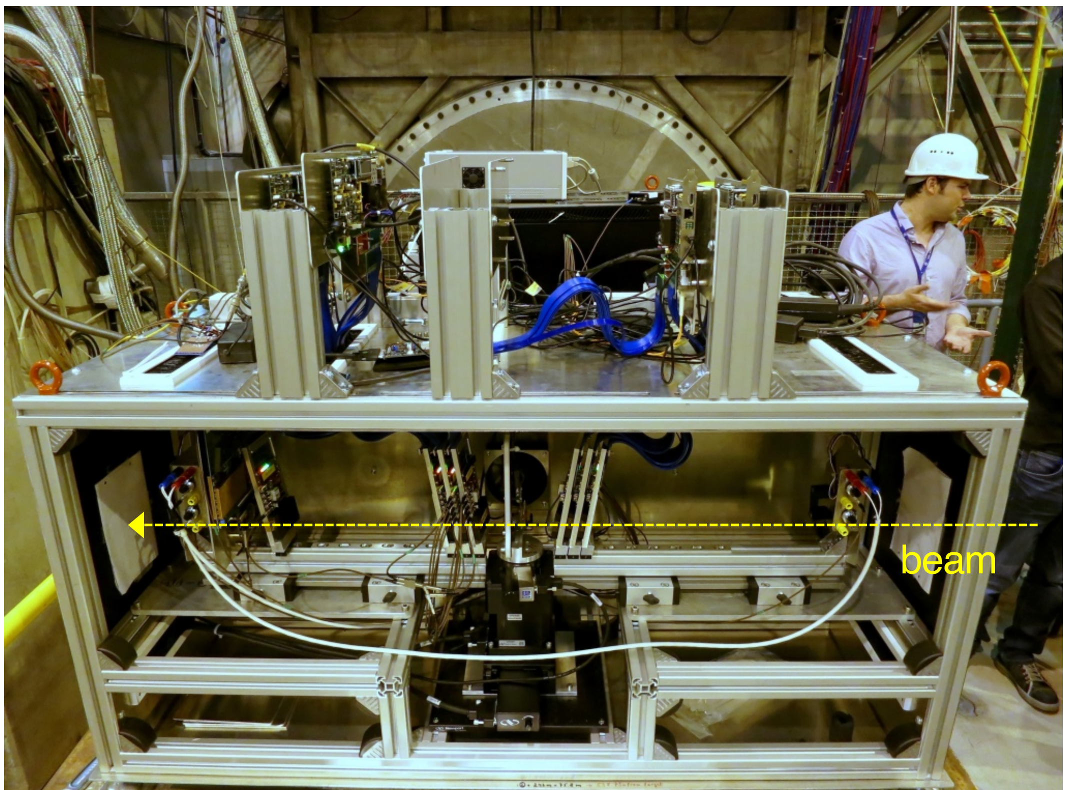
- Integrated R&D effort, simultaneously addressing CLIC vertex+tracking detector challenges
- Examples of recent developments on the following slides (focus on sensors & readout)

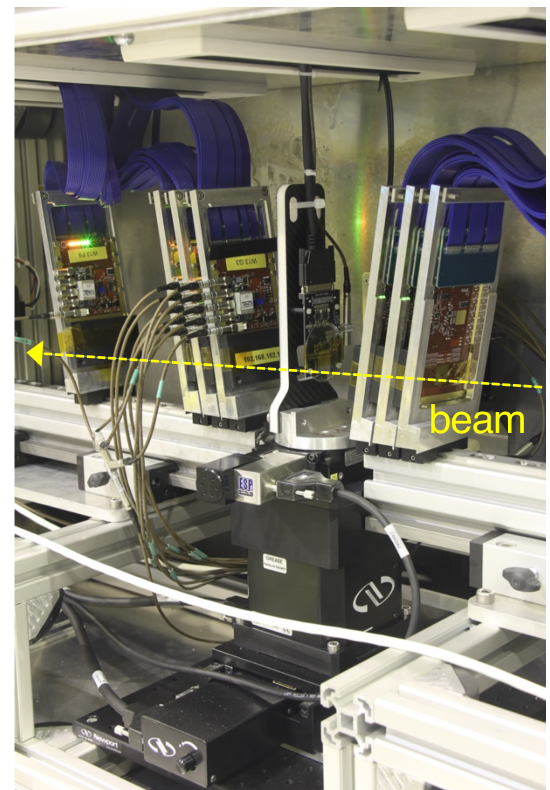
Test-beam data taking

EUDET/AIDA telescopes:
- Used for initial test-beam studies at DESY II, CERN PS and CERN SPS
- Rolling-shutter r/o over ~230 μs
  → limited rate and timing capabilities
- Pointing resolution at DUT ~1.6-3 μm

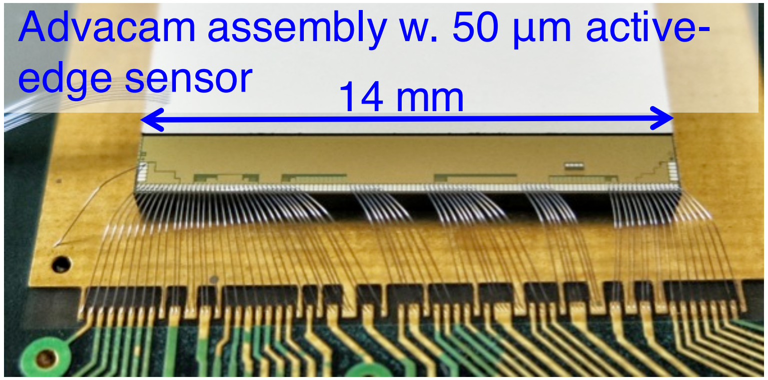
CERN-LCD Timepix3 telescope:
- Permanent installation at CERN SPS H6B
- Movement and rotation stages for automatic scans
- High rate: up to 10M particles / s
- Track timing with <2 ns accuracy
- Track pointing resolution at DUT ~2 μm

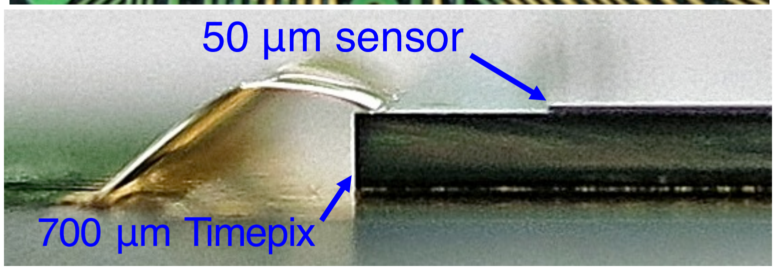
CERN-LCD Timepix3 telescope in SPS H6B





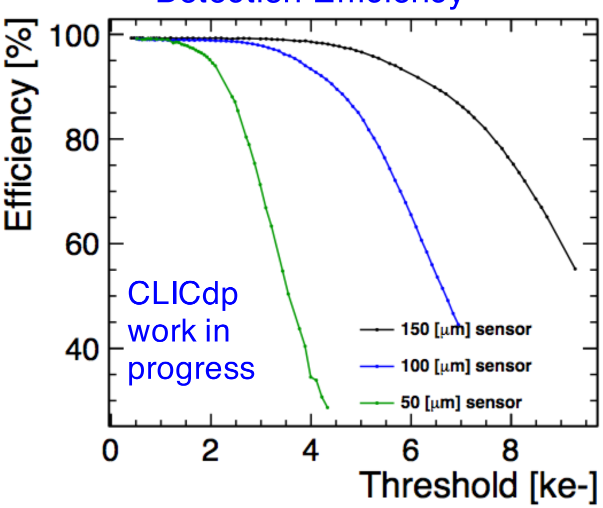
Thin sensor test-beam results



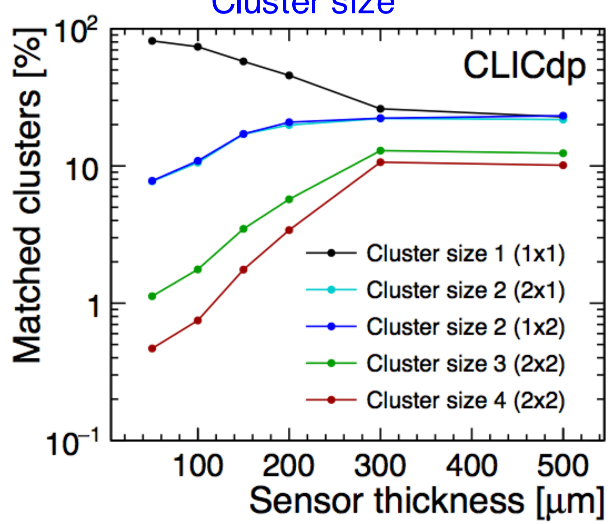


- Test-beam measurements of Timepix/Timepix3 assemblies (Micron, Advacam) with different sensor thicknesses, 55 µm pixel pitch
- Goal: test feasibility of ultra-thin sensors with minimized inactive regions
  - High detection efficiency (>99%) under normal operating conditions, even for 50 µm sensors
  - Resolution limited by single-pixel clusters → worse resolution for thinner sensors

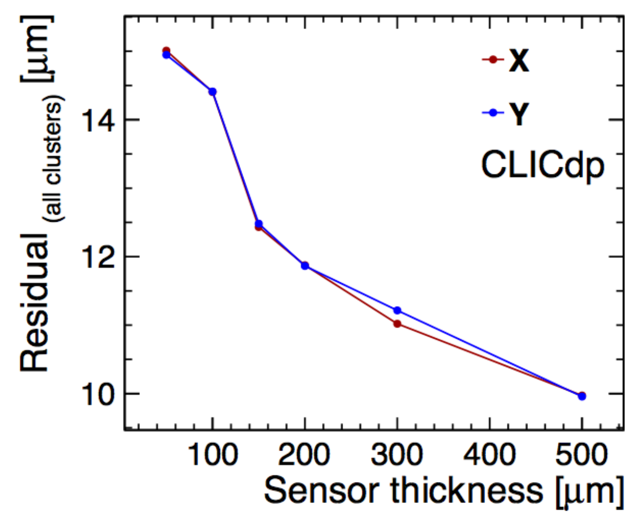
Detection Efficiency



Cluster size

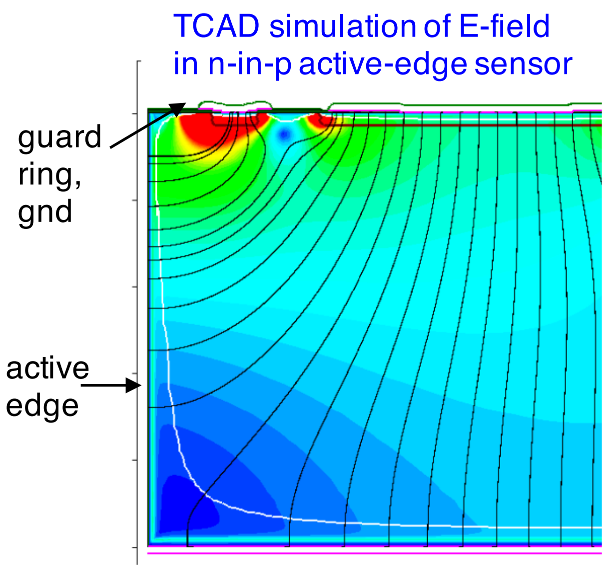


Resolution

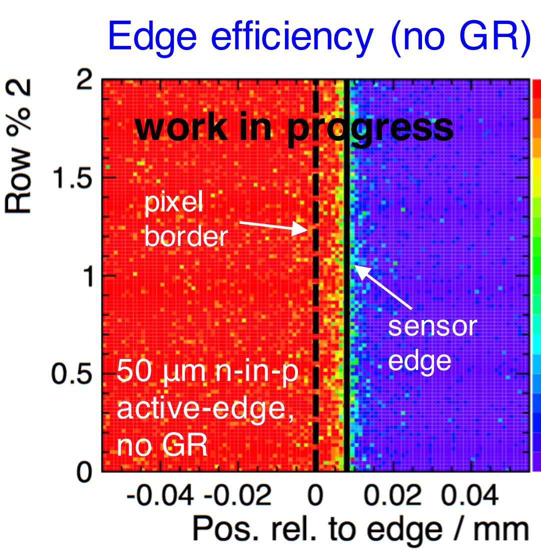


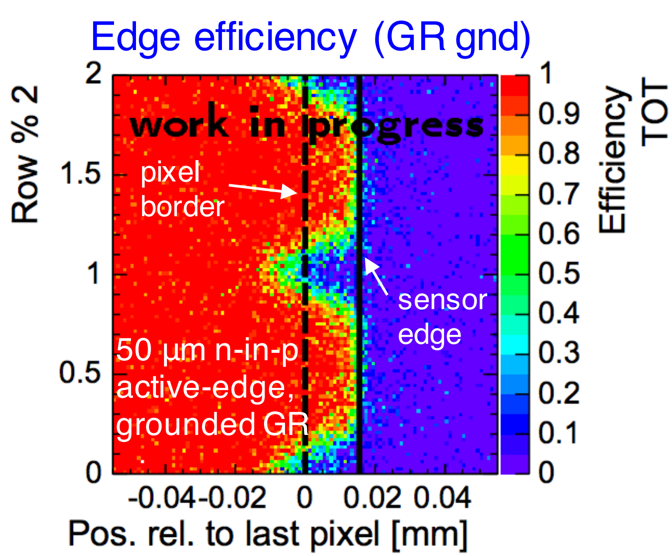
CLICdp-Note-2016-001

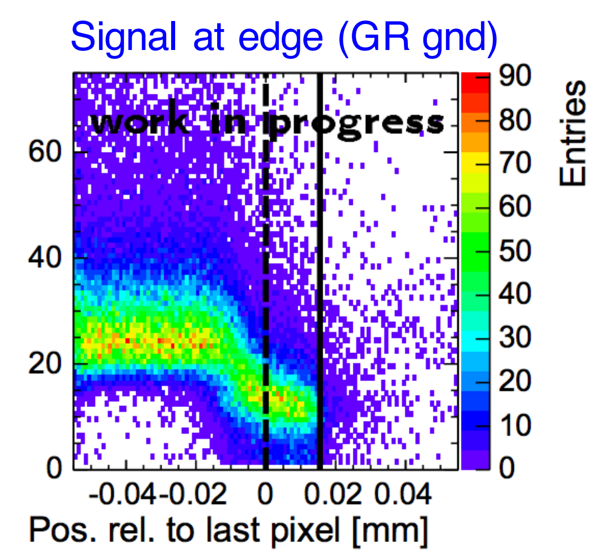
Active edge sensors



- Deep Reactive Ion Etching (DRIE) process:
  - Implantation on the sensor sidewalls: extension of the backside electrode to the edge
  - Efficiency extends to the physical edge → allows for seamless tiling of sensors
- Comparing different edge layouts: w/o guard ring (GR), floating GR and grounded GR → signal loss to GR for very thin sensors, in agreement with TCAD simulations







Hybrid r/o technology: CLICpix

- 65 nm CMOS hybrid r/o chip, targeted to CLIC vertex detectors
- based on Timepix/Medipix chip family,

- demonstrator chip: 64 x 64 pixel matrix
- 25 µm pixel pitch
- simultaneous 4-bit time (ToA) and energy (ToT) measurement per pixel

→ front-end time slicing < 10 ns

- selectable compression logic: pixel, cluster + column-based

→ full chip r/o in less than 800 µs (at 10% occup., 320 MHz r/o clock)

- power pulsing scheme

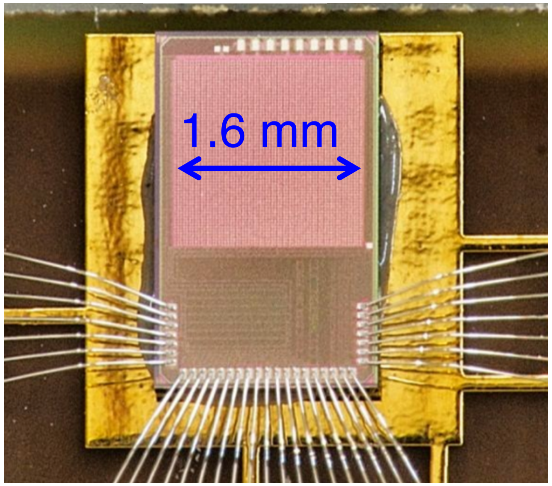
→ P_{avg} < 50 mW/cm^2

- lab measurements

→ performance in agreement with simulations

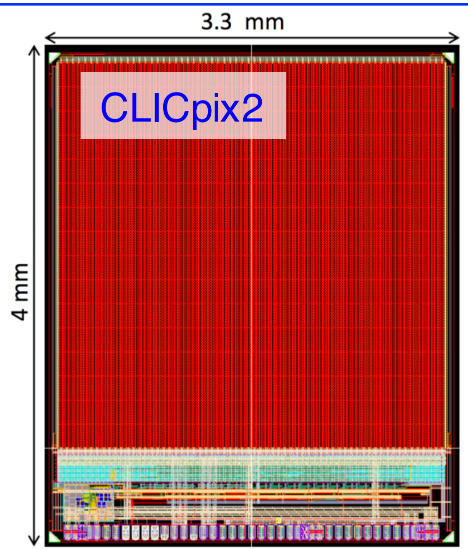
- test assemblies with planar and active HV-CMOS sensors

CLICpix



New version CLICpix2:

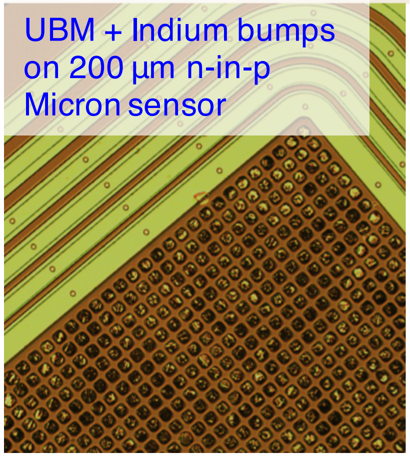
- 128x128 pixels
- 5 bit ToT, 8 bit ToA
- Improved I/O
- design currently under validation (UVM)
- to be submitted in coming weeks

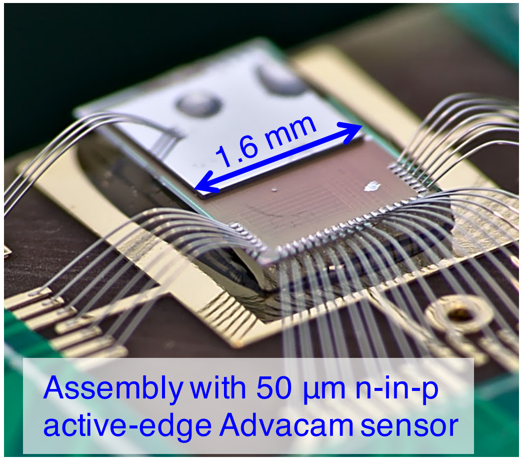


LCD-Note-2012-018

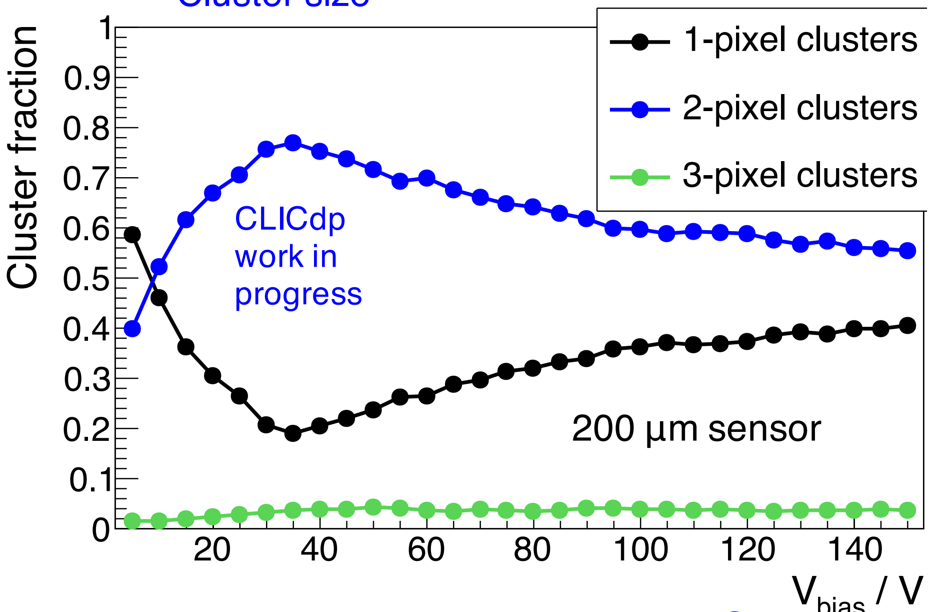
CLICpix planar sensor assemblies

- Single-chip bump-bonding process for 25 µm pitch developed at SLAC (C. Kenney, A. Tomada)
- Results for 3 test assemblies with 200 µm Micron sensors :
  - 0.2-3% unconnected channels
  - 1-2% shorted channels
  - Test-beam measurements:
    - Operation threshold ~1000 e^-, V_{dep}~35 V
    - High detection efficiency (>99.5%)
    - ~20% single-pixel clusters at V_{dep}
    - ~4 µm single-point resolution
- Validation of assembly with 50 µm Advacam active-edge sensor ongoing

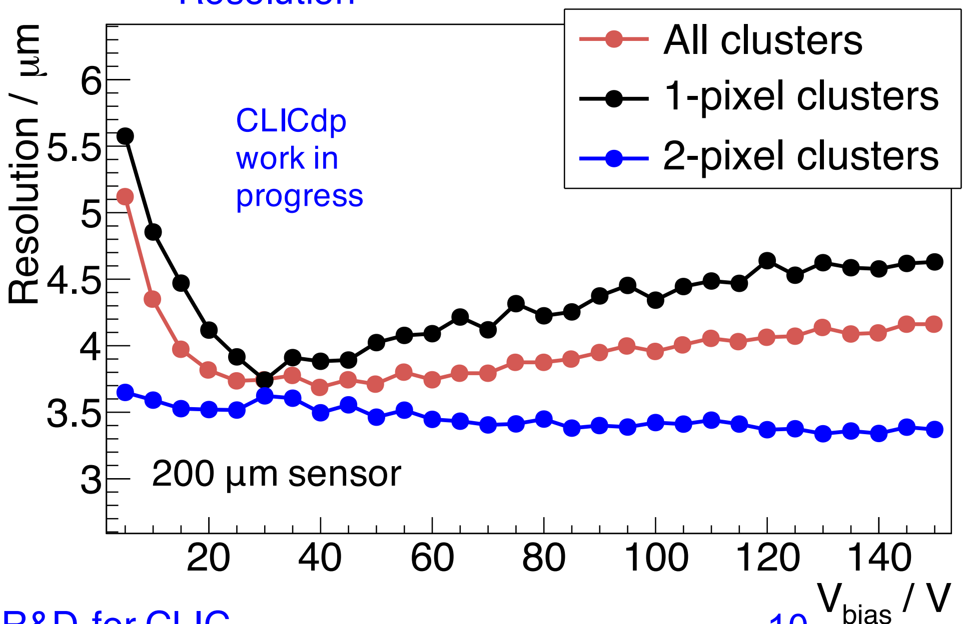




Cluster size



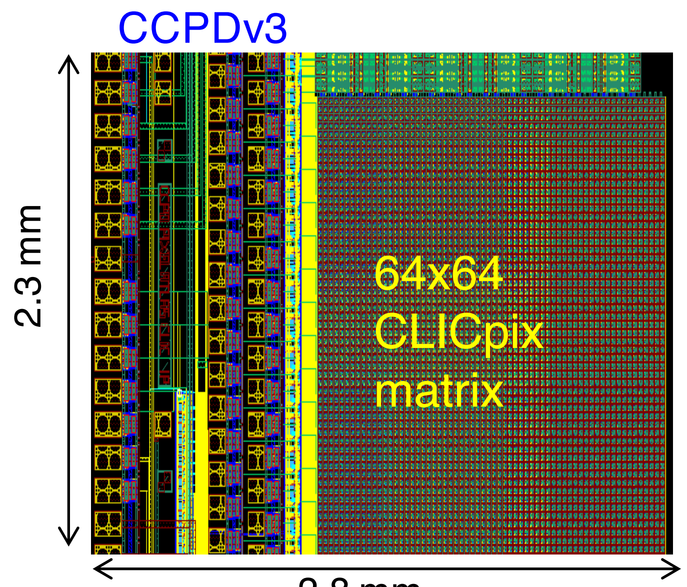
Resolution



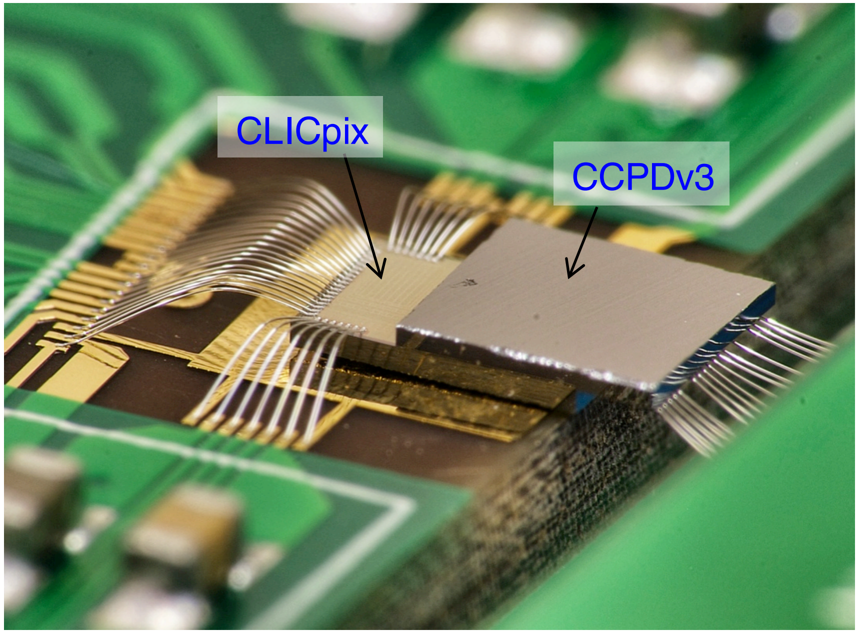
HV-CMOS active sensor with capacitive coupling

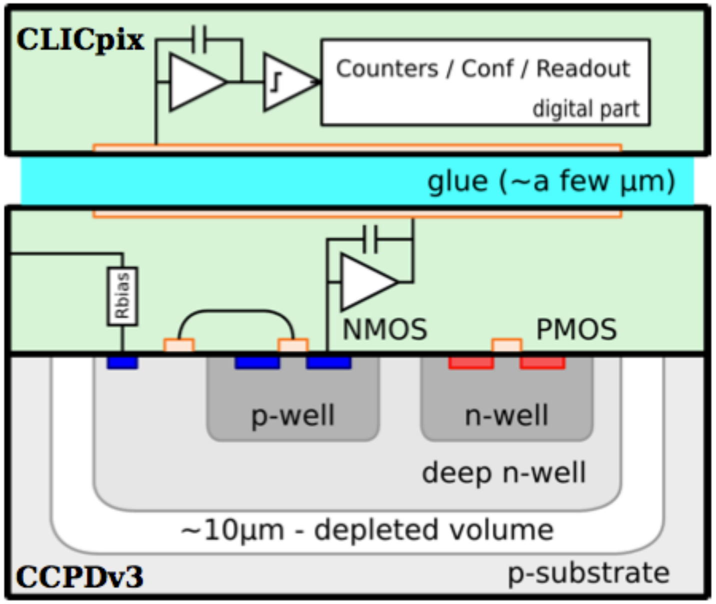
Capacitive Coupled Pixel Detector (CCPD)

- Prototype for ATLAS (FEI4) and CLIC: CCPDv3
- Commercial 180 nm High-Voltage-CMOS process
- V_{bias}~30-90 V → depletion layer ~10-20 μm
- 2-stage amplifier, capacitive coupling to readout ASIC through thin glue layer (few μm)
- Includes 64x64 matrix (25 μm pitch)
- glue assemblies with CLICpix readout chips
  → lab and test-beam results (next slide)
- new improved chip version C3PD matching CLICpix2
  → chip functional, lab tests ongoing



Ivan Peric



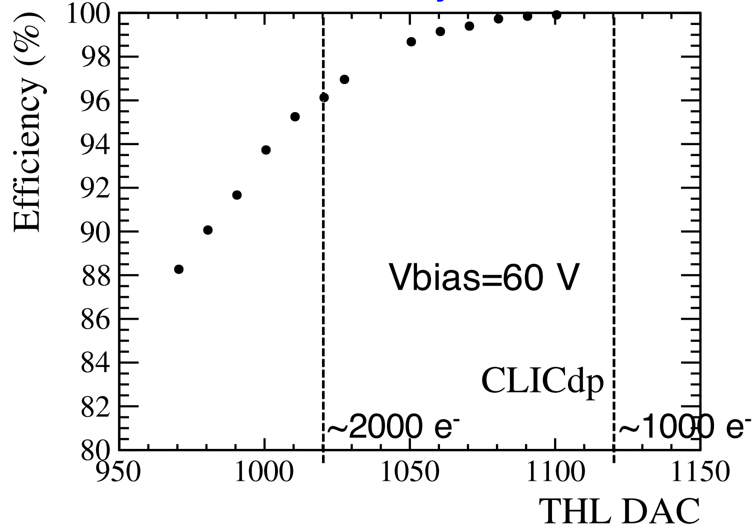


Nucl. Instrum. Meth. A731 (2013) 131 *Nucl. Instrum. Meth. A823 (2016) 1*

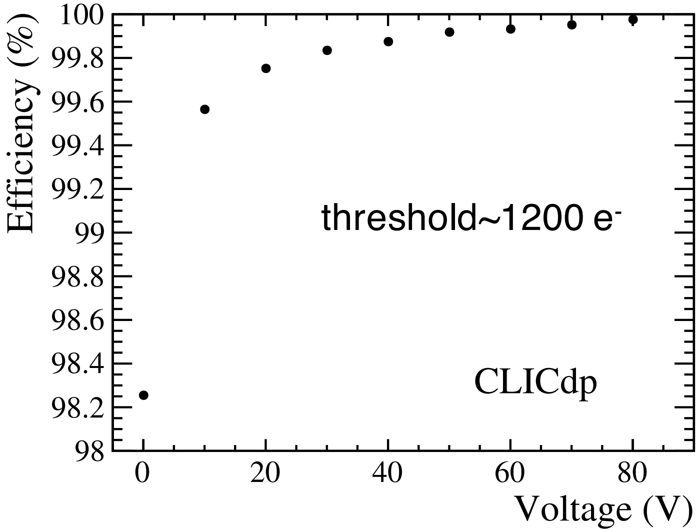
CLICpix+CCPDv3 test-beam results

CERN SPS test beam with AIDA telescope:
- High detection efficiency, even without bias (diffusion)
- Measured mean charge (ToT) varies across matrix → non-uniformity of glue thickness, observed in early assemblies produced without control of planarity
- ~6 µm single-point resolution

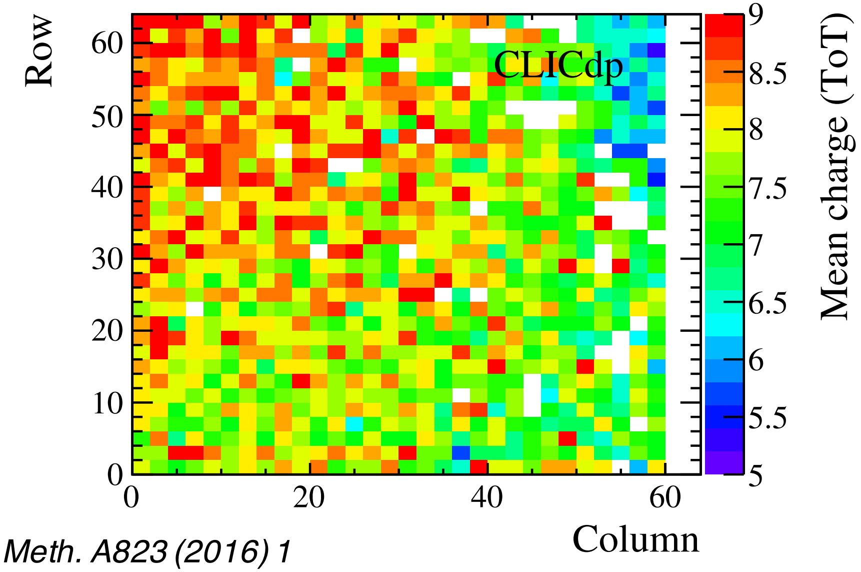
Detection efficiency vs. threshold



Detection efficiency vs. bias



ToT uniformity



CLICdp-Pub-2015-003

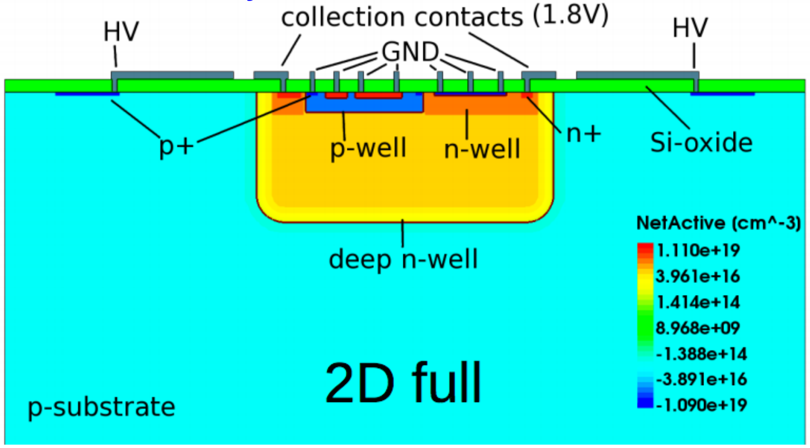
Nucl. Instrum. Meth. A823 (2016) 1

HV-CMOS TCAD simulation

- Implemented CCPDv3 pixel layout in TCAD
- 2-D and 3-D transient simulation for MIPs at different positions within pixel → input for ASIC simulation

- Measured leakage current breakdown of ~90 V well reproduced
- Fast rise of collected charge within ~ns (drift in depleted volume)
- Increasing pulse height over hundreds of ns (diffusion in bulk)

Layout for 2-D simulation



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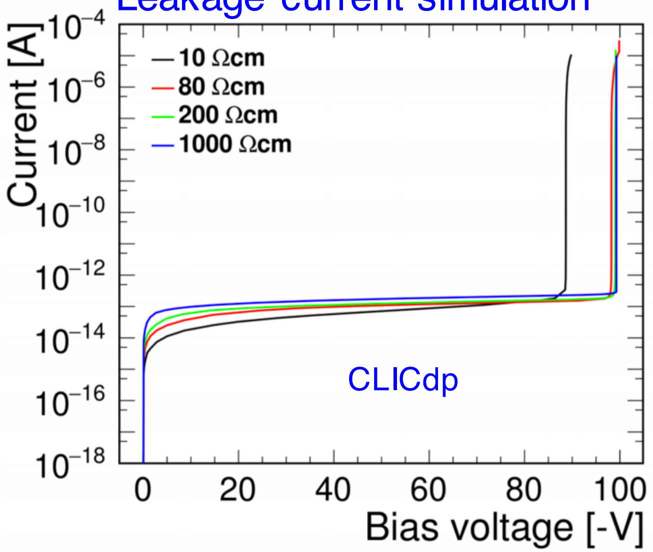
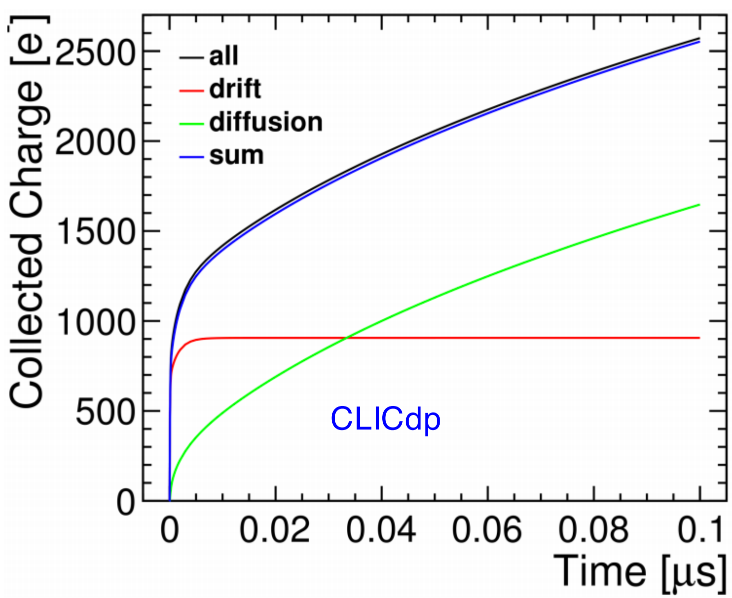
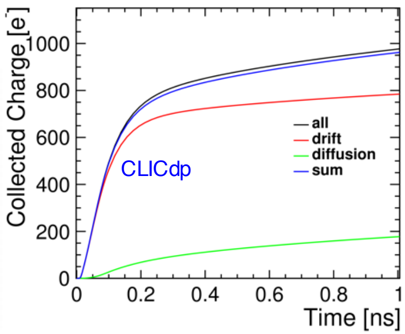
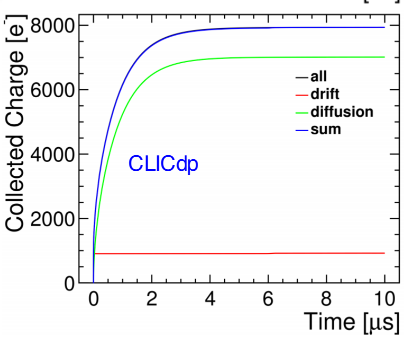
Leakage current simulation



MIP response in CCPDv3





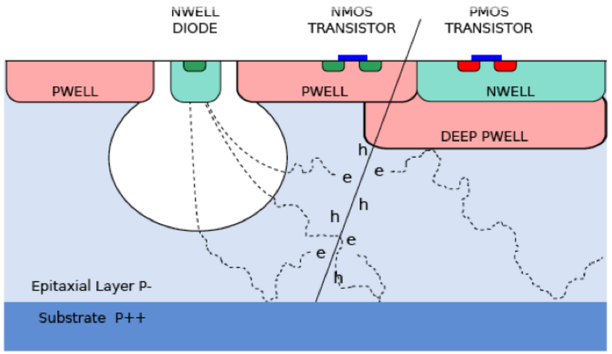


Integrated CMOS technologies for tracker

TowerJazz 180 nm High-Resistivity CMOS:

- Quadruple well process with full CMOS: n-wells shielded by deep p-wells
- 15-40 μm / 1-8 kΩcm epitaxial layer, not fully depleted (Vbias ≲ 6 V)
- ALICE Investigator analog test chip
- Pixel sizes: 20x20 to 50x50 μm^2
- Optimization of collection-diode geometry to minimize capacitance (~2 fF)
- Readout with external sampling ADCs
- Integration in CLIC test-beam setup
  → good time resolution obtained (few ns)

TowerJazz HR CMOS process



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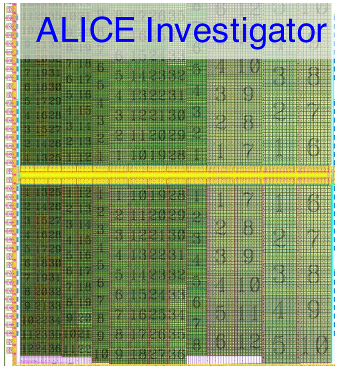
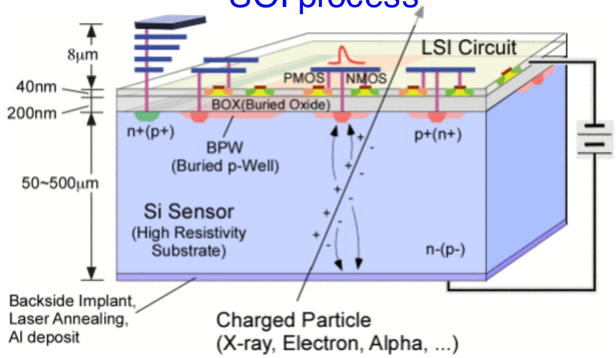


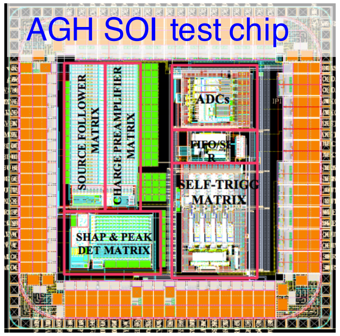
NIM A 765 (2014) 177

Lapis 200 nm SOI:

- CMOS sensor on Silicon On Insulator (SOI) wafers
- Electronics on low resistivity wafer, separated by buried oxide from fully depleted high-resistivity sensing layer
- Test-chip from AGH Cracow:
  - Different pixel sizes (≥ 30 x 30 μm^2)
  - Targeted towards CLIC requirements (position, amplitude and few ns timing)
  - Integration in CLIC test-beam setup
    → chip functional, data taking and analysis ongoing

SOI process





arXiv:1507.00864

Summary and Conclusions

- CLIC accelerator provides:
  - unique potential for discovery and precision physics at the TeV scale
  - challenging requirements for vertex and tracking detectors
- Ongoing integrated R&D program on CLIC vertex + tracking detectors:
  - Sensor and readout technologies for precision measurements:
    - Hybrid readout ASICs with planar sensors
    - Hybrid readout ASICs with active HV-CMOS sensors
    - Integrated CMOS sensors
  - Not shown today: powering, cooling and mechanical integration studies incorporating realistic constraints

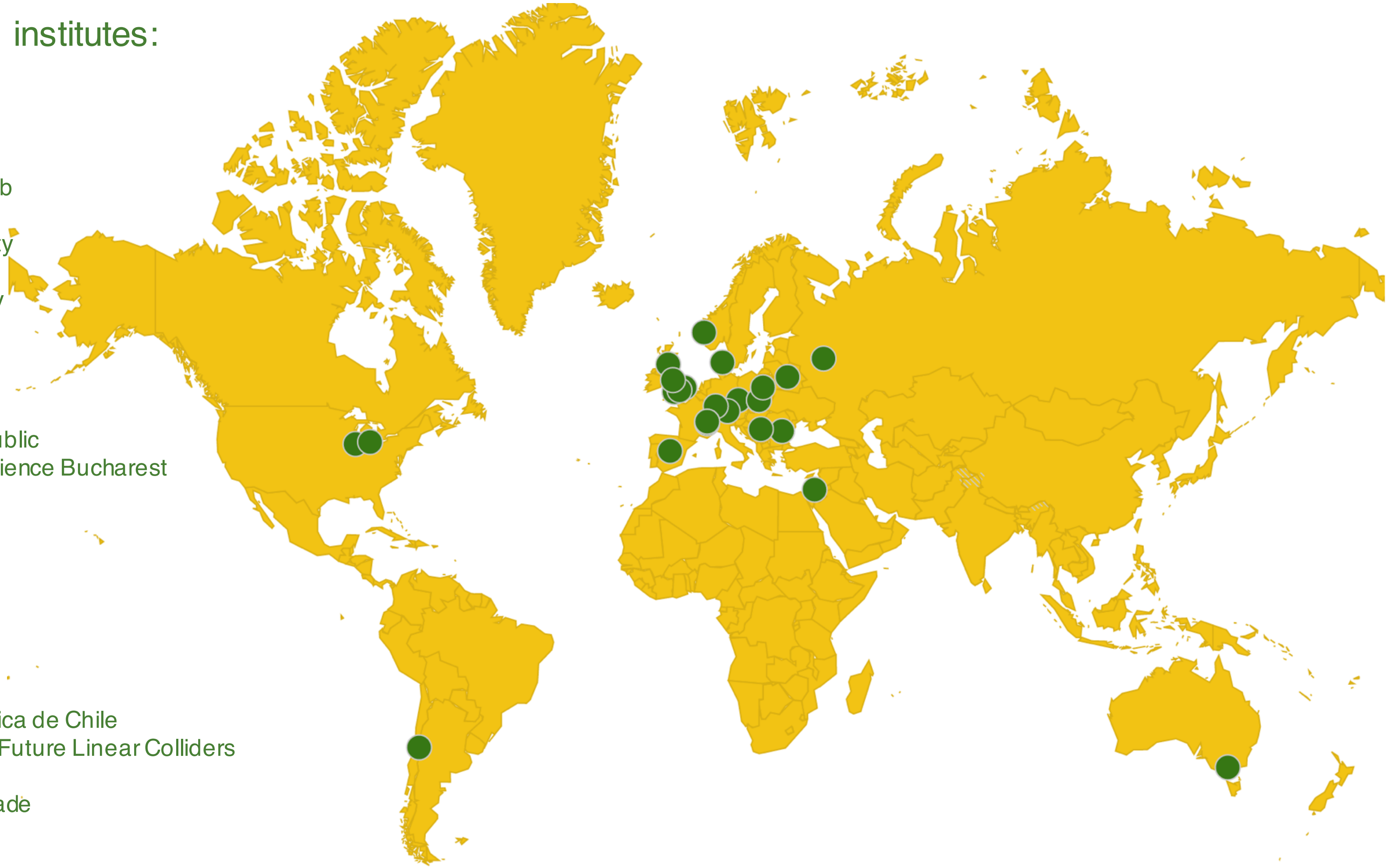
Thanks to everyone who provided material for this talk!

Additional material

CLIC detector & physics collaboration

CLICdp member institutes:

- Aarhus University
- ACAS Australia
- AGH-UST Cracow
- Argonne National Lab
- Bergen University
- Birmingham University
- Bristol University
- Cambridge University
- CERN
- DPNC Geneva
- Glasgow University
- IFJPAN Cracow
- IPASCR Czech Republic
- Institute of Space Science Bucharest
- JINR Dubna
- KIT IPE Karlsruhe
- LAPP Annecy
- Liverpool University
- Michigan University
- MPI Munich
- NC PHEP Belarus
- Oxford University
- Pontificia Univ. Catolica de Chile
- Spanish Network for Future Linear Colliders
- Tel Aviv University
- Vinca Institute Belgrade
- University of Warsaw

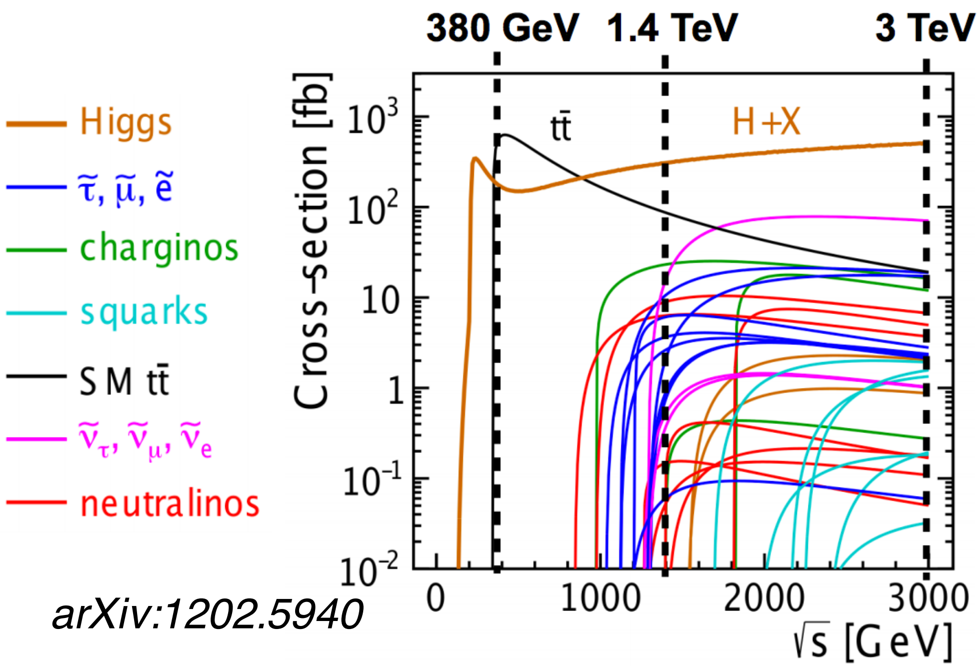


•The CLICdp collaboration is addressing detector and physics issues for the future Compact Linear Collider (CLIC) http://clicdp.web.cern.ch/
•CERN acts as host laboratory
•Currently 27 institutes from 17 countries
•The CLIC accelerator R&D is being conducted in collaboration with ~48 institutes

CLIC physics program

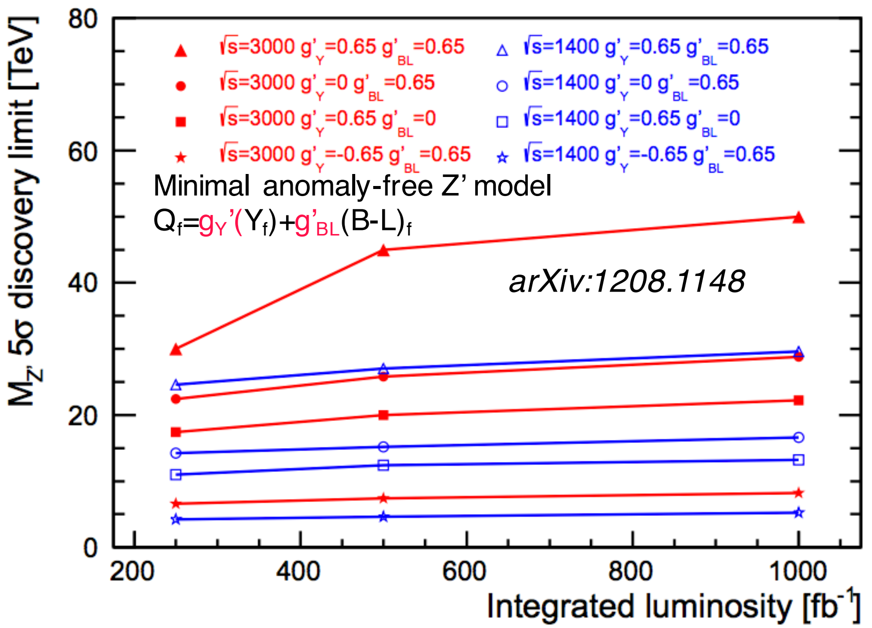
- CLIC (Compact LInear Collider): linear e^+e^- collider concept for post HL-LHC phase
- Staged construction: $\sqrt{s}$ from few hundred GeV up to 3 TeV
- Physics goals:
  - Precision measurements of SM processes (Higgs, top)
  - Precision measurements of new physics potentially discovered at 14 TeV LHC
  - Search for new physics: unique sensitivity to particles with electroweak charge

CLIC physics reach: SM + SUSY example



arXiv:1202.5940

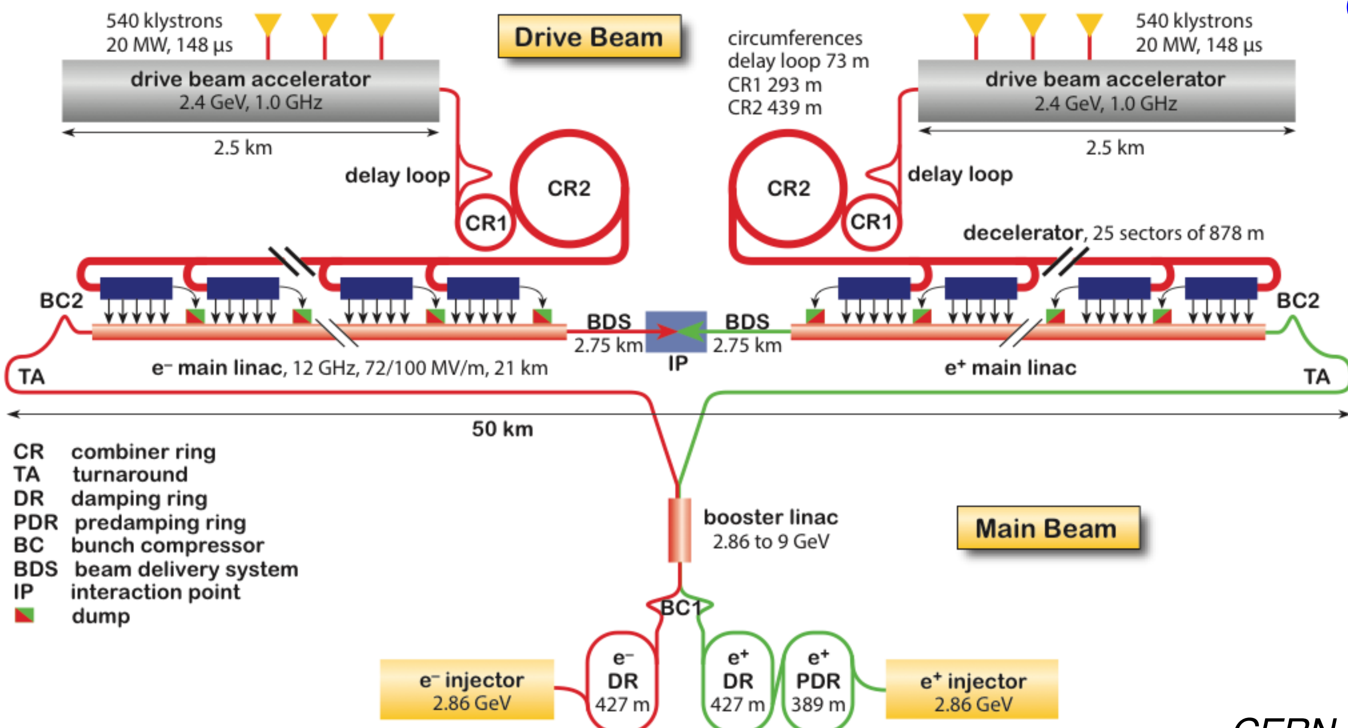
Z' 5σ mass discovery limit from $e^+e^- \rightarrow \mu^+\mu^-$



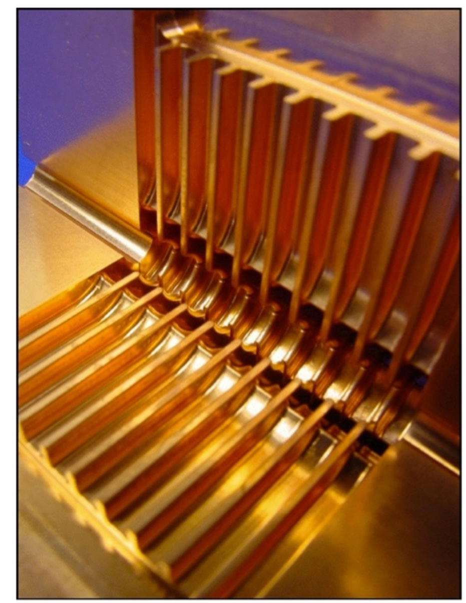
CLIC accelerator

- Linear e^+e^- collider
- 2-beam acceleration scheme, operated at room temperature
- Gradient: 100 MV/m
- $\sqrt{s}$ up to 3 TeV
- Luminosity: 6×10^{34} $cm^{-2}s^{-1}$ (at 3 TeV)
- Physics + Detector studies for 350 GeV - 3 TeV

CLIC layout at 3 TeV



CLIC accelerating structure



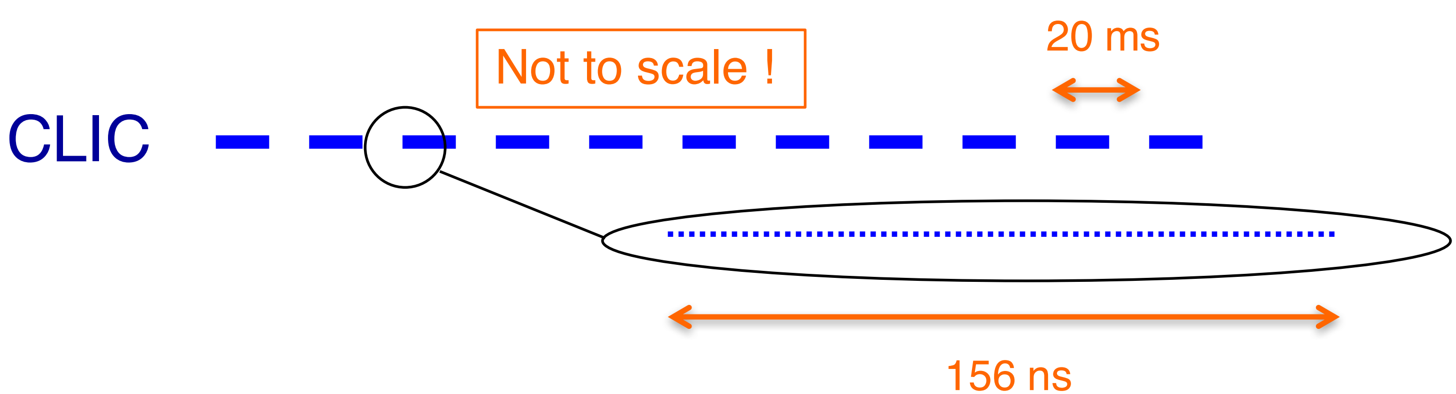
CERN-2012-007

Machine parameters

	LHC at 14 TeV	CLIC at 3 TeV
L ($cm^{-2}s^{-1}$)	1×10^{34}	6×10^{34}
BX separation	25 ns	0.5 ns
#BX / train	N/A	312
Train duration	N/A	156 ns
Train repetition	N/A	50 Hz
Duty cycle	~1	0.00078%
σ_x / σ_y [nm]	15000 / 15000	≈ 45 / 1
σ_z [μm]	~50000	44

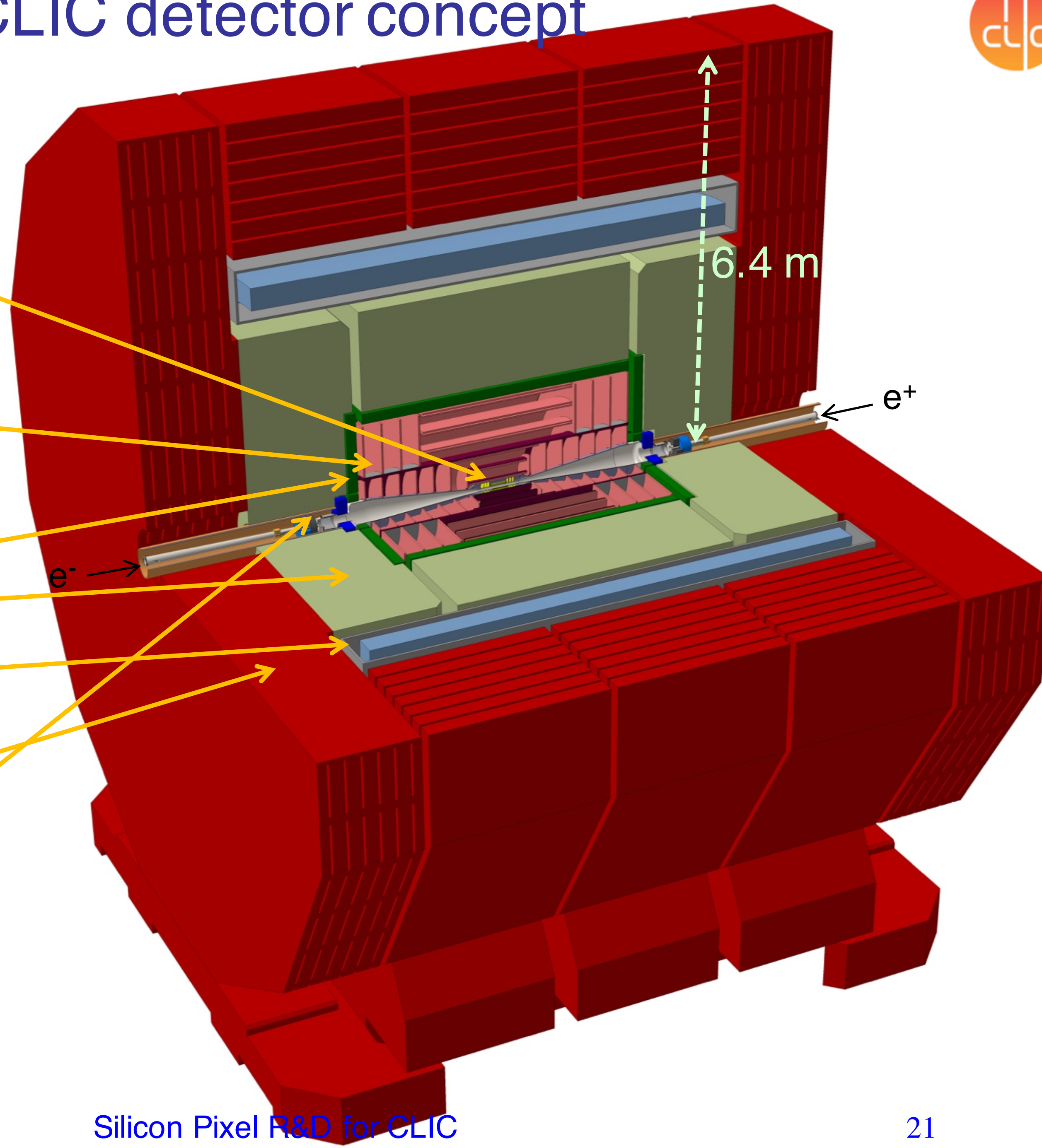
drives timing requirements for detectors

very small beam sizes at interaction point



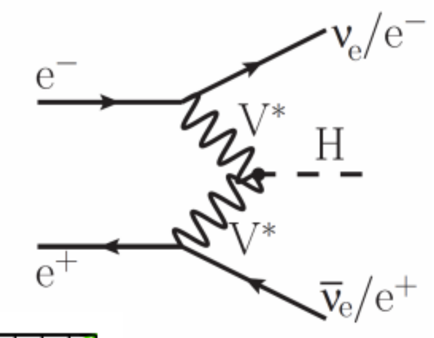
CLIC detector concept

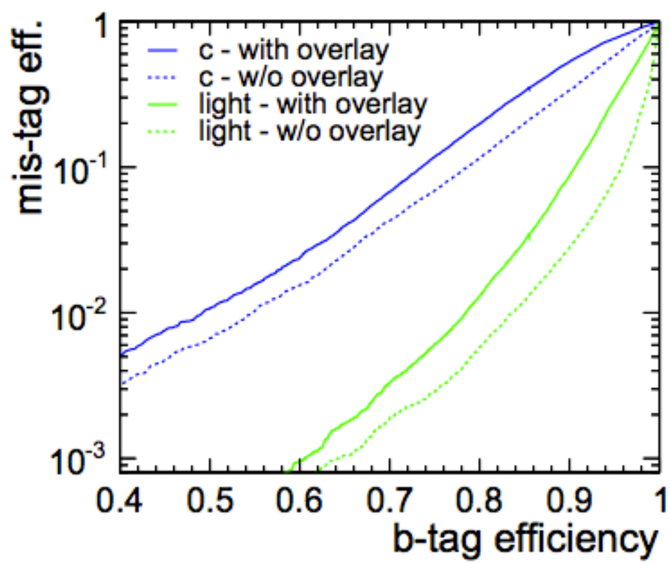
- low-mass **vertex detector** with ~25x25 μm^2 pixels
- **silicon tracker**
- fine-grained **PFA calorimetry**, 1+7.5 Λ_i W-ECAL + Fe-HCAL
- 4 T **solenoid**
- **return yoke** with muon ID
- Complex instrumented **forward region**

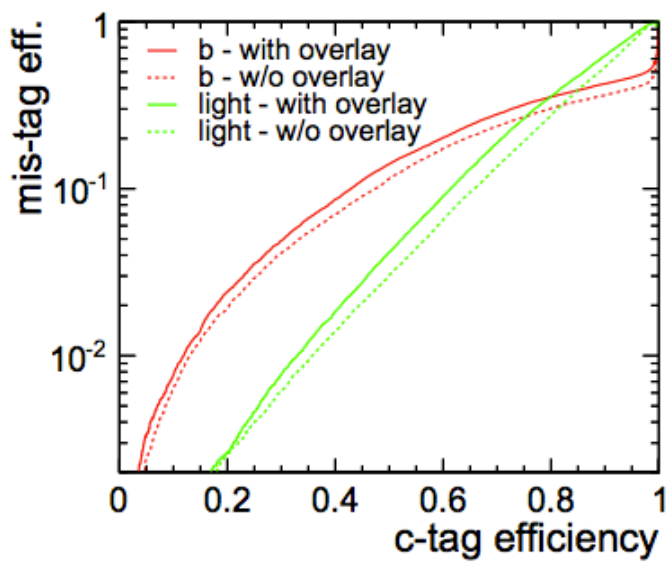


Flavor tagging: impact on physics performance

- $e^+e^- \rightarrow H\nu\nu$: dominating Higgs production process at $\sqrt{s}$=3 TeV
- σ × BR measurement for the decays to bb and cc
- flavor tagging crucial for achievable precision







$\sqrt{s}$=3 TeV
L_{int}=2 ab^{-1}

$p_{T,jet}$~70 GeV
E_{jet}~130 GeV

channel	stat. unc. on σxBR	change for +/-20% fake r.
H→bb	0.23%	0.24% / 0.21%
H→cc	3.1%	3.6% / 2.6%

LCD-Note-2011-036, CLICdp Note-2014-002

- consider ±20% change in fake rates
- sizeable effect, in particular for H→cc: 30% more integ. luminosity required for same precision when increasing fake rate by 20% (>1 year of additional running!)

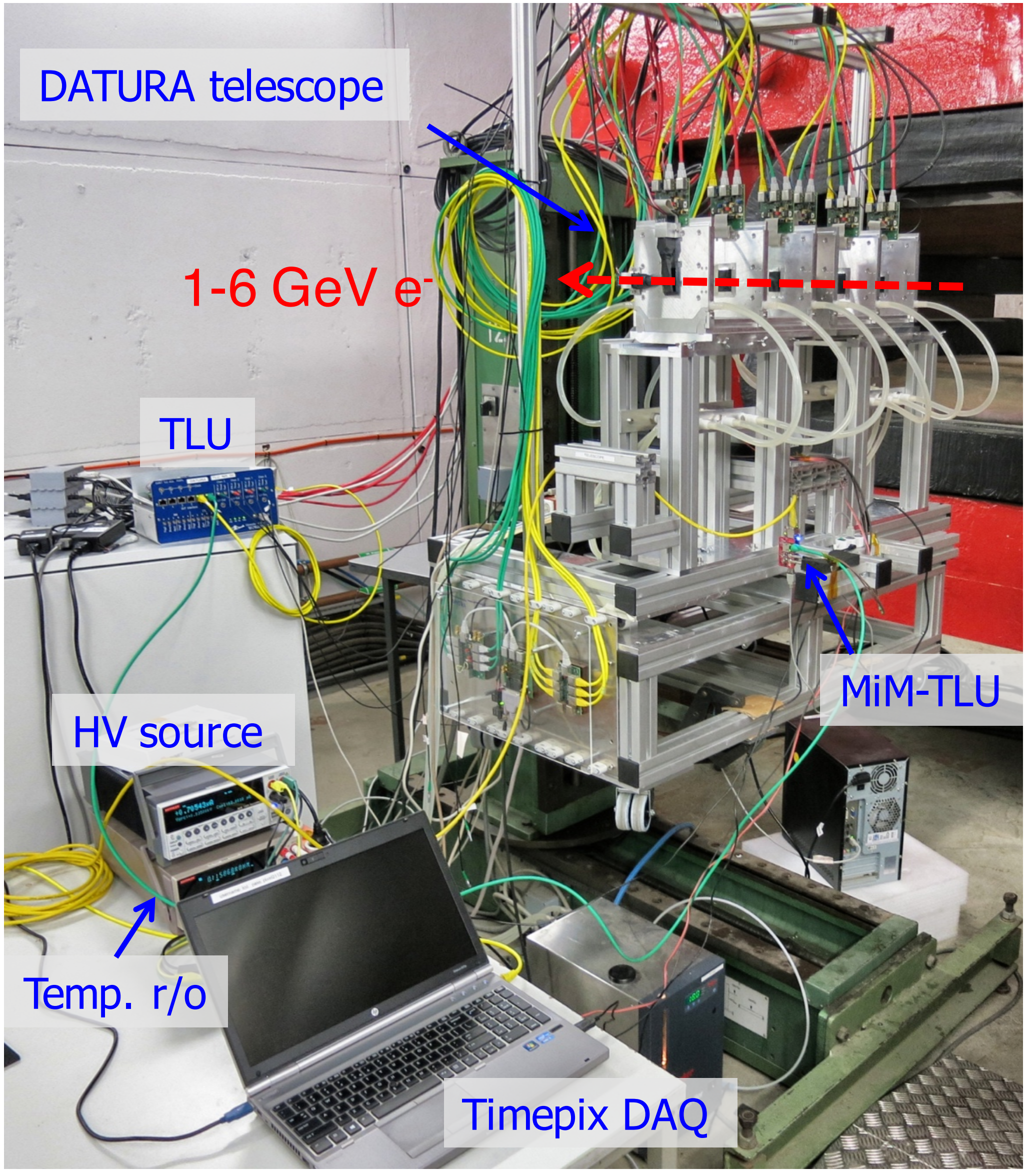
Medipix/Timepix hybrid r/o chip family

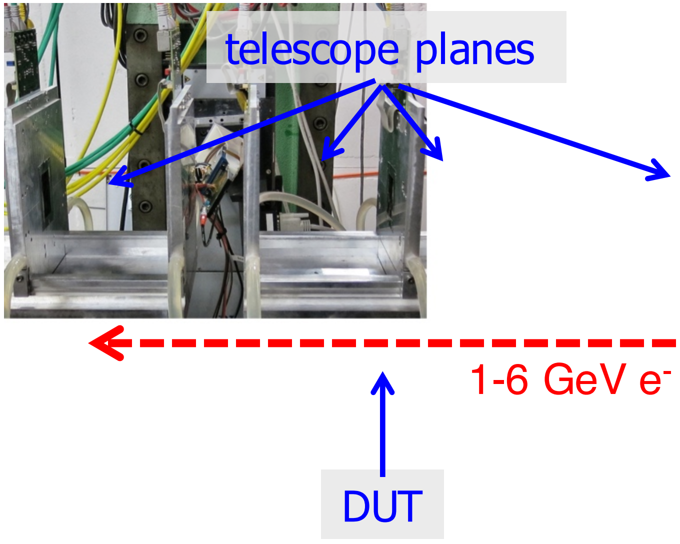
Chip	Year	CMOS Process	Pitch [μm^2]	Pixel operation modes	r/o mode	Main applications
Timepix	2006	250 nm	55x55	∫ToT or ToA or γ counting	Sequential (full frame)	HEP, Medical
Medipix3RX	2012	130 nm	55x55	γ counting	Sequential (full frame)	Medical
Timepix3	2013	130 nm	55x55	ToT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical
CLICpix/ CLICpix2	2013/ 2016	65 nm	25x25	ToT + ToA	Sequential (data compr.)	Test chips targeting CLIC requirements
Velopix	2016	130 nm	55x55	ToT + ToA, γ counting + ∫TOT	Data driven	LHCb (10x Timepix3 rate)
Medipix4/ Timepix4	tbd	65 nm	~35x35	ToT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical 4-side buttable

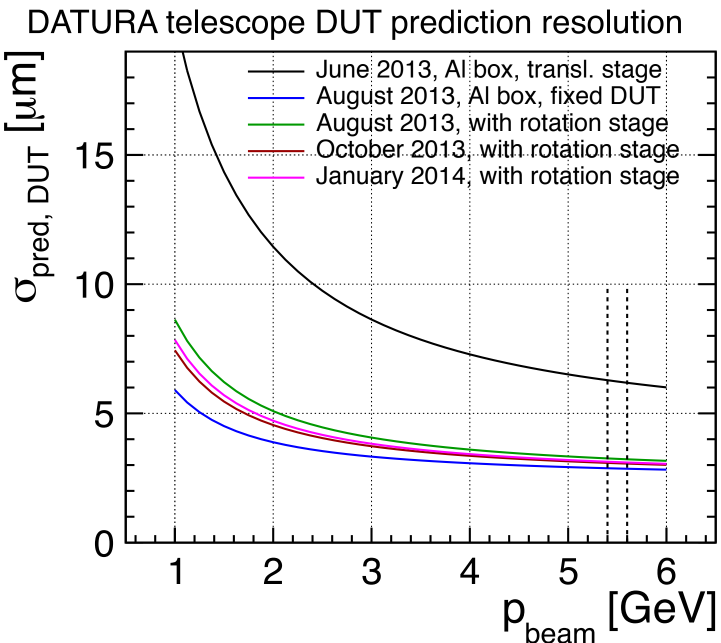
ToT: Time-over-Threshold
→ Energy
ToA: Time-of-Arrival
→ Time

- Taking advantage of smaller feature sizes:
  - Increased functionality and/or
  - Reduced pixel size
  - Improved noise performance

Test beam setup at DESY



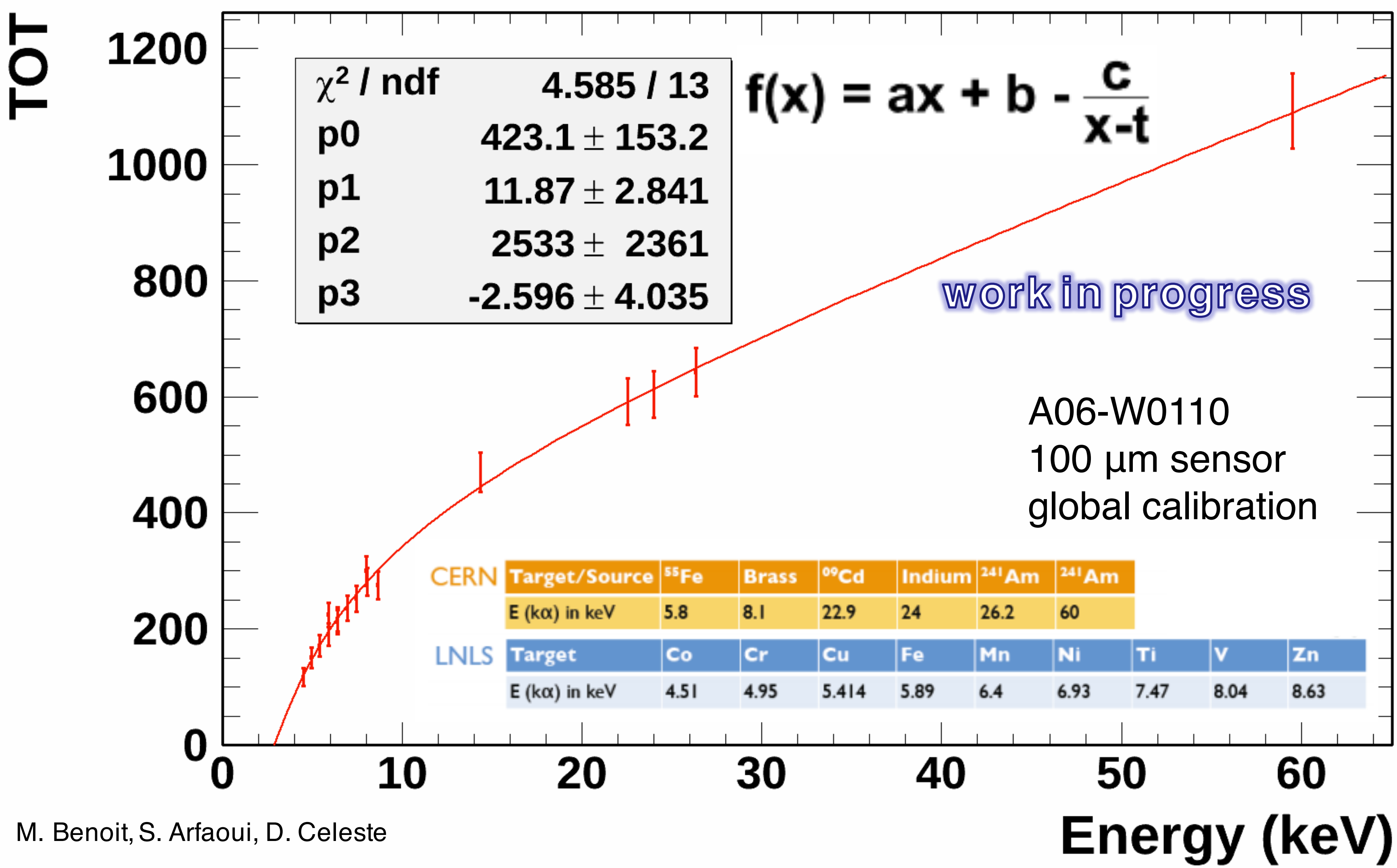




Timepix calibration

- Calibration of non-linear Timepix energy response with radioactive sources + fluorescence
- Parameterization with 4 parameters; global and per-pixel

→ Improves accuracy of position determination with charge-weighting methods



CERN Target/Source	^{55}Fe	Brass	^{109}Cd	Indium	^{241}Am	^{241}Am
E (kα) in keV	5.8	8.1	22.9	24	26.2	60

LNLS Target	Co	Cr	Cu	Fe	Mn	Ni	Ti	V	Zn
E (kα) in keV	4.51	4.95	5.414	5.89	6.4	6.93	7.47	8.04	8.63

M. Benoit, S. Arfaoui, D. Celeste

Characteristics of Medipix chips

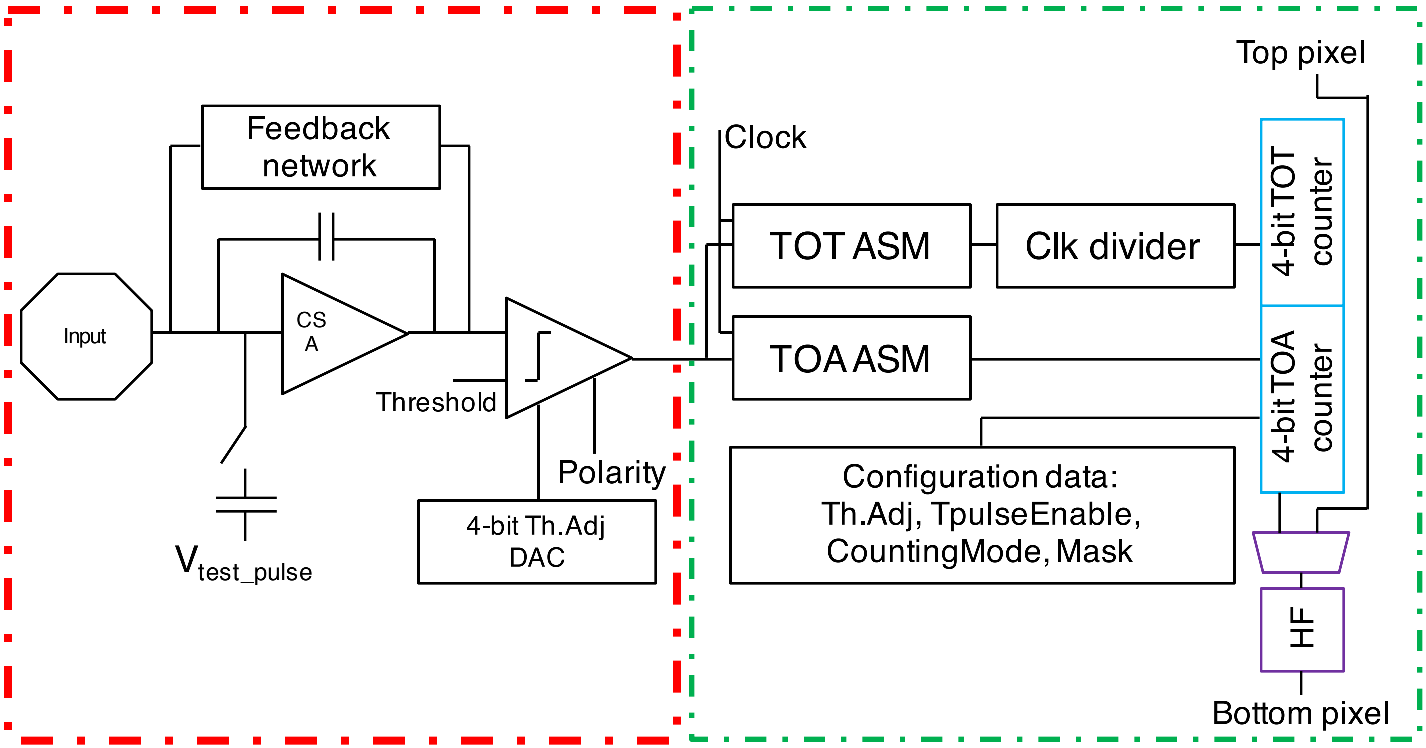
	Medipix2	Timepix	Medipix3	Timepix3	Medipix4	Timepix4
Pixel side (μm)	55	55	55/110	55	x/2x/3x	y
Technology (nm)	250	250	130	130	65	65
# pixels in x and y	256	256	256/128	256	512/256/128	512
Readout architecture	Frame based Sequential RW	Frame based Sequential RW	Frame based Continuous RW	Data driven/ frame based	Frame based Continuous RW	Data driven/ frame based
Charge summing and allocation mode (CSM)	No	No	Yes	No	Yes	No
# thresholds	2 (window discriminator)	1	2/4/8 Seq RW 1/4 Cont RW	1	?	1
ToT/ToA	No	ToT (14 bit) OR ToA (14 bit, 10ns precision)	No	ToT (10 bit) AND ToA (14 bit, 1.56ns precision)	No	ToT AND ToA
Front end noise (e^- rms)	110	100	80(SPM) 174(CSM)	62	≤ 80 (SPM) ≤ 174 (CSM)	≤ 62
Peaking time (ns)	150	100	120	30	≪120	≪30
Max count rate ($Mc/mm^2/s$)*	826	-	826 (SPM 55μm) 164 (CSM 55μm) 376 (SPM 110μm) 28 (CSM 110μm)	0.43 (data driven)	x5 Medipix3	x10 Timepix3
Number of sides available for tiling	3	3	3	3	4	4

*Depends strongly on exact conditions of threshold, sensor material and energy of illumination

Brown indicates parameters which are still be to defined

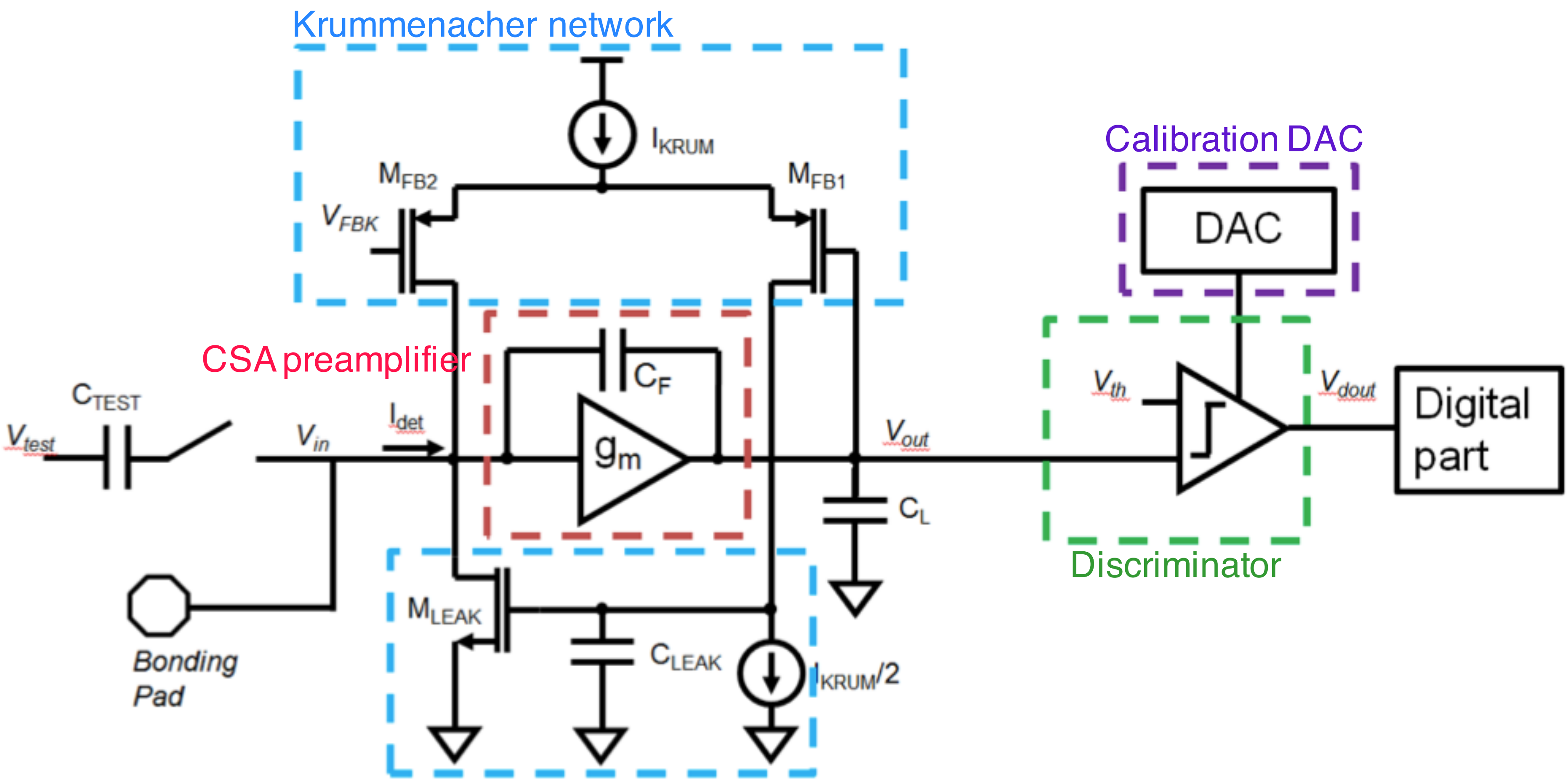
M. Campbell
October 15, 2015

CLICpix: pixel architecture



- The analog front-end shapes photocurrent pulses and compares them to a fixed (configurable) threshold
- Selectable polarity (positive / negative signals)
- Digital circuits simultaneously measure Time-over-Threshold and Time-of-Arrival of events and allow for zero-compressed readout

CLICpix analog frontend



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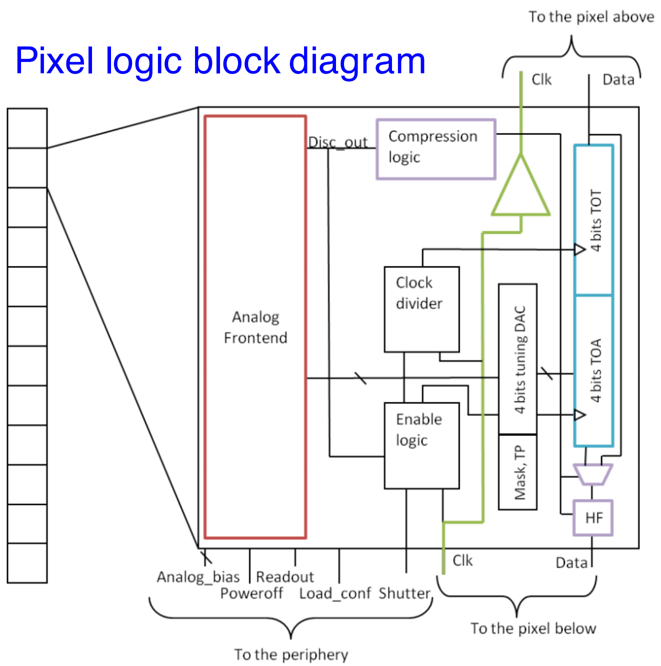
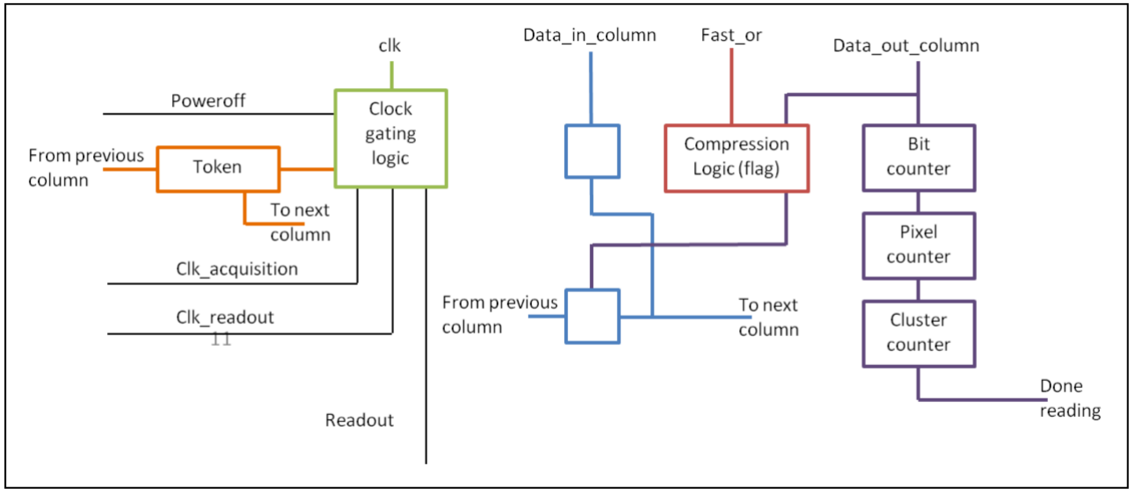
CLICpix digital architecture

Pixel logic block diagram

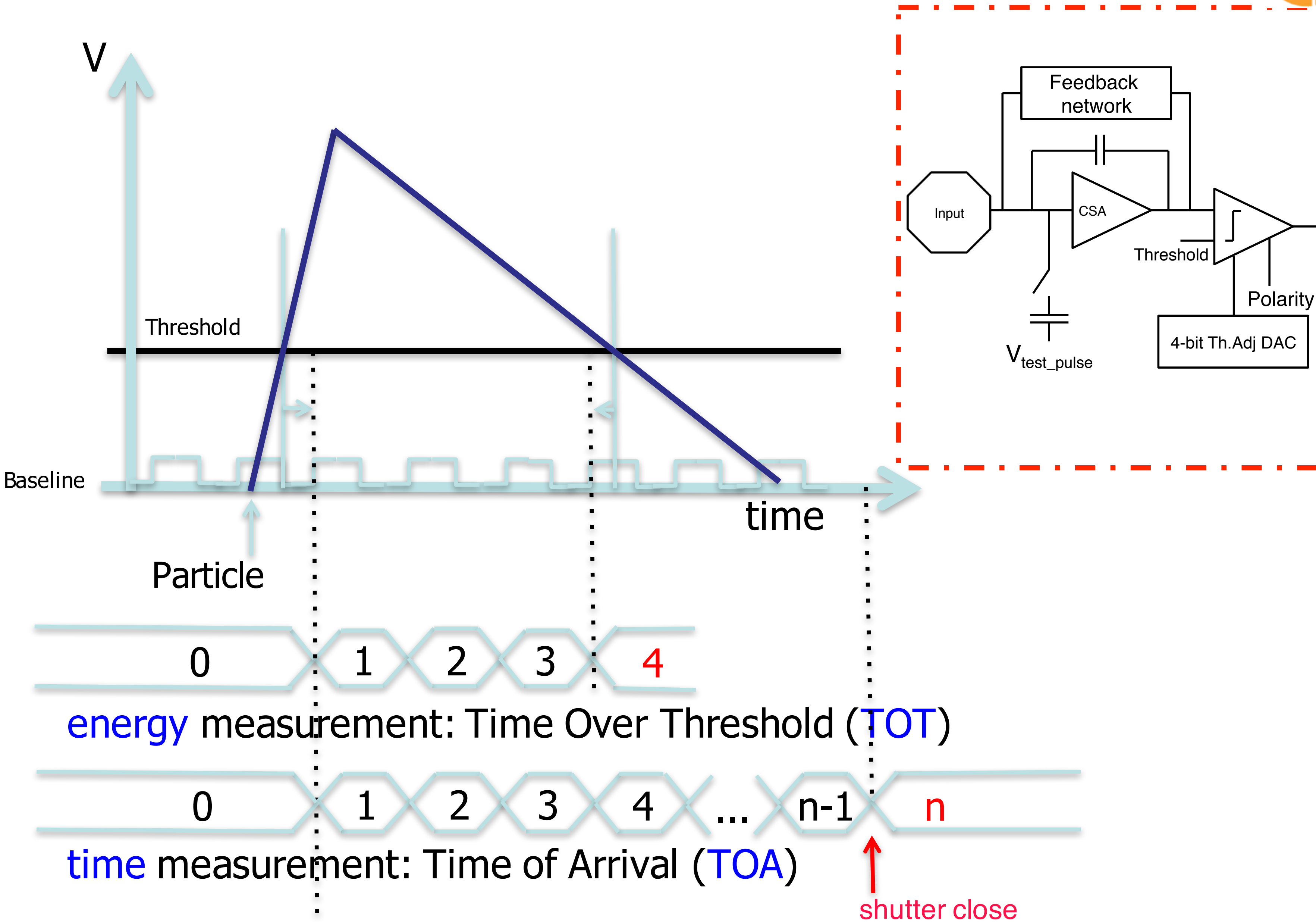


End of column block diagram



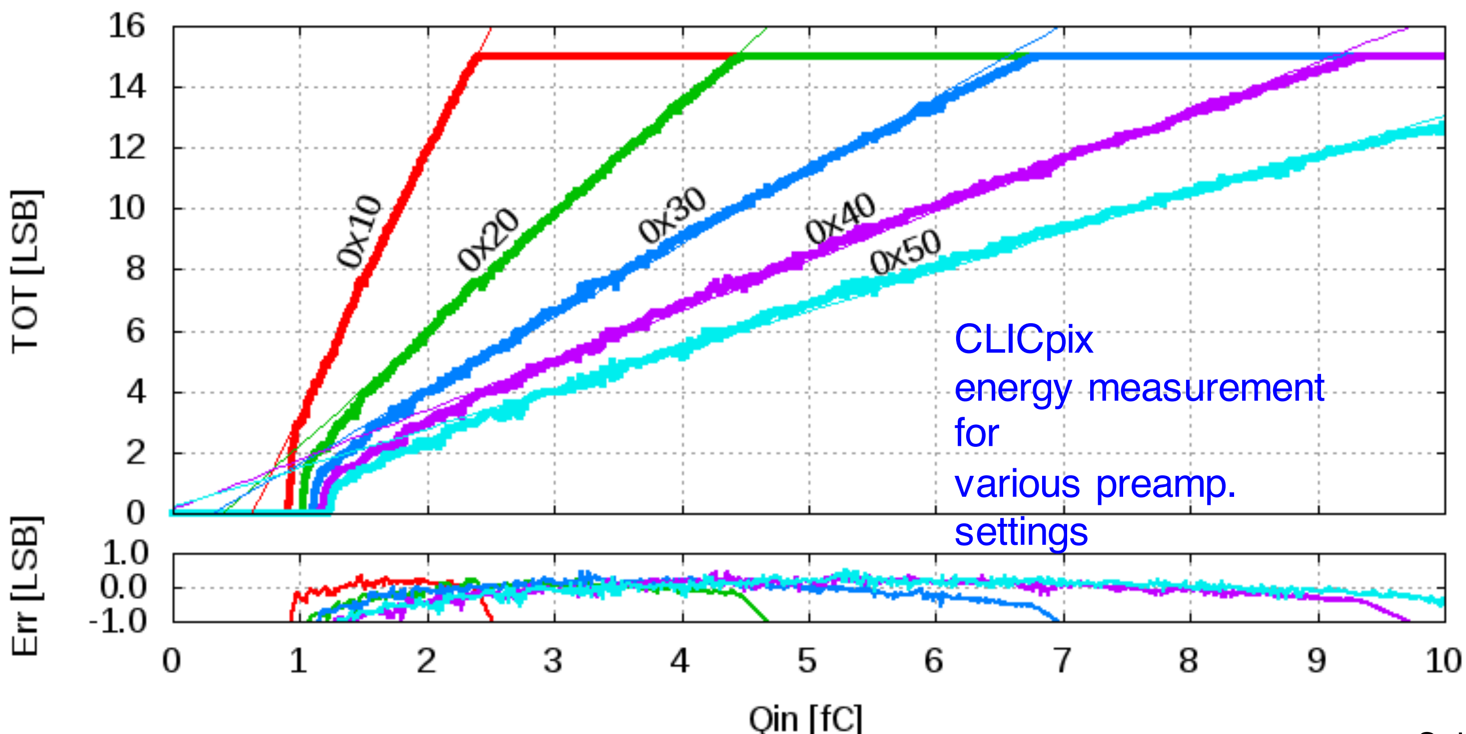
P. Valerio et al.

CLICpix: time and energy measurement



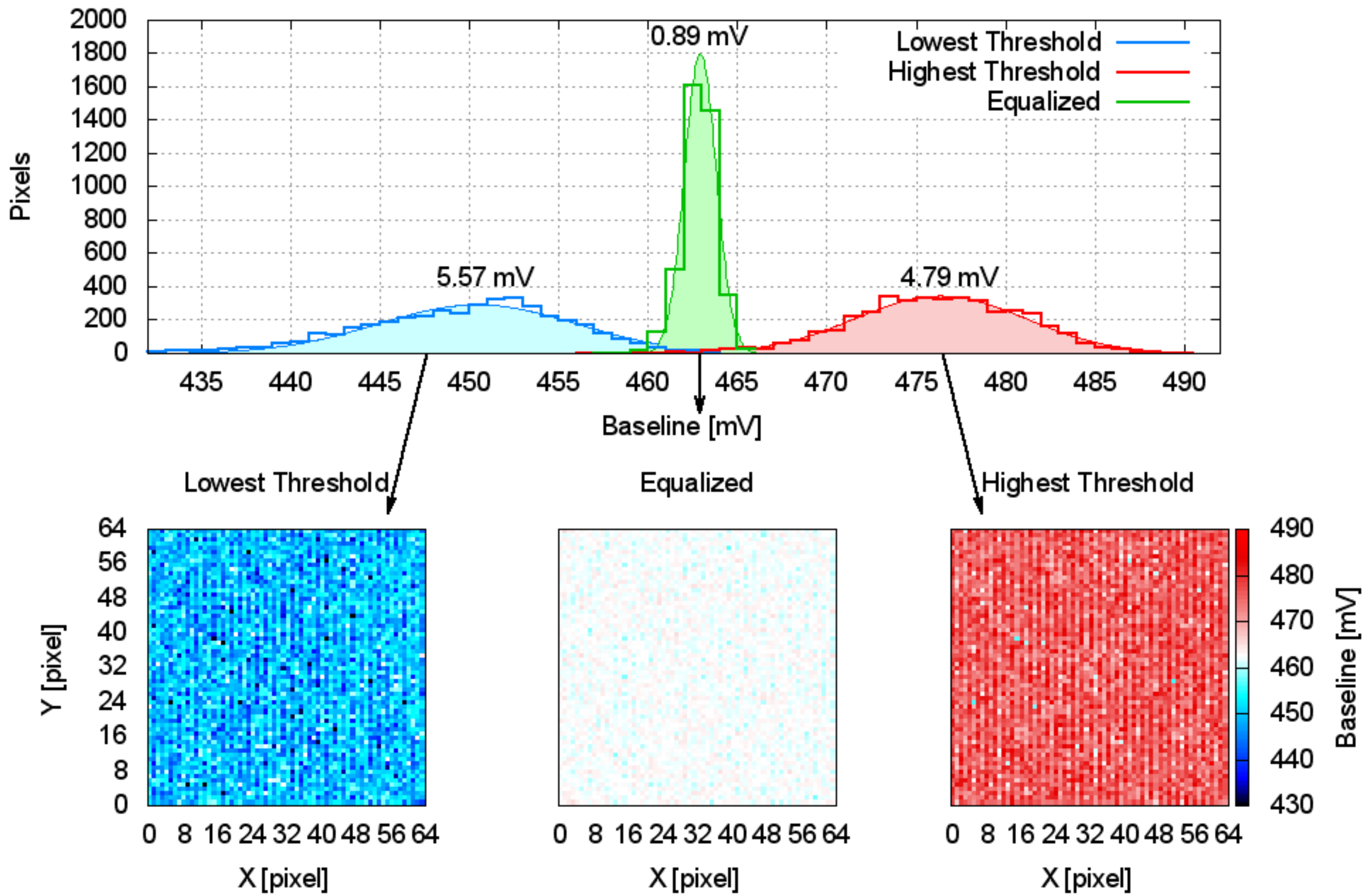
CLICpix: energy measurement

- Measure charge released in each pixel
  → Improve position resolution through interpolation
- Time-Over-Threshold (TOT) measurement (4-bit precision)
- Calibration measurement using external test pulser:



S. Kulis, P. Valerio

CLICpix: baseline equalization

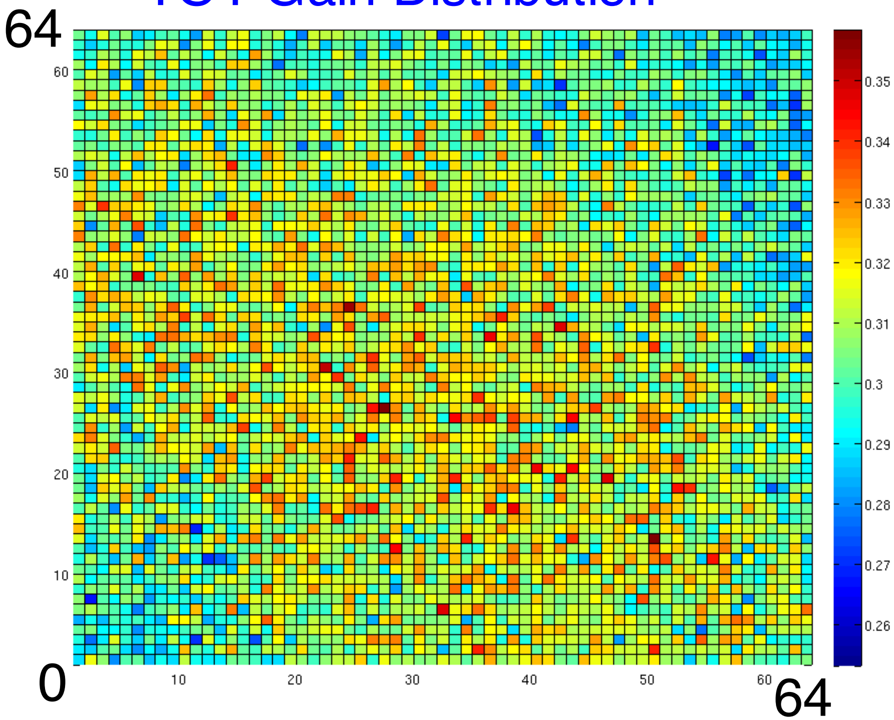


Calibrated spread across the whole matrix is 0.89 mV RMS (~22 e^-)
For comparison: MIP signal in 50 µm silicon ~3700 e^-

S. Kulis, P. Valerio

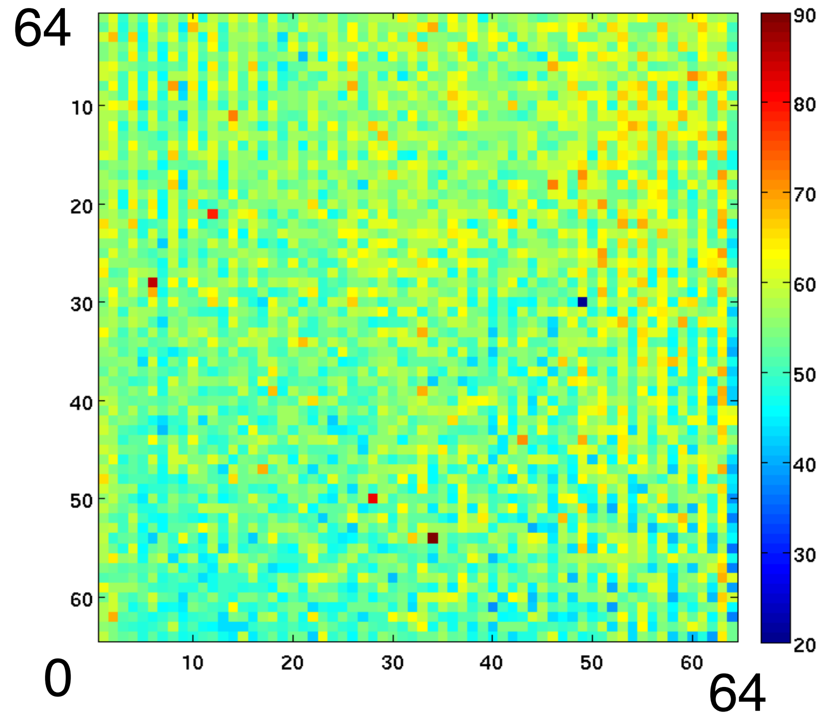
CLICpix: uniformity of gain and noise

TOT Gain Distribution



- Uniform gain across the matrix
- Gain variation ~4.2% r.m.s. (for nominal feedback current)

Equivalent Noise Charge



- Uniform ENC across the matrix
- Mean ENC: 55 e^-, SD: 5.7 e^- (without sensor)

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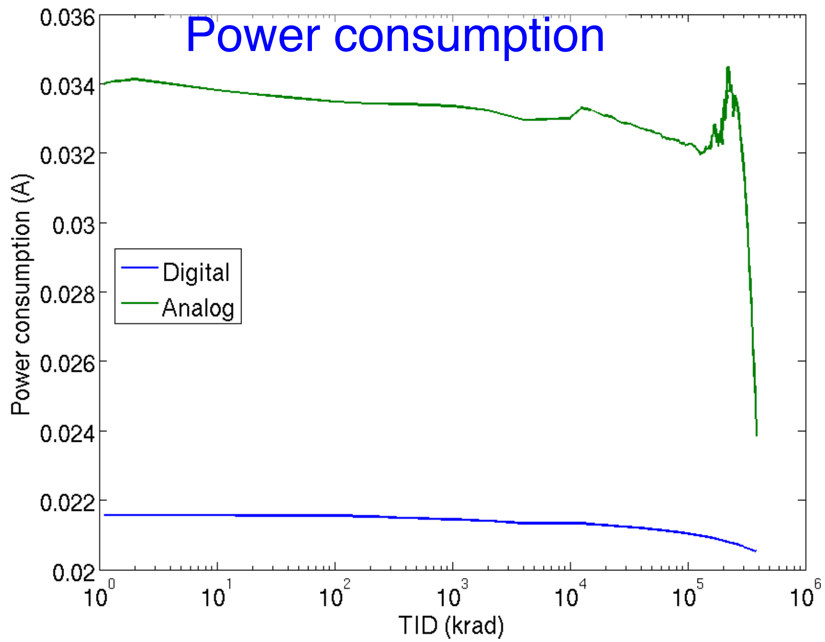
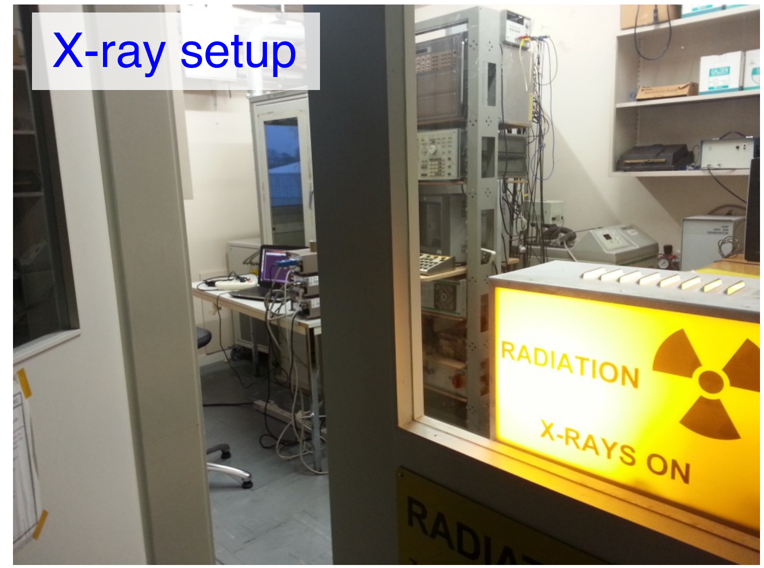
CLICpix: radiation qualification

- Moderate radiation-tolerance requirements at CLIC: <100 kRad TID
- However: building blocks can be re-used for RD53 (~1 GRad required)
- Results of radiation testing useful for gaining deeper understanding of the chip

→ performed radiation test up to 1 GRad (up to 150 kRad/minute) in calibrated X-ray setup





- No significant changes observed in sub-MRad range relevant for CLIC
- For >250 MRad: PMOS switches in current mirror fail

→ Break-down of analog power (note: band gap foreseen for final chip, instead of current mirror)

- digital components kept working normally

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CLICpix: summary

Parameter	Unit	Simulation	Measurement
Rise time	[ns]	50	-
TOA accuracy	[ns]	<10	<10
Gain	[mV/ke$^-$]	44	40 *
Dynamic range	[ke$^-$]	44 (configurable)	40 * (configur.)
Integr. nonlinearity (TOT)	[LSB]	<0.5	<0.5
ENC (w/o sensor)	[e$^-$]	~60	~55 *
DC spread σ (uncalibrated)	[e$^-$]	160	128 *
DC spread σ (calibrated)	[e$^-$]	24	22 *
Power consumption	[µW/pixel]	6.5	7

* results obtained with electrical test pulses

S. Kulis, P. Valerio

- good agreement between simulations and measurements
- power pulsing works according to specifications (~100x reduction of average power)
- programmable power on/off times, front-end wake up within ~15 µs
- Radiation test: chip functional up to ~250 MRad

CLICpix+HV-CMOS glue assemblies

- Study of glue parameters:
  - Viscosity
  - Bonding force
  - Alignment
  - Glue-layer uniformity

- Cross sections of glue assemblies

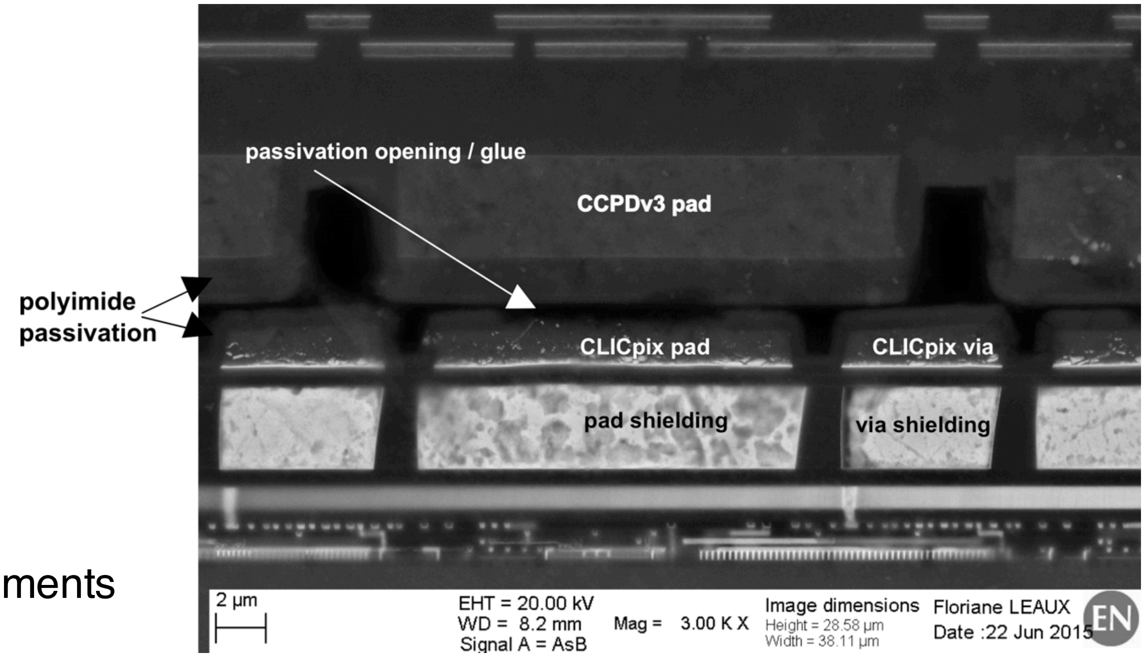
→ alignment precision ~1 μm

→ glue-layer thickness ~0.5 μm (+2 μm polyimide passivation)

- Laboratory and test-beam measurements

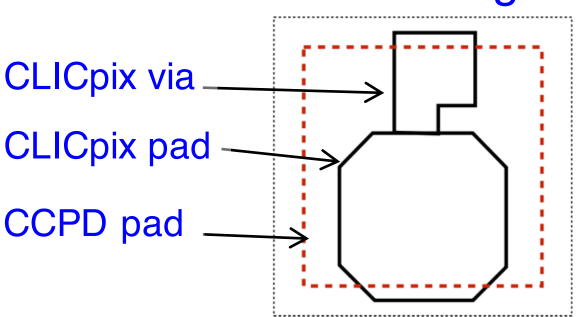
→ correlate performance with glue parameters (coupling strength, uniformity)

SEM picture CCPDv3-CLICpix assembly

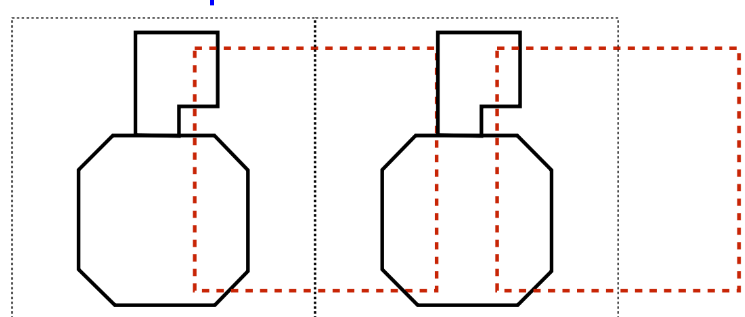


viscosity: 450 Pas, F=5 N, T=100 °C, t=10 min

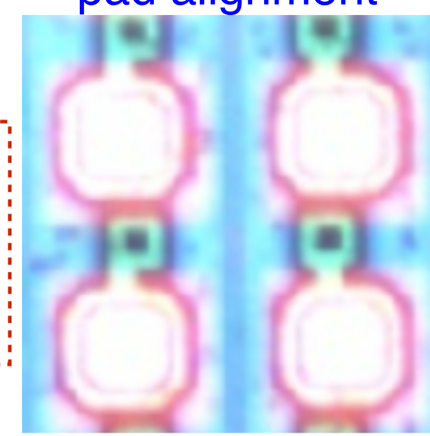
centered alignment



½ pixel offset



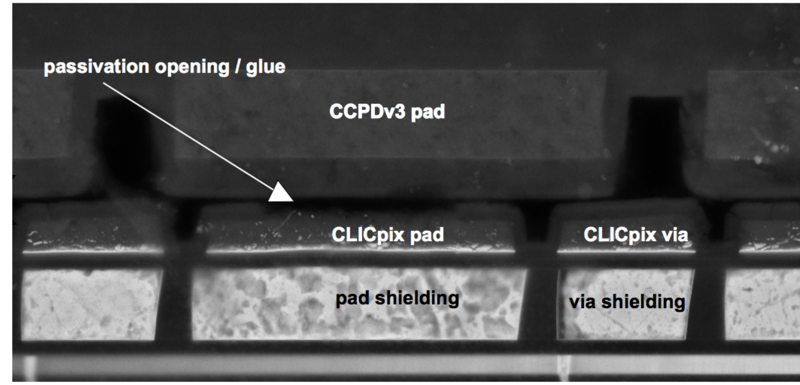
pad alignment



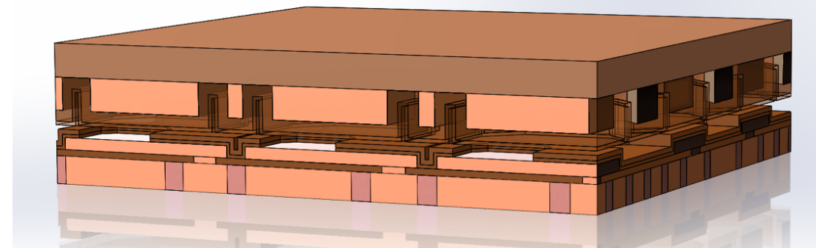
Simulation of capacitive coupling

- COMSOL multi-physics simulation of capacitance between sensor and r/o ASIC
- Detailed model of the major metal and passivation layers and the glue in 3x3 matrix
- Obtain coupling capacitance (~3 fF) and cross capacitances
- Significant cross coupling (~4%) to neighboring pads for current CCPDv3 version
- Cross coupling largely reduced for newly designed C3PD active sensor with guard ring

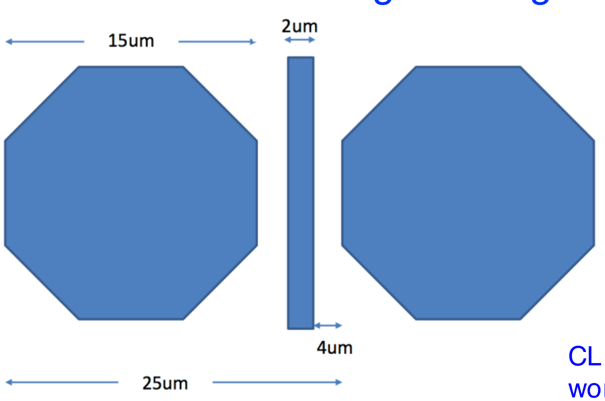
CCPDv3+CLICpix cross section



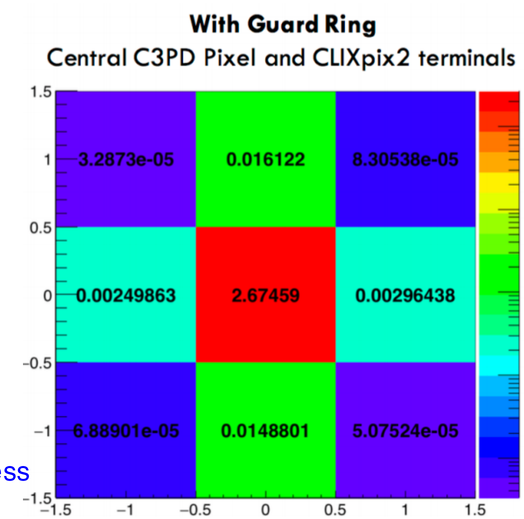
COMSOL simulation model

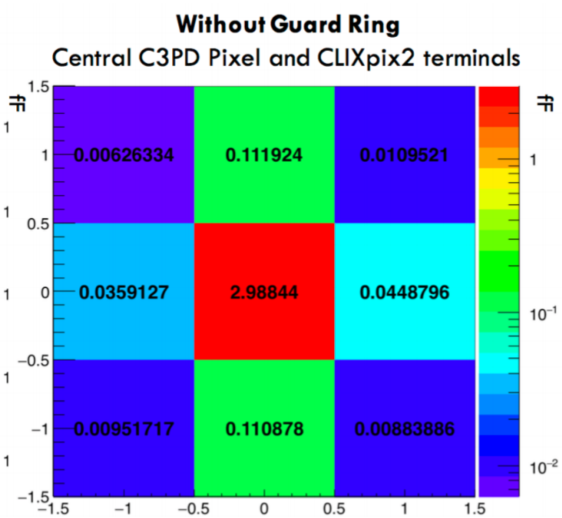


C3PD sensor with guard ring



CLICdp work in progress

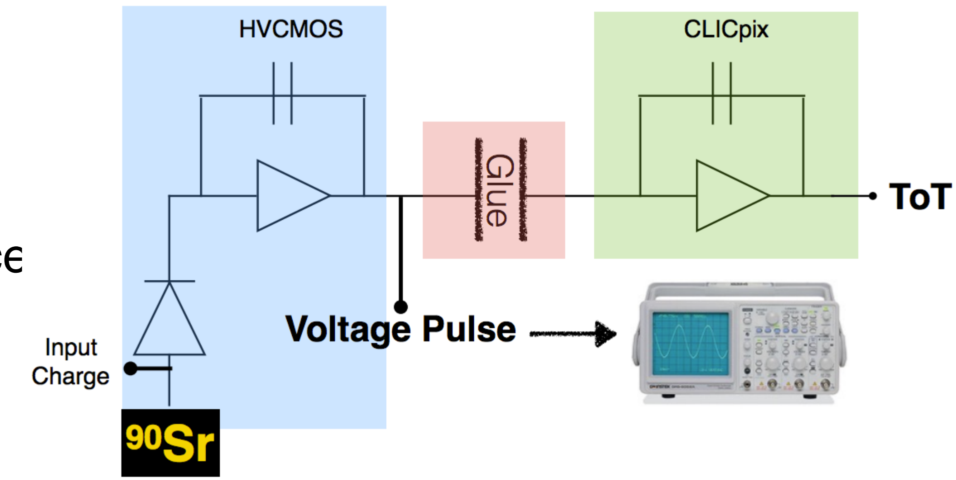




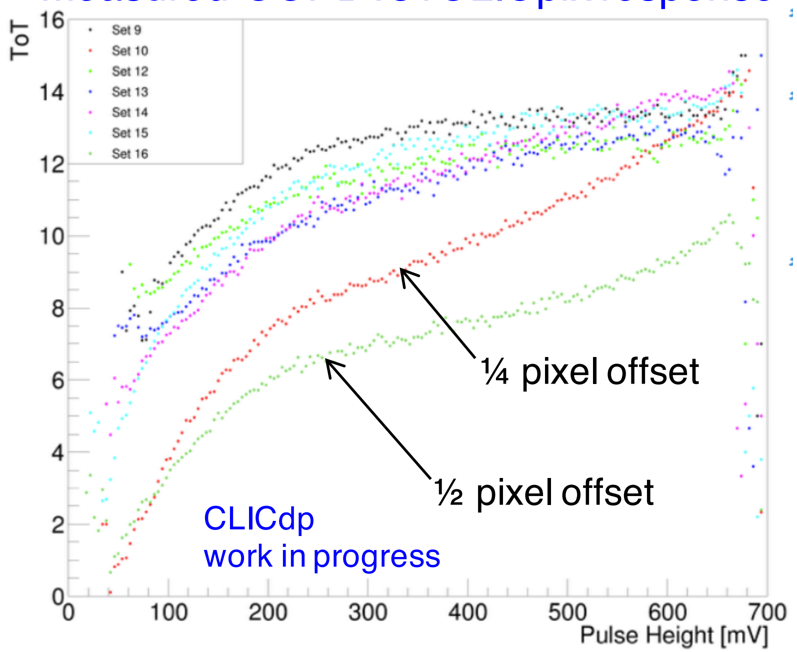
CLICpix+HV-CMOS calibration

- Dedicated test pixels: direct access to CCPDv3 output signal
- Used to calibrate CLICpix ToT response
- Simulation of CLICpix ToT response for different values of coupling capacitance

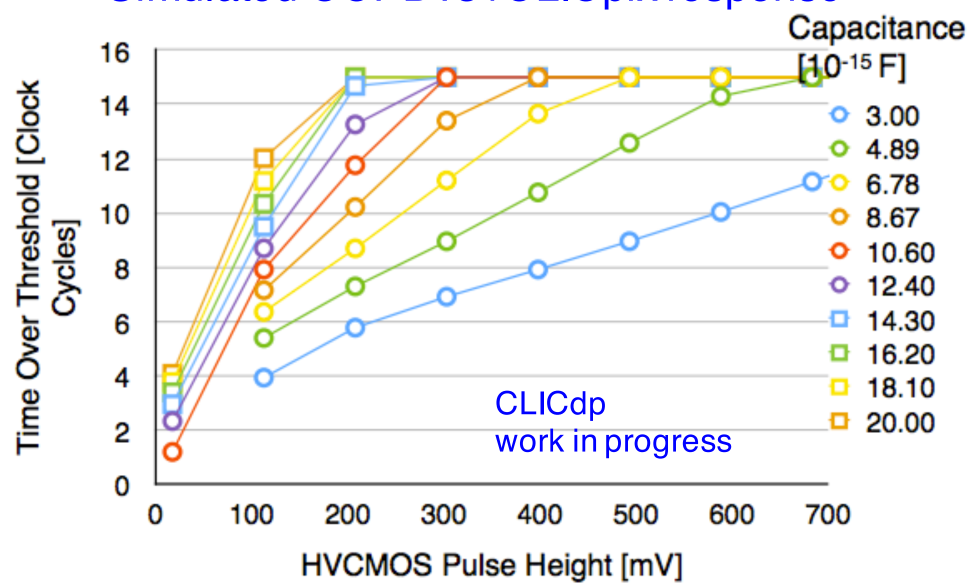
→ estimate coupling capacitance by comparison of measured and simulated response: ~10 fF



Measured CCPDv3+CLICpix response

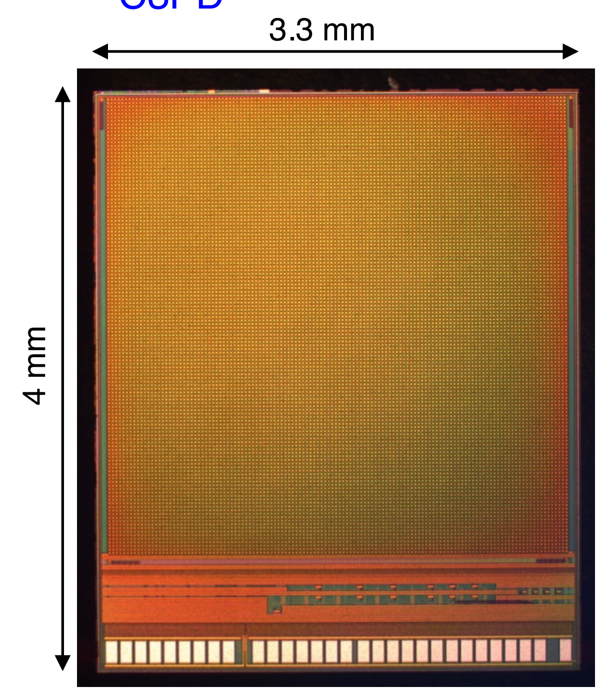


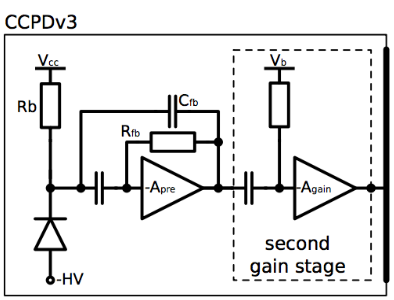
Simulated CCPDv3+CLICpix response

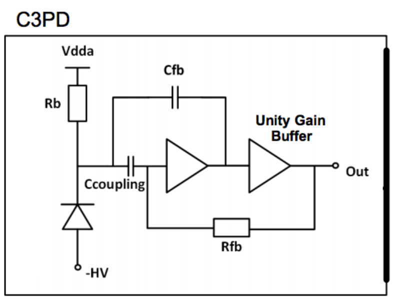


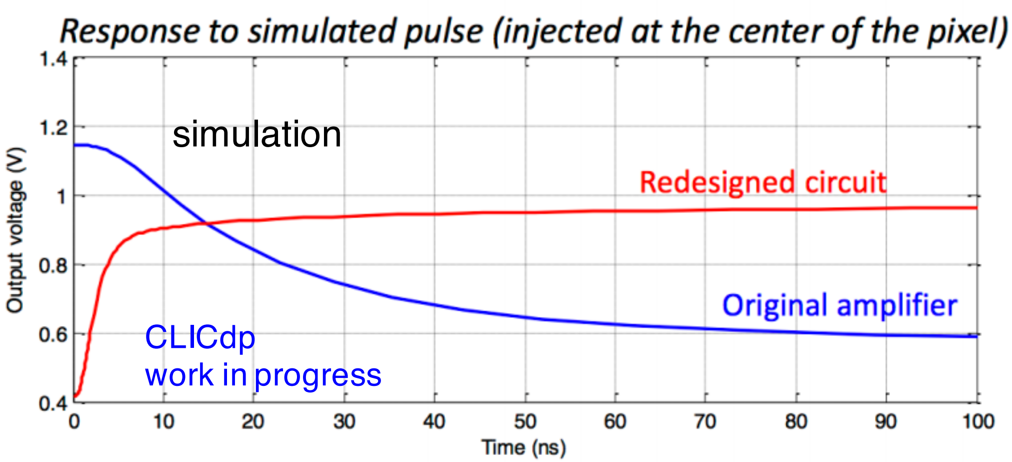
New HV-CMOS active sensor

- New HV-CMOS chip C3PD produced in same process:
  - Increased matrix size to 128 × 128 pixels
  - Major redesign of the full chip:
    - On-pixel amplification scheme significantly changed → reduced peaking time to some ~10 ns
    - Guard ring around coupling pads → reduced cross capacitance
    - Power pulsing circuitry introduced
    - Testpulsing of the matrix
    - 10 Ω cm substrate
  - possible future submissions with substrate resistivities of 100, 200, 1k Ω cm
  - Lab measurements for first chips ongoing

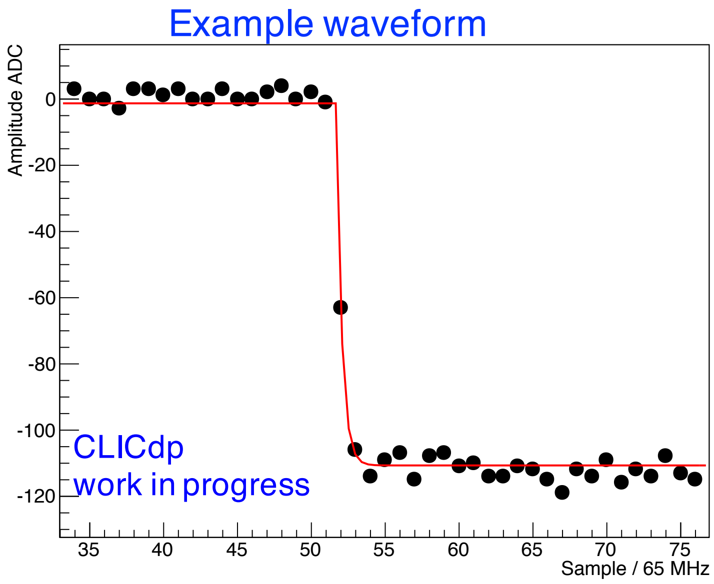


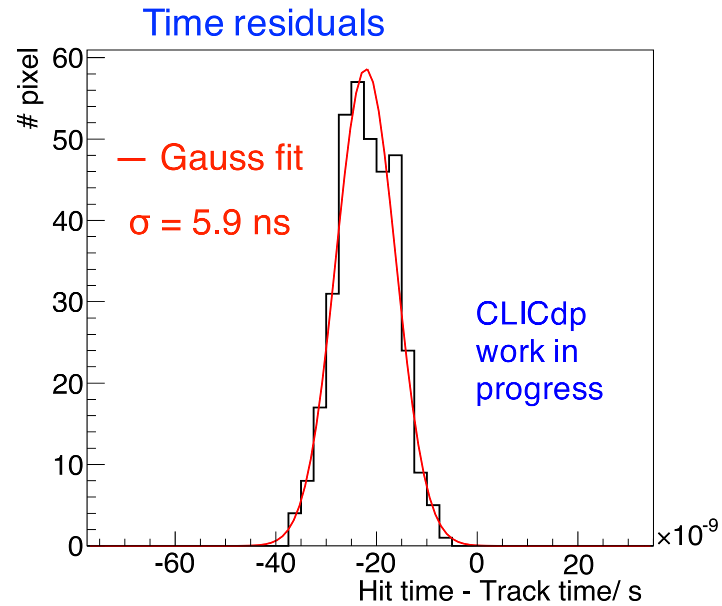






First results from ALICE Investigator





- First test-beam performance results:
  - Good time resolution ~5 ns
  - Cluster size distributions and spatial resolution in agreement with expectations
- Caveats:
  - Results based on full waveform analysis of signals from external sampling ADC
  - Unknown absolute efficiency (r/o deadtime not recorded)