Level-1 Track Trigger for the Upgrade of CMS Detector at HL-LHC

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Overview

The High Luminosity of the LHC (HL-LHC) will provide an order of magnitude increase in the instantaneous luminosity, increasing the number of collisions/bunch crossing. This poses unique challenges for the trigger requiring changes to both the algorithms and architecture at level-1. A key component of the CMS HL-LHC upgrade is a level-1 Track Trigger (TT) system using information from the Outer Tracker, which will help CMS maintain a rich and efficient physics program during this period. A silicon-based level-1 TT has never been realized with such a complexity.

L1 Track Trigger Upgrade

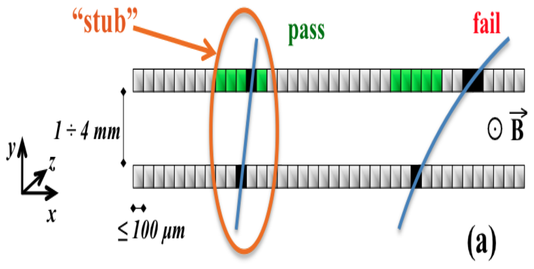
The HL-LHC upgraded system has to deal with a very high pileup environment (pileup $\sim$ 140-200) and maintain optimal performance upto 3000 fb^{-1}.

- Level-1 (L1) trigger delivers data with high efficiency up to rate of 750 kHz (latencies up to 12.5 μs).
- L1 tracking (latency $\sim$ 4 μs) provides a completely new handle in L1 trigger decision making.

The outer tracker will consist of modules composed of two closely spaced silicon sensors read out by a common frontend (FE). The modules will provide data both for L1 reconstruction & for the global event processing. Including tracking information at L1 will help in

- Improved p_T identification of charged leptons.
- Track isolation (leptons and photons).
- Vertexing for charged leptons and jet objects.
- Large rate reductions.

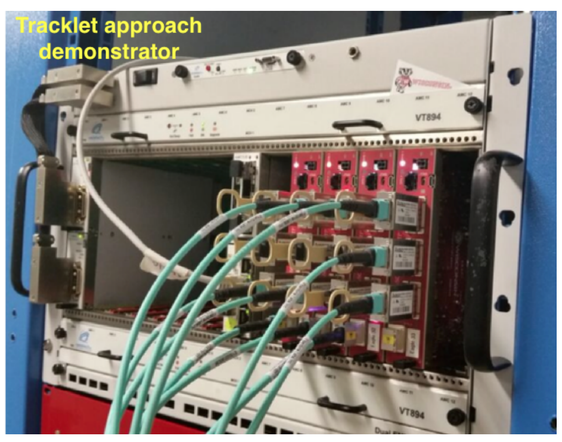
Outer tracker p_T modules

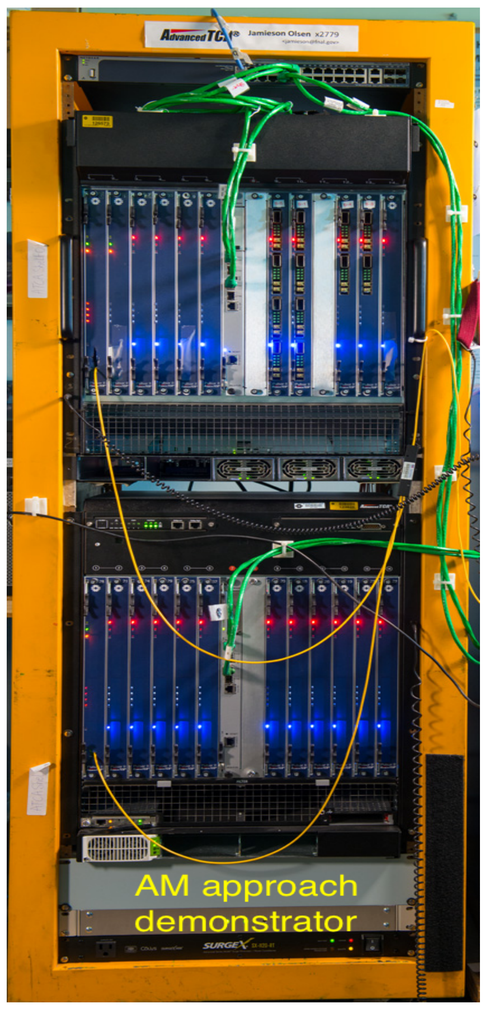


On-detector selective data readout - stubs: pair of correlated FE signals from a module (p_T > threshold (tunable)).

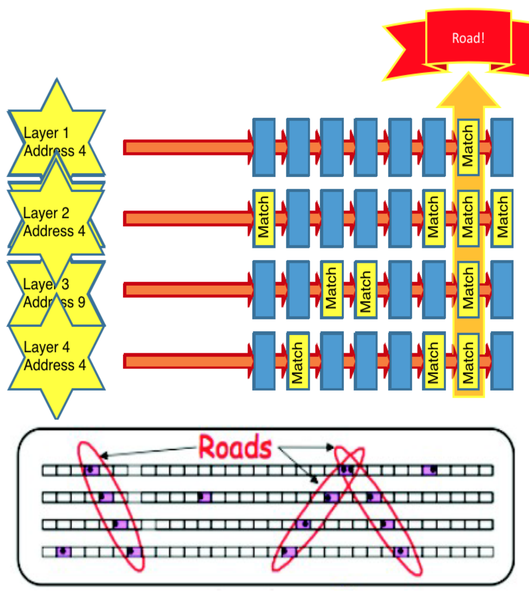
- Data reduction by one order of magnitude (sufficient for the purposes of L1 data transmission).
- Pattern recognition performed on stub data to reconstruct L1 tracks.

Three L1 track finding approaches are being pursued currently (Associative Memory, Tracklet, Time Multiplexed). Demonstration test benches are being setup for each, to measure the performance (latency, efficiency, fake rate) using simulated data with HL-LHC occupancy and rate, and to compare different technologies & component choices. The final goal is to demonstrate a viable L1 track finding system by the end of the year.





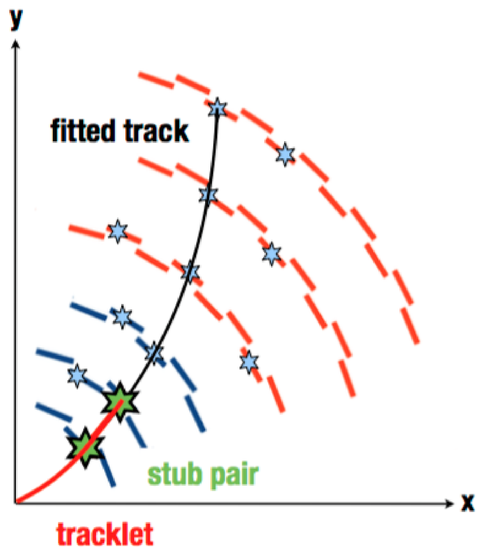
Associative Memory (AM)



- Massive fast parallel processing for complex combinatorics of track finding algorithm.
- AM pattern recognition with custom-designed AM chips & latest generation FPGA.
- ATCA based custom Pulsar2b boards with pattern recognition mezzanines hosting FPGA & AM chips, used in the demonstrator.
- Full-mesh backplance Advanced TCA platform (providing high bandwidth, low latency processing with Pulsar2b).
- Linearized track fitting performed in the FPGA using algorithms such as Principal Component Analysis.

Tracklet

- A road-based track search, seeded by tracklets (stub pairs).
- Tracklets projected to other layers to search for matching stubs.
- Linearized χ^2 track fit used to determine track parameters.
- Naturally pipelined implementation & low time multiplexing. Operates at fixed latency.



- Uses commercially available FPGA technology. μTCA based CTP7 boards used for demonstration.

Time Multiplexed Track Trigger

(Details about the TMTT approach will be presented in a dedicated poster in this conference by Luigi Calligaris.)

- Track candidates built based on (r,ϕ) Hough transform.
- Full data event assembly & processing at single node. Avoids replication of data shared across regional detector boundaries.
- Two processing layers (pre & main processors) are required, for data organization/formatting & track finding, respectively.
- Divided into 5 trigger regions along η.
- Uses μTCA based MP7 boards for demonstration.

Acknowledgements

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References

[1] CMS Collaboration, "Technical Proposal for the Phase-II Upgrade of the CMS Detector", **CERN-LHCC-2015-010 ; LHCC-P-008 ; CMS-TDR-15-02**.