

A new μ TCA-based waveform digitizer for the Muon g-2 experiment

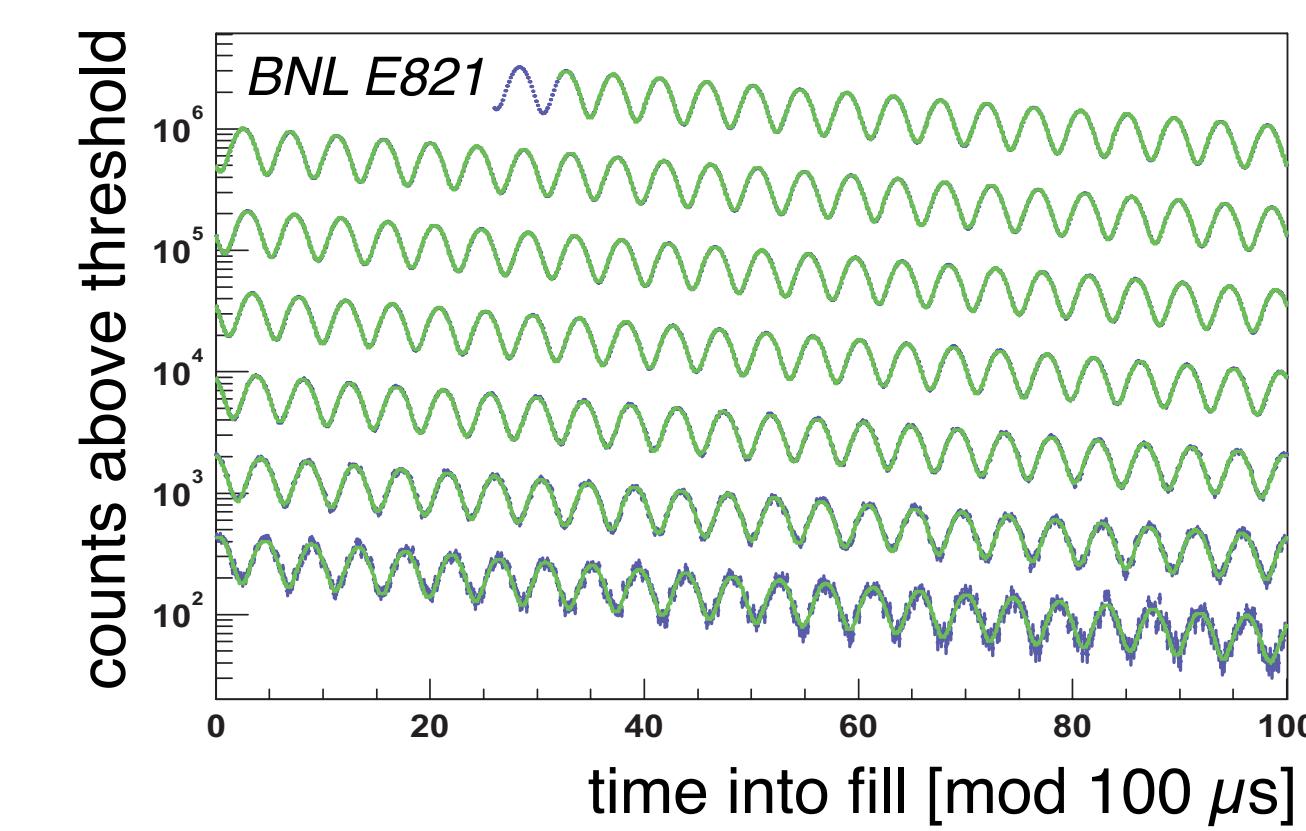
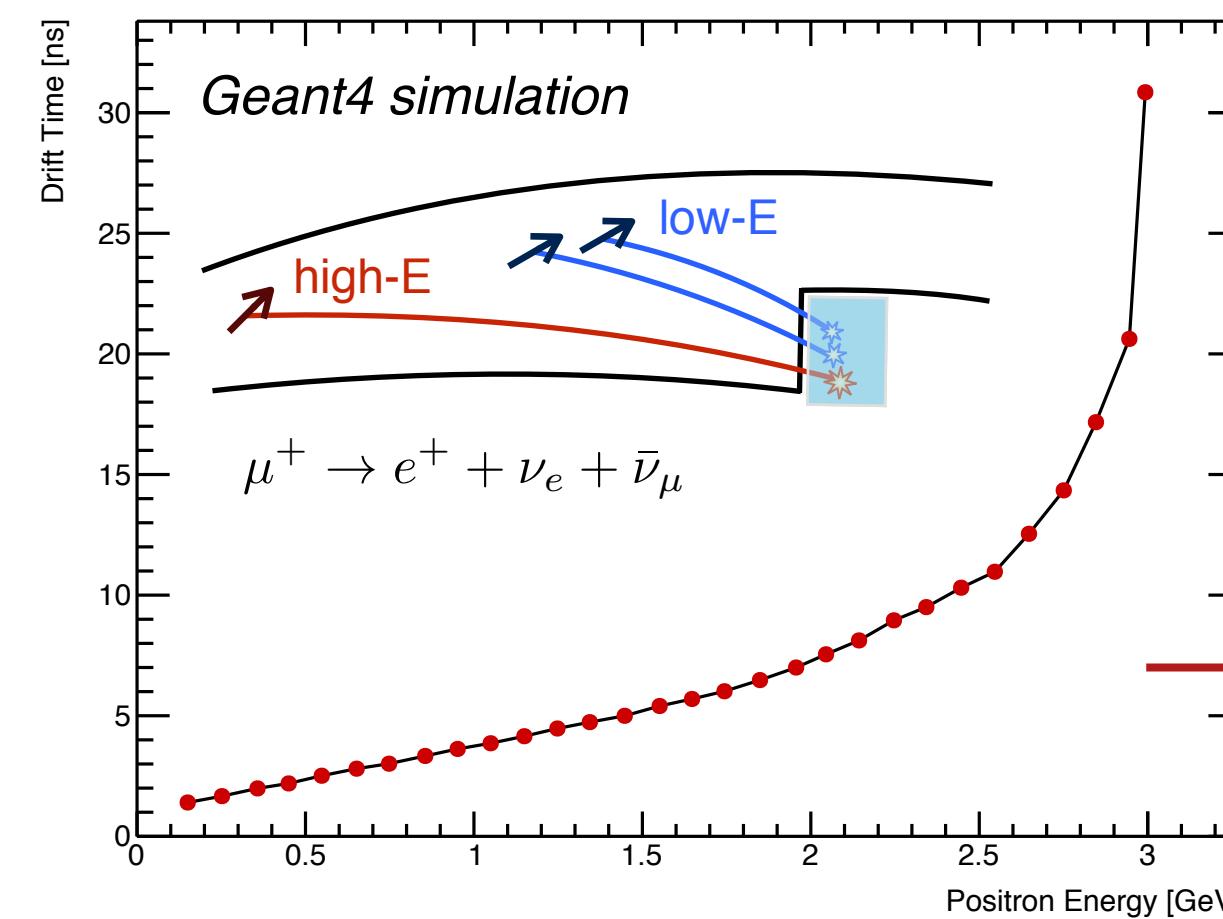
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Muon g-2 pileup requirements

Goal: measure the muon's anomalous magnetic moment to 140 ppb

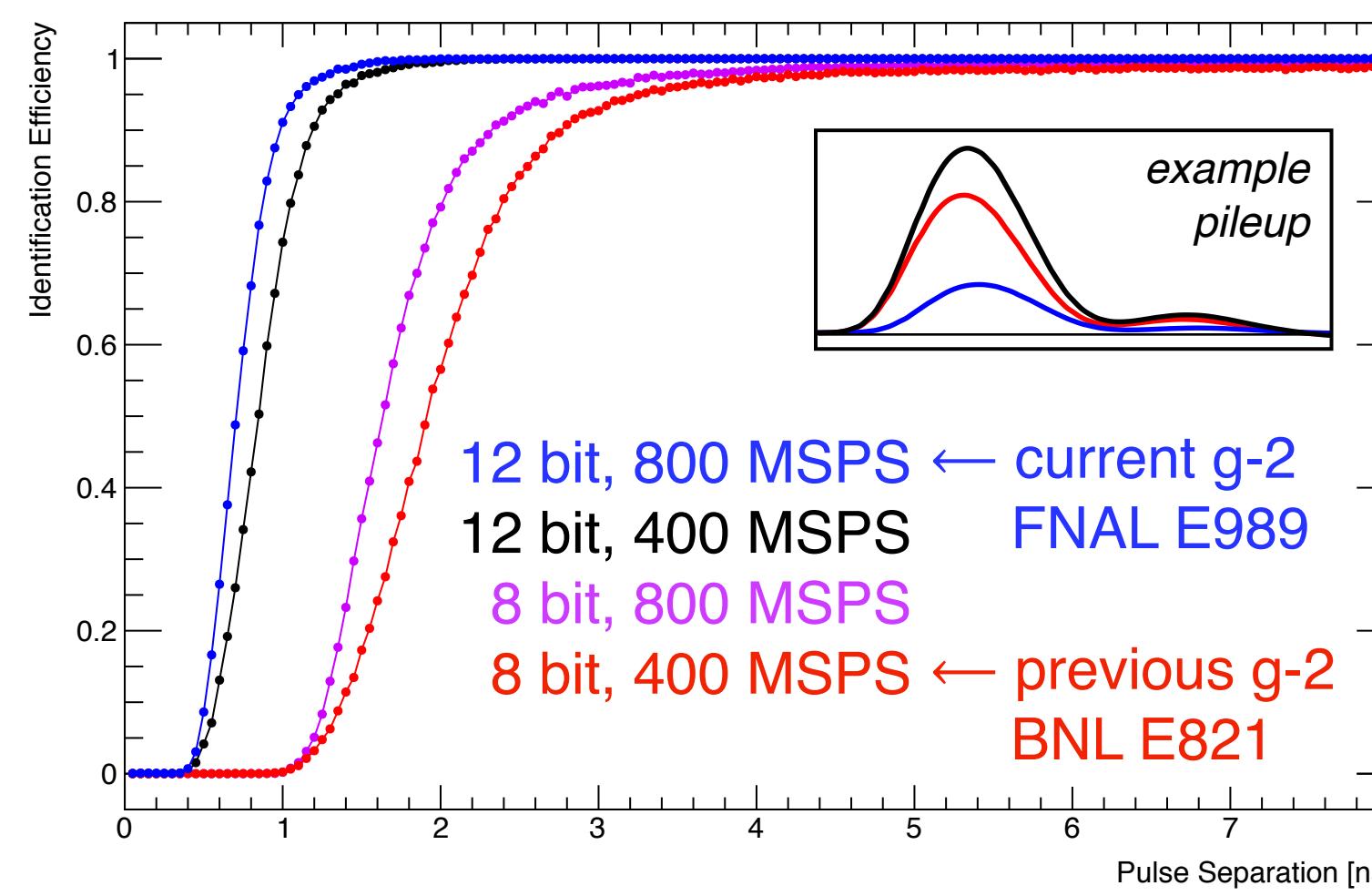
$$a_\mu \equiv \frac{g - 2}{2} = \frac{m \omega_a}{e B}$$

70 ppb allotted to $(\omega_a)_{\text{sys}}$
40 ppb allotted to pileup



5-parameter model:
 $N(t; E_{\text{th}}) = N_0 e^{-t/\tau} [1 + A \cos(\omega_a t + \phi)]$

wrong phase!

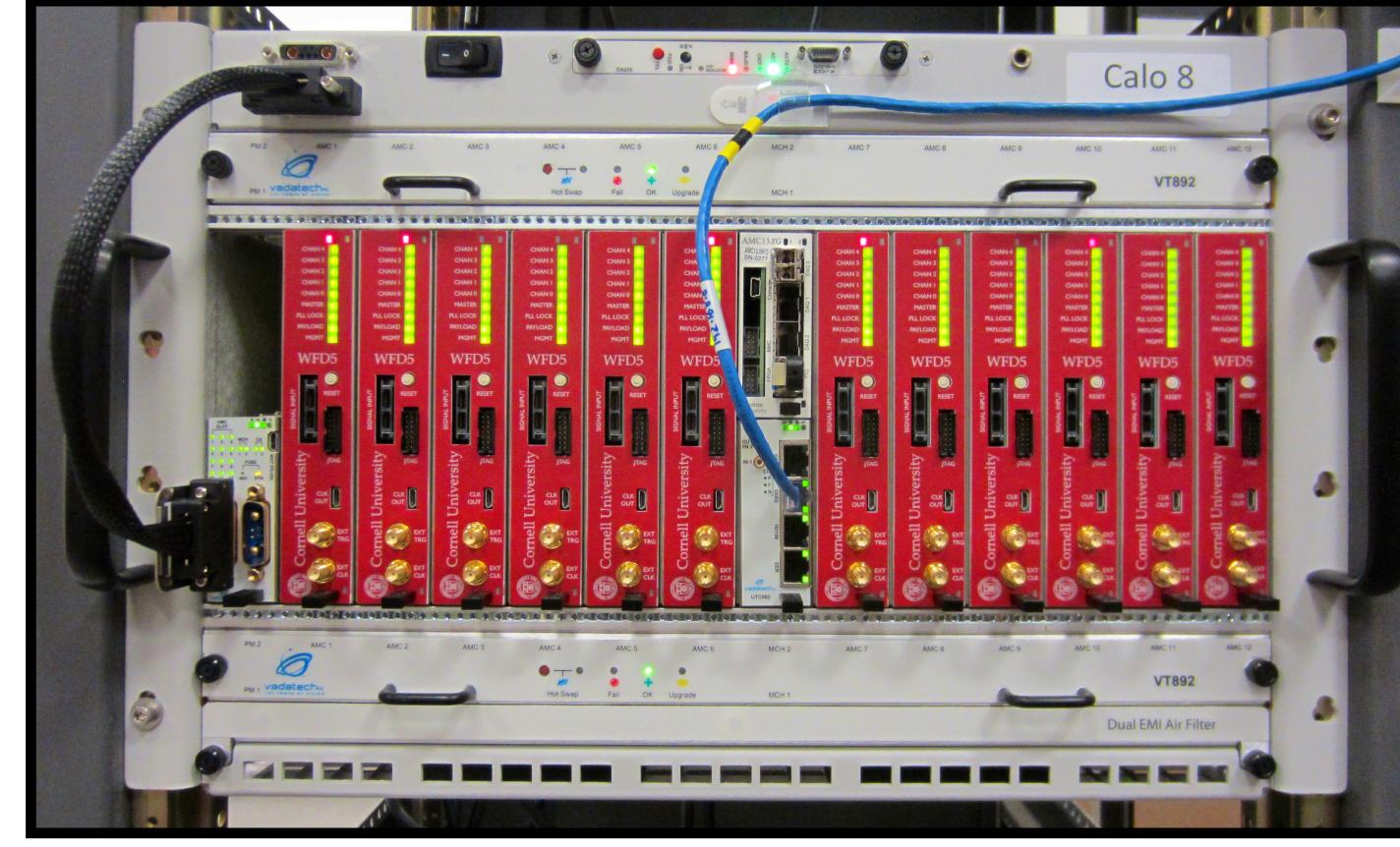
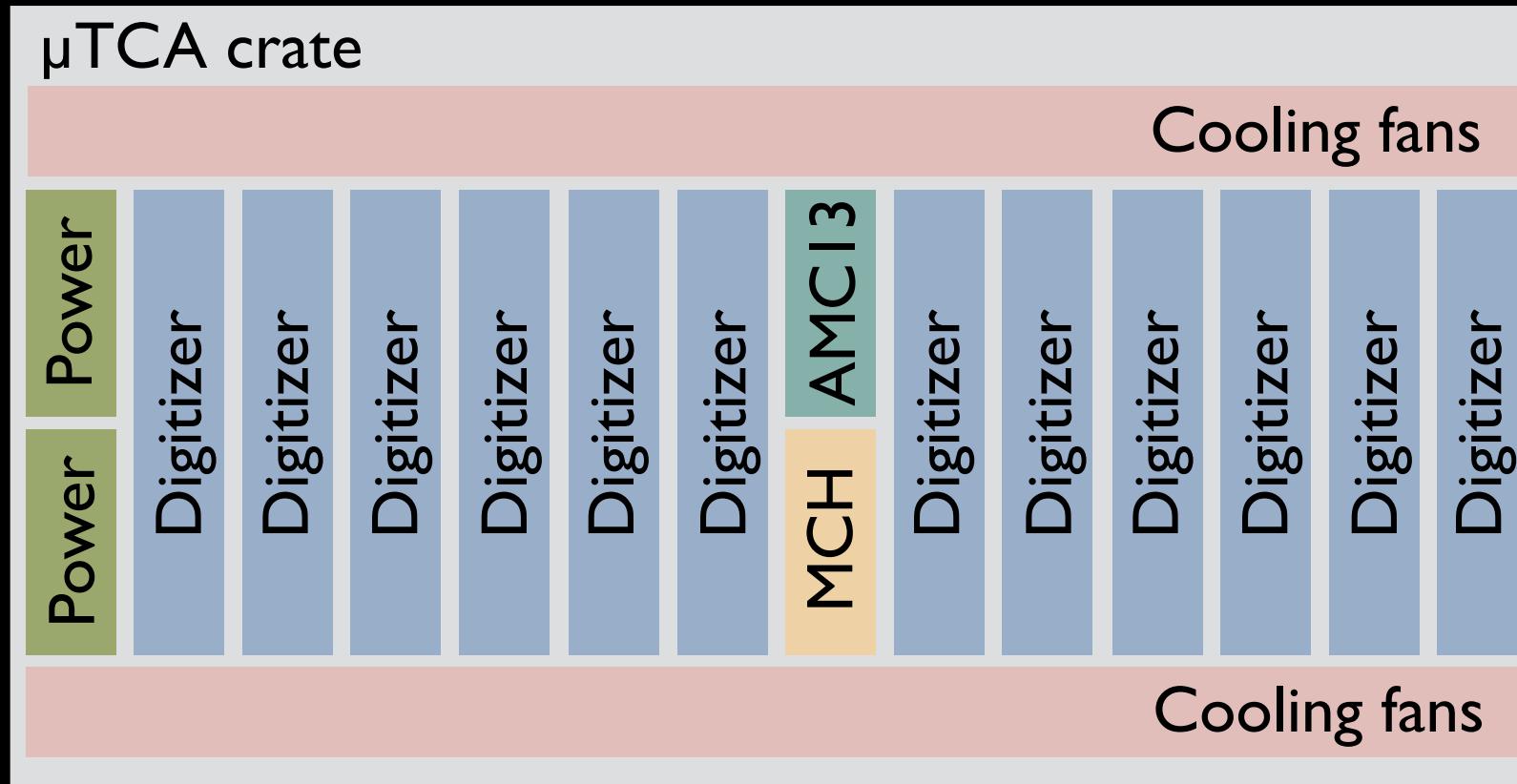


× 4 in muons expected for new experiment
 × 16 in pileup rate expected → 312 ppb

≥ 8-fold pileup reduction required:

3-fold from separation in space
 → segmented calorimeter
 3-fold from separation in time
 → custom waveform digitizer
 73% from bit depth
 27% from sampling rate

μ TCA-based architecture



- μTCA crate**: Provides standard platform for power, cooling, and dual-star connectivity [*Commercial, VadaTech VT892*]
- MCH**: Provides Ethernet communications, controls, and monitoring via backplane [*Commercial, VadaTech UTC002*]
- AMC13**: Provides experimental clock, triggers, controls, and 10-Gbit/s data readout [*Custom, Boston University's CMS Group*]
- Digitizer**: Conforms to the Advanced Mezzanine Card (AMC) standard [*Custom, Cornell University's Muon g-2 Group*]

Waveform digitizer design

Number of Channels	5
Bit Depth	12 bit
Max Sampling Rate	800 MSPS
Input Signal Range	1 Vpp
Input Bandwidth	230 MHz
Memory Size	1 Gbit / channel

Processing

- Dedicated Xilinx Kintex-7 FPGA per channel
- Dedicated Xilinx Kintex-7 FPGA for μ TCA interface

Clocking

- TI LMK04906 clock synthesizer in dual PLL mode with an internal VCO and an external VCXO
- Independent sampling clock for each channel with configurable output frequency and delay
- Reference frequency selected from μ TCA backplane or from a front-panel SMA connector

Triggering

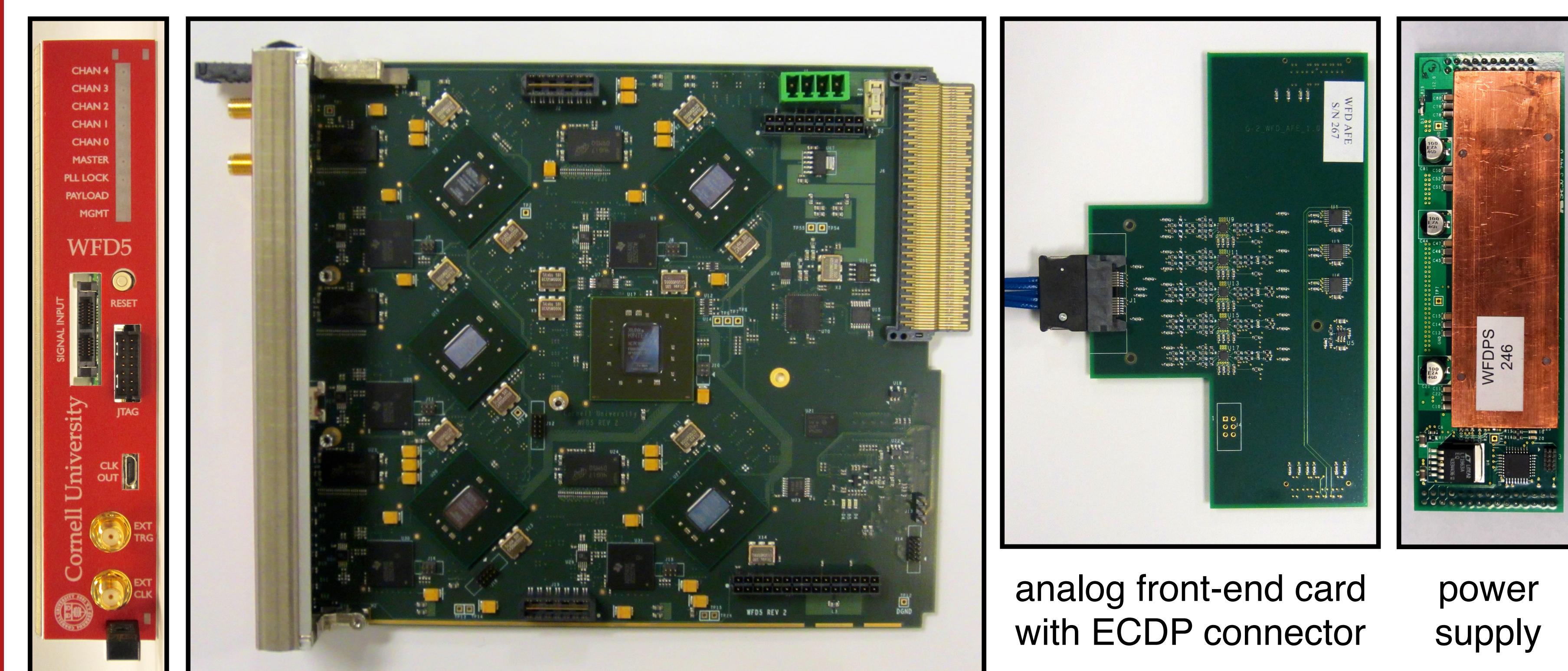
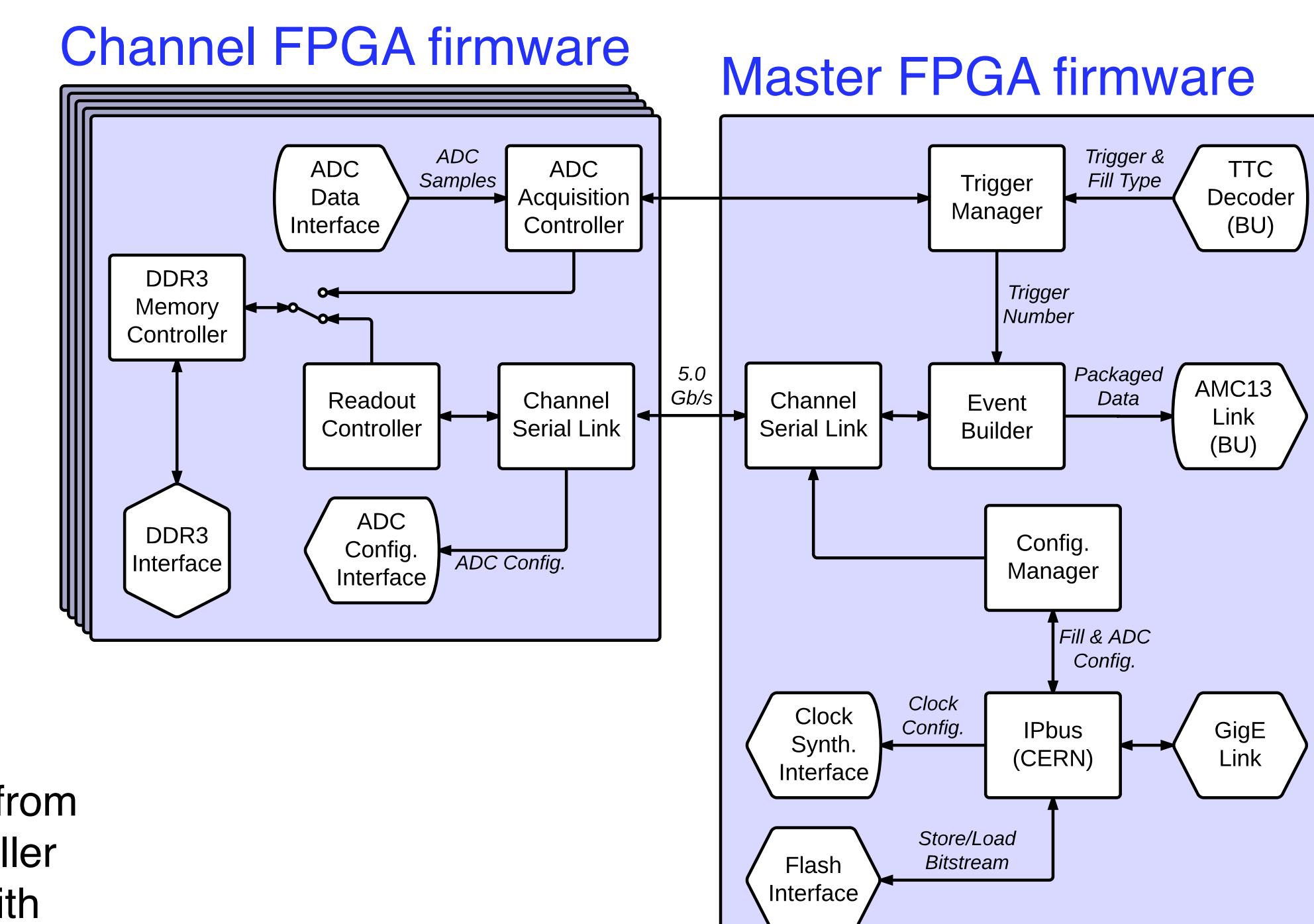
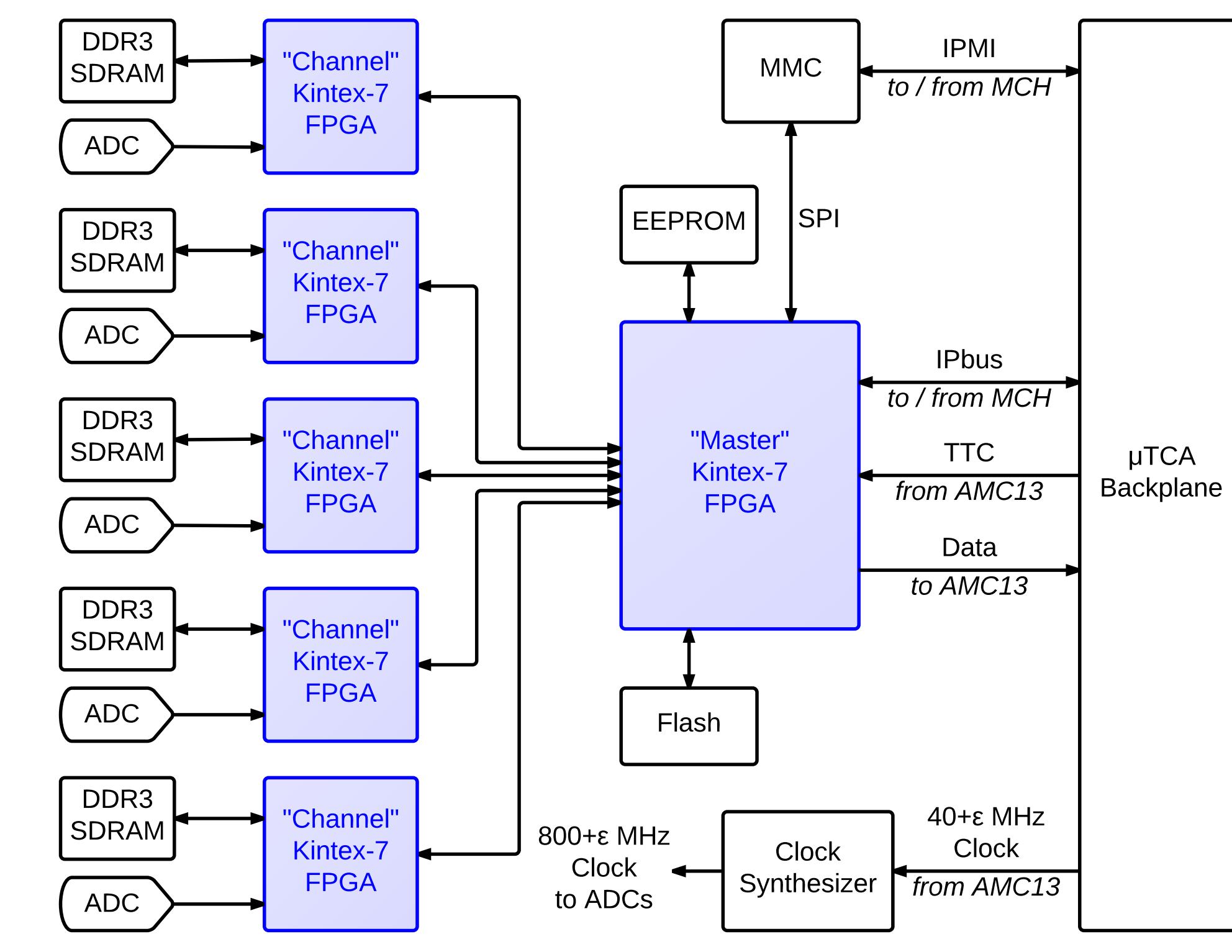
- Acquisition triggers received from μ TCA backplane via the AMC13 or from a front-panel SMA connector
- Independent trigger logic possible for each channel

Communication

- Dedicated 5-Gb/s serial links over μ TCA backplane
 - Master FPGA to MCH : Gigabit Ethernet
 - Master FPGA to AMC13 : LHC TTC
 - Master FPGA to AMC13 : DAQ data readout
- Each channel has a dedicated 5-Gb/s serial link to Master FPGA for configuration and data readout

Modularity

- Power supply card to generate internal voltage rails from the μ TCA crate supply, equipped with a micro-controller
- Analog front-end card for input-signal conditioning with digital input-signal offsets, programmable via Master FPGA
- Allows for inexpensive customization of the digitizer

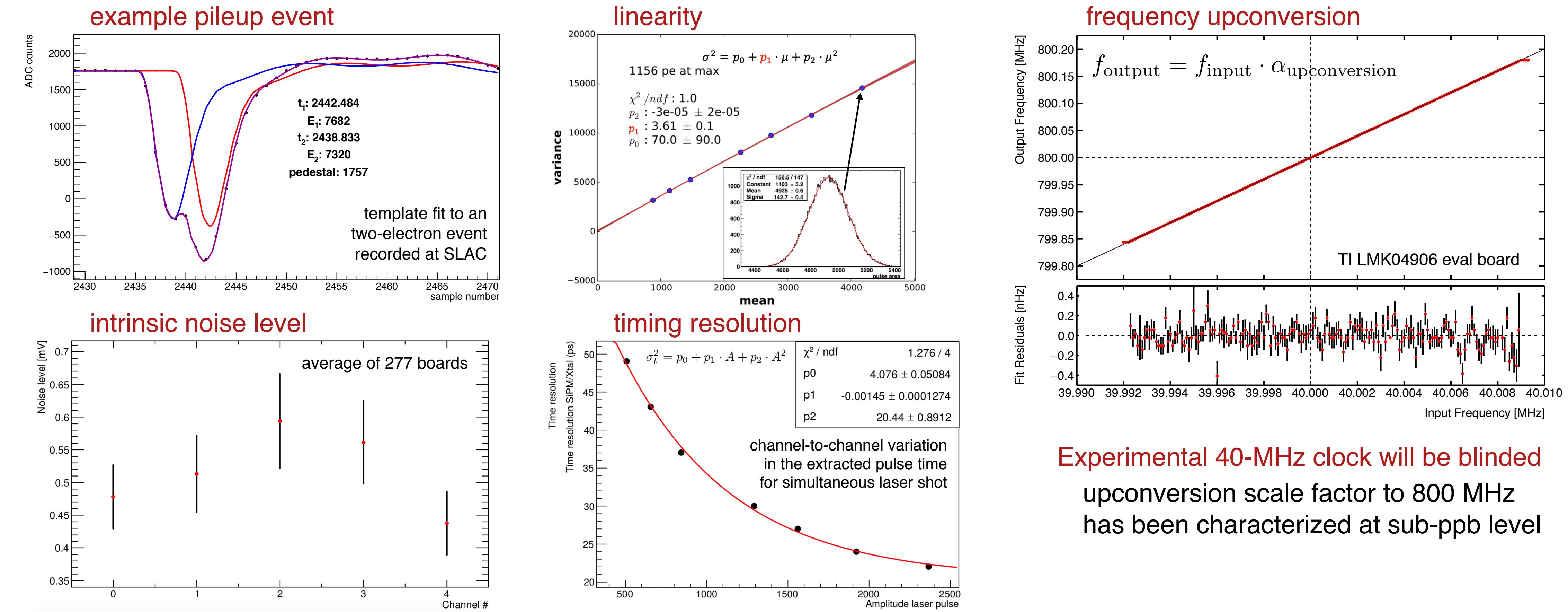


analog front-end card with ECDP connector power supply

Characterization results

- 308 waveform digitizers produced, passing initial quality control
- 18 digitizers heavily stress-tested in SLAC T-536 test beam run
- Intrinsic board noise level of 0.51 ± 0.13 mV among channels
- System is acceptably linear with an $O(10^{-5})$ quadratic term
- Timing resolution between channels is better than 22 ps
- 40-MHz to 800-MHz upconversion factor known to 0.1 ppb
- No observed crosstalk between channels in prototype boards
- No observed performance differences within a 46 gauss field

332 digitizers will be deployed at FNAL by early 2017



Experimental 40-MHz clock will be blinded
 upconversion scale factor to 800 MHz
 has been characterized at sub-ppb level