Belle II

SVD

INFN Istituto Nazionale di Fisica Nucleare
SEZIONE DI PISA

The Silicon Vertex Detector of the *BelleII* experiment

Antonio Paladino on behalf of the BelleII SVD group - 4/08/2016

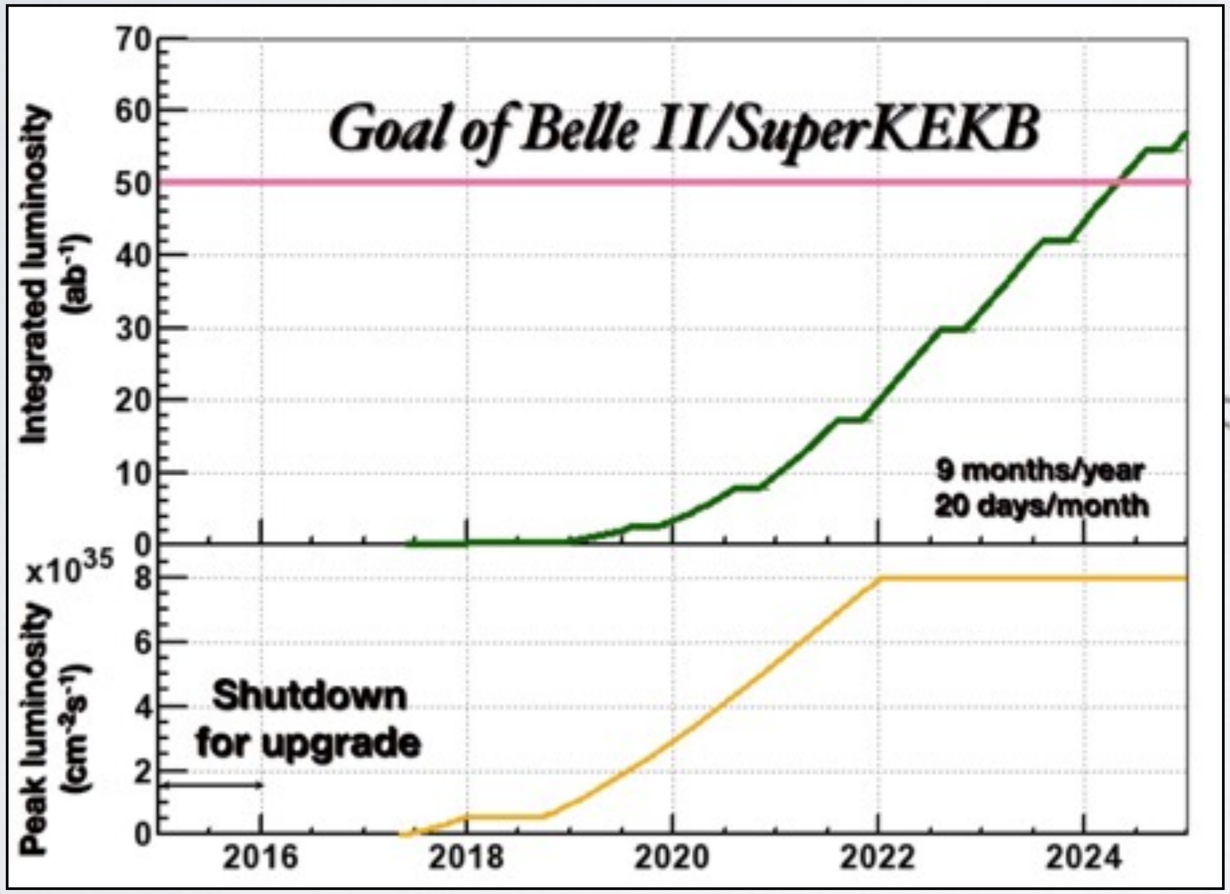
Chicago - ICHEP2016

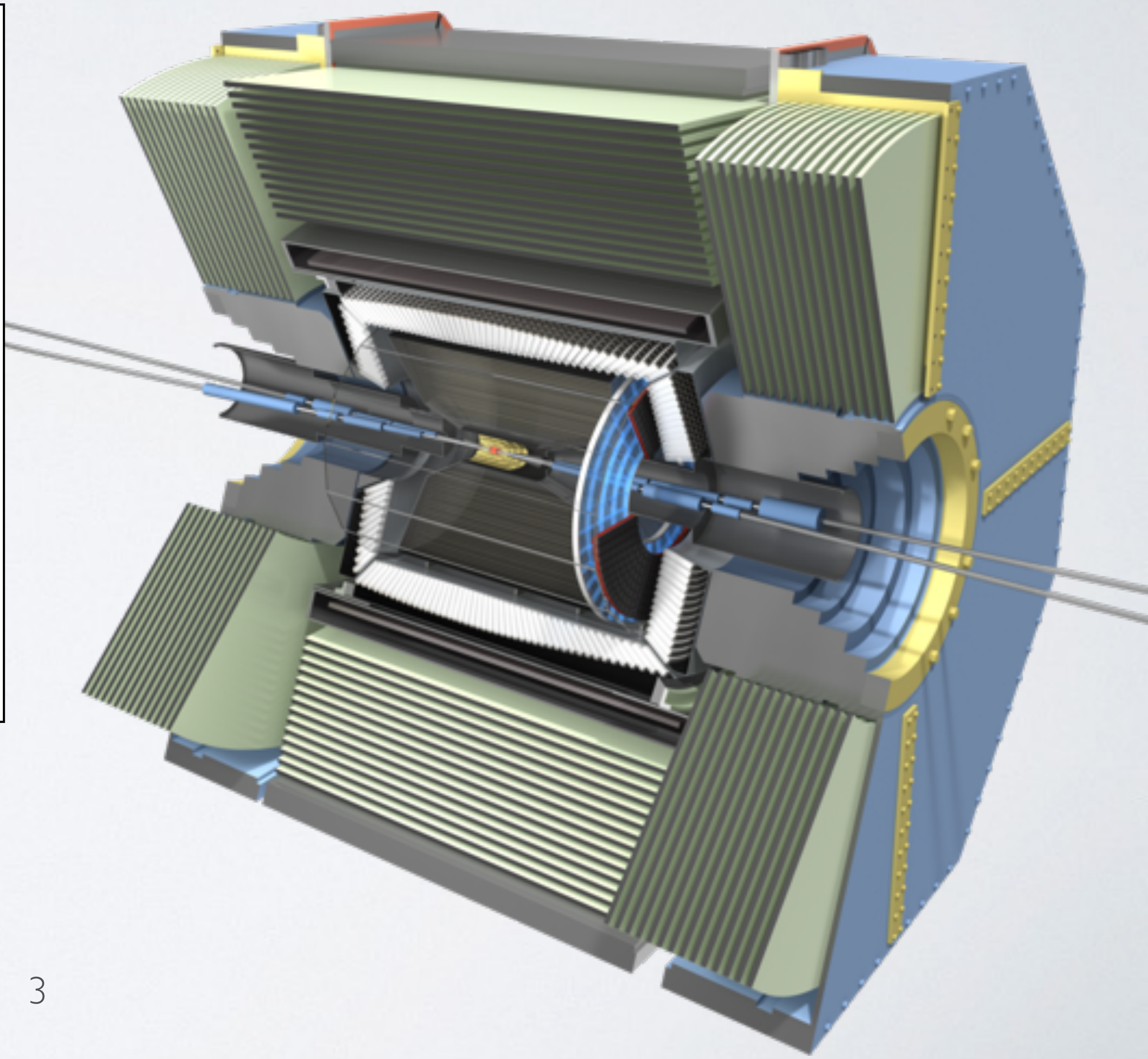
OUTLINE

- BelleII at SuperKEKB
- The BelleII Silicon Vertex Detector
- Ladders overview and the Origami concept
- Performance evaluation

The BelleII experiment at SuperKEKB

The BelleII detector will operate at the asymmetric e^+e^- collider SuperKEKB (Tsukuba, Japan) based on the "Nano-Beam" scheme through which a target luminosity of $L=8.0 \times 10^{35}$ cm^{-2} s^{-1} will be achieved.
Precision measurements in heavy flavour Physics could open channels for New Physics beyond the Standard Model.





- BelleII first Physics run in fall 2018

- For the status of SuperKEKB:
  Peter Lewis, tomorrow at 9:20.

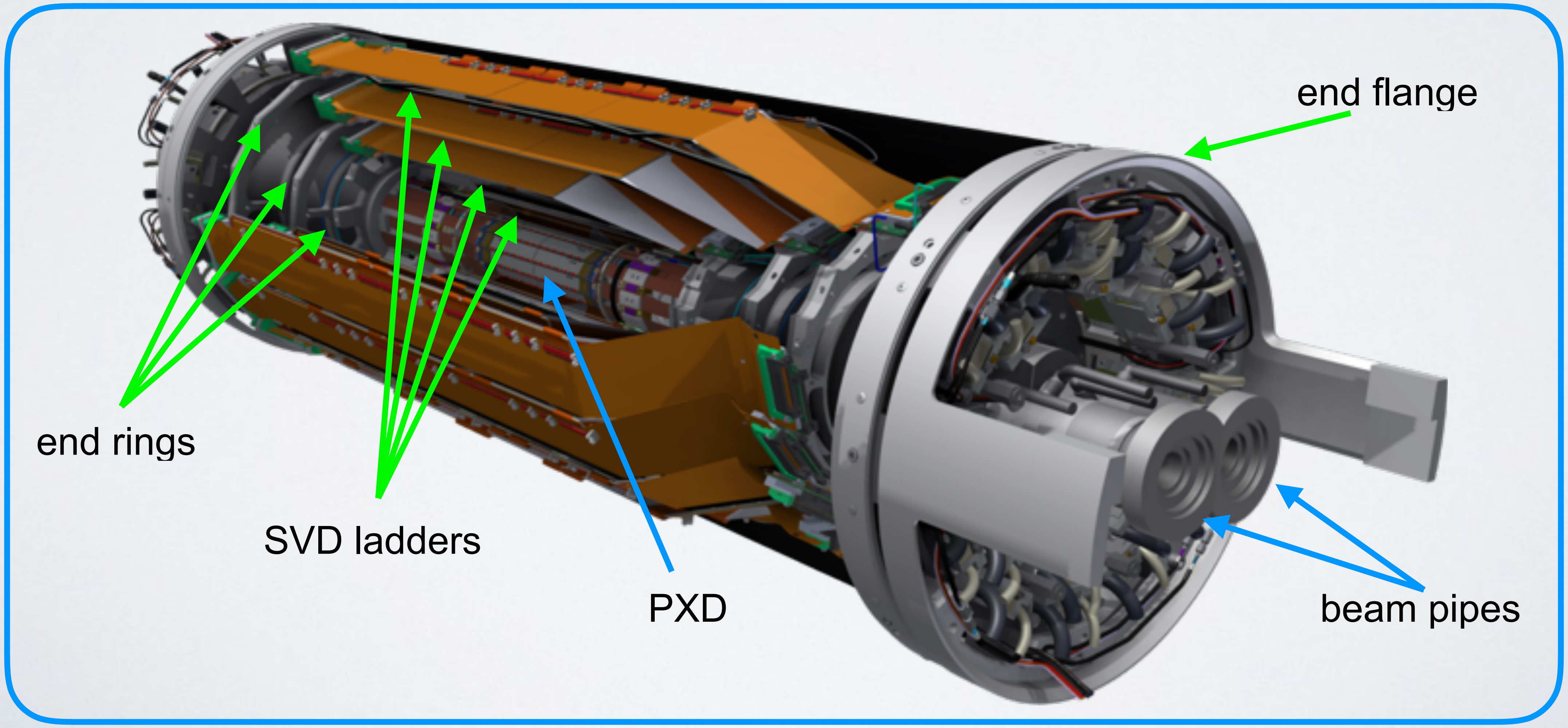
The BelleII VerteX Detector

The vertex detector design has been optimised for the very precise vertex reconstruction of the short-lived meson decays.

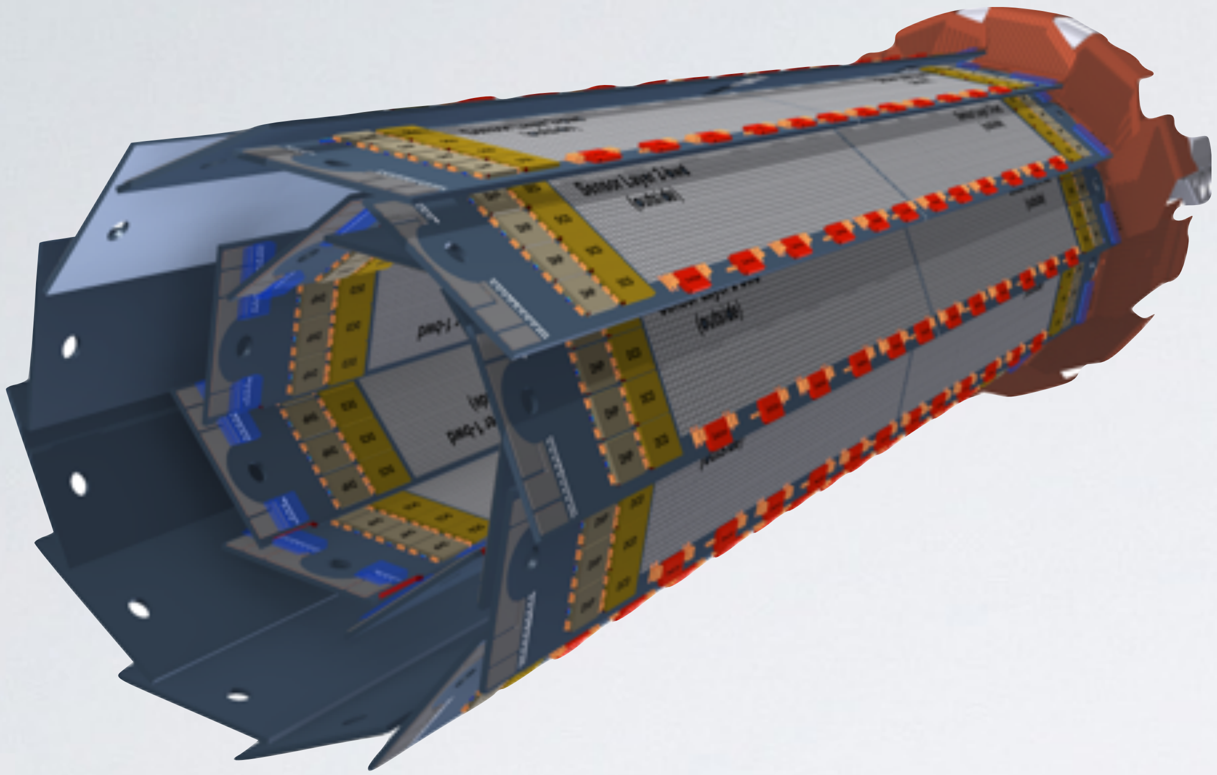
- reduced boost ($\beta\gamma$ = 0.28) & high luminosity/background → thin pixel detector at small radius & silicon strip detector with fast readout electronics.
- bigger radius and acceptance extended in forward region.

VerteX Detector **(VXD)** is composed of:

- **PiXel Detector (PXD):** two layers of DEPFET pixels.
- **Silicon Vertex Detector (SVD):** four layers of Double-Sided Silicon Strip Detectors (DSSD).



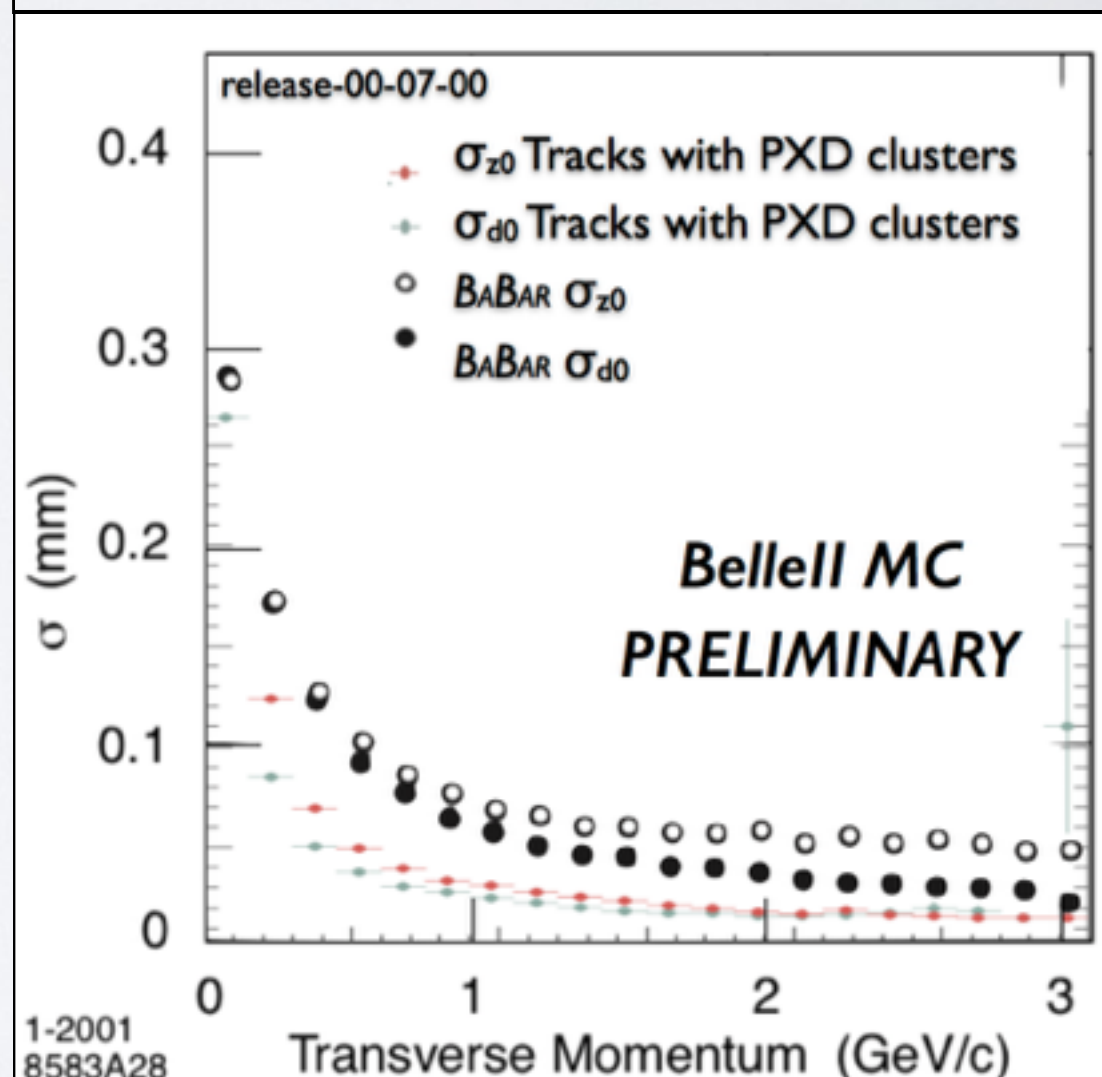
The BelleII PXD



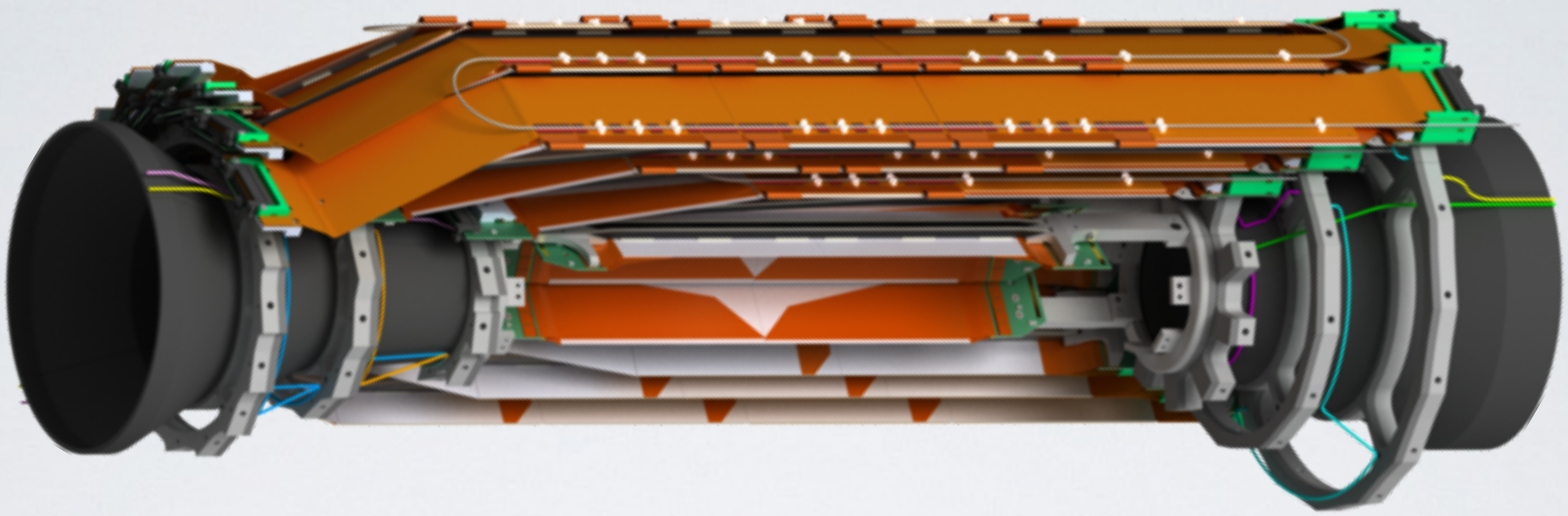
Layer	# of ladders	radius (mm)
L1	8	14
L2	12	22

- **Two layers of DEPFET pixels:**
  - Thickness: 75 μm
  - Pixel size: 50x55 μm^2
  - Low noise
  - Low power consumption
- **On-line data reduction:**
  1. Software trigger
  2. SVD track reconstruction
  3. Region Of Interest definition
  4. Readout of data inside ROIs

Impact parameter resolution



The BelleII SVD features



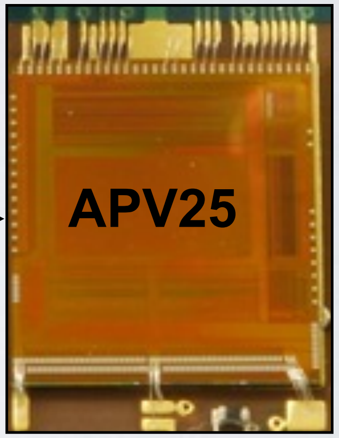
- Occupancy reduction
- Capacitive load reduction on read-out electronics

↓

- Single sensor read-out
- Electronics on the active volume

Electronics requirements
- short shaping time
- radiation hardness
- reduced material budget

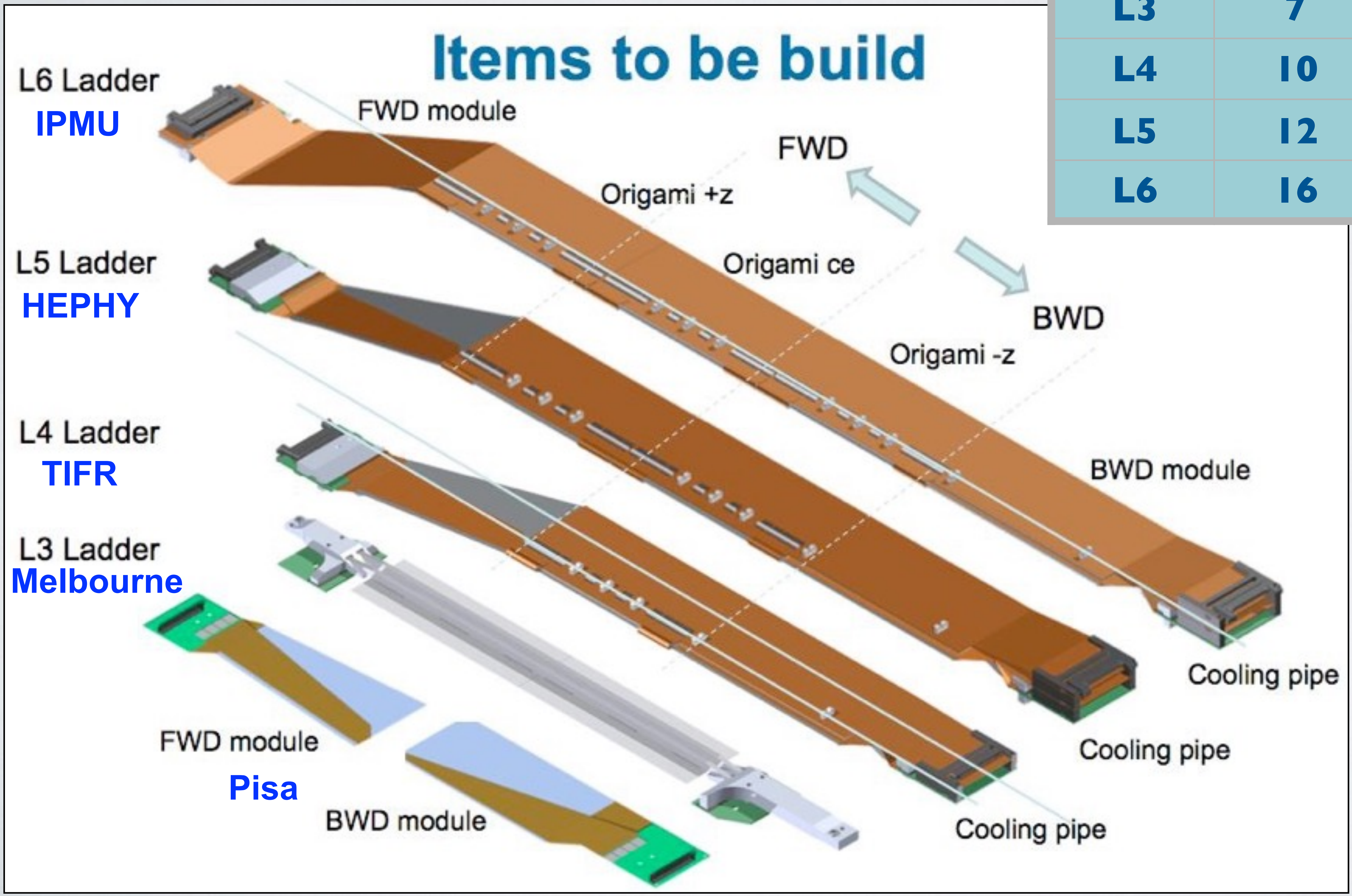
→



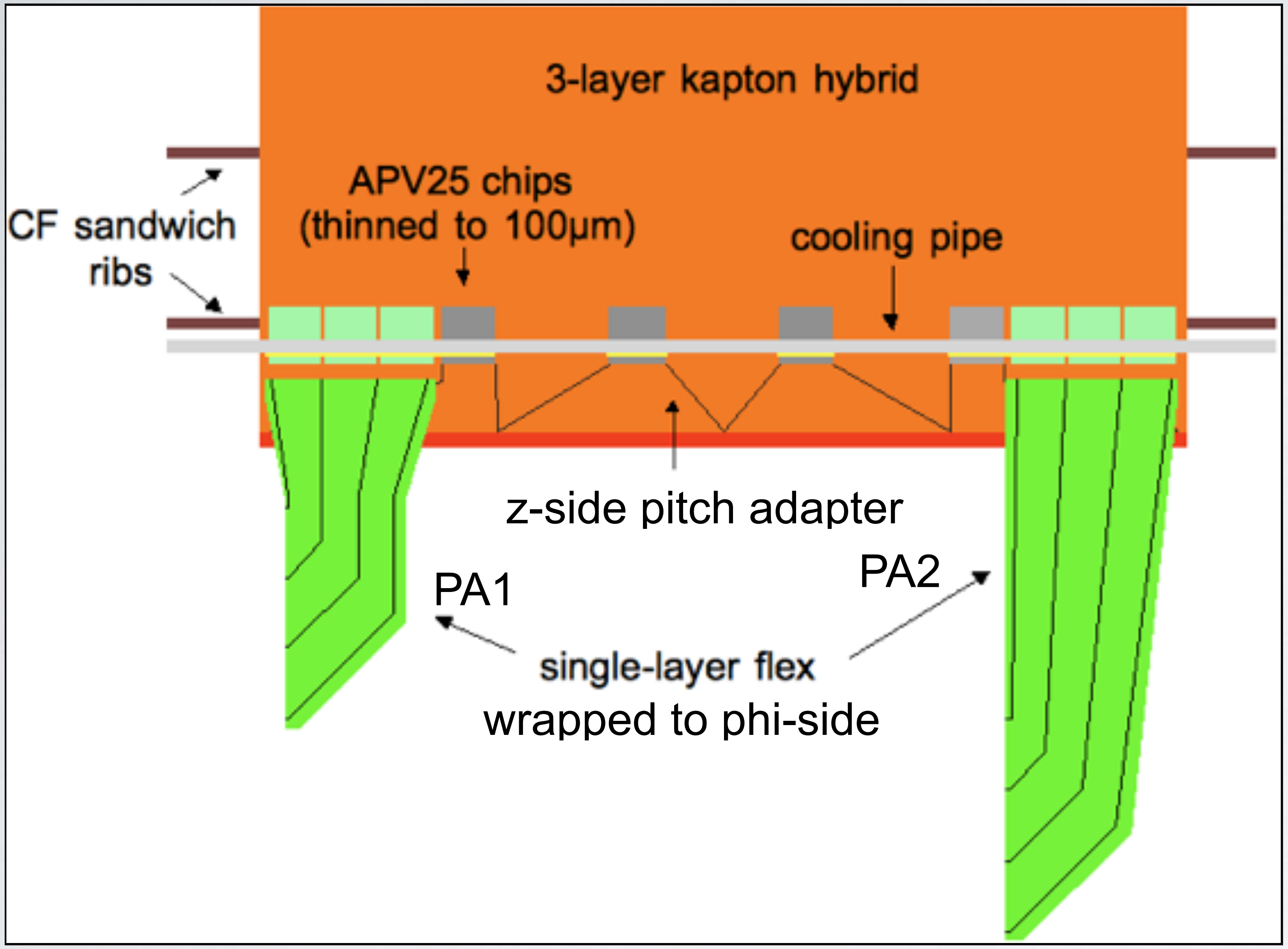
Development of the
“Origami chip-on-sensor” concept

The SVD ladders overview

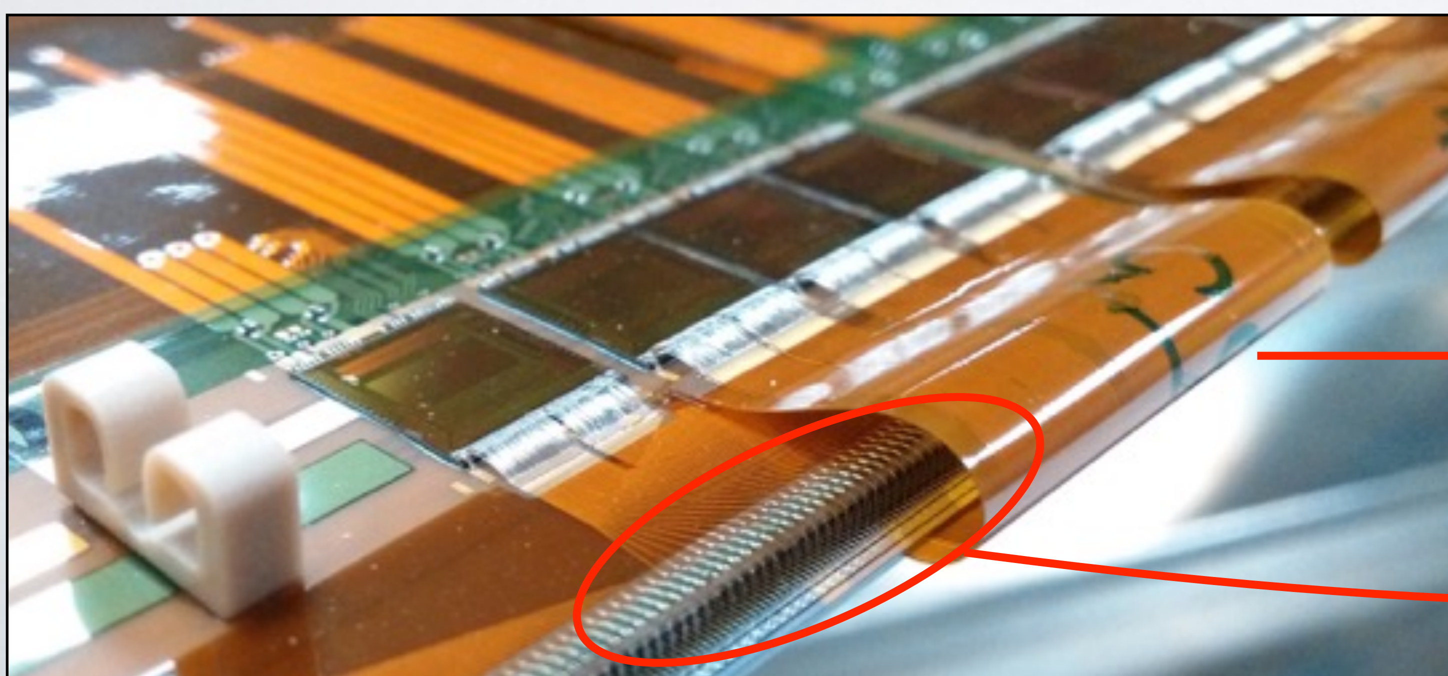
Layer	# of ladders	radius (mm)
L3	7	39
L4	10	80
L5	12	115
L6	16	140



The Origami concept



- Signals on phi-side of inner sensors transferred to the z-side by flex circuits → all APV25 chips can be mounted on z-side.
- Placing read-out chips on the same line, only one cooling channel is required, keeping low the material budget.
- Actual average material budget for a ladder: **x/X_0 = 0.6%**



PA2 wrapped from phi-side to z-side

z-side wire bondings DSSD ⟷ PA

SVD Sensor performance - efficiency

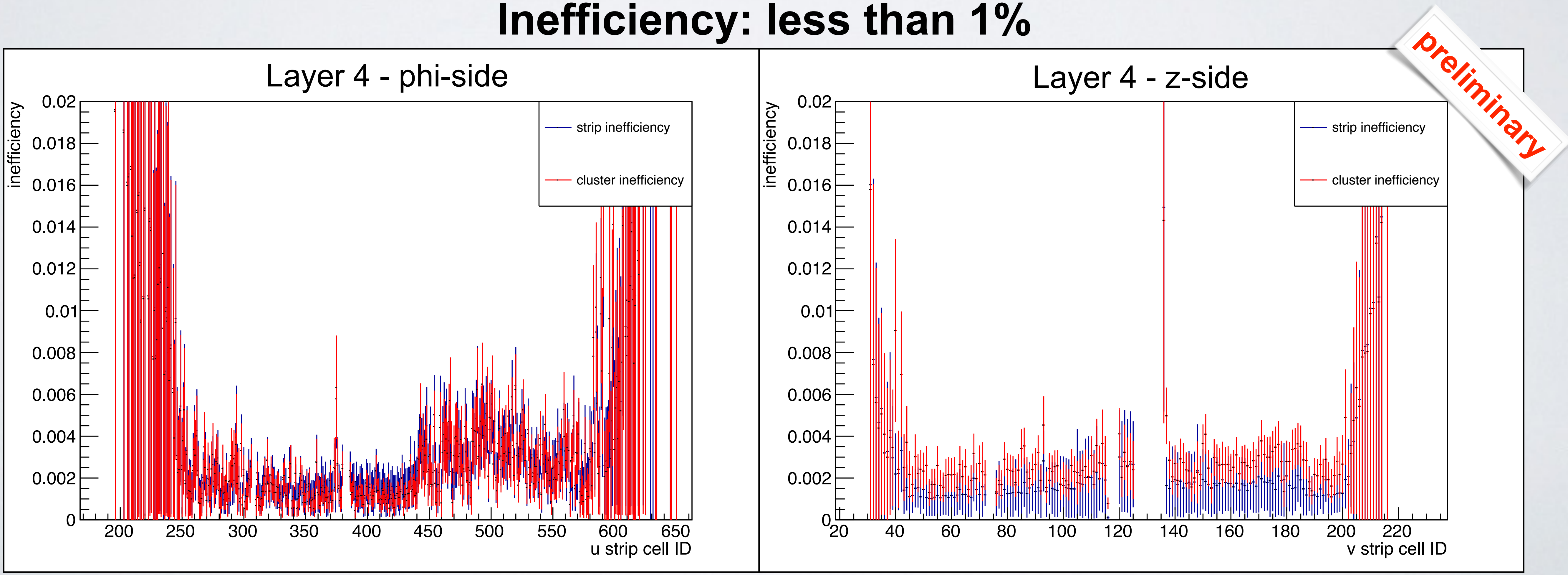
In April 2016 a beam test was done at DESY (Hamburg, Germany) with a combined system PXD+SVD. For the first time a slice of the Belle II VXD was assembled and tested under realistic conditions.

- e^- beam 2÷5 GeV
- B field up to 1 T

Beam test main task:

- PXD and SVD systems integration;
- Software and hardware systems verification;
- **SVD efficiency and resolution studies.**

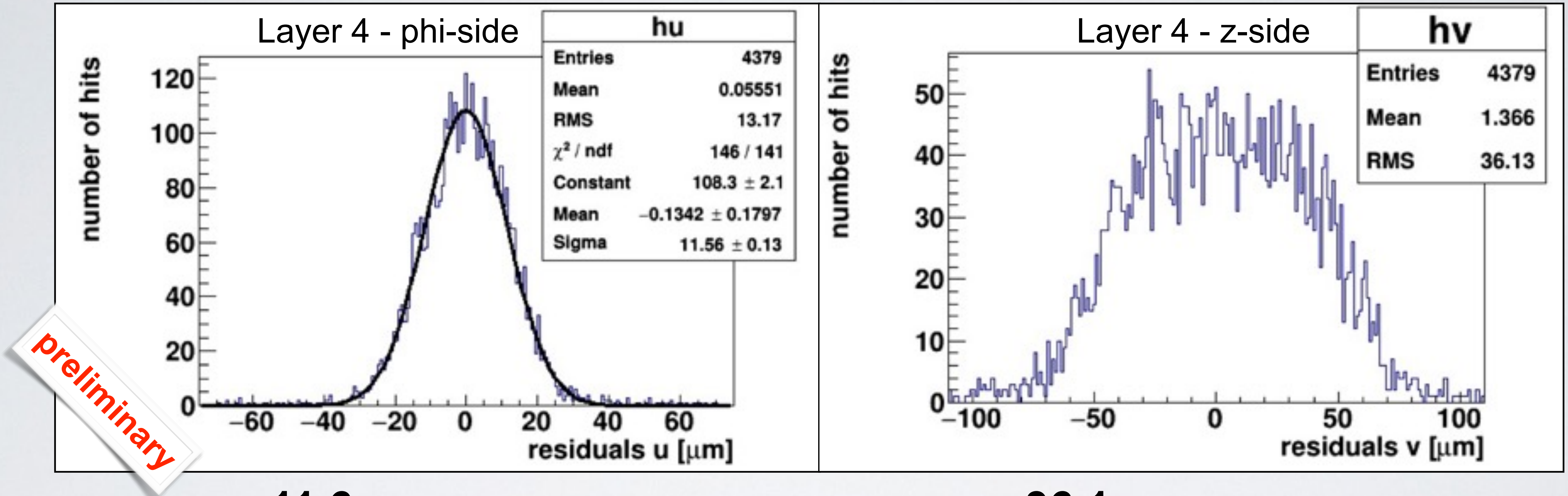
Inefficiency: less than 1%



Plots of the other inefficiencies for every layer available in backup slides

SVD Sensor performance - resolution

- Eudet Telescope with 3 downstream + 3 upstream layers
- Tracks with at least 10 hits in PXD+SVD+Telescope set required

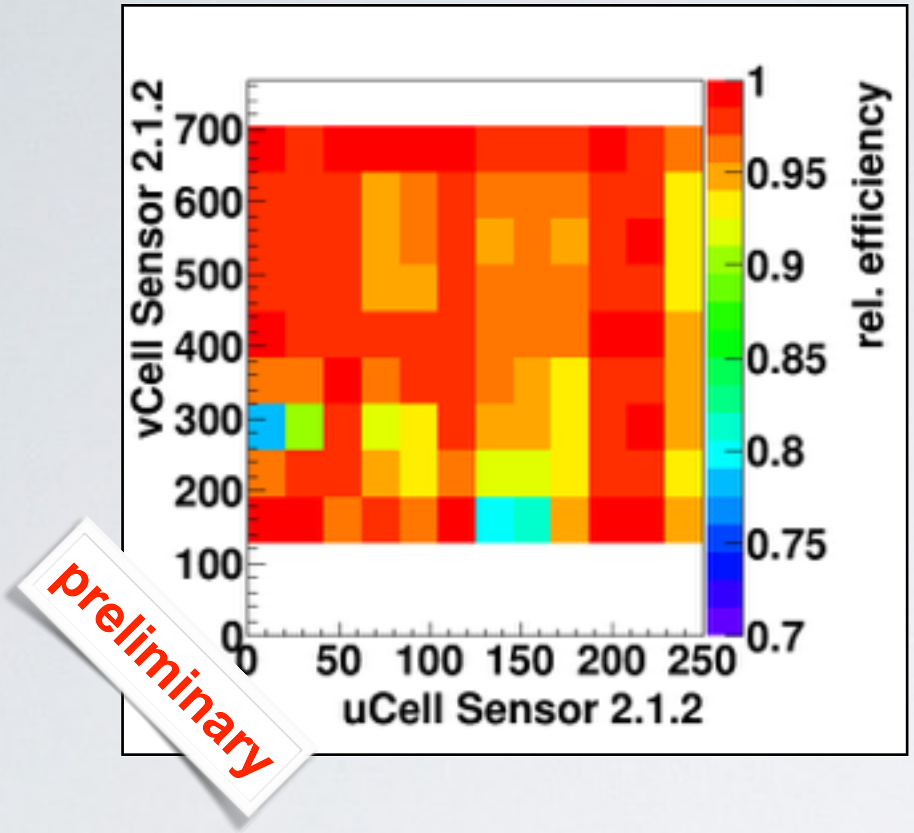


- **σ = 11.6 *μm***
- pitch = 75 *μm*
- digital resolution = 10.8 *μm*

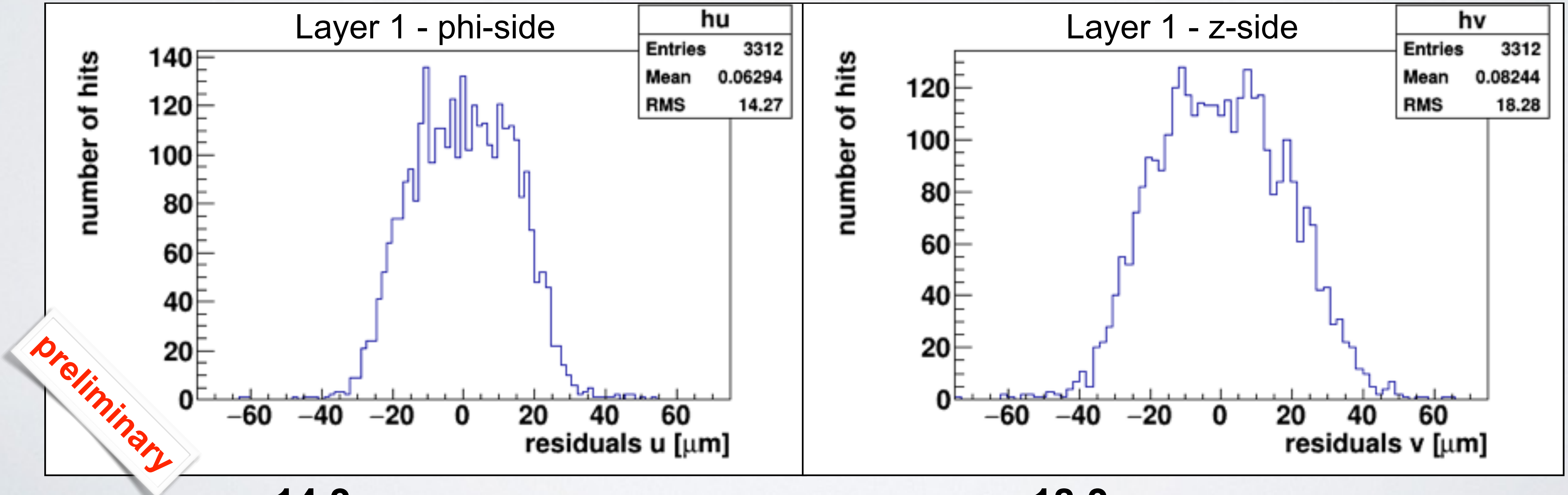
- **σ = 36.1 *μm***
- pitch = 240 *μm*
- digital resolution = 34.6 *μm*

- SVD estimated efficiency > 99%
- Resolution estimation for perpendicular tracks compatible with digital resolution
- Excellent efficiency and resolution results

PXD performance



- Average PXD efficiency > 95%
- Resolutions compatible with digital resolution
- Region Of Interest extrapolation successfully tested



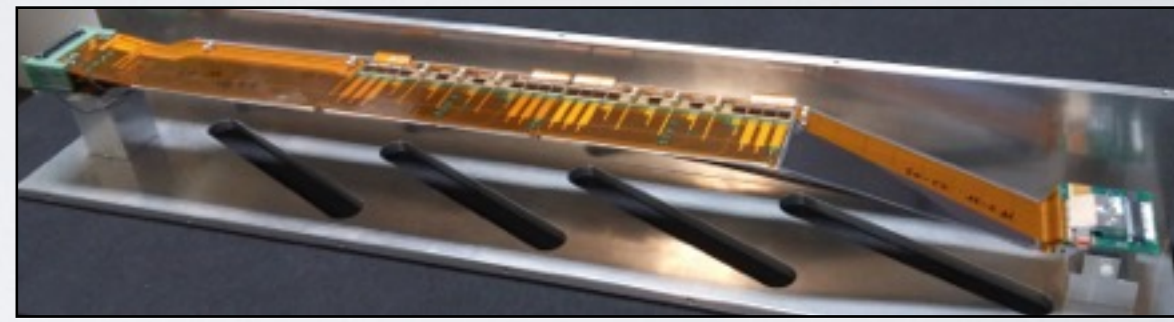
- **σ = 14.3** μm
- digital resolution = 14.3 μm

- **σ = 18.3** μm
- digital resolution = 17.3 μm

Summary and remarks

L6 ladder
IPMU

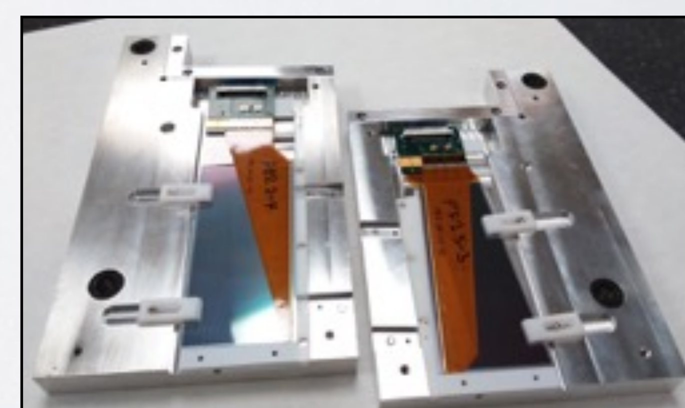
L5 ladder
HEPHY



L4 ladder
TIFR

L3 ladder
Melbourne

FW/BW
Pisa



- All sites have started assembling production grade ladders.
- SVD ladder mount scheduled in February 2017.
- SVD commissioning in October 2017.
- BelleII first physics run foreseen in fall 2018.

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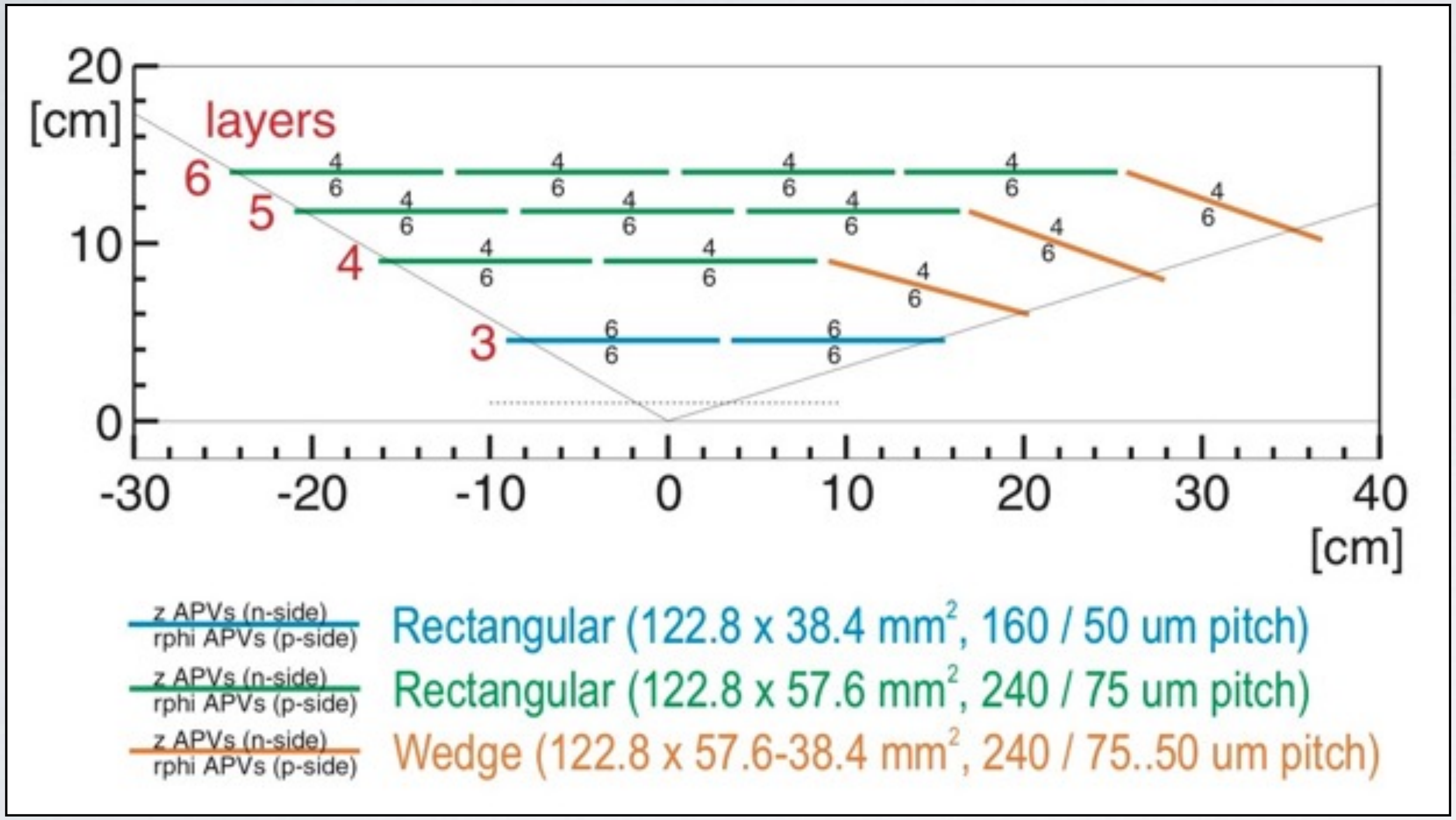
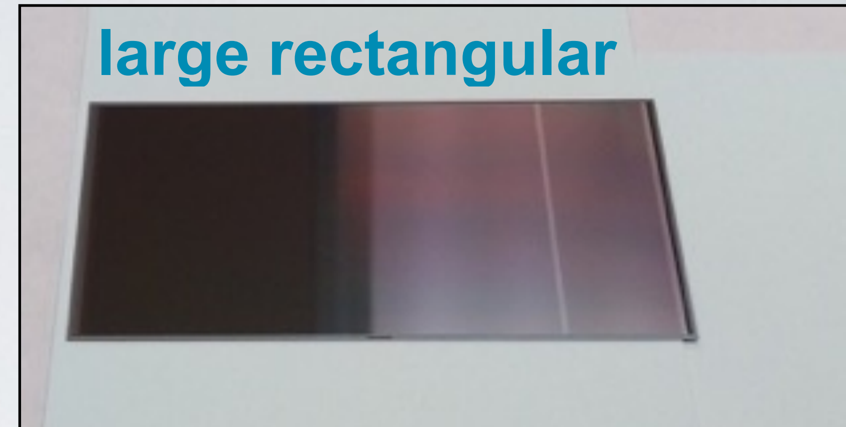
Thanks

BACKUP SLIDES

SVD Silicon sensors

Double Sided silicon Strip Detectors of 300 μm thickness



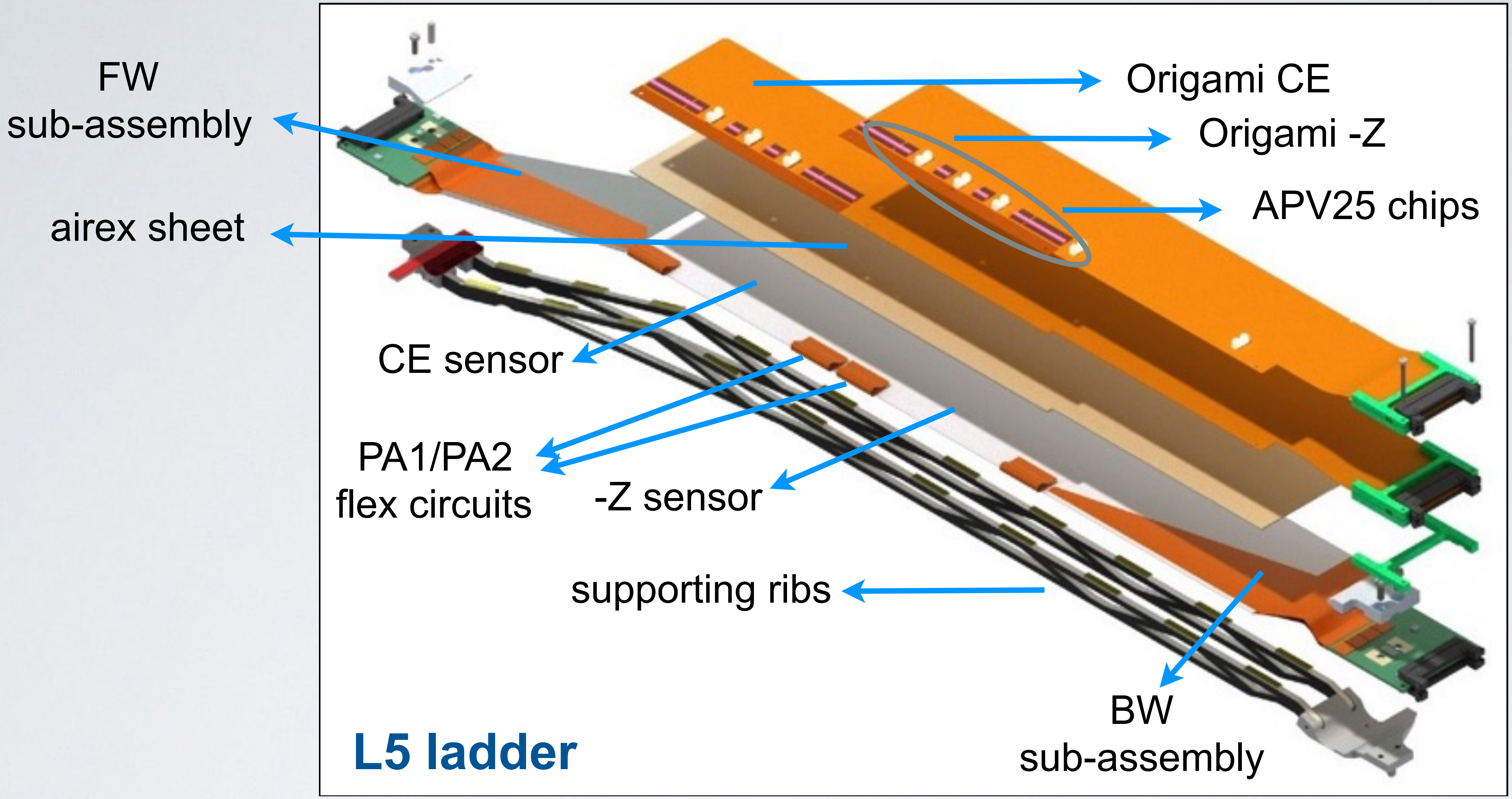


Rectangular sensors provided by HPK
Wedge sensors provided by Micron

HPK sensors	Large sensor	Small sensor
# strips p-side	768	768
# strips n-side	512	768
# intermediate strips p-side	767	767
# intermediate strips n-side	511	767
Pitch p-side	$75\,\mu m$	$50\,\mu m$
Pitch n-side	$240\,\mu m$	$160\,\mu m$
Area (total)	$7442.85\,mm^2$	$5048.90\,mm^2$
Area (active)	$7029.88\,mm^2$ (94.5%)	$4737.80\,mm^2$ (93.8%)

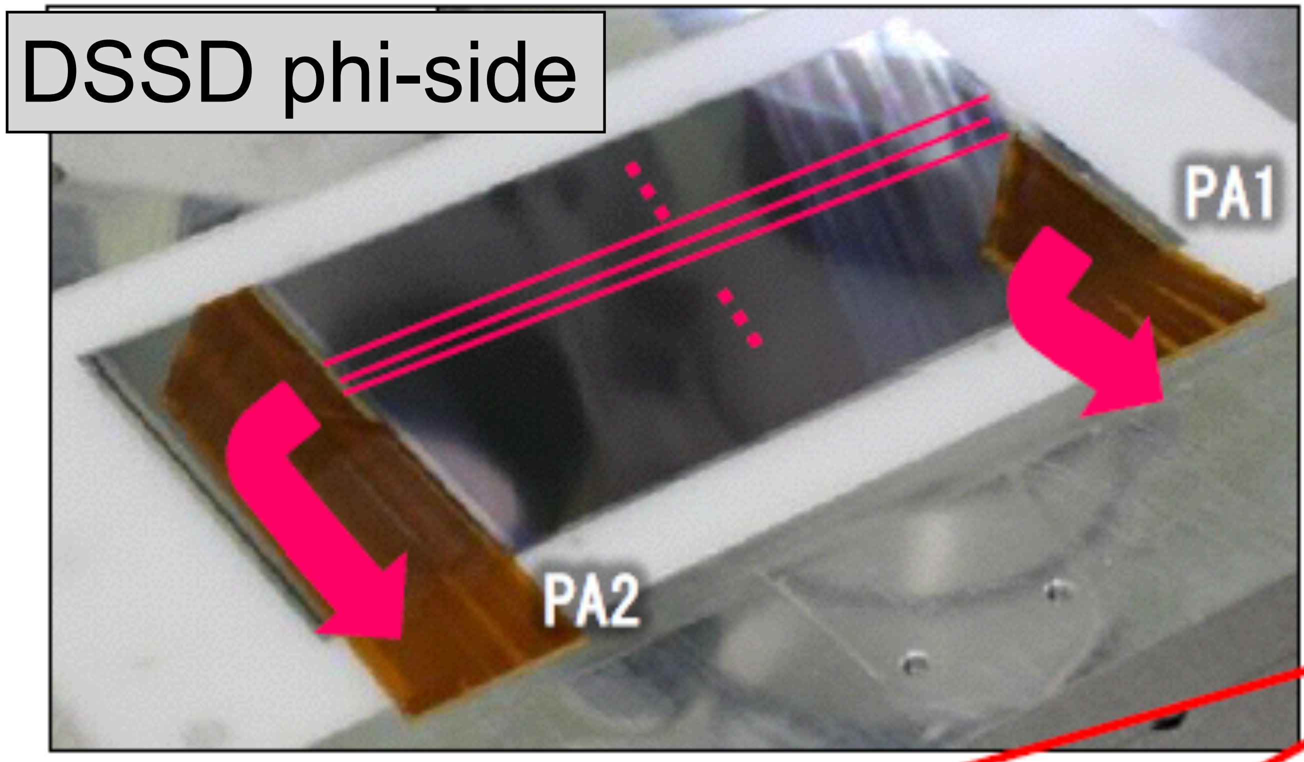
Micron sensors	Value
# strips p-side	768
# strips n-side	512
# intermediate strips p-side	767
# intermediate strips n-side	511
Pitch p-side	$75 \ldots 50\,\mu m$
Pitch n-side	$240\mu m$
Area (total)	$6382.6\,mm^2$
Area (active)	$5890\,mm^2$ (92.3%)
Slant angles	Layer 6: 21.1° Layer 5: 17.2° Layer 4: 11.9°

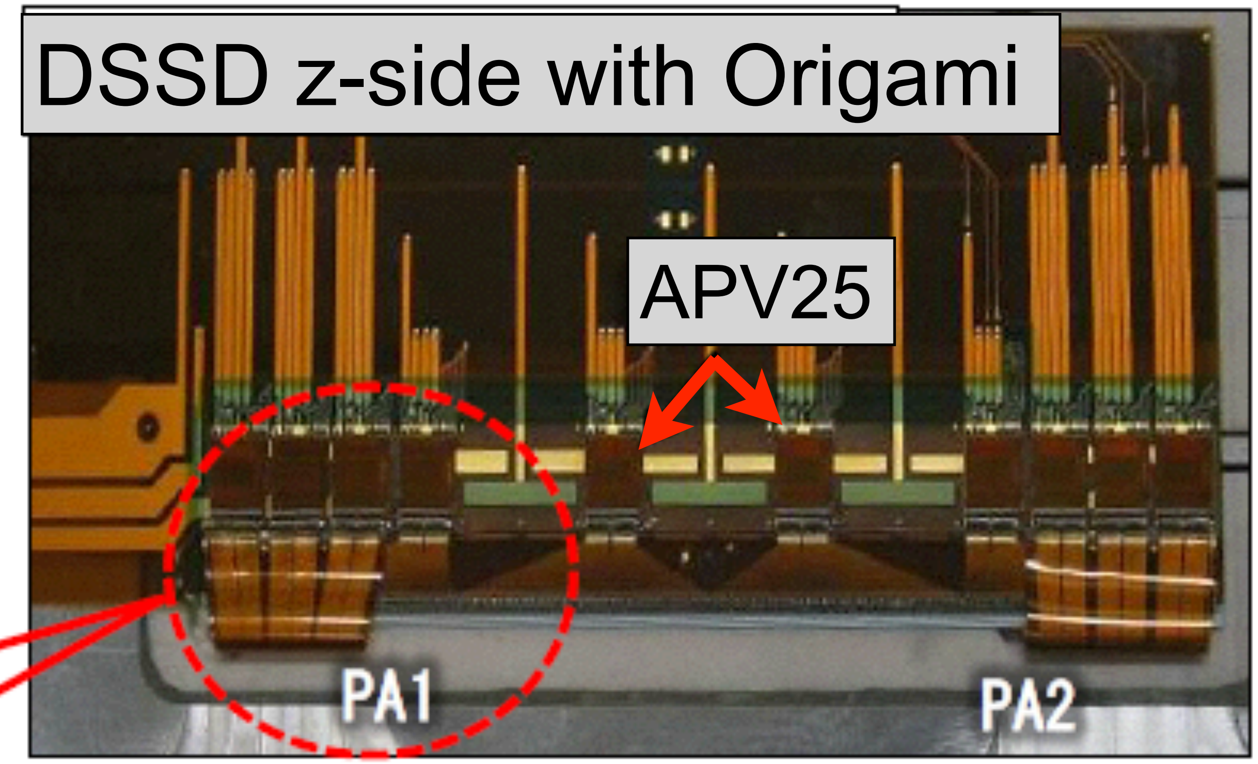
The SVD ladder design

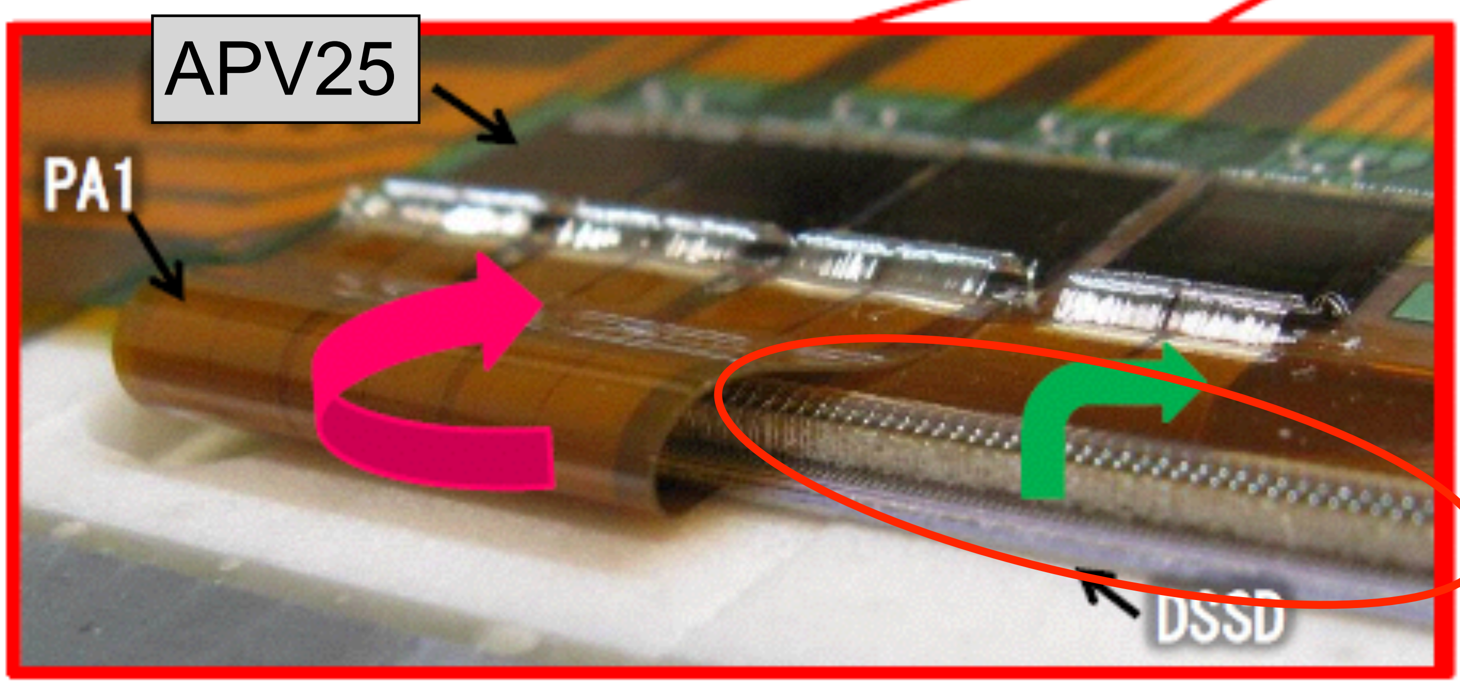


FW and BW parts of ladders are read out by APV25 chips on hybrid boards placed outside of sensible volume of SVD.
For inner sensors APV25 chips are placed on a 3-layer kapton hybrid circuits called Origami, which are glued onto the sensors.

The Origami concept



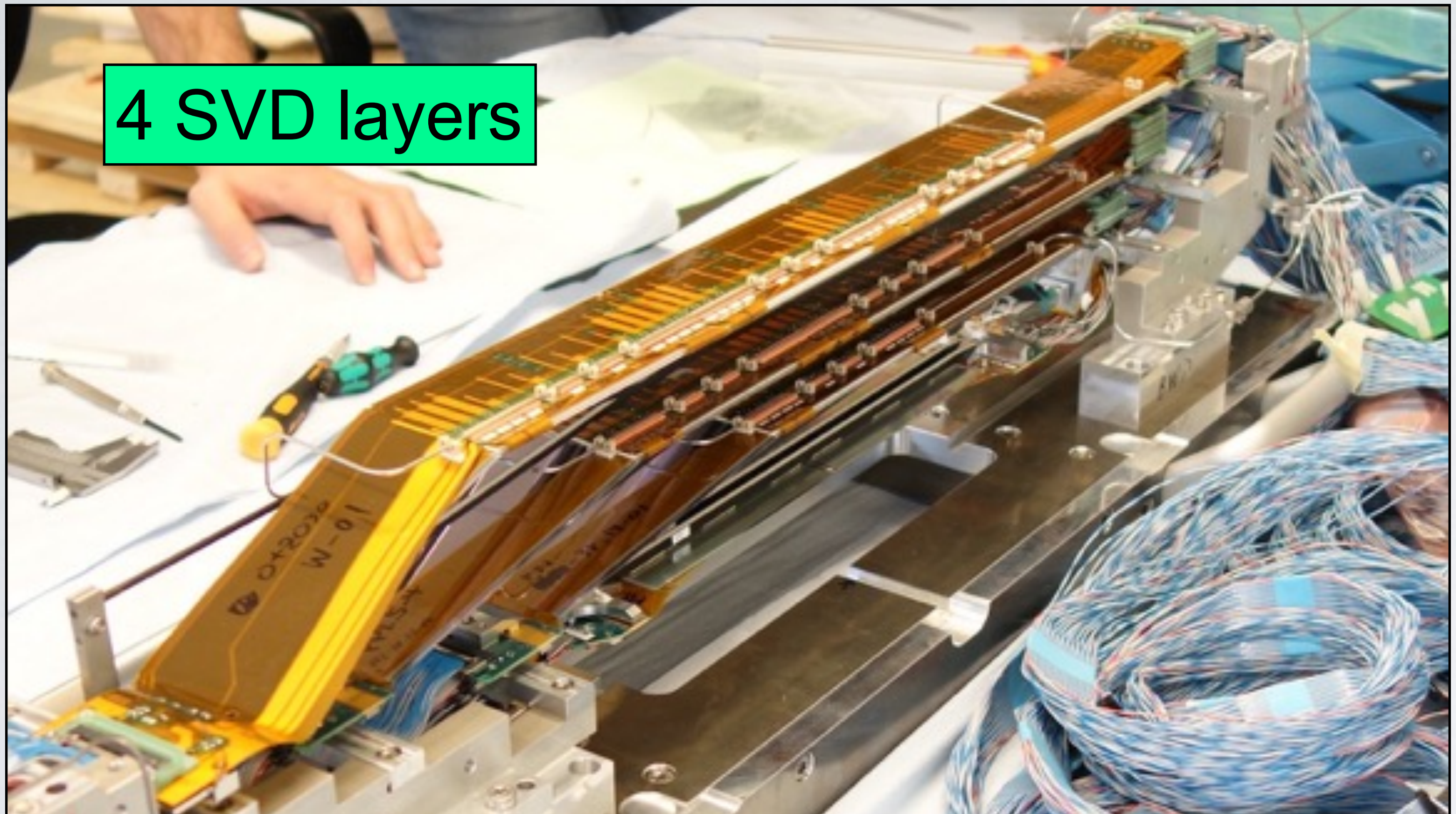


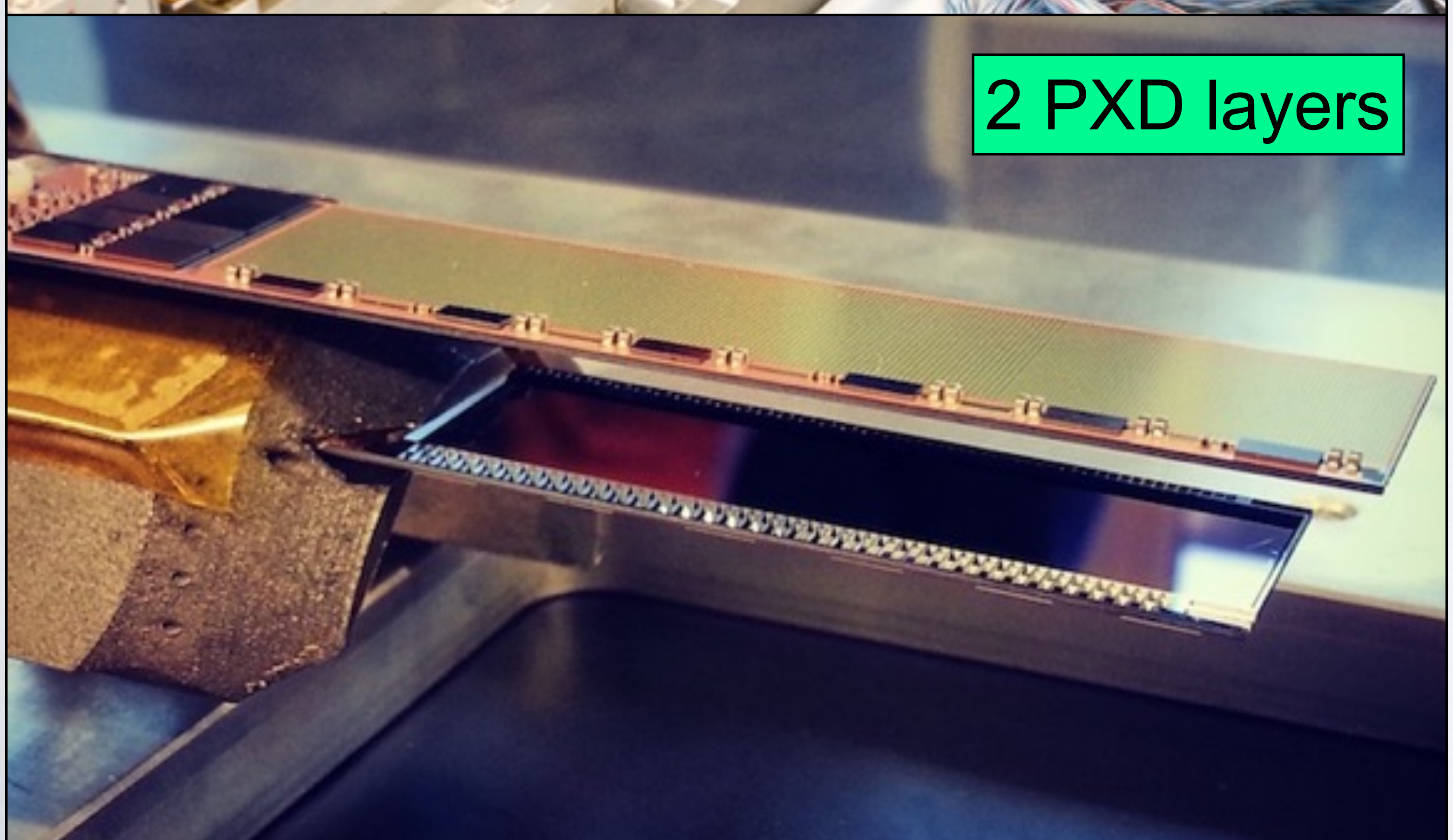


PA1/PA2 flex circuits are wrapped to bring signals from phi-side to z-side of the DSSD and are glued above the micro bondings of the z-side.

Wire bondings DSSD ↔ PA0

VXD Beam-test





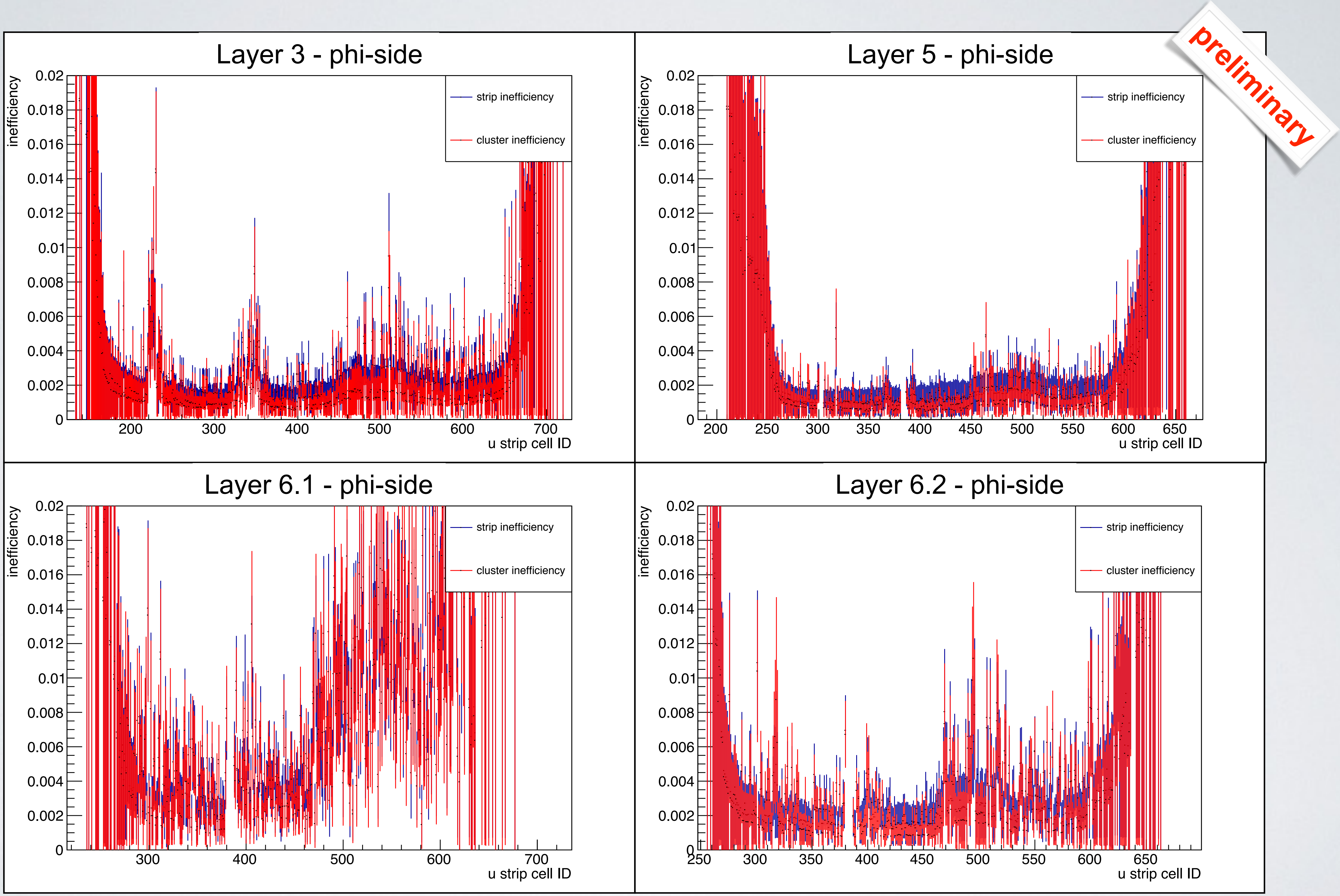
- Solenoid magnetic field up to 1T
- e^- beam with energy between 2 and 5 GeV

Verify:
- PXD+SVD integration
- Complete DAQ read-out chain
- CO_2 cooling system
- Slow control
- Monitoring and environmental sensors
- Alignment and tracking algorithms
- On-line data reduction
- Efficiency and resolution

Beam-test results - SVD efficiency

- Environment conditions: B-field = 1T, p_{e-}= 5 GeV
- efficiency for every SVD layer was evaluated with the following method:
  - extrapolate tracks using hits on three SVD layers;
  - predict the position of the extrapolated track on the fourth SVD layer;
  - define a region 300 um wide around the predicted track position;
  - count the number of hits (clusters) on that region and calculate the efficiency of the layer as: $\varepsilon = \frac{\#hits}{\#tracks}$
  - inefficiency defined as: $\eta = 1 - \varepsilon$

Beam-test results - SVD efficiency



Beam-test results - SVD efficiency