The Silicon Vertex Detector of the \textit{Belle II} experiment

Antonio Paladino on behalf of the Belle II SVD group - 4/08/2016
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OUTLINE

- BelleII at SuperKEKB
- The BelleII Silicon Vertex Detector
- Ladders overview and the Origami concept
- Performance evaluation
The BelleII experiment at SuperKEKB

The BelleII detector will operate at the asymmetric e⁺e⁻ collider SuperKEKB (Tsukuba, Japan) based on the “Nano-Beam” scheme through which a target luminosity of $L = 8.0 \times 10^{35}$ cm⁻² s⁻¹ will be achieved. Precision measurements in heavy flavour Physics could open channels for New Physics beyond the Standard Model.

- BelleII first Physics run in fall 2018

- For the status of SuperKEKB: Peter Lewis, tomorrow at 9:20.
The Bellell VerteX Detector

The vertex detector design has been optimised for the very precise vertex reconstruction of the short-lived meson decays.

- reduced boost ($\beta\gamma = 0.28$) & high luminosity/background $\rightarrow$ thin pixel detector at small radius & silicon strip detector with fast readout electronics.
- bigger radius and acceptance extended in forward region.

VerteX Detector (VXD) is composed of:
- **PiXel Detector (PXD):** two layers of DEPFET pixels.
- **Silicon Vertex Detector (SVD):** four layers of Double-Sided Silicon Strip Detectors (DSSD).
The Belle II PXD

- Two layers of DEPFET pixels:
  - Thickness: 75 $\mu m$
  - Pixel size: 50x55 $\mu m^2$
  - Low noise
  - Low power consumption

- On-line data reduction:
  1. Software trigger
  2. SVD track reconstruction
  3. Region Of Interest definition
  4. Readout of data inside ROIs

<table>
<thead>
<tr>
<th>Layer</th>
<th># of ladders</th>
<th>radius (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>8</td>
<td>14</td>
</tr>
<tr>
<td>L2</td>
<td>12</td>
<td>22</td>
</tr>
</tbody>
</table>

Impact parameter resolution
The Bellell SVD features

- Occupancy reduction
- Capacitive load reduction on read-out electronics
- Single sensor read-out
- Electronics on the active volume

Electronics requirements
- short shaping time
- radiation hardness
- reduced material budget

Development of the “Origami chip-on-sensor” concept
The SVD ladders overview

<table>
<thead>
<tr>
<th>Layer</th>
<th># of ladders</th>
<th>Radius (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L3</td>
<td>7</td>
<td>39</td>
</tr>
<tr>
<td>L4</td>
<td>10</td>
<td>80</td>
</tr>
<tr>
<td>L5</td>
<td>12</td>
<td>115</td>
</tr>
<tr>
<td>L6</td>
<td>16</td>
<td>140</td>
</tr>
</tbody>
</table>

Items to be build

- **L6 Ladder**
  - IPMU
- **L5 Ladder**
  - HEPHY
- **L4 Ladder**
  - TIFR
- **L3 Ladder**
  - Melbourne

**Pisa**

**Layer**

**FWD module**

**Origami +z**

**BWD module**

**Origami -z**

**FWD**

**BWD**

**Cooling pipe**
The Origami concept

- Signals on phi-side of inner sensors transferred to the z-side by flex circuits → all APV25 chips can be mounted on z-side.
- Placing read-out chips on the same line, only one cooling channel is required, keeping low the material budget.
- Actual average material budget for a ladder: $x/X_0 = 0.6\%$

PA2 wrapped from phi-side to z-side

z-side wire bondings

DSSD ↔ PA
SVD Sensor performance - efficiency

In April 2016 a beam test was done at DESY (Hamburg, Germany) with a combined system PXD+SVD. For the first time a slice of the Belle II VXD was assembled and tested under realistic conditions.

Beam test main task:
- PXD and SVD systems integration;
- Software and hardware systems verification;
- SVD efficiency and resolution studies.

Inefficiency: less than 1%

Plots of the other inefficiencies for every layer available in backup slides
**SVD Sensor performance - resolution**

- Eudet Telescope with 3 downstream + 3 upstream layers
- Tracks with at least 10 hits in PXD+SVD+Telescope set required

![Graphs](image)

- $\sigma = 11.6 \, \mu m$
  - pitch = 75 $\mu m$
  - digital resolution = 10.8 $\mu m$

- $\sigma = 36.1 \, \mu m$
  - pitch = 240 $\mu m$
  - digital resolution = 34.6 $\mu m$

- SVD estimated efficiency > 99%
- Resolution estimation for perpendicular tracks compatible with digital resolution
- Excellent efficiency and resolution results
PXD performance

- Average PXD efficiency > 95%
- Resolutions compatible with digital resolution
- Region Of Interest extrapolation successfully tested

Layer 1 - phi-side

- $\sigma = 14.3 \ \mu m$
- digital resolution = 14.3 $\mu m$

Layer 1 - z-side

- $\sigma = 18.3 \ \mu m$
- digital resolution = 17.3 $\mu m$
Summary and remarks

- All sites have started assembling production grade ladders.
- SVD ladder mount scheduled in February 2017.
- SVD commissioning in October 2017.
- BelleII first physics run foreseen in fall 2018.
THANKS
Backup slides
SVD Silicon sensors

Double Sided silicon Strip Detectors of 300 µm thickness

Rectangular sensors provided by HPK
Wedge sensors provided by Micron

<table>
<thead>
<tr>
<th>Micron sensors</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td># strips p-side</td>
<td>768</td>
</tr>
<tr>
<td># strips n-side</td>
<td>512</td>
</tr>
<tr>
<td># intermediate strips p-side</td>
<td>767</td>
</tr>
<tr>
<td># intermediate strips n-side</td>
<td>511</td>
</tr>
<tr>
<td>Pitch p-side</td>
<td>75...50 µm</td>
</tr>
<tr>
<td>Pitch n-side</td>
<td>240 µm</td>
</tr>
<tr>
<td>Area (total)</td>
<td>6382.6 mm²</td>
</tr>
<tr>
<td>Area (active)</td>
<td>5890 mm² (92.3%)</td>
</tr>
<tr>
<td>Slant angles</td>
<td></td>
</tr>
<tr>
<td>Layer 6: 21.1°</td>
<td></td>
</tr>
<tr>
<td>Layer 5: 17.2°</td>
<td></td>
</tr>
<tr>
<td>Layer 4: 11.9°</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>HPK sensors</th>
<th>Large sensor</th>
<th>Small sensor</th>
</tr>
</thead>
<tbody>
<tr>
<td># strips p-side</td>
<td>768</td>
<td>768</td>
</tr>
<tr>
<td># strips n-side</td>
<td>512</td>
<td>768</td>
</tr>
<tr>
<td># intermediate strips p-side</td>
<td>767</td>
<td>767</td>
</tr>
<tr>
<td># intermediate strips n-side</td>
<td>511</td>
<td>511</td>
</tr>
<tr>
<td>Pitch p-side</td>
<td>75 µm</td>
<td>50 µm</td>
</tr>
<tr>
<td>Pitch n-side</td>
<td>240 µm</td>
<td>160 µm</td>
</tr>
<tr>
<td>Area (total)</td>
<td>7442.85 mm²</td>
<td>5048.90 mm²</td>
</tr>
<tr>
<td>Area (active)</td>
<td>7029.88 mm² (94.5%)</td>
<td>4737.80 mm² (93.8%)</td>
</tr>
</tbody>
</table>
FW and BW parts of ladders are read out by APV25 chips on hybrid boards placed outside of sensible volume of SVD. For inner sensors APV25 chips are placed on a 3-layer kapton hybrid circuits called Origami, which are glued onto the sensors.
The Origami concept

PA1/PA2 flex circuits are wrapped to bring signals from phi-side to z-side of the DSSD and are glued above the micro bondings of the z-side.

Wire bondings DSSD ↔ PA0
VXD Beam-test

4 SVD layers

2 PXD layers

• Solenoid magnetic field up to 1T
• e⁻ beam with energy between 2 and 5 GeV

Verify:
• PXD+SVD integration
• Complete DAQ read-out chain
• CO2 cooling system
• Slow control
• Monitoring and environmental sensors
• Alignment and tracking algorithms
• On-line data reduction
• Efficiency and resolution
Beam-test results - SVD efficiency

- Environment conditions: B-field = 1T, $p_e = 5$ GeV
- Efficiency for every SVD layer was evaluated with the following method:
  - Extrapolate tracks using hits on three SVD layers;
  - Predict the position of the extrapolated track on the fourth SVD layer;
  - Define a region 300 um wide around the predicted track position;
  - Count the number of hits (clusters) on that region and calculate the efficiency of the layer as: $\varepsilon = \frac{\#\text{hits}}{\#\text{tracks}}$

- Inefficiency defined as: $\eta = 1 - \varepsilon$
Beam-test results - SVD efficiency

Layer 3 - phi-side

Layer 5 - phi-side

Layer 6.1 - phi-side

Layer 6.2 - phi-side

preliminary
Beam-test results - SVD efficiency

Layer 3 - z-side

Layer 5 - z-side

Layer 6.1 - z-side

Layer 6.2 - z-side