High Luminosity LHC Pixel Readout Test Chip and RD53A Prototype Plans

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HL-LHC Main Challenge: Intensity

Normal intensity, nice image

High intensity, over-exposed

• Need the high intensity to make more Higgs Bosons, etc
• Pixel detector (~imager) must handle higher and higher intensity
Pixel Readout Perspective

Particles / Hits

Raining

Pouring

Onto detector surface area

* Store full time sequence of drops until trigger (not collect in a bucket)
* Can quantify rate as memory bits / area / time
  (note: no mention of pixel size)
Readout Chip Evolution

10 yrs ago

today

HL-LHC

<1 Gbps/cm²

5 Gbps/cm²

40 Gbps/cm²

Another way to say memory per unit area: Logic Density. We follow Moore’s Law.
Rad Hard Logic Density Scaling

28nm?

65nm

130nm

0.25um

ELT

Not quite minimum size due to pesky radiation damage

* Huge amount of work done on radiation hardness.
* Quite well understood by now
* Will not cover in this talk

65nm Narrow Transistors

Change in full-on current [%]

1Grad

NMOS

PMOS
65nm, RD53

RD-53 Collaboration Home

RD-53 will develop the tools and designs needed to produce the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC. There is also interest and participation by CLIC. More details can be found in the collaboration proposal.

RAL meeting, 2014:
FE65-P2 test chip

* Stepping stone to RD53A (flow, layout, isolation...)

* 64x64 pixels on 50μm grid

There’s the logic density a.k.a digital sea

Miniature sensor bump bonded to single chip

4.3mm

3.5mm
Threshold Evolution with Radiation

Measure without retuning

0 dose

Tuned to 800e +/-40e

Example of Column 5 (without Leakage Current Compensation circuit) and Column 8 (with Leakage Current Compensation circuit)
Threshold Dispersion vs. dose

1 Mrad per run at HL-LHC! But dose rate here was ~5x higher than at HL-LHC

Column Flavor Dispersion - 88" Irradiation

- Flavor 1
- Flavor 2
- Flavor 3
- Flavor 4
- Flavor 5
- Flavor 6
- Flavor 7
- Flavor 8

Effect from temp increase to 20°C

Retuned at 1 Mrad
Same study vs. Temperature

After chips have been irradiated to high dose

**Column Flavor 8 (LCC) Tuned at +20°C**

- Green: 0 Mrad
- Blue: 150 Mrad
- Red: 350 Mrad

**Column Flavor 8 (LCC) measured at -20°C**

- Green: 0 Mrad
- Blue: 150 Mrad
- Red: 350 Mrad
All flavors in 350Mrad Chip

Dispersion change with Temperature after tuning at +20C

Column Flavor Dispersion 350 Mrad Irradiation

Dispersion [e]

Temperature [C]

Flavor 1
Flavor 2
Flavor 3
Flavor 4
Flavor 5
Flavor 6
Flavor 7
Flavor 8
# All Threshold Stability Results so Far

<table>
<thead>
<tr>
<th>Flavor</th>
<th>Temperature</th>
<th></th>
<th></th>
<th>Irradiation</th>
<th></th>
<th></th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Threshold Shift</td>
<td>Detuning</td>
<td></td>
<td>Threshold Shift</td>
<td>Detuning</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Mrad</td>
<td>150 Mrad</td>
<td>350 Mrad</td>
<td>0 Mrad</td>
<td>150 Mrad</td>
</tr>
<tr>
<td>4&amp;7 (RH + LCC)</td>
<td>e/°C</td>
<td>4.27</td>
<td>6.5</td>
<td>8.8</td>
<td>2.13</td>
<td>3.95</td>
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<tr>
<td>1&amp;5 (No LCC)</td>
<td>e/Mrad</td>
<td>17.9</td>
<td>14.6</td>
<td></td>
<td>7.0</td>
<td>Planned Aug 24 2016</td>
</tr>
<tr>
<td>3 (LCC + PD)</td>
<td></td>
<td>22.5</td>
<td>19.3</td>
<td>Planned Aug 24 2016</td>
<td></td>
<td></td>
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<tr>
<td>2,6,8 (LCC)</td>
<td></td>
<td>22.2</td>
<td>20.9</td>
<td></td>
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</tbody>
</table>
Mini Modules

Chip over Sensor
Superimposed in flip-chip aligner
(red frame around chip)

Am-241 Source scan
Aug. 4, 2016
RD53A: Submission March 2017

- Specs document (public):
Design Work In Full Swing

400x192 matrix

Digital EoC 1
20 mm x 300 µm

Digital EoC 2
6.5 mm x 300 µm

Analog Chip Bottom
7 mm x 300 µm (4 FE × 30 DACs)

Digital EoC 3
6.5 mm x 300 µm
High Bandwidth Serial I/O

- 4x1.28 Gbps
- 5 Gbps

CMD

IN_n
IN_p

CDR/PLL

data_out

tx_clk

Ch_Sync

locked

rx_data_16b

load

clk_40

HIT DATA

JTAG

JTAG_clk

JTAG_si

JTAG_so

Aurora 64/66

Ch #0

Ch #1

Ch #2

Ch #3

4x1.28 Gbps

5 Gbps

Output FIFO

Data Builder

Commands

Conf

Addr

IP Interface

IP Block

PIXEL MATRIX

EoC
Conclusion

- Critical feature of near future pixel detectors is hit rate
- High logic density needed to handle high rate
- 65nm CMOS pixel chip being developed by RD53 (RD53A)
- FE65-P2 demonstrator is a stepping stone to RD53A
  - Excellent bare chip results. Mini-modules are working.
  - (a second demonstrator Chipix65 just submitted this July)
- On track for RD53A submission in March 2017
- Basis for ATLAS and CMS pixel detector readout in HL-LHC
Credits

- **FE65-P2 design**
  - R. Carney#, M. Garcia-Sciveres, D. Gnani, A. Mekkaoui*- LBNL
  - T. Hemperek- Bonn U.

- **FE65-P2 test**
  - D. Allum, K. Dunne, M. Garcia-Sciveres, T. Heim, A. Mekkaoui*, V. Wallangen#- LBNL
  - L. Kashif- U. of Wisconsin
  - C-A. Gottardo, T. Hemperek, H. Krueger, M. Strandke- Bonn U.

- **Mini-modules**
  - KEK, Hamamatsu (mini sensor)
  - A. Tomada, C. Kenney- SLAC (Bump bonding)

- **RD53**
  - Bonn U., CERN, CPPM, Fermilab, FNSPE-CTU / IP-ASCR, INFN Bari, INFN Milano, INFN Padova, INFN Pavia, INFN Perugia, INFN Pisa, INFN Torino, LBNL, LPNHE, NIKHEF, RAL (CFI), U. of Sevilla, U. of New Mexico, U.C.Santa Cruz

* now FNAL    # also Stockholm U.
References

- **RD53A Specifications**
  http://cds.cern.ch/record/2113263

- **Radiation Induced Narrow Channel Effect:**
  http://dx.doi.org/10.1109/TNS.2005.860698

- **Radiation Induced Short Channel Effect:**
  http://dx.doi.org/10.1109/TNS.2015.2492778

-
BACKUP
Noise optimized for low threshold operation. Goal is 500e threshold operation.

Fast shaping needed to avoid in-pixel pileup.
Single Pixel Perspective

**Pixel size**

- For 50um x 50um HL-LHC pixels up to 3Ghz / sq. cm. In ATLAS / CMS
- Need to save these hits FOR ENTIRE TRIGGER LATENCY (12μs up from 6μs)
On-Chip Storage and Trigger

Storage of all individual hits W/ ADC value

On-chip memory

Readout ~5Gbps cable limit

Triggers (selected slice times)
• Change in effective doping is insignificant, because doping levels in CMOS transistors are very high.
• All radiation damage effects to CMOS are due to parasitic electric fields form charge trapped in oxides and oxide-silicon interfaces
• Meet the oxides:
  • Gate oxide
  • Field Oxide
  • Buried Oxide (only for SOI)
  • Shallow trench Isolation (STI)
  • Gate Spacer
STI, Gate, Spacer

- STI (thick)
- Gate oxide (thin)
- Spacer (thick)

Diagram showing the layout of STI, Gate, and Spacer.
Radiation Induced Narrow Channel Effect

Wide Transistor

Narrowest Transistor
Radiation Induced Short Channel Effect

Long Transistor

Shortest Transistor

Regions strongly influenced by the trapped charge
Limited Readout Bandwidth

Can’t use optical transmitters

Can’t use heavy shielded cables

w/o equ. 5Gbps Simulation w/equalization
FE-I4 Digital Region

- Digital block is shared with 4 inputs- each form an identical analog pixel.