38th INTERNATIONAL CONFERENCE
ON HIGH ENERGY PHYSICS
AUGUST 3 - 10, 2016
CHICAGO

Contribution ID: **1597** Type: **Oral Presentation**

Overview of the ATLAS Fast Tracker Project (12' + 3')

Thursday, 4 August 2016 15:45 (15 minutes)

The next LHC runs, with a significant increase in instantaneous luminosity, will provide a big challenge for the trigger and data acquisition systems of all the experiments. An intensive use of the tracking information at the trigger level will be important to keep high efficiency for interesting events despite the increase in multiple collisions per bunch crossing. In order to increase the use of tracks within the High Level Trigger, the ATLAS experiment planned the installation of a hardware processor dedicated to tracking: the Fast TracKer processor. The Fast Tracker is designed to perform full scan track reconstruction of every event accepted by the ATLAS first level hardware trigger. To achieve this goal the system uses a parallel architecture, with algorithms designed to exploit the computing power of custom Associative Memory chips, and modern field programmable gate arrays. The processor will provide computing power to reconstruct tracks with transverse momentum greater than 1 GeV in the whole tracking volume. The tracks will be available at the begin of the trigger selections, allowing to develop new more pileup resilient triggering strategies as well as allow for entirely new ones. The Fast Tracker system will be massive, with about 8000 Associative Memory chips and 2000 field programmable gate arrays, providing full tracking with a rate up to 100 KHz and an average latency below 100 microseconds. The system will begin the commissioning in 2016, with a full barrel coverage reached by the end of the year. The final version of the electronic boards is presented, reporting on the commissioning status as well as the first data-taking experience. An overview of the Fast Tracker processor is presented, reporting the design of the system, the expected performance from simulation studies and the status of the latest hardware prototypes.

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Session Classification: Detector: R&D and Performance

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