The iFDAQ of COMPASS - An intelligent, FPGA-based event builder as an example for the future?

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“Traditional” Event Building

FE data

Buffer PCs

Event Builder PCs

Data Storage Network

Properties of iFDAQ

Built-in intelligence:
• Self Diagnostics
• Data check/FE-error handling
• Redundancy & self-reconfiguration (development) => Continuous data taking

Form factor: μTCA / AMC standard
6U VME carrier card

FPGA: Xilinx Virtex6

Memory: 4GB DDR3 SDRAM

Firmware:
• DHCmx (12:1 multiplexer)
• DHCsw (8x8 switch)
• DHCsb (PCIe spillbuffer)

Interfaces:
• TCS (Trigger Control System)
• 1 Gb Ethernet control network (IPbus)
• 16 serial data links (SLINK)

Throughput: 3 GB/s as DHCsw

Data Handling Card (DHC)

Future Upgrades – ATCA and crosspoint switch

Crosspoint switch: Vitesse – VSC3144-02
• fully programmable
• cross switch control and monitoring
• Hub to AMC modules

FPGA Modules of iFDAQ

Scaling Possibilities & Costs

10 GB/s

100 GB/s

1 TB/s

1 DHCsw

2 layers of DHCsw

4 layers of DHCsw

Scalability of Hardware EB

Software Tools

Run Control GUI

• Control of DAQ configuration through web and C++ GUI
• Multithreaded event processing and error detection
• DAQ status monitoring and system overview

Supported by

Place/Time

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