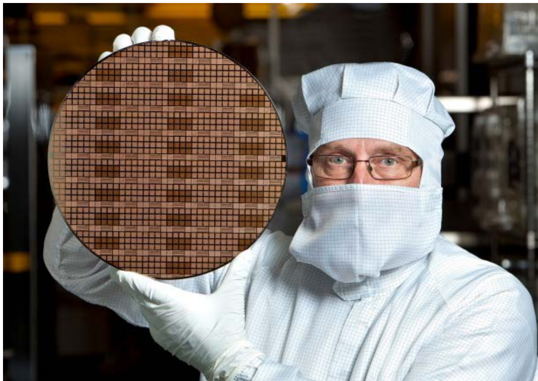
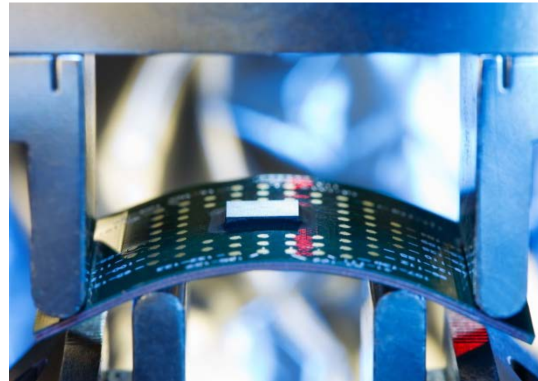
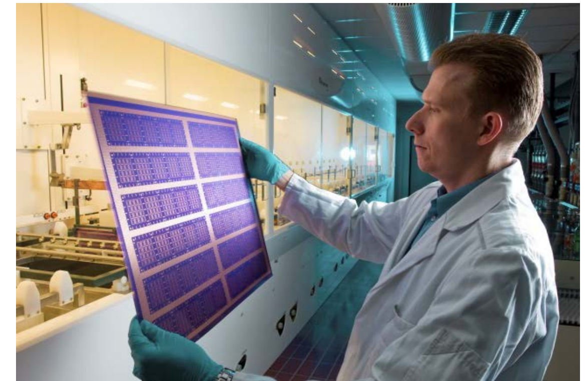
Applied Research in Electronic Packaging for High Energy Physics Experiments

Fraunhofer IZM

Oswin Ehrmann - Thomas Fritzsch







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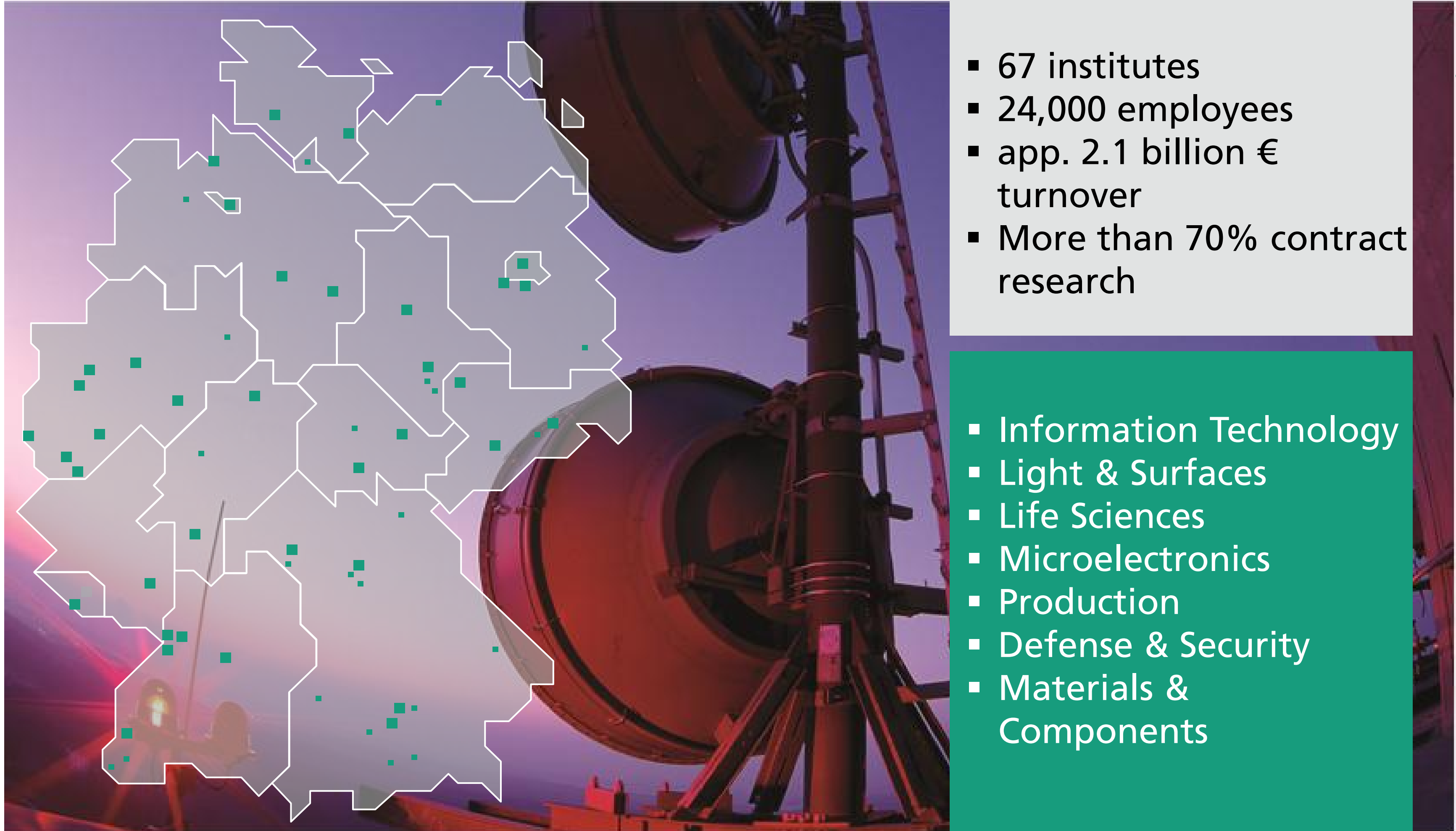
Fraunhofer IZM

Outline

- Introduction to Fraunhofer IZM
- High-density and ultra-fine Pitch Interconnect Formation
- Pixel Detectors for Science and Industry
- Neuromorphic Computing
- 3D Integration

Overview Fraunhofer Gesellschaft



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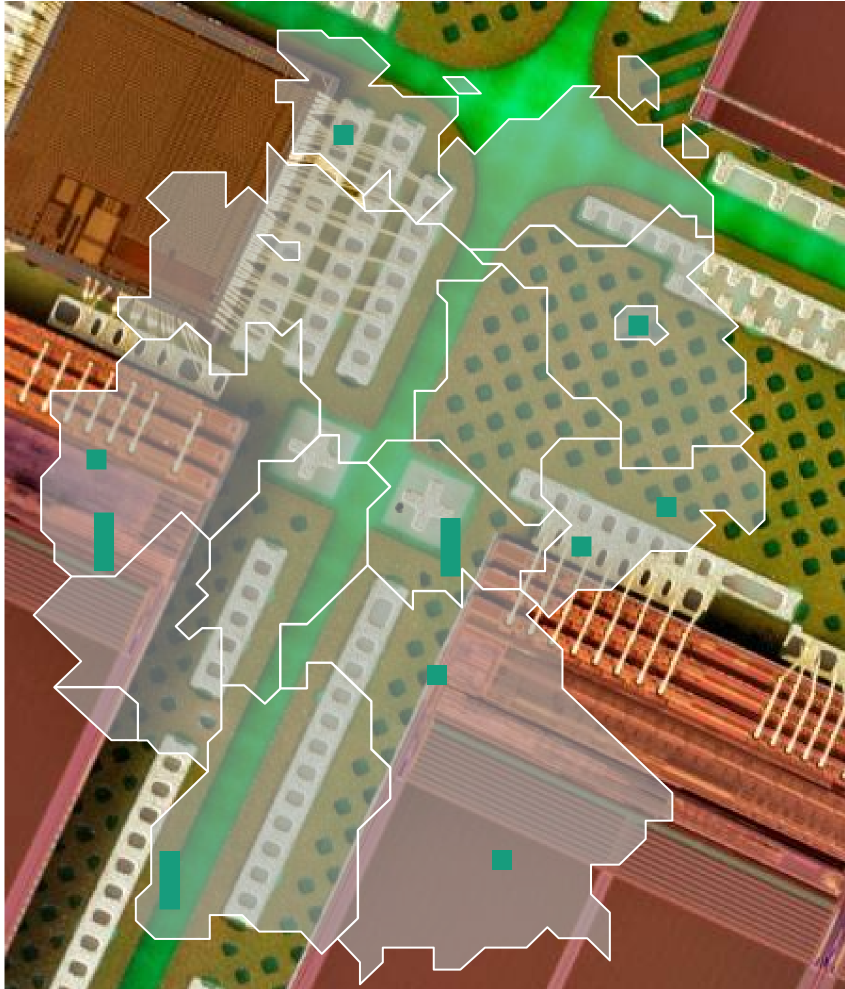
Overview Fraunhofer Group Microelectronics



Organization

- 16 institutes – 3,000 employees – 345 Mio € budget (2015)
  - More than 50% industrial contracts
  - 18% basic funding
  - 32% public projects / other revenues

Competencies:

Systems - Components - Technologies

Business Fields

- Ambient Assisted Living, Health & Well-being
- Energy Efficient Systems
- Mobility & Urbanization
- Smart Living

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Fraunhofer IZM – Facts

Figures 2015

- 28.1 Mio. € turnover
- 82 % contract research
- 356 employees
  (237 full time, 119 PhD, trainee)

Locations

- Berlin
- Dresden
- Oberpfaffenhofen

Director

Prof. K.-D. Lang

University Cooperation

- Long term contract with Technical University of Berlin
- Research Center Microperipheric Technologies
- Approx. 90 additional staff
- Joint use of equipment, facilities and infrastructure

- Material characterization
- Process evaluation
- Reliability testing
- Failure analysis
- Sample production
- Training courses

CORE COMPETENCIES

- Wafer Level Integration Technologies
- Substrate Integration Technologies
- Materials & Reliability
- System Design

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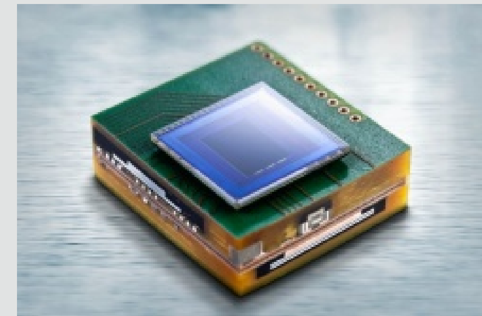
Research Focus

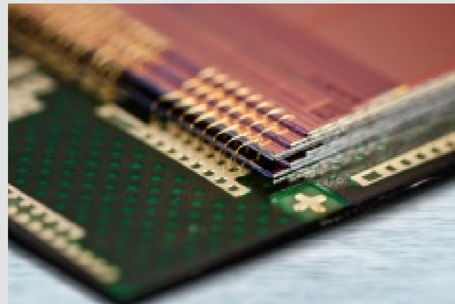
Functionality



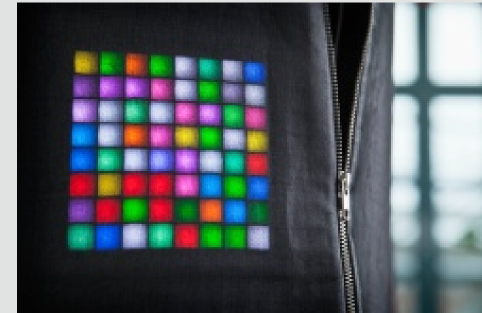
Reliability

Application Trends

Form Factor



Cost



skip trends in application

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How to Work with Fraunhofer IZM

Industrial Contract Research
(e.g. R&D-projects world-wide, feasibility studies, technology & process development)

Services for Industry
(e.g. demonstrators, prototypes, technology service, equipment, personnel)

Technology Transfer
(technologies and processes)

Strategic Alliances
(e.g. packaging manufacturing lines, personnel)

Cooperative Projects
(funded jointly by public & industrial sources, State, EU)

Common Basic Research
(with institutes and universities world-wide)

skip how to work with

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Our Customers and Partners (Selection)

Applications

Equipment Manufacturers // Material Suppliers

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Wafer Level System Integration

Infrastructure

- 2 process lines in Berlin and Dresden (process compatibility across locations)
- High flexibility in processes and wafer size (4“-12“)
- Industry-compatible processing of 300 mm silicon wafers (IZM-ASSID)
  - >95% tool compatibility

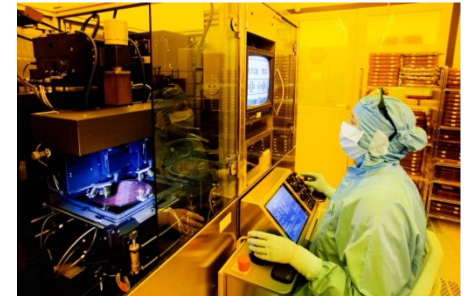
Berlin

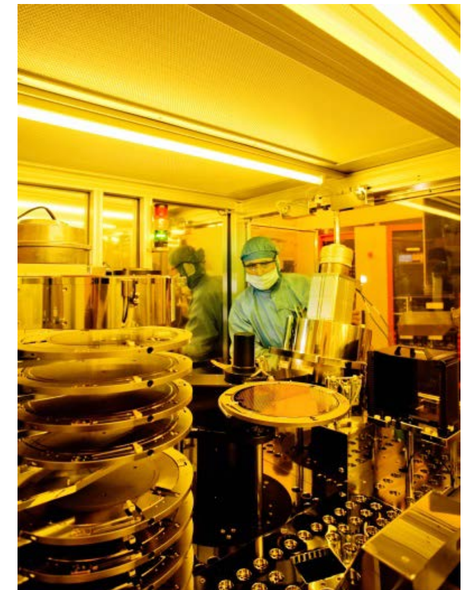
Dresden

Wafer Level System Integration

Process Modules

- Lithography: Coater, Maskaligner, Developer, Spray
  Excimer-Laser-Stepper, Laminator
- Sputtering
- Silicon dry etching
- CVD deposition MOCVD, PETEOS, O3-TEOS
- Galvanic deposition (Cu, Ni, Au, SnAg, AuSn, In)
- Wet-chemical cleaning and etching
- CMP (Cu)
- Temporary Bonding / Debondig, permanent Bonding
- Thinning of single and compound wafers
- Stress relief etching, chip-side wall healing
- TAIKO wafer processing





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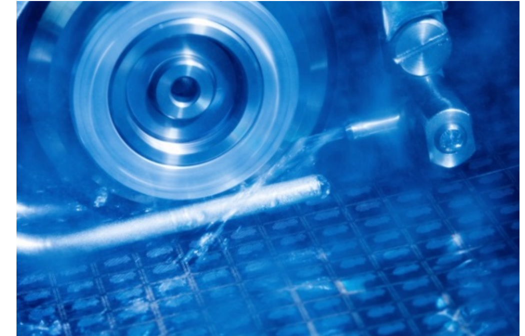
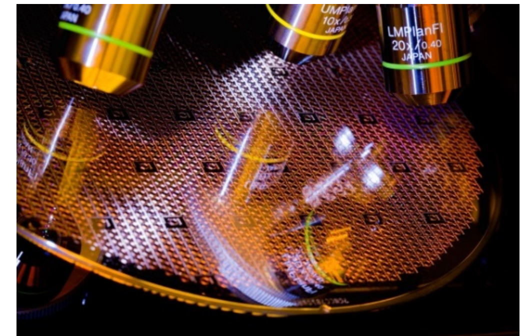
Wafer Level System Integration

Process Modules

- Singulation
- Mechanical blade dicing, laser grooving
- Laser stealth dicing
- Wafer-edge trimming; circle-cut
- Assembly
  - die-to-wafer /interposer assembly

    (Flip Chip soldering, wafer-to-wafer temporary and permanent bonding, thermo-compression and anodic wafer Bonding)
- Metrology and analytics tools
- Optical Inspection (wafer mapping)
- Optical Microscopy, SEM, x-ray
- Topography, TSV depth measurement
- Electrical wafer test (DC, RF)





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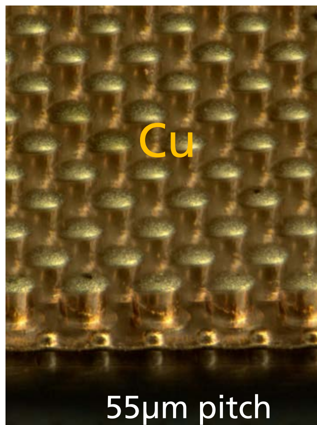
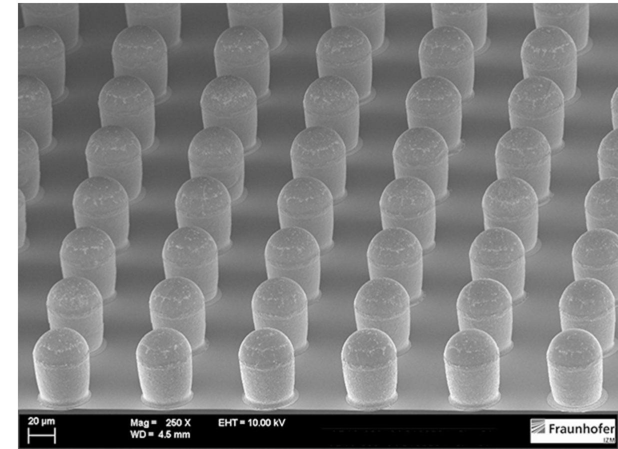
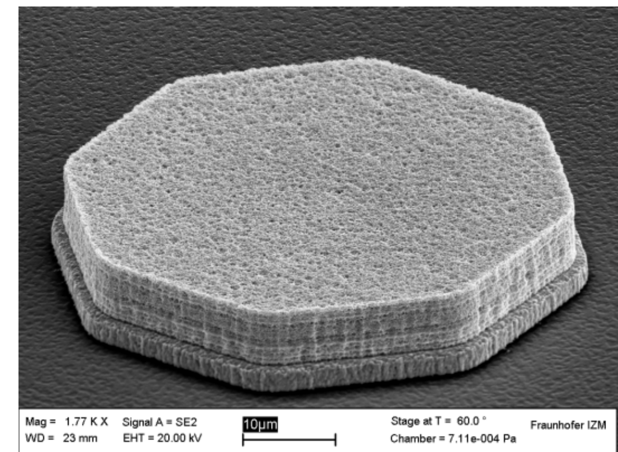
High-Density and Ultra-Fine Pitch Interconnect Formation

- wafer bumping using electroplating
- Broad spectrum of materials and processes (SnAg, CuSn, Cu, In, Sn, Au…)
- Fine pitch arrays – micro bumps
- Pillar-bumps (Cu, Ni)
- Low-temperature and nano interconnect (nano porous gold (Au) sponge)







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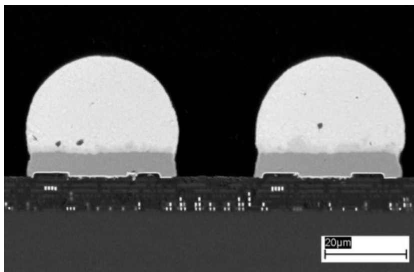
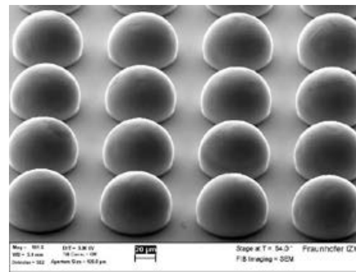
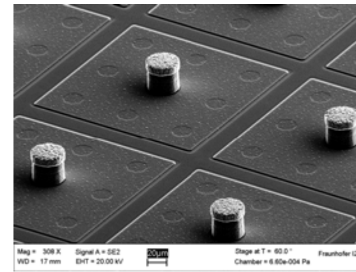
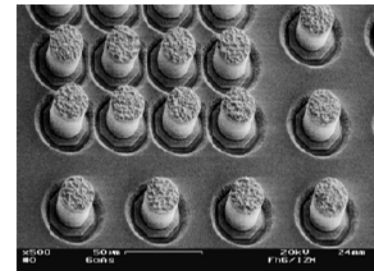
Ultra-Finepitch Bumping for Hybrid Pixel Detectors

SnAg3.5	Indium	Cu-Sn Pillar	Au-Sn
			

- Formation of high-density interconnects by electroplating
- (> 65000 bumps per chip and ultra-fine pitch ≤ 55 µm)
- C2C and C2W assembly with thin and ultra thin Chips (50 –150 µm)
- Main application: hybrid pixel detector multi-chip modules for particle detection and imaging (x-ray, IR)
- Sensor material: Silicon, GaAs, Germanium, Diamond, CdTe

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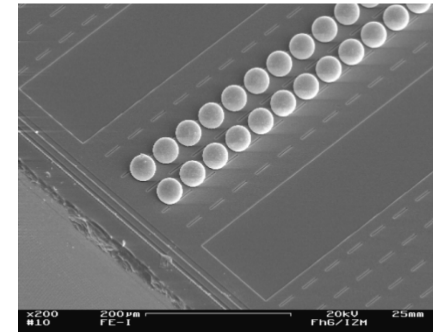
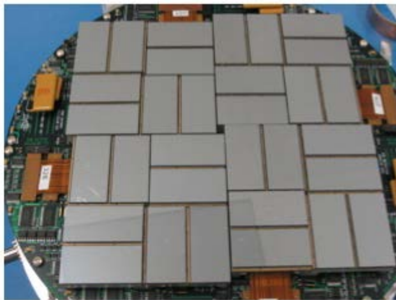
Pixel Detectors for Science and Industry

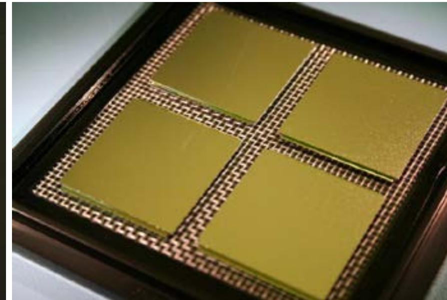
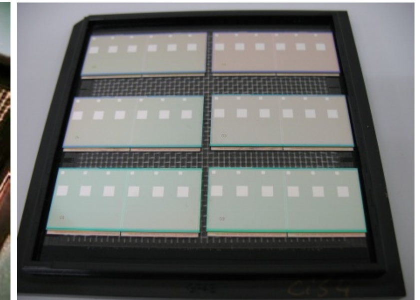
- Fine pitch wafer bumping
- Chip-to-module FC bonding



- TSVs (Via Last)
- Ultra-fine pitch bumping
- Low-temperature bonding

- Silicon
- Diamond
- CdTe



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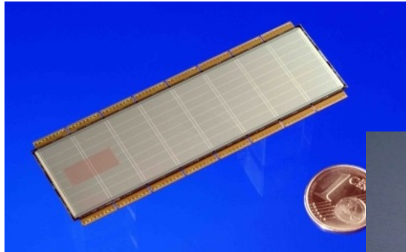
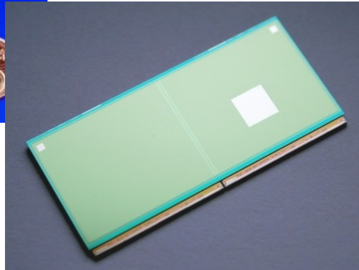
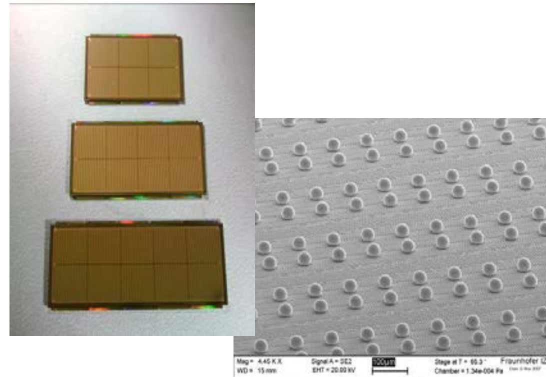
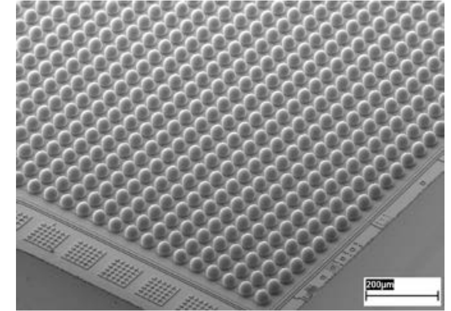
Hybrid Pixel Detector Projects at Fraunhofer IZM

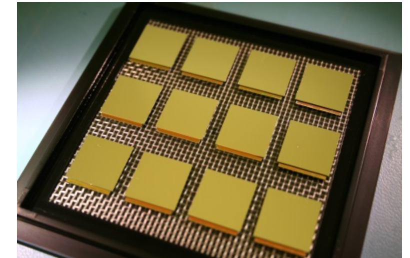



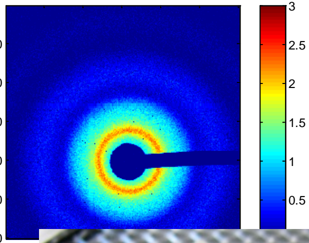
ATLAS FE-I3/FE-I4
Bare Modules
CERN

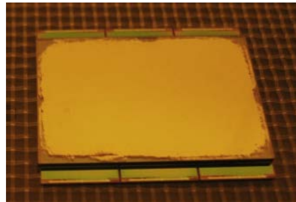


CMS FPIX – Pixel Detector
CERN





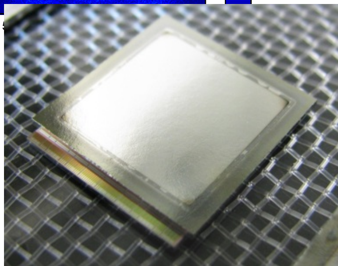




CVD Diamond
Sensor
ATLAS, FERMILAB

X-Ray Detector
SLAC LCLS Stanford

MEDIPIX/TIMEPIX
X-Ray Detector



MEDIPIX Germanium
X-ray Sensor (DESY)

More than 14 years experience in pixel detector hybridization

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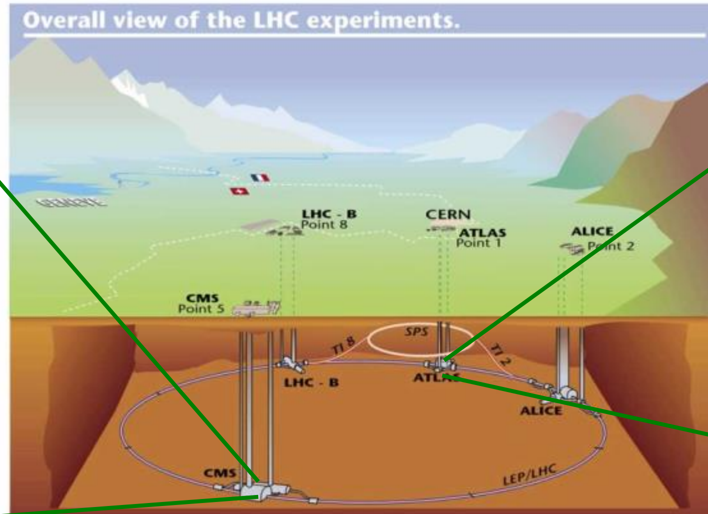
Pixel Detectors for High Energy Physics

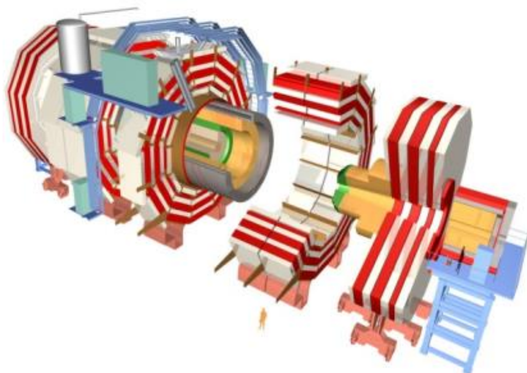
Large Hadron Collider (LHC) at CERN, Geneva, Switzerland

CMS Detector

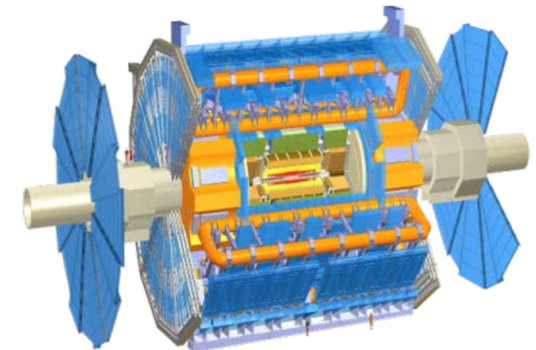


© CERN

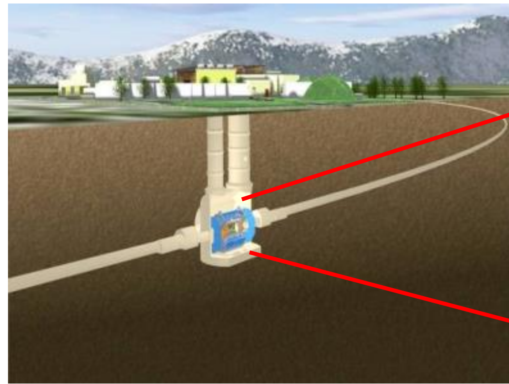
ATLAS Detector

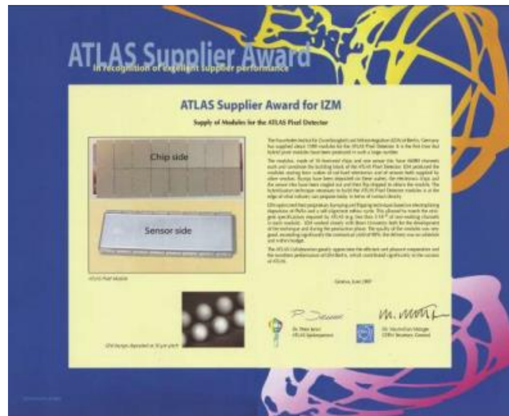


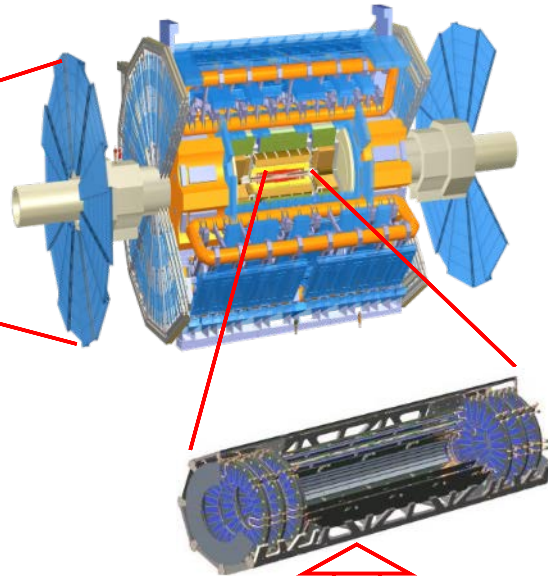
- Silicon pixel tracking detectors are the innermost part of the detector
- Consist of
  - 1744 modules (ATLAS before upgrade)
  - 1888 modules (CMS after upgrade)

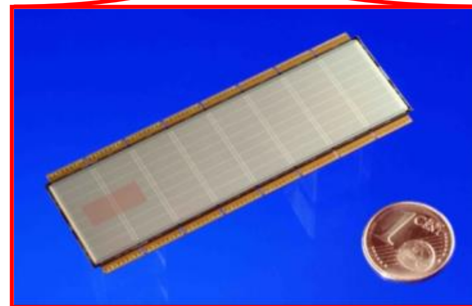


Silicon Pixel Detector Modules for the ATLAS Tracking Detector



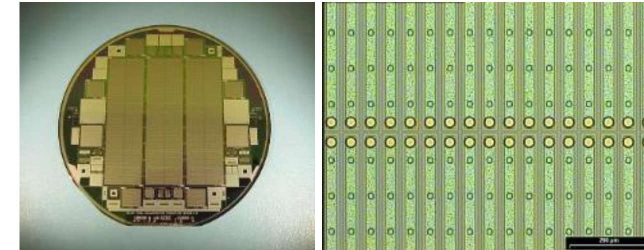






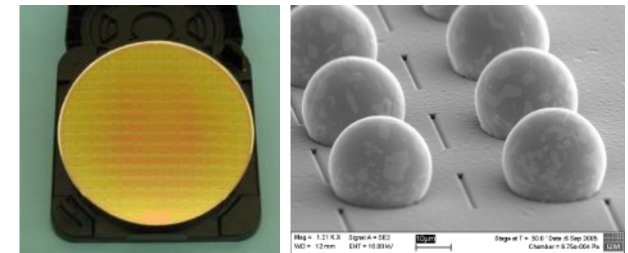
Process steps at IZM:

1. UBM Processing of Sensorwafer



520 processed 4“ Sensor Pixel Wafer

2. Bumping of the FE-I Chipwafer



98 SnPb bumped 8“ Si-Wafer

3. Module Assembly

1150 assembled bare modules

Production Phase 2003-2007:

- **1150 ATLAS Bare Modules assembled at Fraunhofer IZM**
- **Assembled FE-I3 Chips: ~ 18600 chips**
- **Total Module Yield: 97 %**

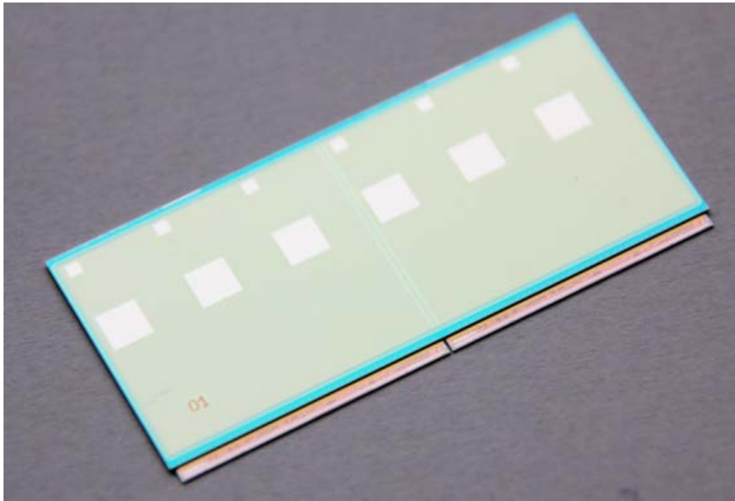
Pixel Detector Modules assembled at Fraunhofer IZM

- **Thin-Film-Multichipmodul**
- **Size 22 x 64 mm²**
- **Silicon Sensor + 16 Readout ICs**
- **46144 IO-Bumps, pitch 50 µm**

Fraunhofer IZM

CERN ATLAS - IBL Detector Upgrade

ATLAS FE-I4B Modules for ATLAS Insertable B-Layer (IBL)



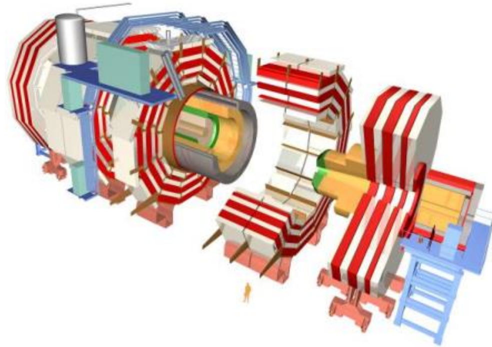
ATLAS FE-I4B double chip modul

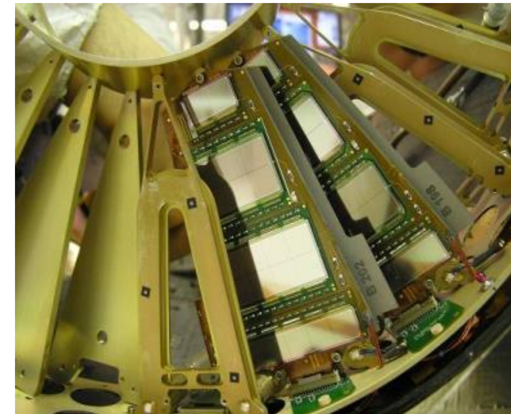
ATLAS IBL insertion (courtesy of Heinz Pernegger/CERN)

- Chip size 2x2cm², Module size 4x2cm² (Double-Module)
- 150µm thin chip assembly using glass carrier technology

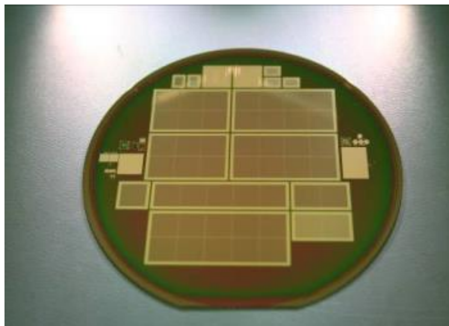
Assembly of 168 double and 112 single chip modules for ATLAS IBL (2012-2014)

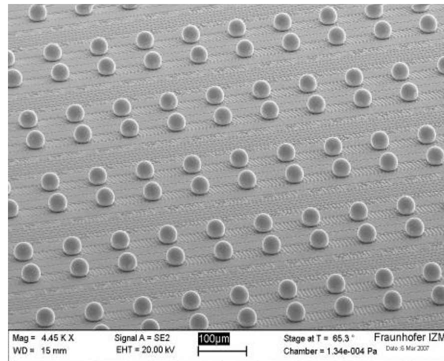
Silicon Pixel Detector Modules for the CMS Detector





CMS silicon pixel detector endcap segments with modules manufactured at Fraunhofer IZM





CMS ROC bumped at Fraunhofer IZM

CMS pixel detector 4" wafer and endcap bare modules after flip chip assembly at Fraunhofer IZM

More than 530 modules have been manufactured during production phase from 2006 to 2008

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CMS

Fermilab

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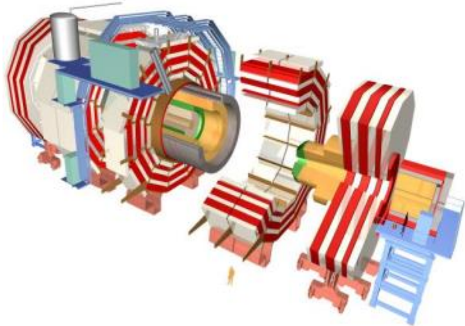
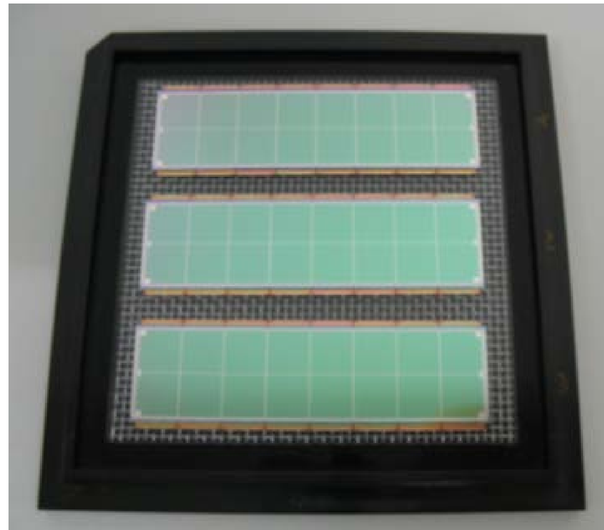
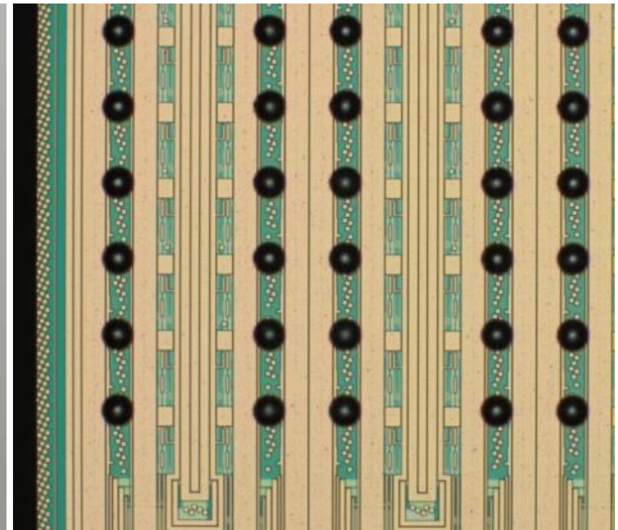
Silicon Pixel Detector Modules for the CMS Detector - Upgrade





8x2 chip modules for CMS barrel pixel detector



PSI46dig Readout chip with solder bumps

CMS silicon pixel detector upgrade phase for the new 4 barrel layer detector

Fraunhofer IZM processed modules for the 3rd layer:

- SnAg Bumping of 26 PSI46dig ROC wafers (6448 ROCs total)
- UBM deposition on 130 sensor wafers
- **More than 300 modules have been assembled from 2015-2016**

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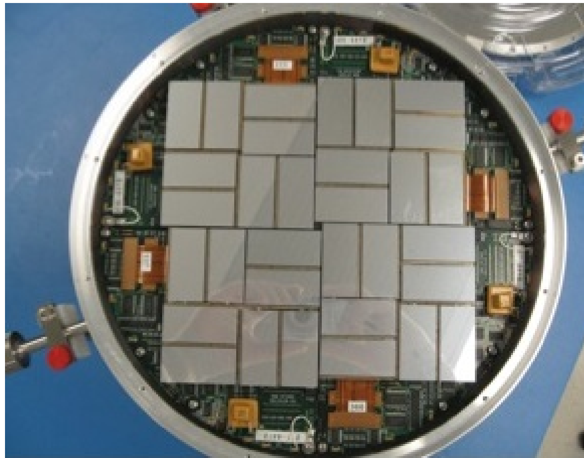
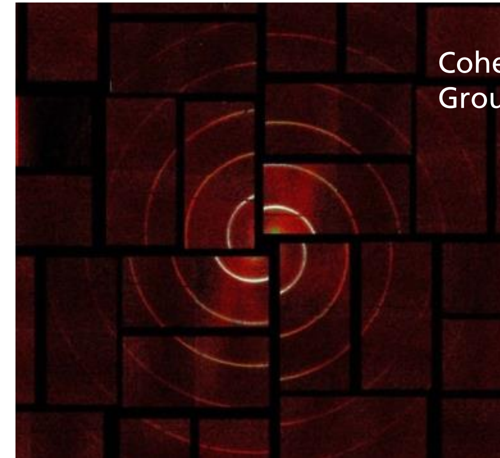
Pixel-Detectors for X-ray Diffraction in Synchrotron Light Sources

- **Hybrid pixel detectors used in x-ray cameras for diffraction analyses of different materials (i.e. protein crystals)**
- **More efficiency than scintillator based detectors**
- **Used in Synchrotron- und free electron laser (XFEL, PETRA, SLAC-LCLS, …)**





X-ray camera at SLAC LCLS

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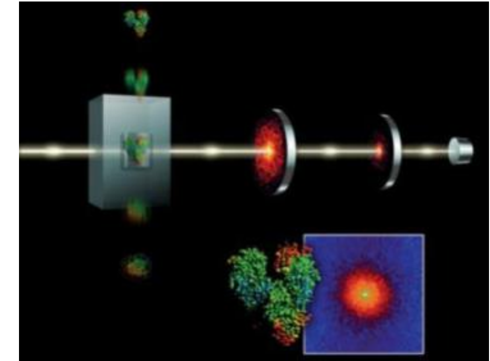
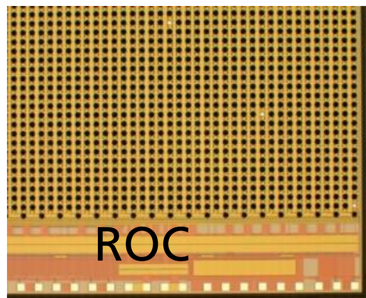
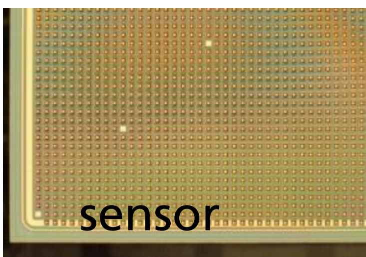
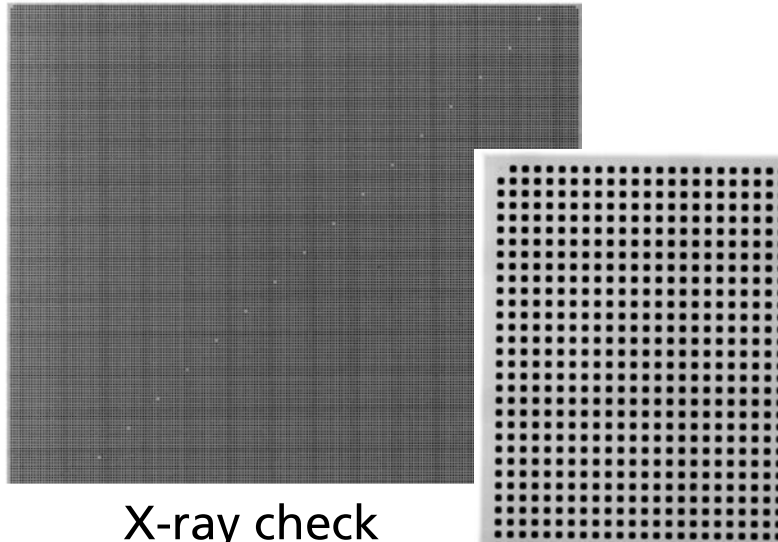
X-ray Pixel Detector Modules for SLACs Linac Coherent Light Source (LCLS)

- ROC: 21,4 x 21,4 mm²
- Sensor: double chip module 43,3 x 20,6 mm²
- Design parameter: 100µm pitch / 60µm bump diameter,
- double pixel matrix 185 x 194 each (~ 72,000 bump interconnections per module)

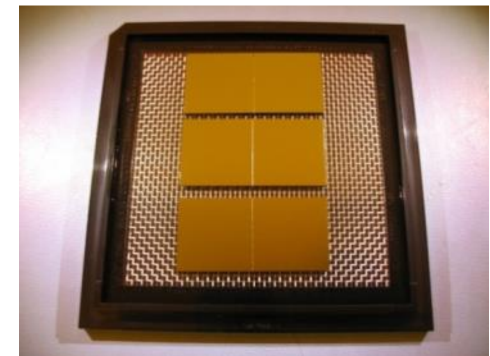








X-ray check after flip chip



Double chip modules ready for shipment

More than 410 modules assembled from 2010 to 2016

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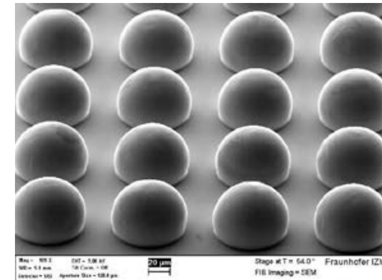
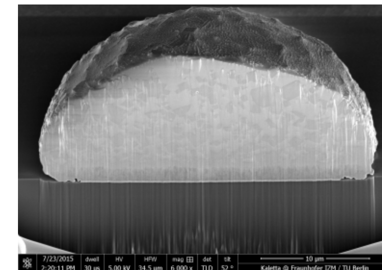
Indium and Indium/Tin for Low Temperature Flip-Chip Interconnections

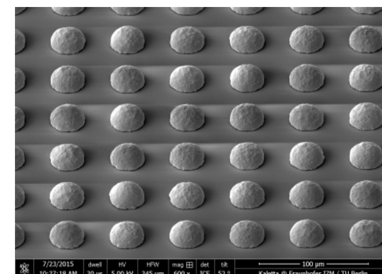
Development of a wafer-level electroplating bumping technique for low-melting Indium solder

- T_M(Indium) = 156 °C; T_M(In52Sn48) = 117 °C for thermally sensitive bonding processes
- Electrochemical deposition of Indium or Indium/Tin
- Flip chip bonding process In to In or In to Au pad surface



Indium bump matrix


Indium-tin bump FIB cut


Indium-tin bump matrix

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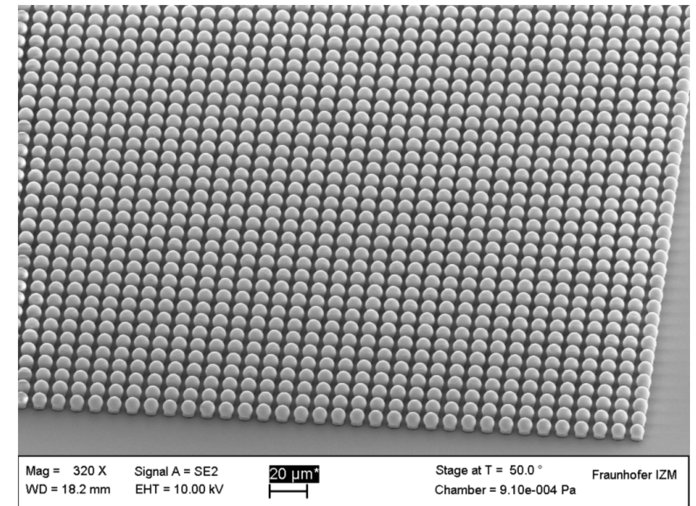
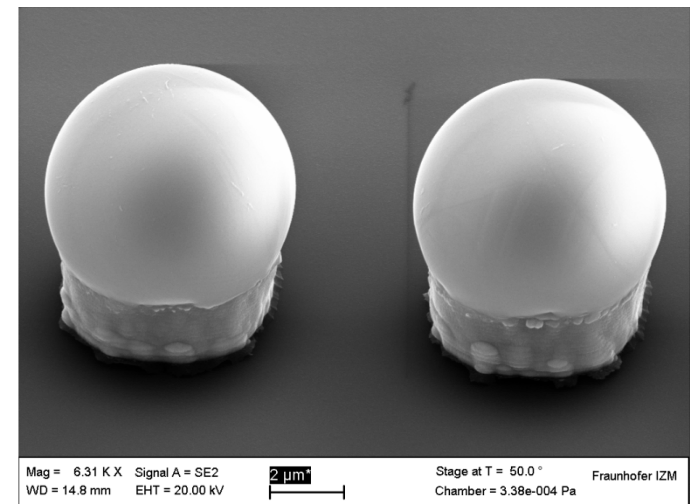
Ultra High Density Fine Pitch Bumping

- Reduction of bump pitch below 50µm
- Adaption of design rules to ultra fine pitch process
- New process development based on Indium bumping by electroplating
- Will be transfered to SnAg bumping and CuSn Pillar bumping

- SEM Images: Indium bumps with 6µm bump diameter in a 10µm bump pitch in X- and Y-direction





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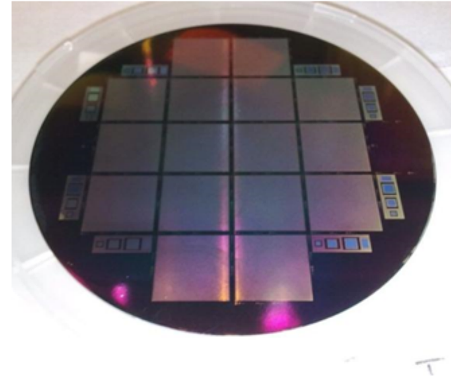
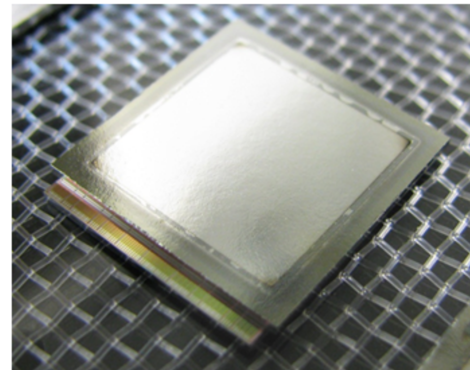
IZM

Germanium X-ray detector using Indium bumping

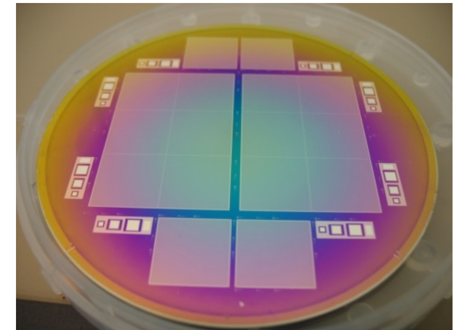
Pixelated Ge detector production

- Sensors produced by Canberra France, based on existing strip technology
- 2 high purity Ge wafers produced
  - 16 Medipix3 singles per 90mm wafer
  - 55µm pixel size, 256 x 256 pixels
  - ~700um thick
  - Electron readout
- Indium bump bonding at Fraunhofer IZM (Berlin)
  - Low-temperature process necessary to avoid damage to Ge
  - Ductility of indium prevents cracking of bonds during cooling





2015: Ge Sensor HEXA Module



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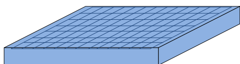
Headlamp Prototypes based on micro-integrated LED arrays

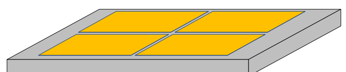
High-resolution ADB (Adaptive Driving Beam) functionality for main light functions without a necessity of any mechanical actuators

OSRAM



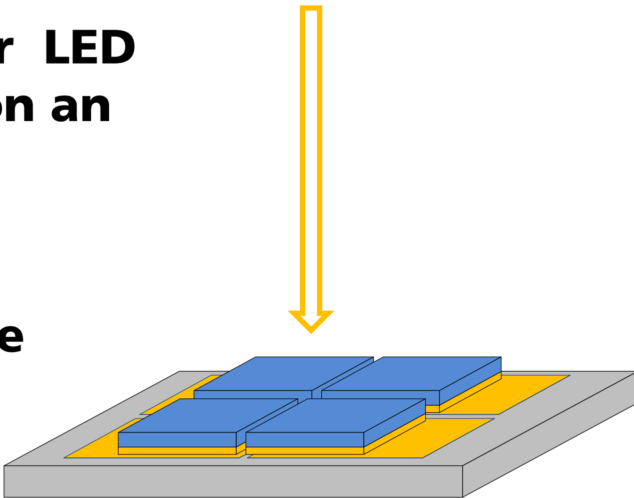
IZM

infineon



Assembly technology for LED pixelated light sources on an intelligent Si-Substrate

Gold Tin Solder
nano porous gold sponge



First picture produced by a 256-Pixel-Chips

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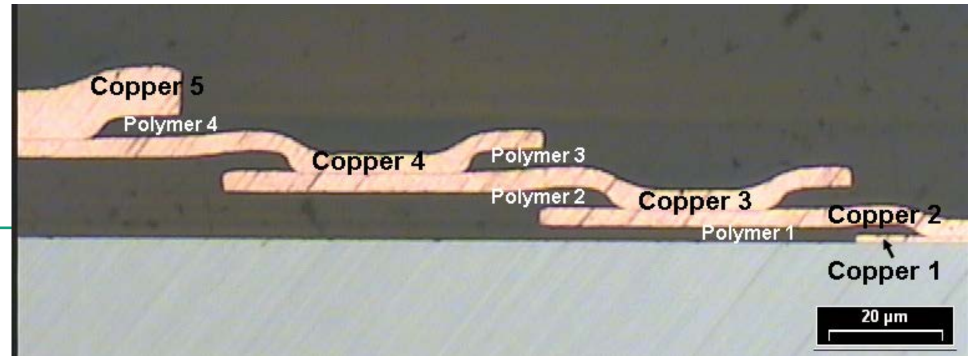
Multilayer



Metal Layer:

- Copper or Gold (sputtered and electroplated thick layers)

Dielectric Layers by Polymers (photo definable)

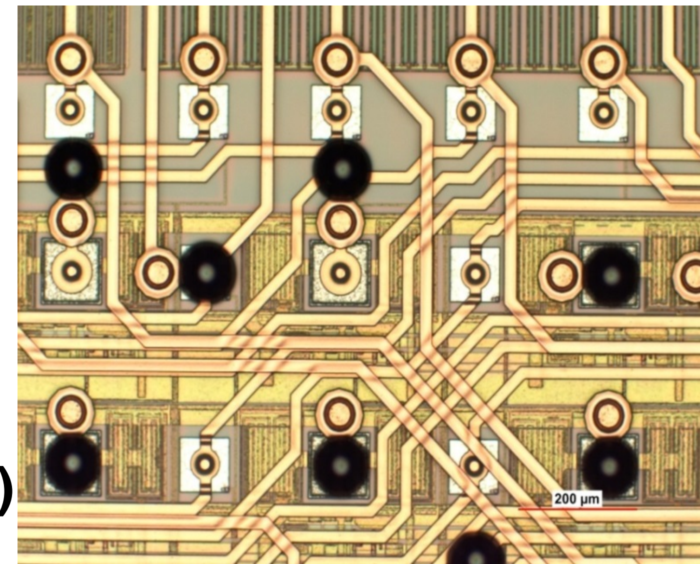
- BCB
- Polyimide
- PBOs

Applications:

- Dielectric Layers for Multilayer
- Passivation
- Wafer Bonding
- Frames for Mounting of Lids (C2C, W2W)

Processing:

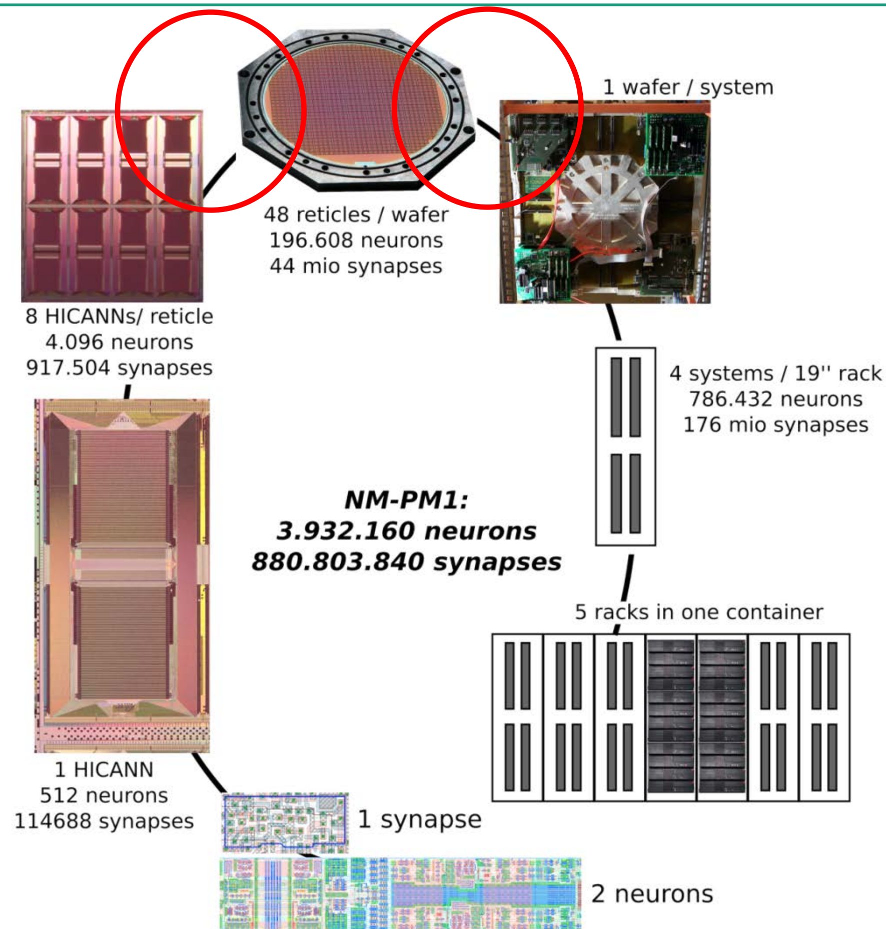
Spin on - Laminated Resist -- Spray Coating



Redistribution

Human Brain Project - EU Flagship

- Neuromorphic Computing Platform



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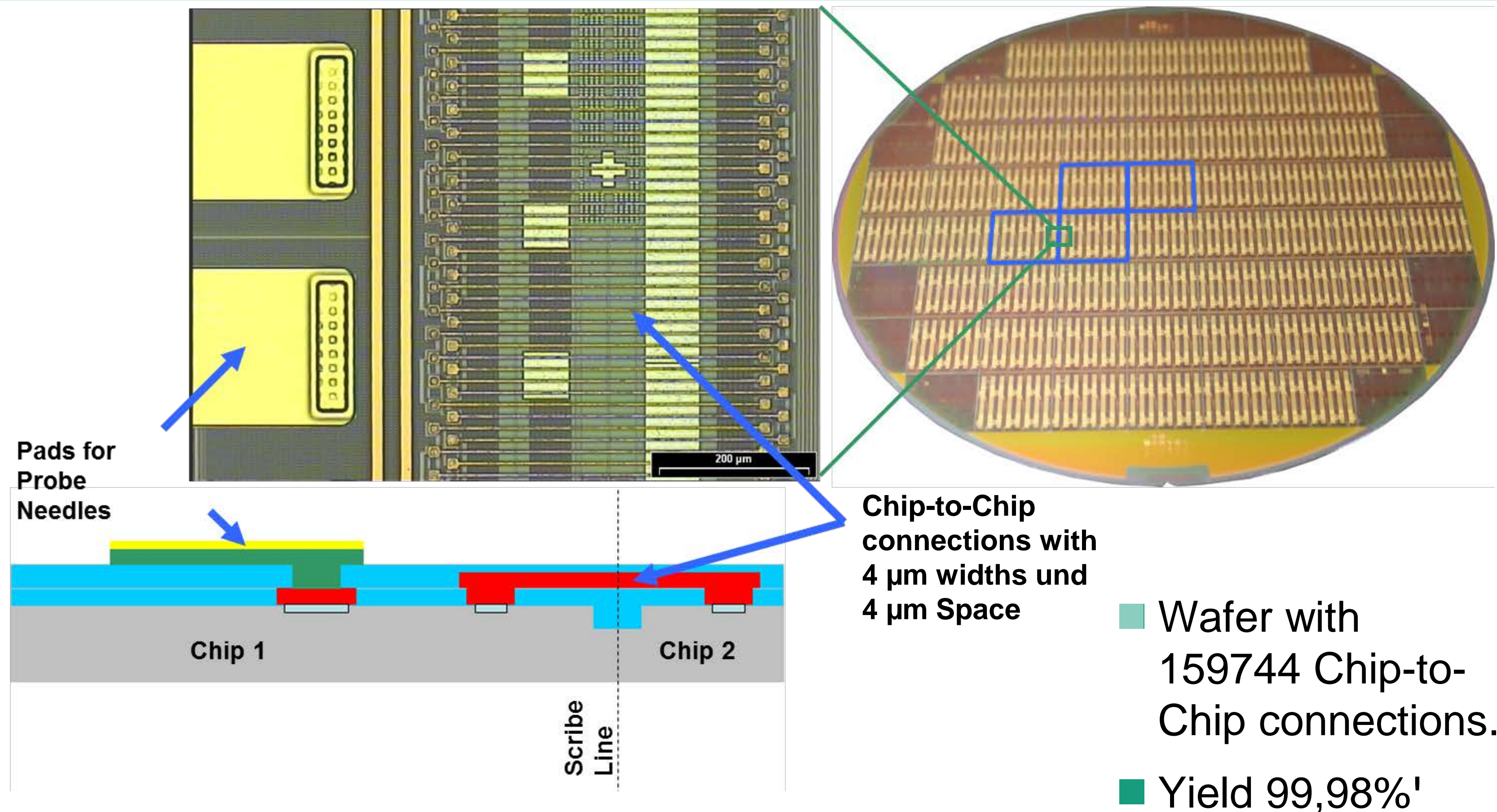
Human Brain Project - EU Flagship

Fabrication of Neuronal Networks based on Wafer-Scale Technology



- Wafer with 159744 Chip-to-Chip connections.
- Yield 99,98%'

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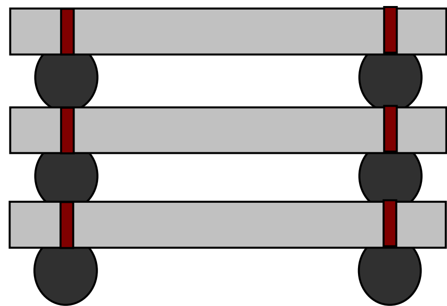
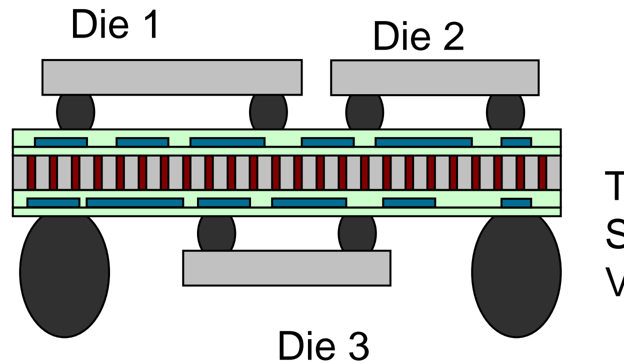
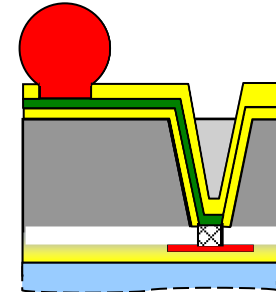
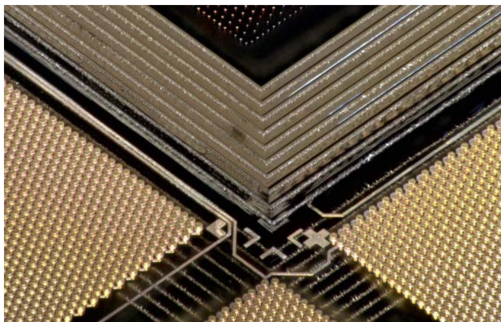
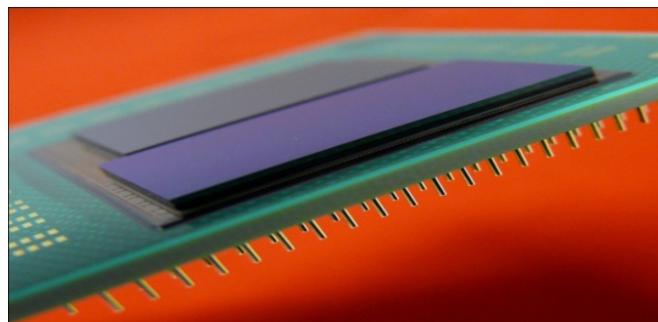
3D Integration – Through Silicon Vias (TSVs)

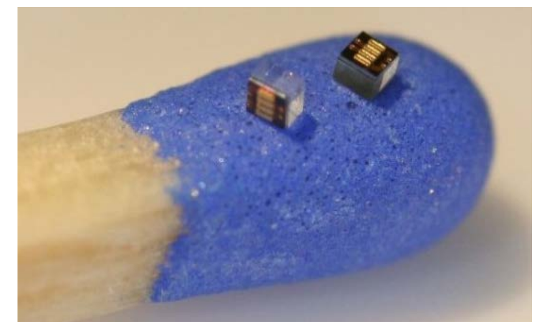







Stacked Chips


Interposer


Sensors

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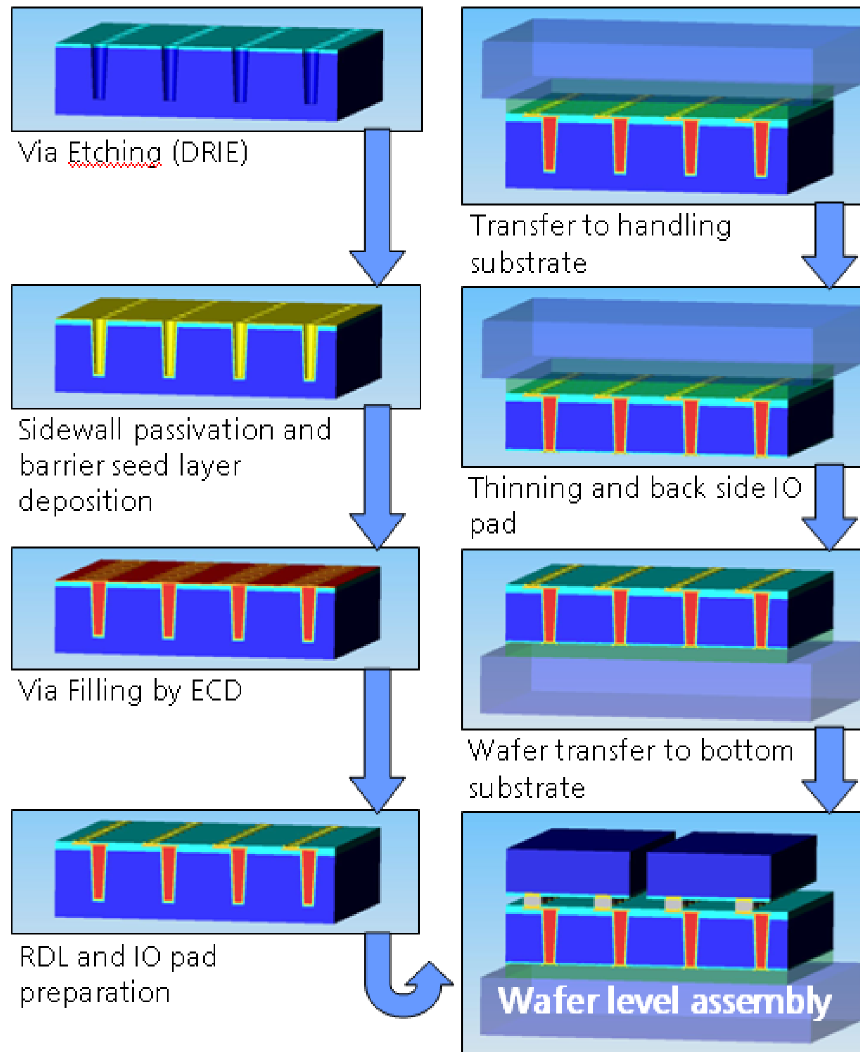
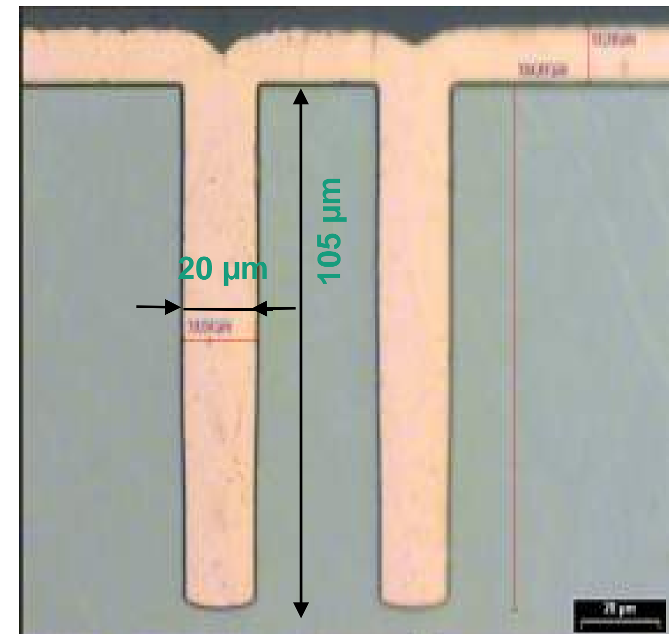
3D Integration using Through Silicon Vias (TSVs) for High Density Interconnects in Stacked Devices



Post Front-End TSV Process Flow

Silicon interposer serves as example



Silicon via: Ø 20µm, depth: 105µm

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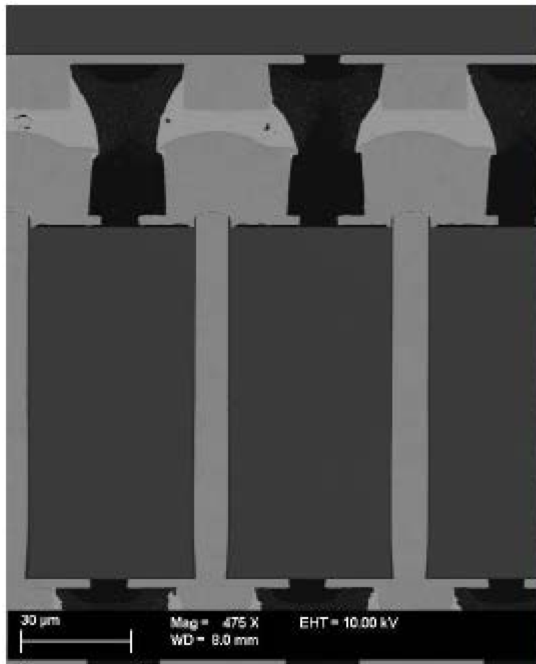
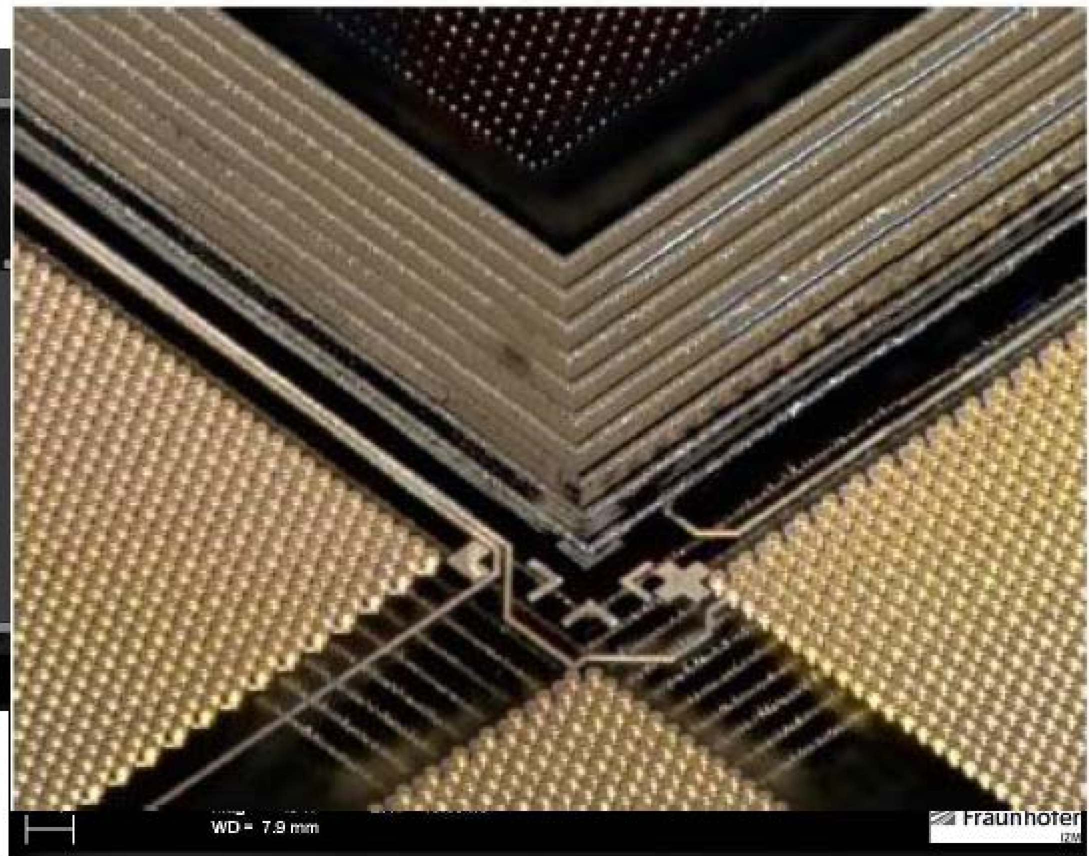
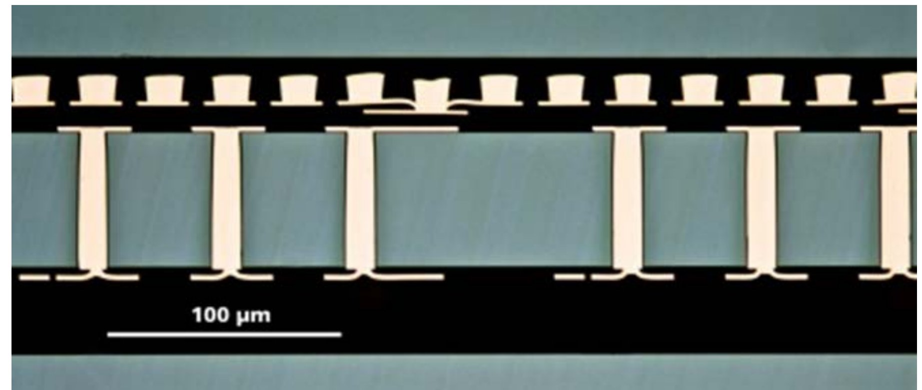
WL-Assembly 3D Chip Stack (10x) with Cu-TSV

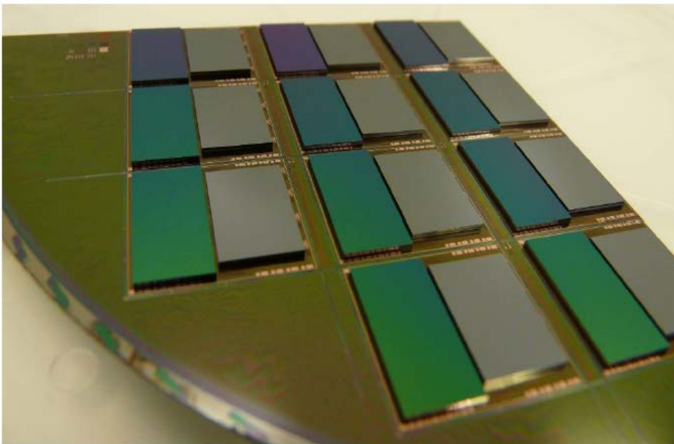




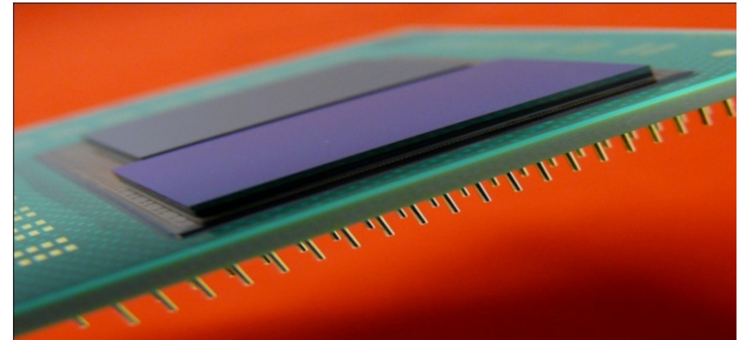
Silicon Interposer

- Cross section of 4-layer FS-RDL, TSV, 1-layer BS-RDL as well as µ-contacts





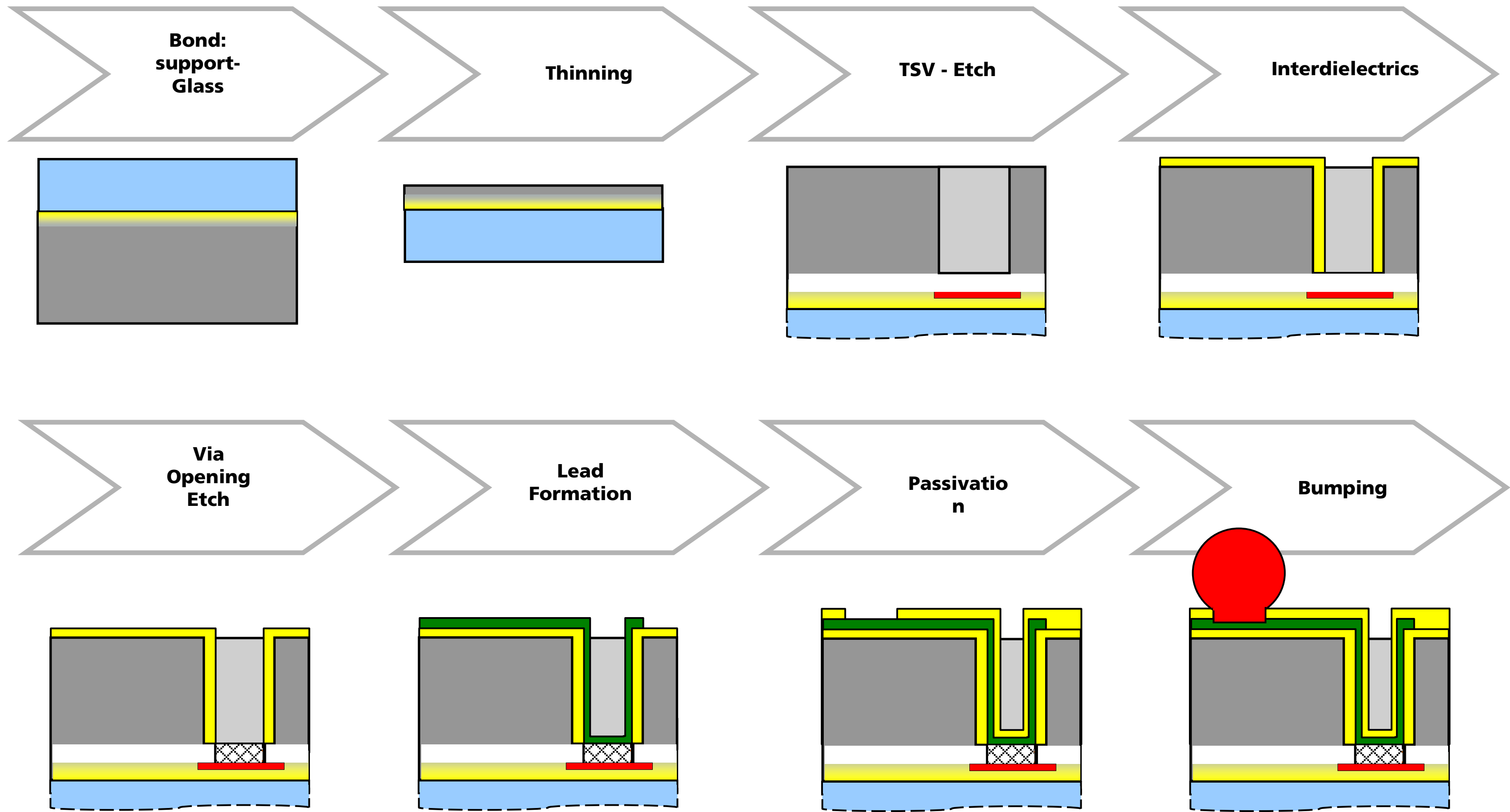
Silicon Interposer with assembled Dies



Silicon Interposer assembled on Substrate

Back side Interconnect

Main process flow



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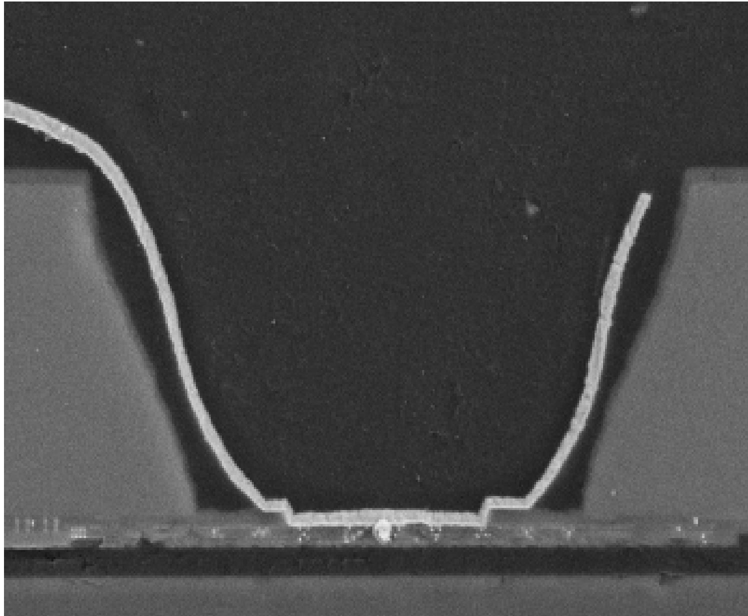
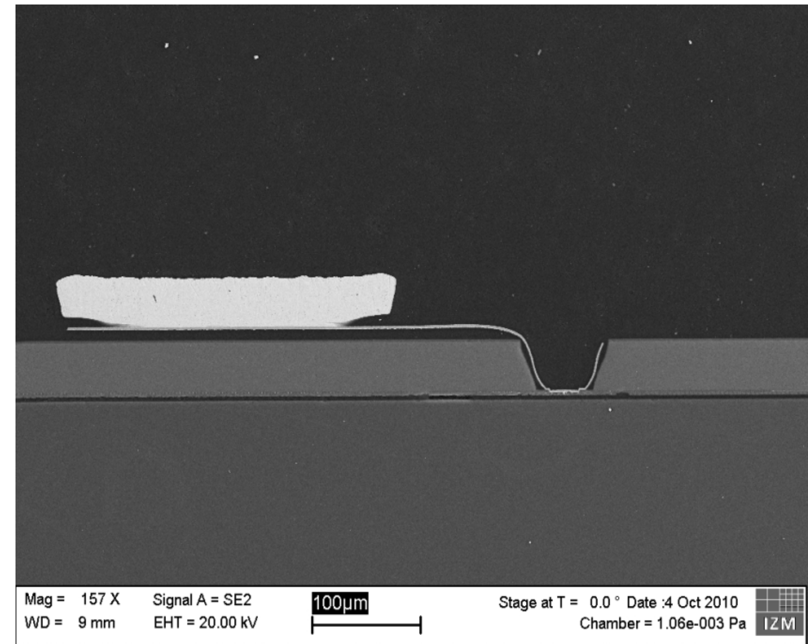
Back side Interconnect





Crosscut of chip with TSV and Au-Bump

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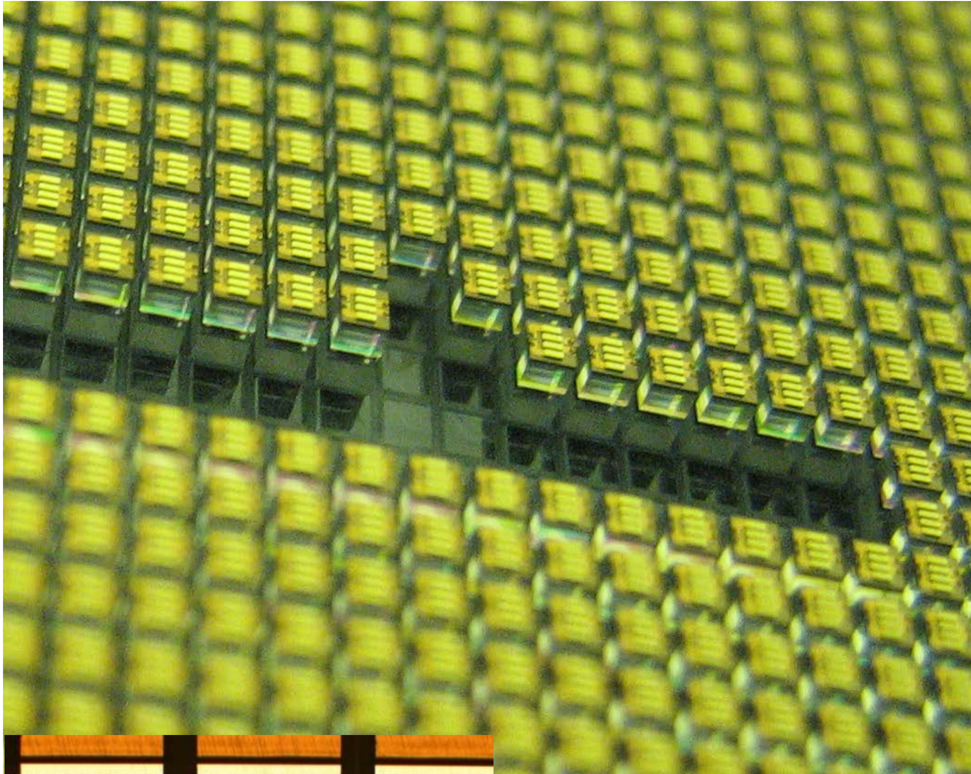
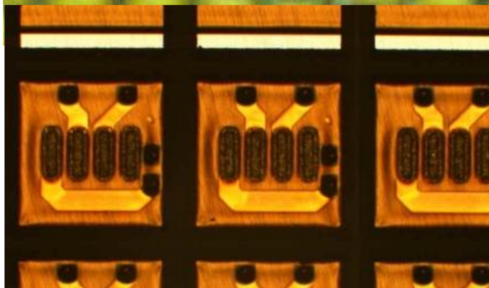
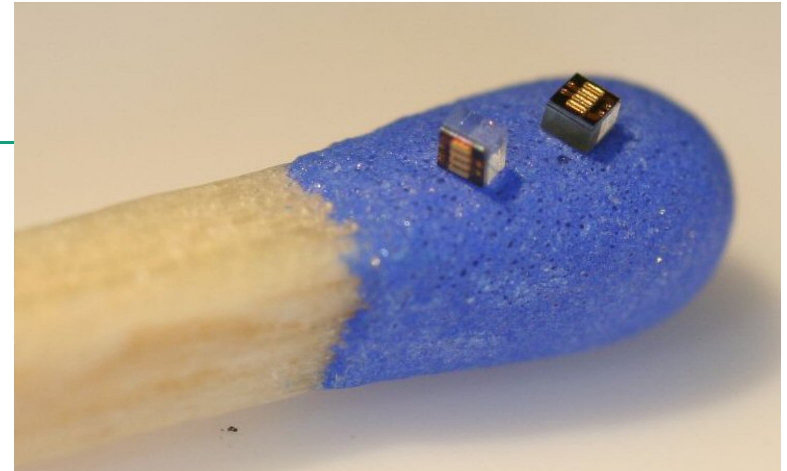
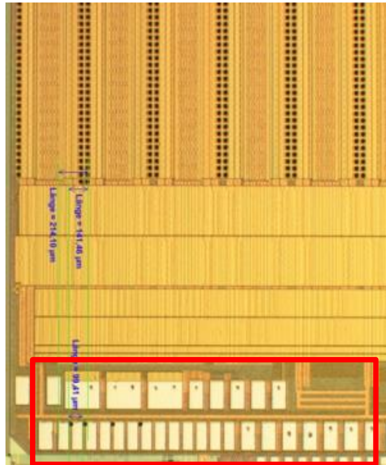
Wafer-Level-Cameras



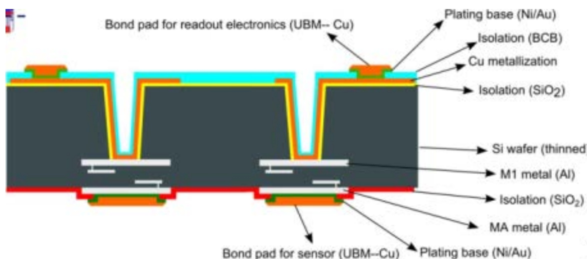




ATLAS FE-I4 TSV Development

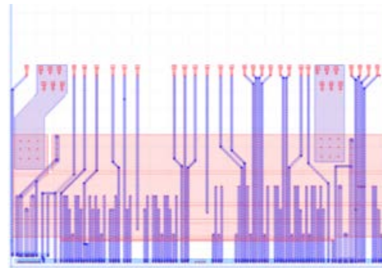


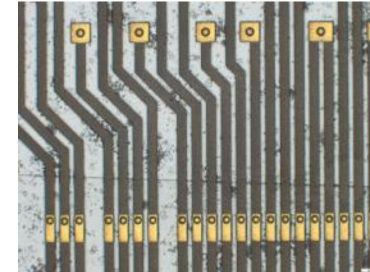
Wire bond pad area for TSV contact from backside

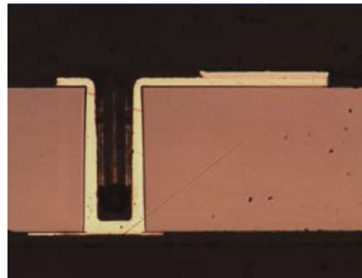


TSV schematical cross section

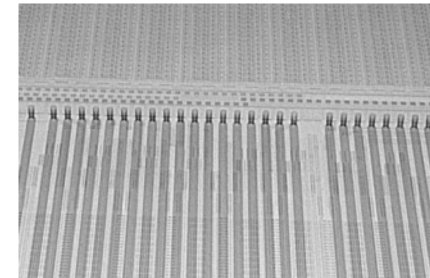
Design of RDL and pad metallisation:







liner-filled TSV (not ATLAS)



ATLAS FE-I4B with Cu-filled TSV (x-ray)

Process steps:

- TSV formation in readout chip wafer
- UBM and RDL
- Bumping of sensor wafer
- Module hybridization
- 2nd level assembly at Bonn University

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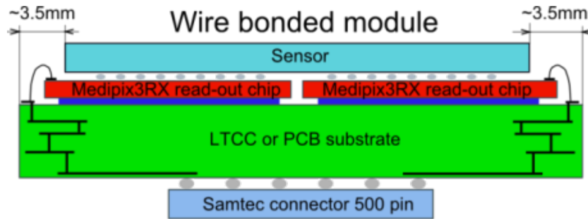
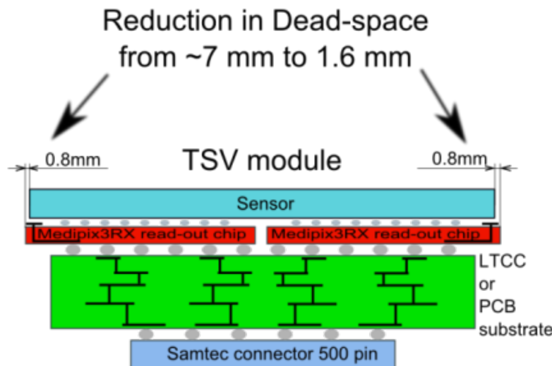
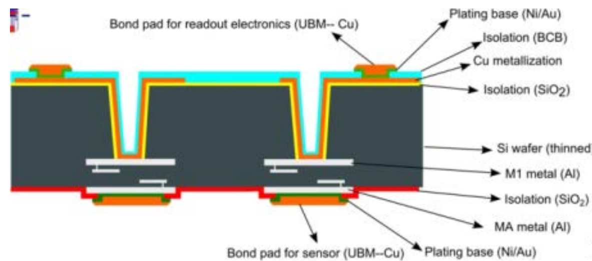
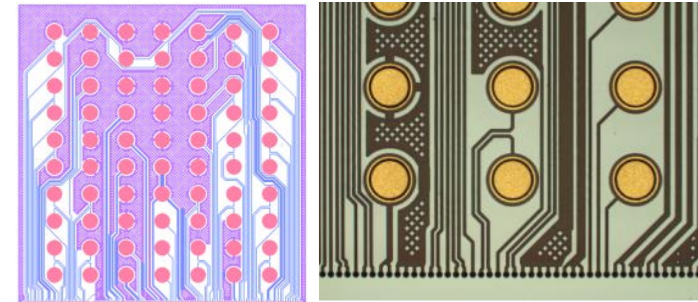
MEDIPIX3 TSV Development

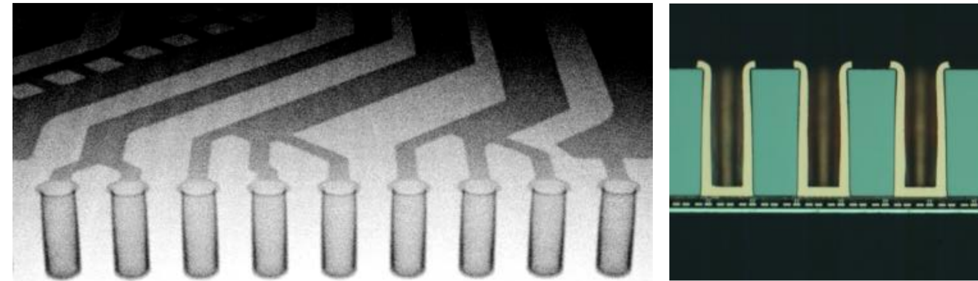








RDL lines and pad metallisation



Cu-filled TSV (x-ray left, cross cut right)

Process steps:

- TSV formation in readout chip wafer
- UBM and RDL
- Bumping of sensor wafer
- Module hybridization
- 2nd level assembly of LTCC/PCB substrate

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Thank You for Your Attention.

Oswin Ehrmann
Head of Department
Wafer Level System Integration

Fraunhofer Institut Zuverlässigkeit und Mikrointegration (IZM)

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