PAUL SCHERRER INSTITUT

PSI

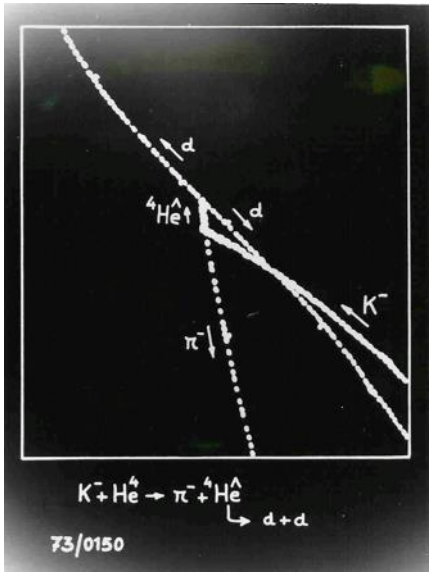
IEEE NPSS
NUCLEAR & PLASMA SCIENCES SOCIETY

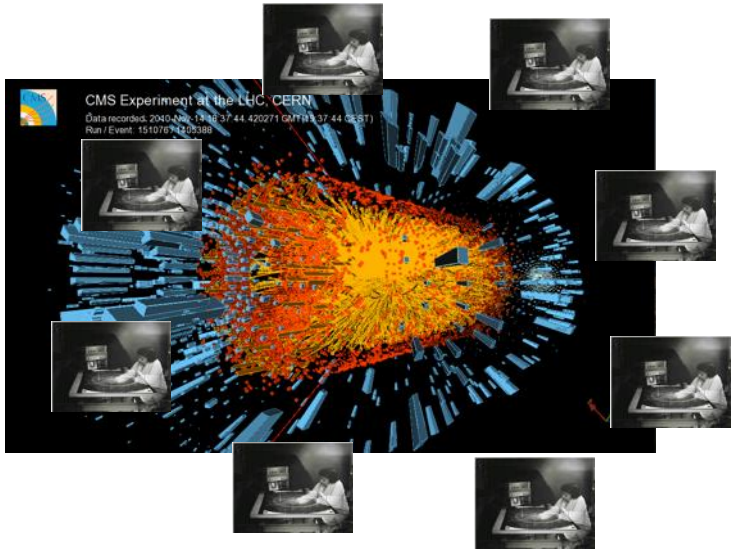
**Paul Scherrer Institute, Switzerland**
**IEEE NPSS distinguished lecturer**

Stefan Ritt

# Waveform Digitizing and Signal Processing

# "Manual" DAQ



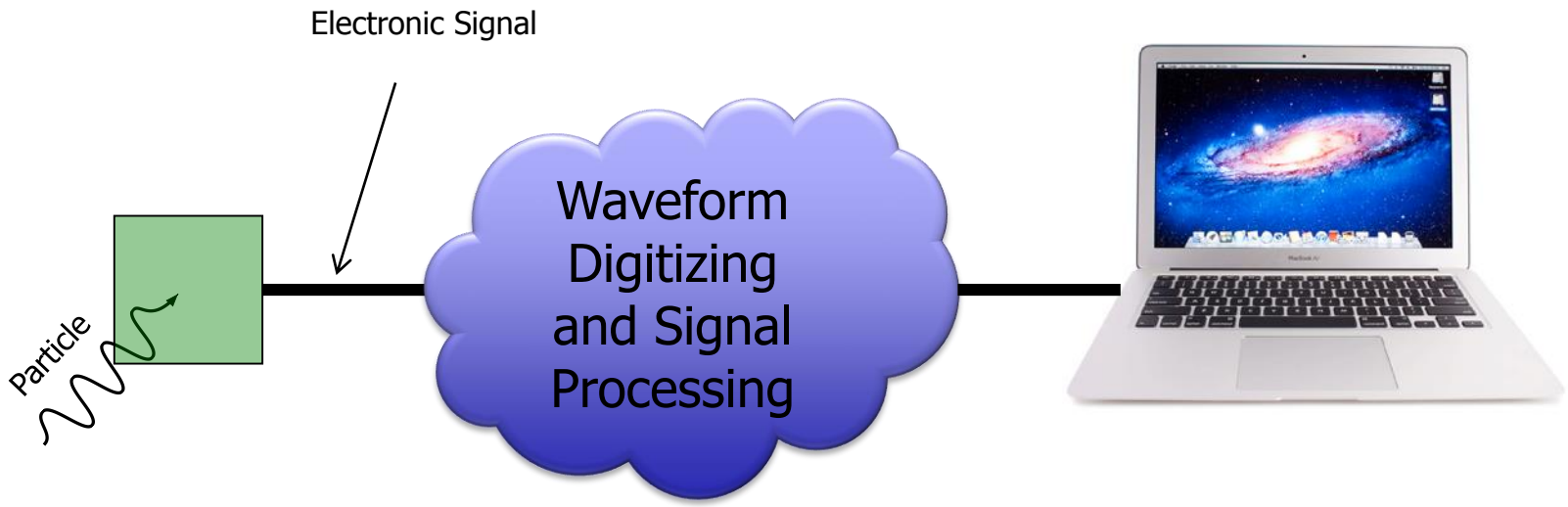




1000 tracks per 25 ns
A4 paper @ 5 g
Truck load @ 40 t

How much paper per second?

200'000 t
5000 Trucks !!!

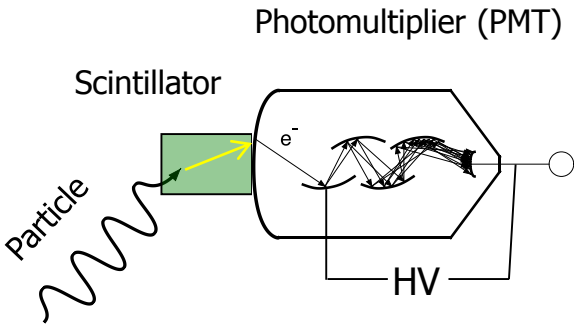
# Electronic Signal Acquisition

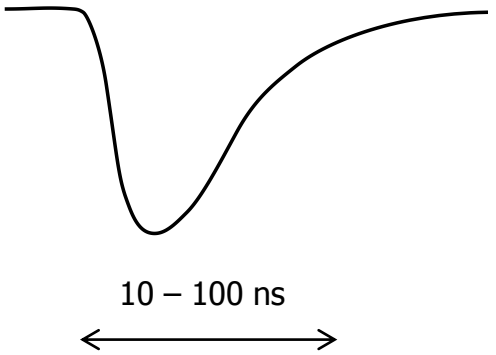



- ADC & TDC technologies
- Signal shaping
- Ultra-fast digitizing (>1 GSPS)
- Digital pulse processing
- Applications

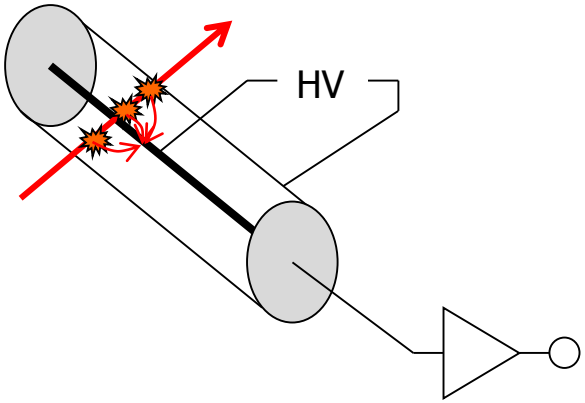
# Signals in particle physics

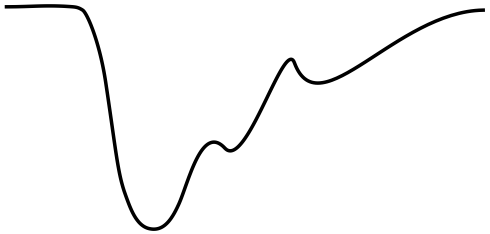
Scintillators (Plastic, Crystals, Noble Liquids, …)



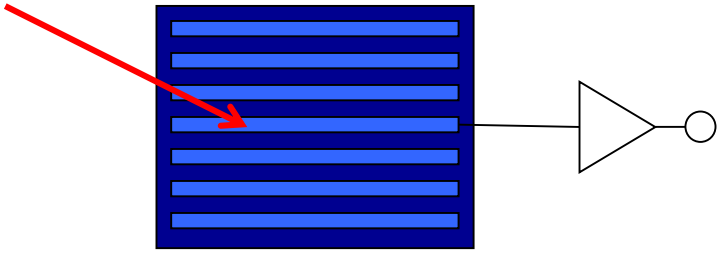



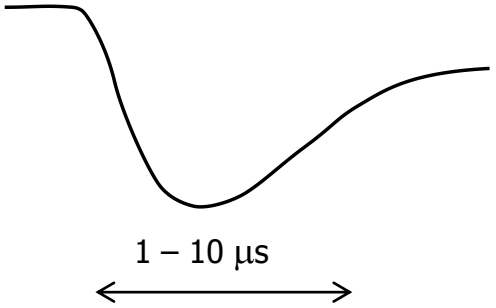

Wire chambers
Straw tubes



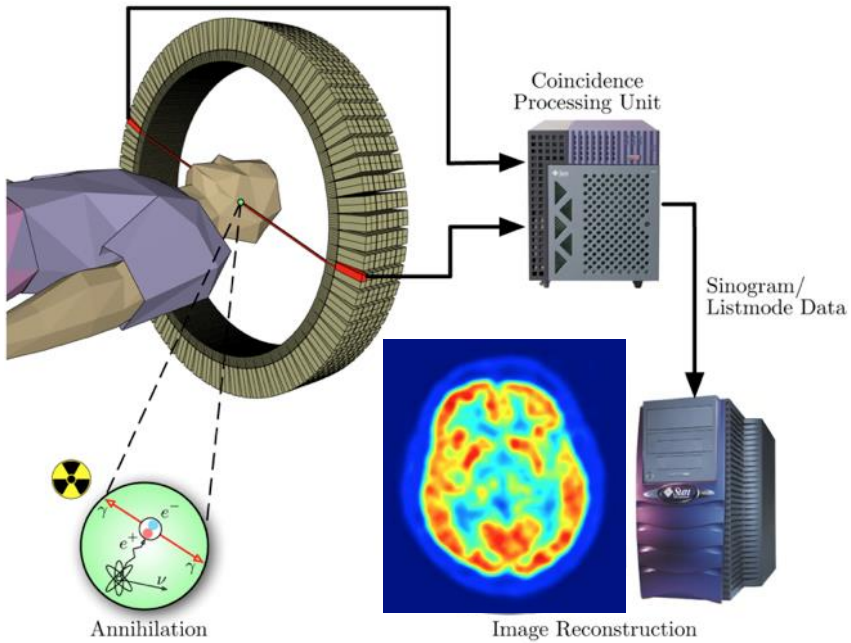
Silicon
Germanium

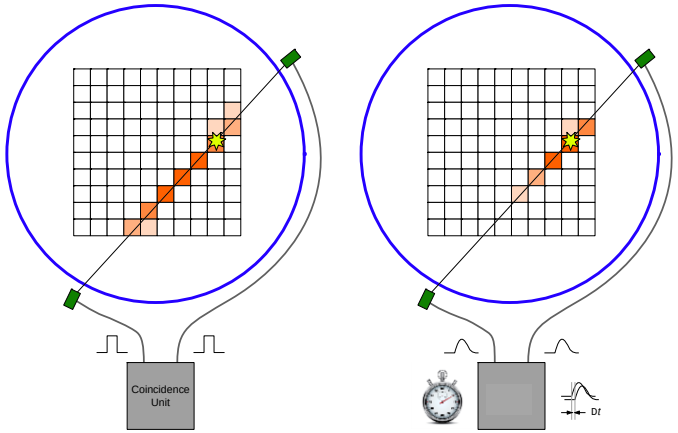




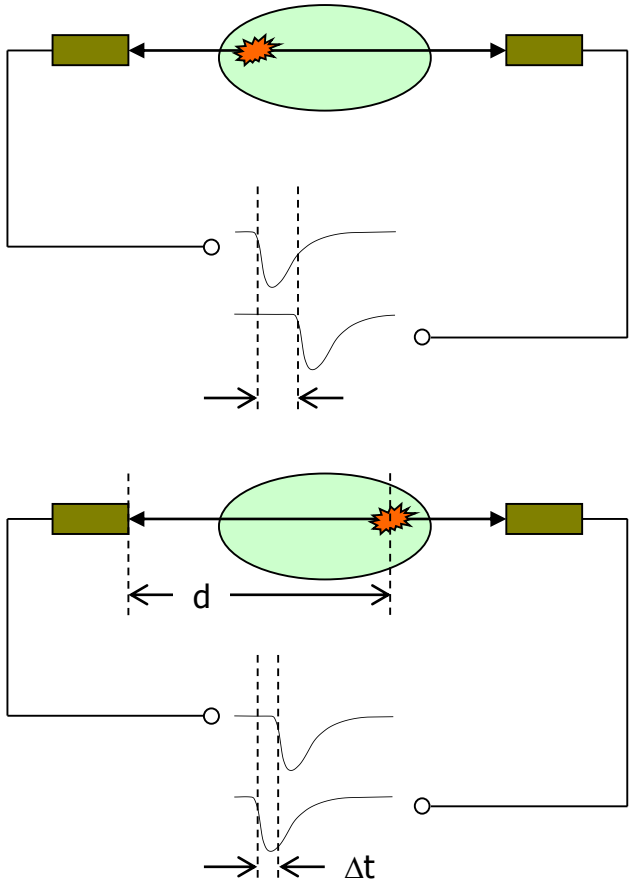
# Measure precise timing: ToF-PET

## Positron Emission Tomography



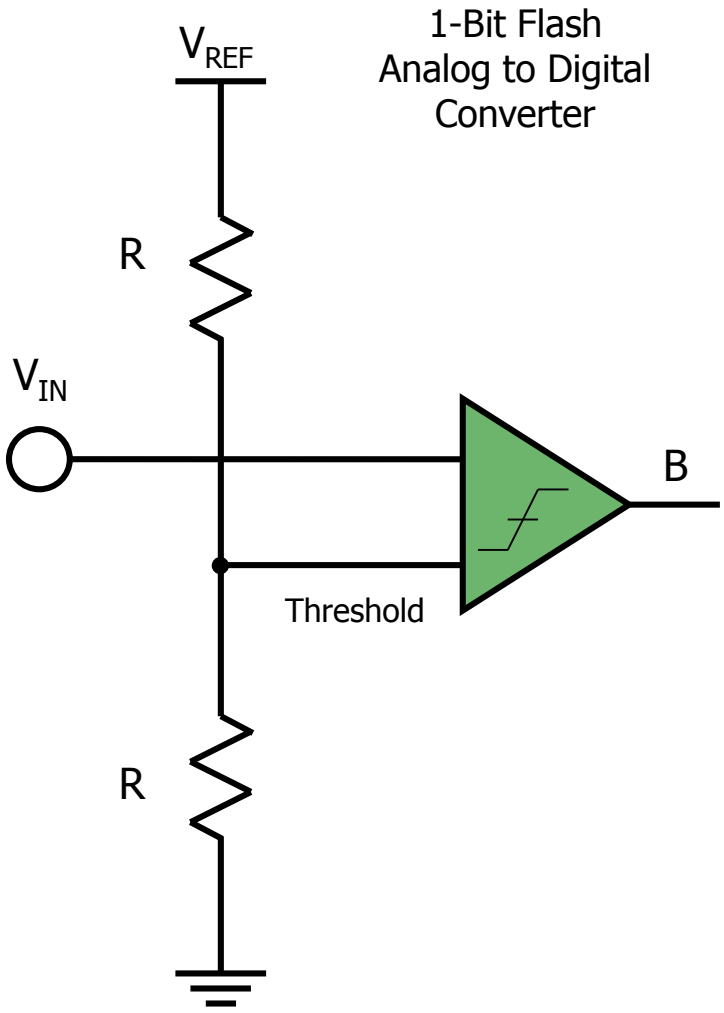

## Time-of-Flight PET

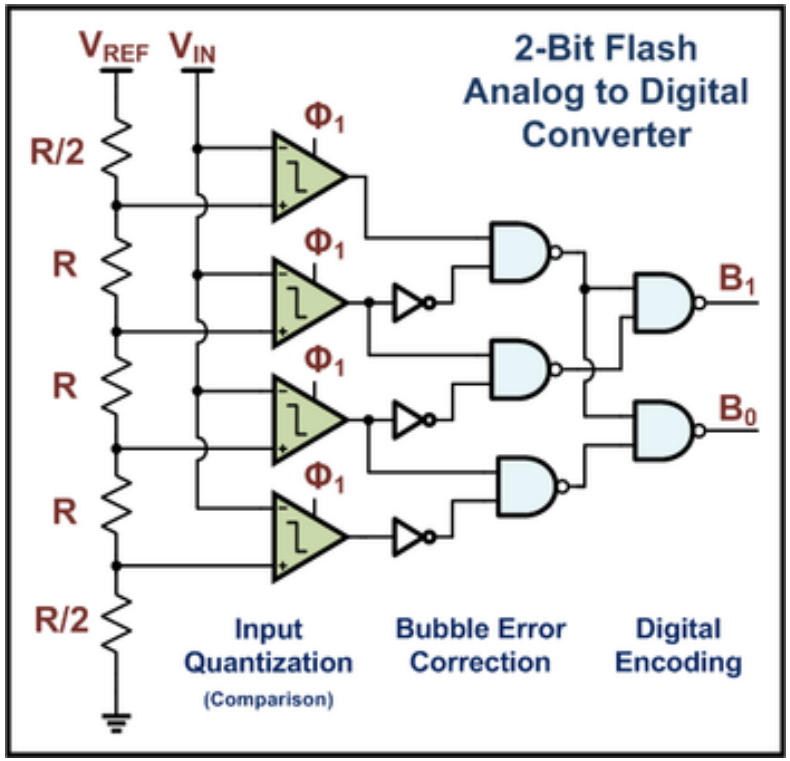



$d \sim c/2 * \Delta t$

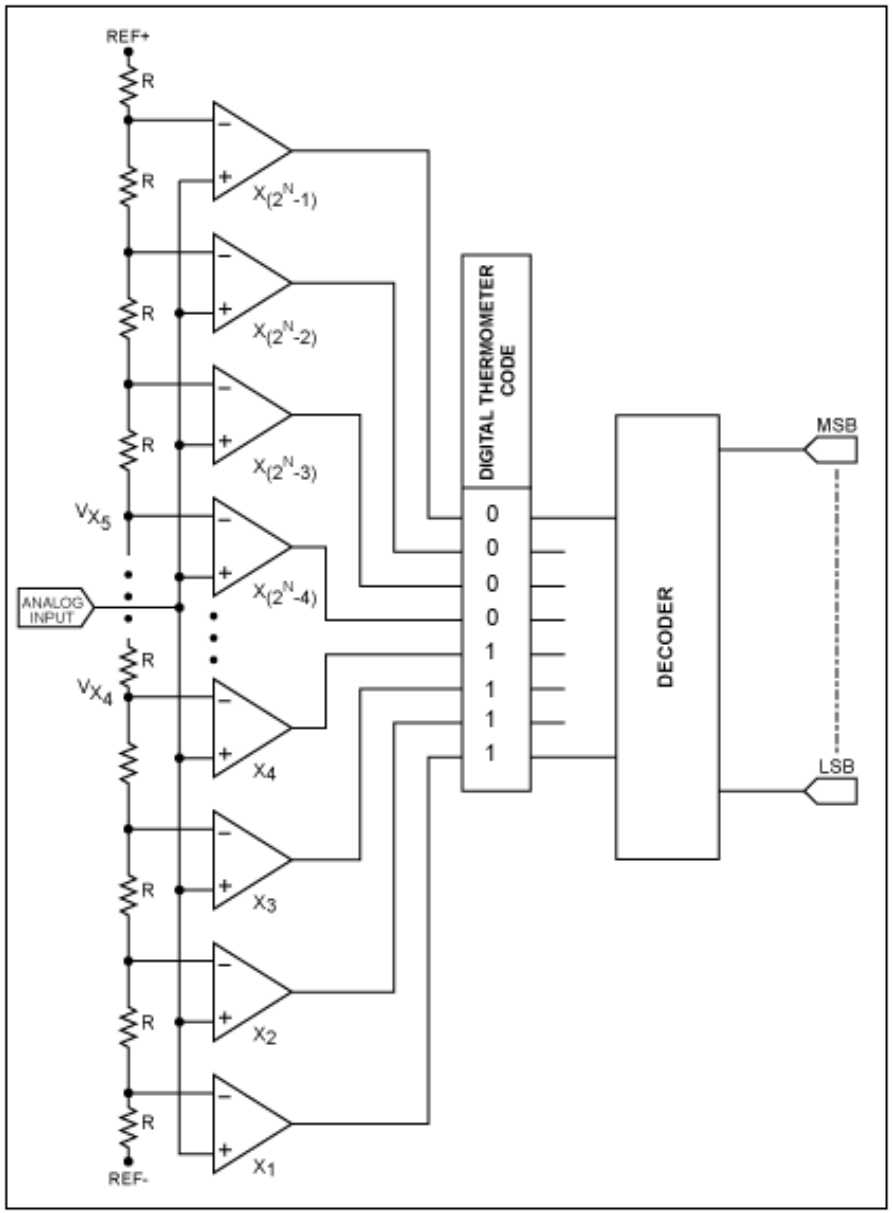
e.g.
d=1 cm → Δt = 67 ps

# 1-bit & 2-bit ADC



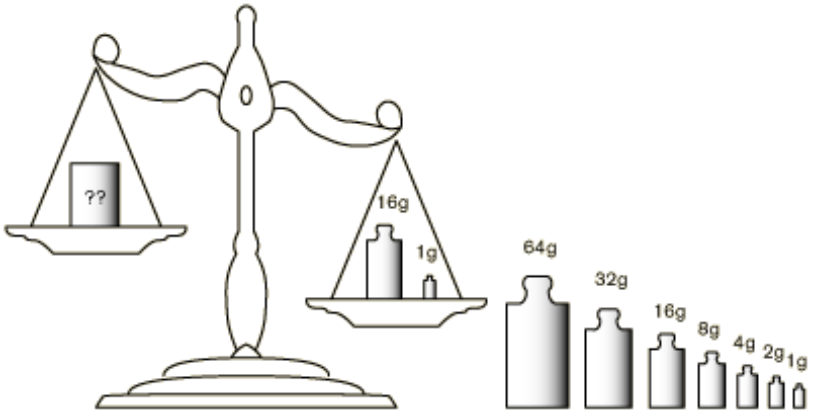



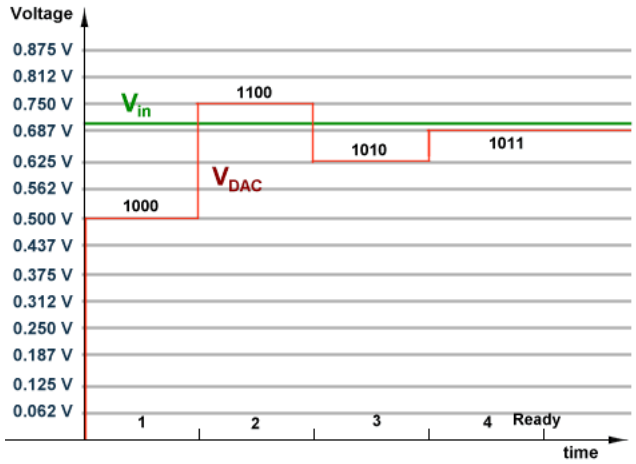
# n-bit ADC

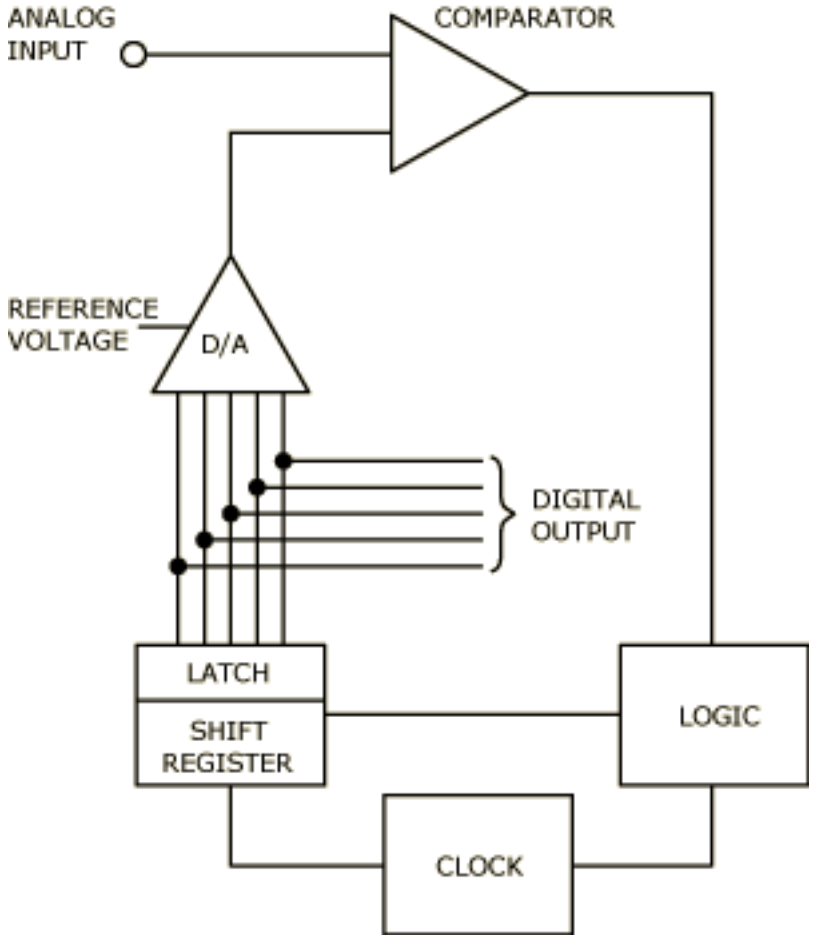



- Flash ADC very fast for small number of bits
- Requires $2^n$ comparators

# Successive approximation ADC



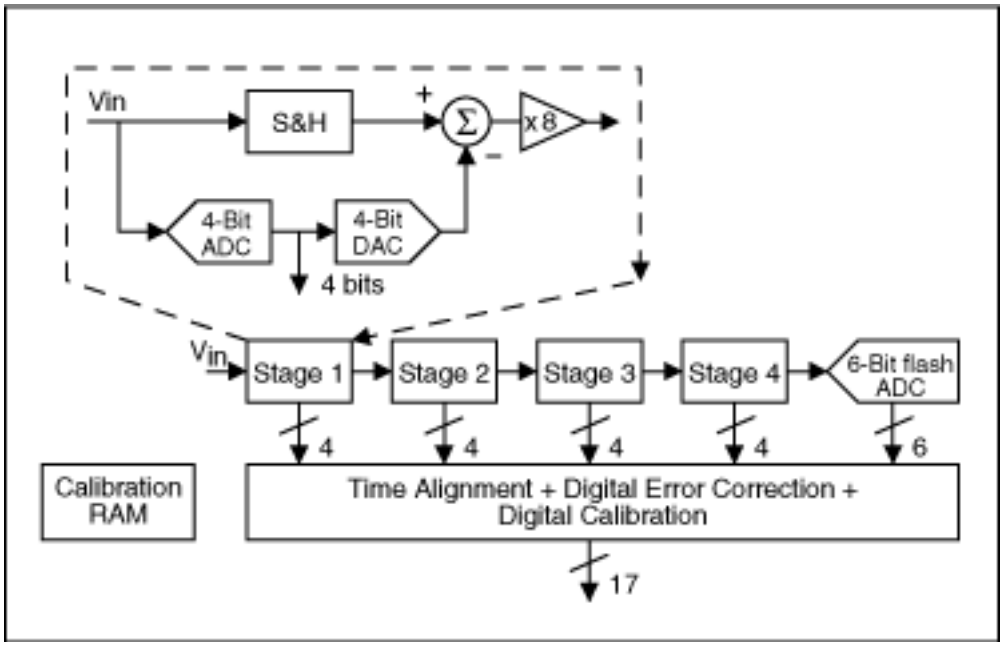



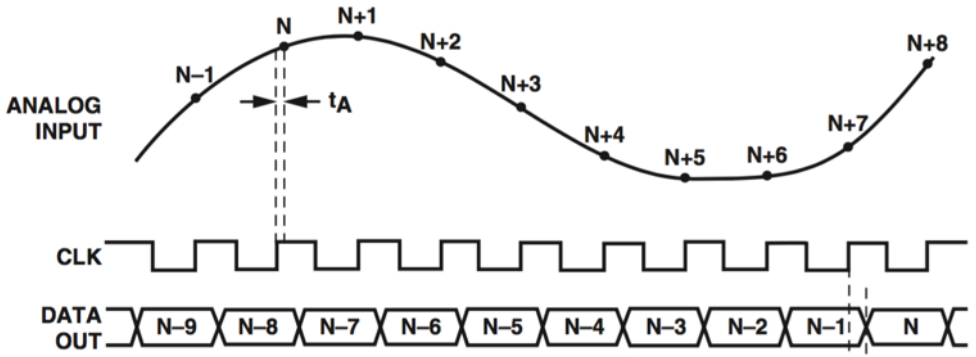



# Pipeline ADC



- Combine 4-Bit flash ADC with successive approximation logic
- Only requires 4-Bit flash ADC
- Can convert one sample in each clock cycle
- Has a latency depending on the number of pipeline stages
- Most common technology for fast ADCs (> 10 MHz)



ANALOG DEVICES

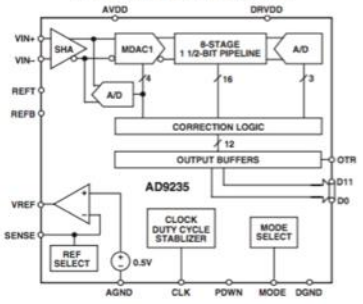
## 12-Bit, 20/40/65 MSPS 3 V A/D Converter

## AD9235

**FEATURES**
- Single 3 V Supply Operation (2.7 V to 3.6 V)
- SNR = 70 dBc to Nyquist at 65 MSPS
- SFDR = 85 dBc to Nyquist at 65 MSPS
- Low Power: 300 mW at 65 MSPS
- Differential Input with 500 MHz Bandwidth
- On-Chip Reference and SHA
- DNL = ±0.4 LSB
- Flexible Analog Input: 1 V p-p to 2 V p-p Range
- Offset Binary or Twos Complement Data Format
- Clock Duty Cycle Stabilizer

**APPLICATIONS**
- Ultrasound Equipment
- IF Sampling in Communications Receivers: IS-95, CDMA-One, IMT-2000
- Battery-Powered Instruments
- Hand-Held Scopemeters
- Low Cost Digital Oscilloscopes

**FUNCTIONAL BLOCK DIAGRAM**




**PRODUCT DESCRIPTION**

The AD9235 is a family of monolithic, single 3 V supply, 12-bit, 20/40/65 MSPS analog-to-digital converters. This family features a high performance sample-and-hold amplifier (SHA) and voltage reference. The AD9235 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 20/40/65 MSPS data rates and guarantee no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available analog-to-digital converters, the AD9235 is suitable for applications in communications, imaging, and medical ultrasound.

A single-ended clock input is used to control all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in straight binary or twos complement formats. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9235 is available in a 28-lead thin shrink small outline package (TSSOP) and a 32-lead chip scale package (LFCSP) and is specified over the industrial temperature range (–40°C to +85°C).

**PRODUCT HIGHLIGHTS**

1. The AD9235 operates from a single 3 V power supply and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
2. Operating at 65 MSPS, the AD9235 consumes a low 300 mW.
3. The patented SHA input maintains excellent performance for input frequencies up to 100 MHz and can be configured for single-ended or differential operation.
4. The AD9235 pinout is similar to the AD9214-65, a 10-bit, 65 MSPS ADC. This allows a simplified upgrade path from 10 bits to 12 bits for 65 MSPS systems.
5. The clock DCS maintains overall ADC performance over a wide range of clock pulsewidths.
6. The OTR output bit indicates when the signal is beyond the selected input range.

REV. B



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Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703 

## AD9235–SPECIFICATIONS

**DC SPECIFICATIONS** (AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, 2 V p-p Differential Input, 1.0 V internal reference, $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

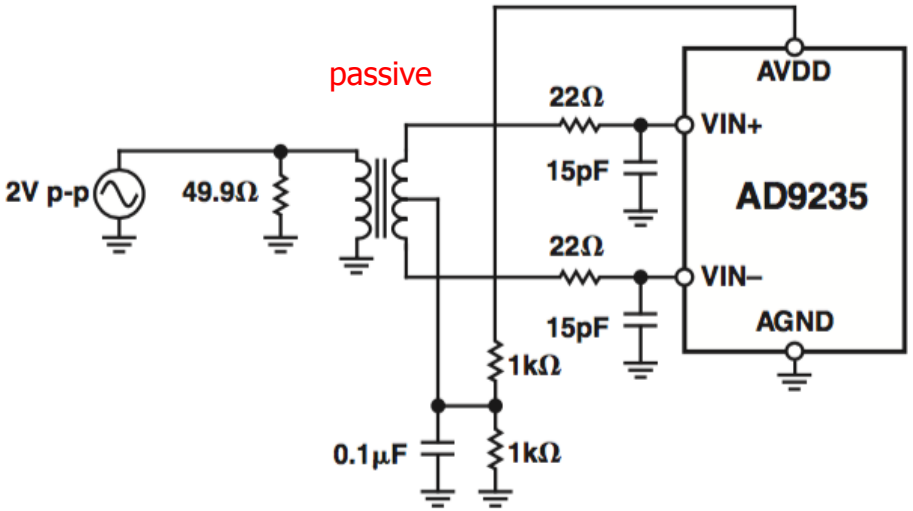
| Parameter | Temp | Test Level | AD9235BRU-20 Min | Typ | Max | AD9235BRU-40 Min | Typ | Max | AD9235BRU/BCP-65 Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESOLUTION | Full | VI | 12 | | | 12 | | | 12 | | | Bits |
| ACCURACY | | | | | | | | | | | | |
| No Missing Codes Guaranteed | Full | VI | 12 | | | 12 | | | 12 | | | Bits |
| Offset Error | Full | VI | | ±0.30 | ±1.20 | | ±0.50 | ±1.20 | | ±0.50 | ±1.20 | % FSR |
| Gain Error[1] | Full | VI | | ±0.30 | ±2.40 | | ±0.50 | ±2.50 | | ±0.50 | ±2.60 | % FSR |
| Differential Nonlinearity (DNL)[2] | Full | IV | | ±0.35 | ±0.65 | | ±0.35 | ±0.75 | | ±0.40 | ±0.80 | LSB |
| | 25°C | I | | ±0.35 | | | ±0.35 | | | ±0.35 | | LSB |
| Integral Nonlinearity (INL)[2] | Full | IV | | ±0.45 | ±0.80 | | ±0.50 | ±0.90 | | ±0.70 | ±1.30 | LSB |
| | 25°C | I | | ±0.40 | | | ±0.40 | | | ±0.45 | | LSB |
| TEMPERATURE DRIFT | | | | | | | | | | | | |
| Offset Error | Full | V | | ±2 | | | ±2 | | | ±3 | | ppm/°C |
| Gain Error[1] | Full | V | | ±12 | | | ±12 | | | ±12 | | ppm/°C |
| INTERNAL VOLTAGE REFERENCE | | | | | | | | | | | | |
| Output Voltage Error (1 V Mode) | Full | VI | | ±5 | ±35 | | ±5 | ±35 | | ±5 | ±35 | mV |
| Load Regulation @ 1.0 mA | Full | V | | 0.8 | | | 0.8 | | | 0.8 | | mV |
| Output Voltage Error (0.5 V Mode) | Full | V | | ±2.5 | | | ±2.5 | | | ±2.5 | | mV |
| Load Regulation @ 0.5 mA | Full | V | | 0.1 | | | 0.1 | | | 0.1 | | mV |
| INPUT REFERRED NOISE | | | | | | | | | | | | |
| VREF = 0.5 V | 25°C | V | | 0.54 | | | 0.54 | | | 0.54 | | LSB rms |
| VREF = 1.0 V | 25°C | V | | 0.27 | | | 0.27 | | | 0.27 | | LSB rms |
| ANALOG INPUT | | | | | | | | | | | | |
| Input Span, VREF = 0.5 V | Full | IV | | 1 | | | 1 | | | 1 | | V p-p |
| Input Span, VREF = 1.0 V | Full | IV | | 2 | | | 2 | | | 2 | | V p-p |
| Input Capacitance[3] | Full | V | | 7 | | | 7 | | | 7 | | pF |
| REFERENCE INPUT | | | | | | | | | | | | |
| RESISTANCE | Full | V | | 7 | | | 7 | | | 7 | | kΩ |
| POWER SUPPLIES | | | | | | | | | | | | |
| Supply Voltages | | | | | | | | | | | | |
| AVDD | Full | IV | 2.7 | 3.0 | 3.6 | 2.7 | 3.0 | 3.6 | 2.7 | 3.0 | 3.6 | V |
| DRVDD | Full | IV | 2.25 | 3.0 | 3.6 | 2.25 | 3.0 | 3.6 | 2.25 | 3.0 | 3.6 | V |
| Supply Current | | | | | | | | | | | | |
| IAVDD[2] | Full | V | | 30 | | | 55 | | | 100 | | mA |
| IDRVDD[2] | Full | V | | 2 | | | 5 | | | 7 | | mA |
| PSRR | Full | V | | ±0.01 | | | ±0.01 | | | ±0.01 | | % FSR |
| POWER CONSUMPTION | | | | | | | | | | | | |
| DC Input[4] | Full | V | | 90 | | | 165 | | | 300 | | mW |
| Sine Wave Input[2] | Full | VI | | 95 | 110 | | 180 | 205 | | 320 | 350 | mW |
| Standby Power[5] | Full | V | | 1.0 | | | 1.0 | | | 1.0 | | mW |

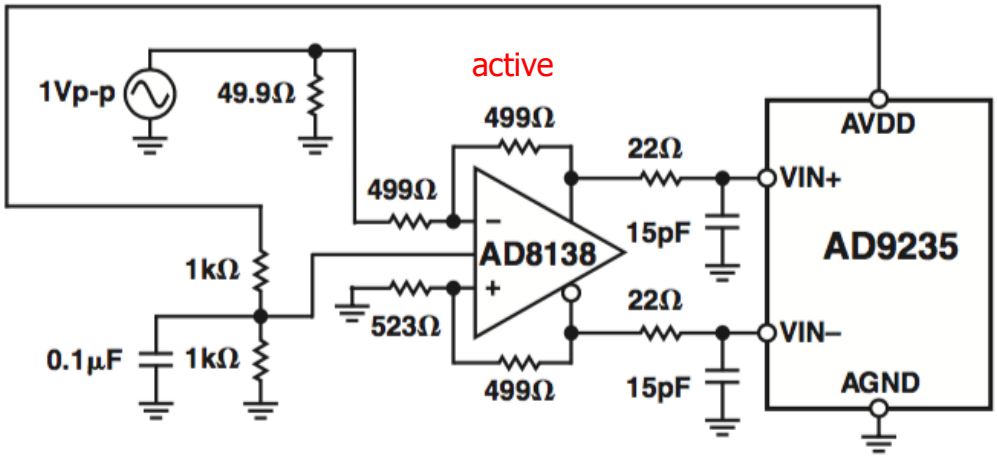
NOTES
[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0 V external reference).
[2]Measured at maximum clock rate, $f_{IN}$ = 2.4 MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3]Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 2 for the equivalent analog input structure.
[4]Measured with dc input at maximum clock rate.
[5]Standby power is measured with a dc input, the CLK pin inactive (i.e., set to AVDD or AGND).

Specifications subject to change without notice.

# ADC input configuration

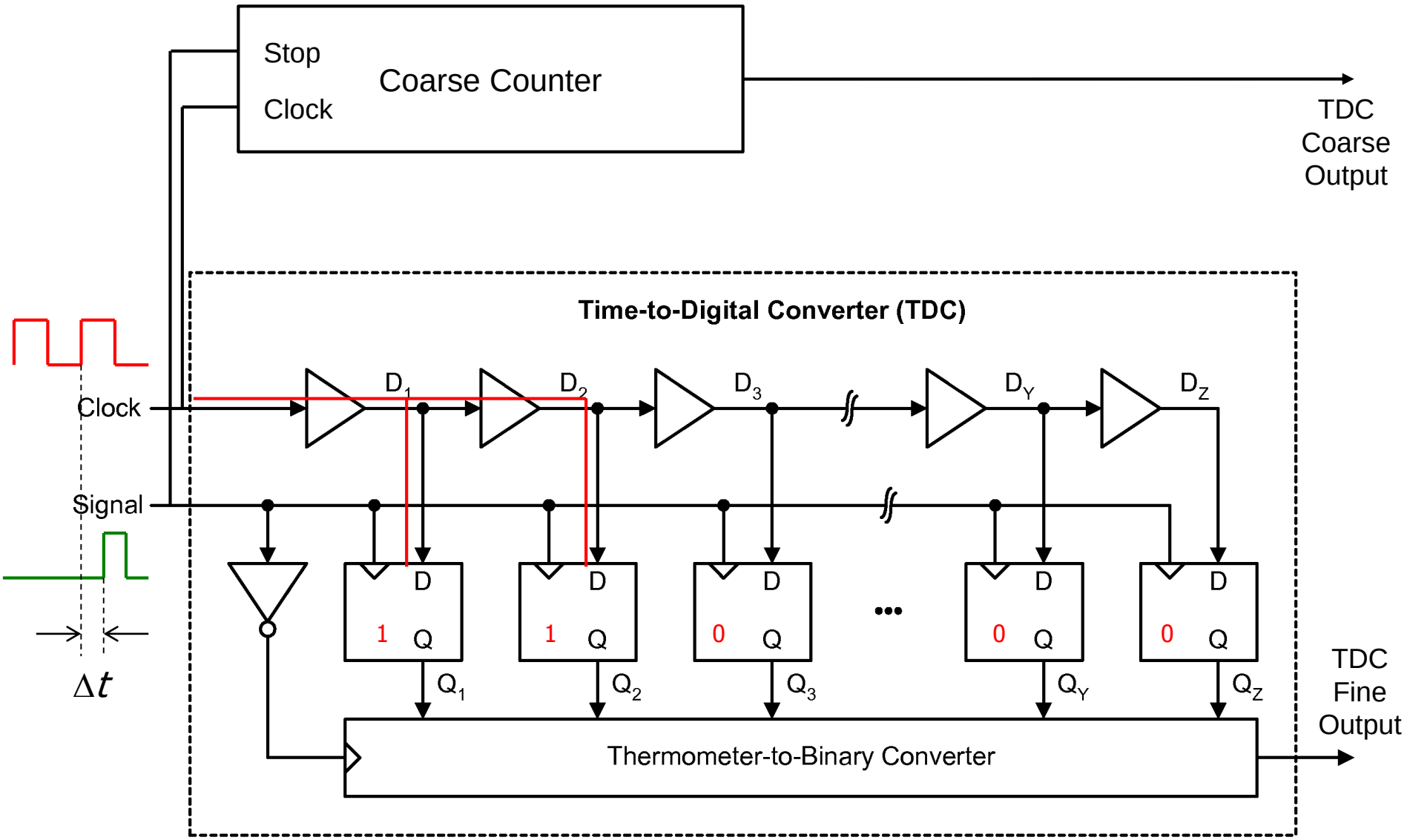
- Modern ADCs have differential inputs
- Out detectors have single-ended output
- We need a converter



# Time-to-Digital Converter

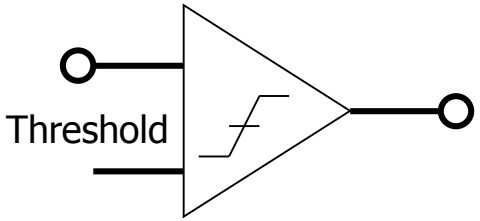




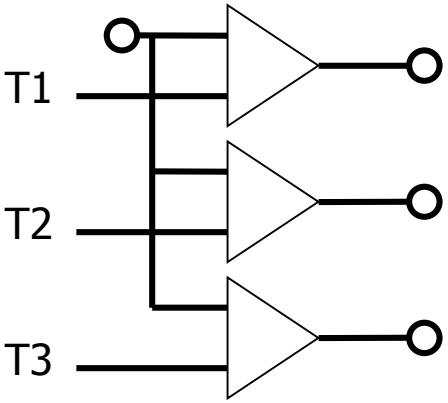
# Signal discrimination



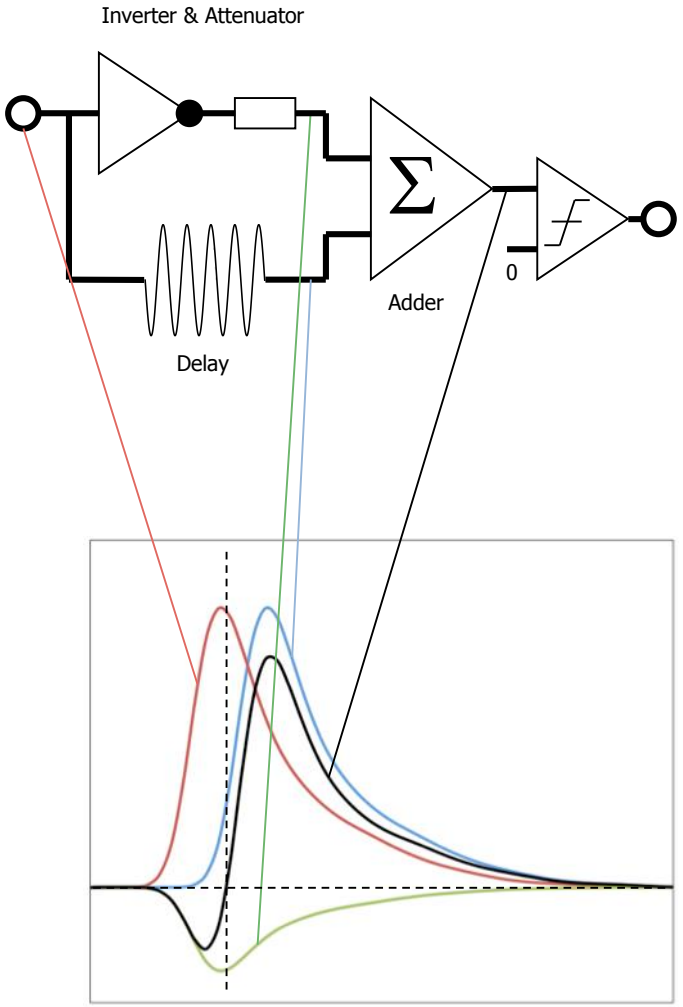
## Single Threshold



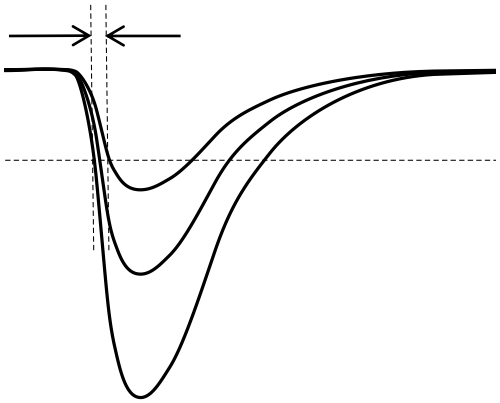

## Multiple Thresholds

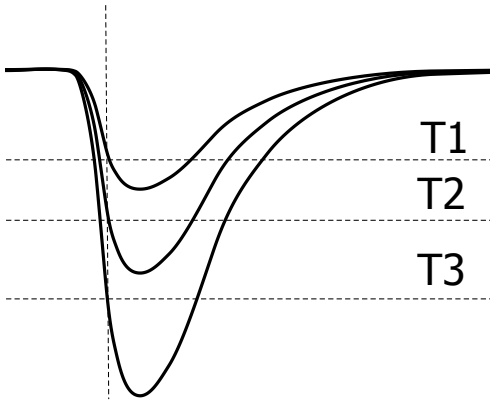



## Constant Fraction (CFD)

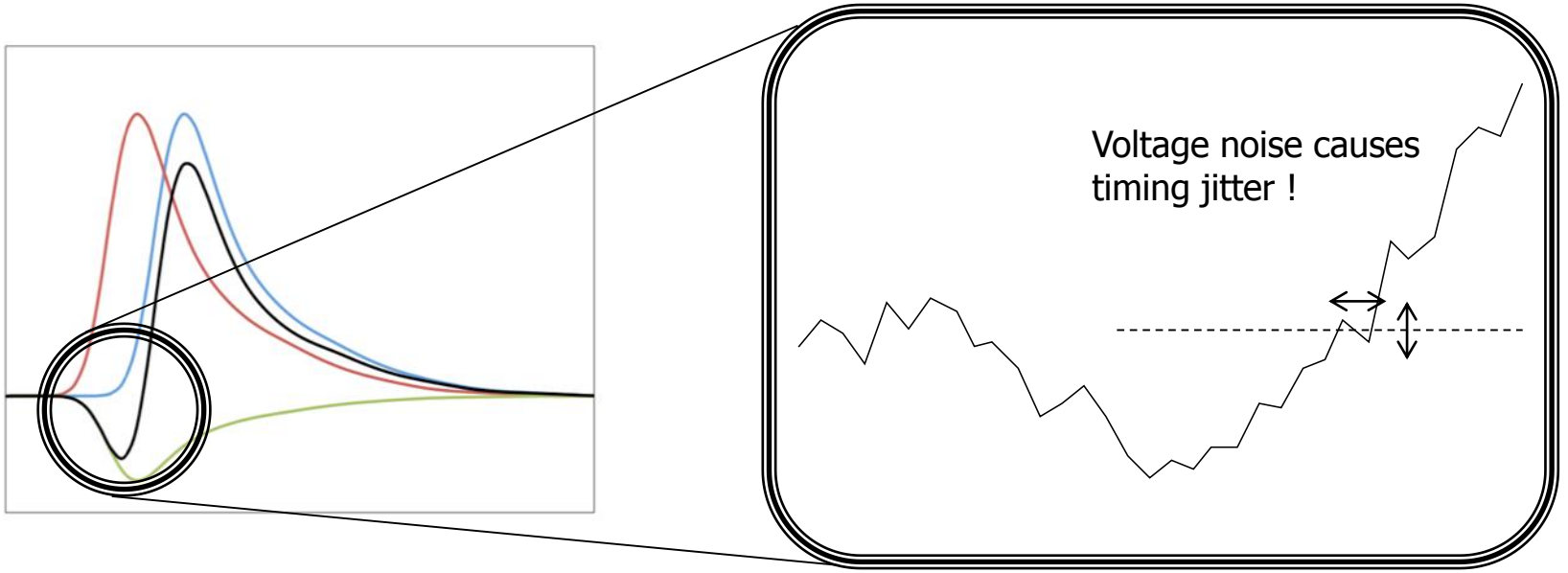


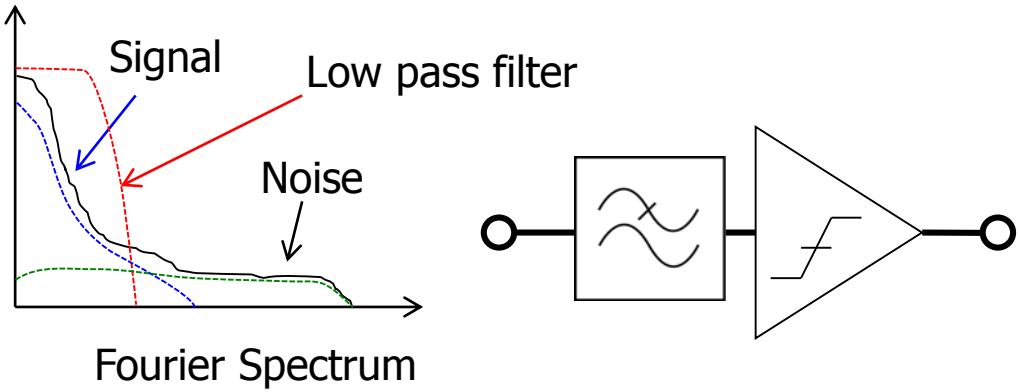

"Time-Walk"

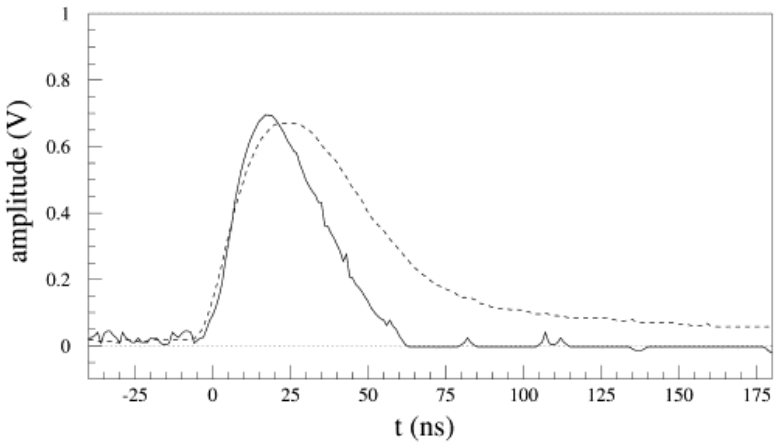




# Influence of noise

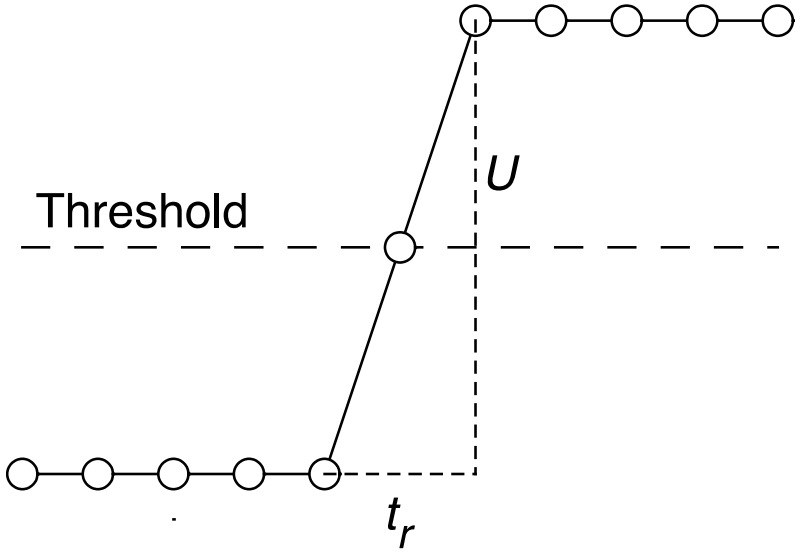


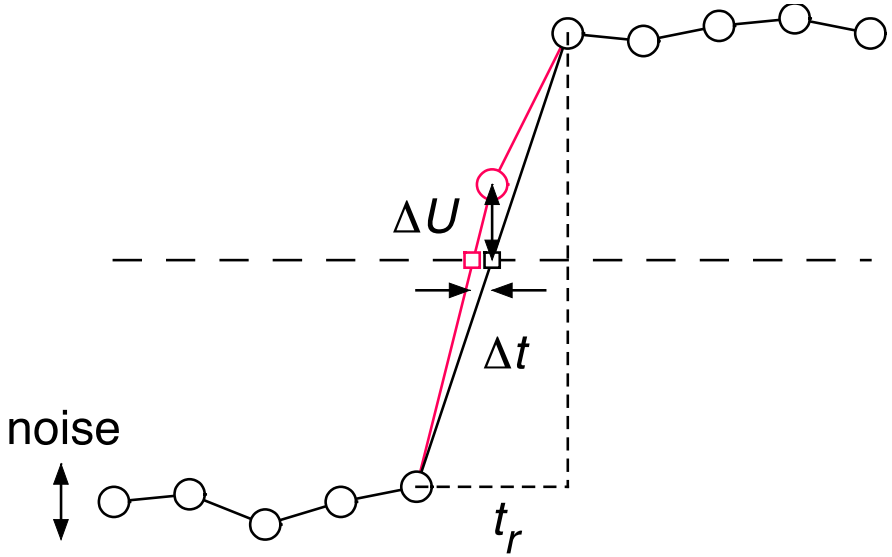




Low pass filter (shaper) reduces noise while maintaining most of the signal

# Noise limited time accuracy




$$\frac{\mathrm{D}U}{\mathrm{D}t} \approx \frac{U}{t_r} \longrightarrow \mathrm{D}t = \frac{\mathrm{D}U}{U} \cdot t_r$$

All values in **this** talk are σ (RMS) !
FHWM = 2.35 x σ

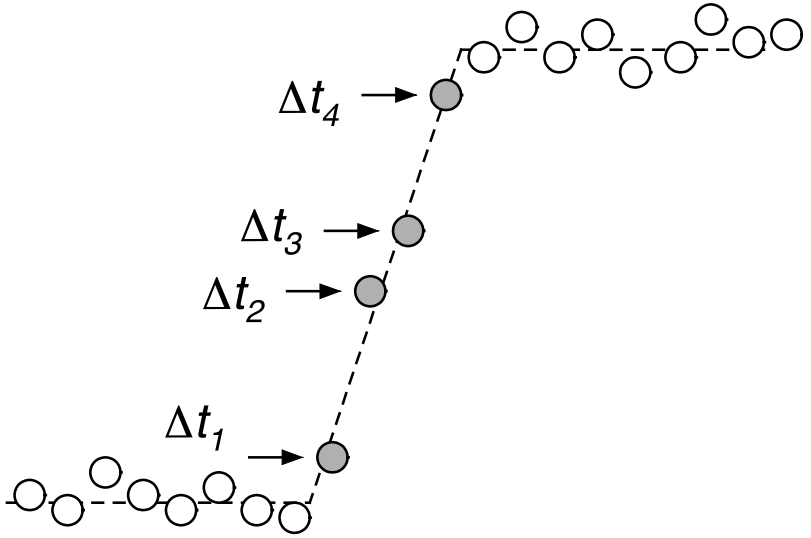
| U [mV] | ΔU [mV] | $t_r$ | Δt |
|---|---|---|---|
| 100 | 1 | 1 ns | 10 ps |
| 10 | 1 | 3 ns | 300 ps |

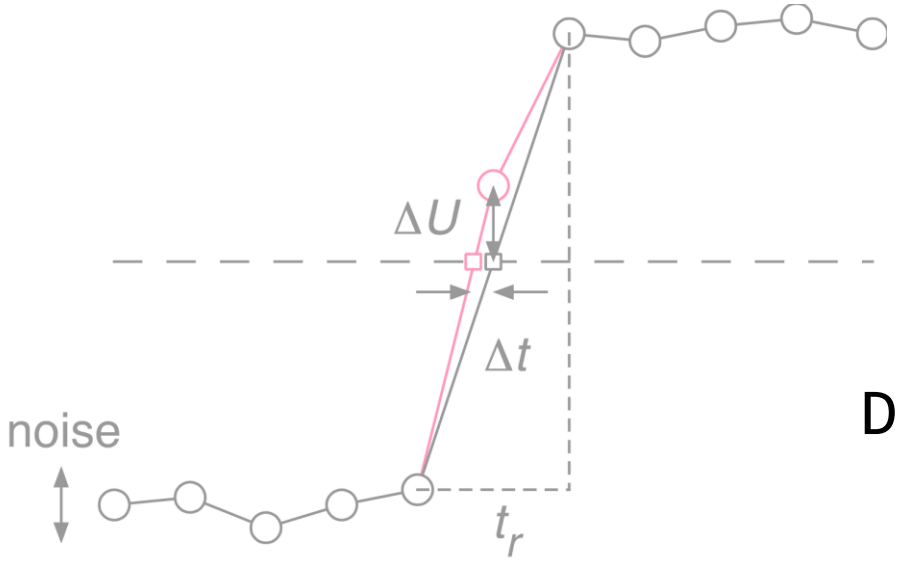
Most today's TDCs have ~20 ps LSB

How can we do better ?

# Noise limited time accuracy



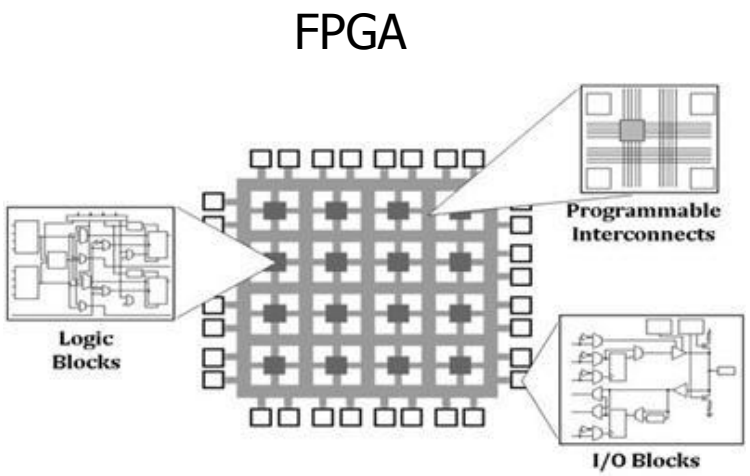



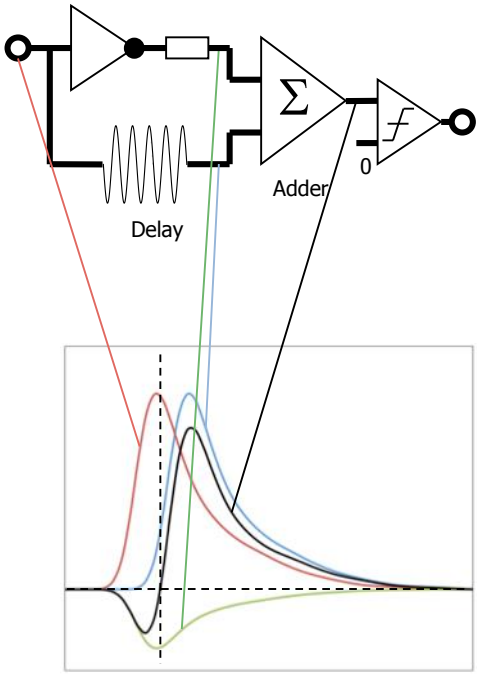



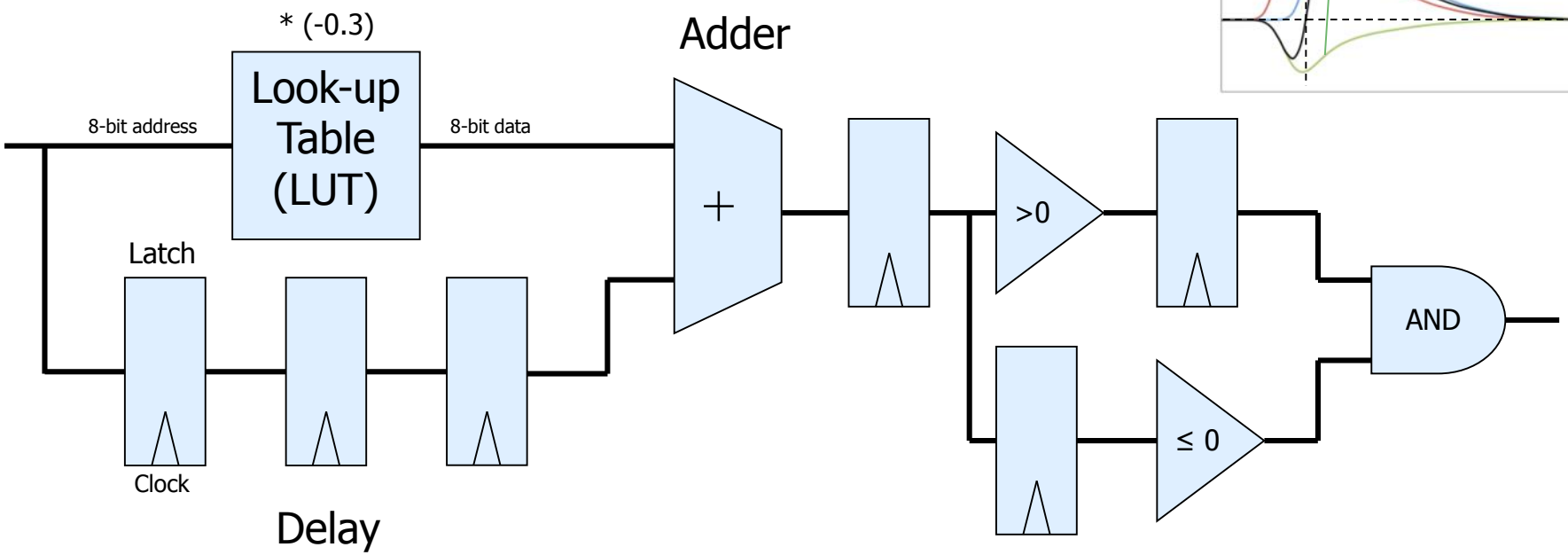

$$\frac{\mathrm{D}U}{\mathrm{D}t} \approx \frac{U}{t_r} \longrightarrow \mathrm{D}t = \frac{\mathrm{D}U}{U} \cdot t_r$$

$$\mathrm{D}t = \frac{\mathrm{D}U}{U} \cdot t_r \cdot \frac{1}{\sqrt{n}} = \frac{\mathrm{D}U}{U} \frac{t_r}{\sqrt{t_r f_S}} = \frac{\mathrm{D}U}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_S}}$$

# Example: CFG in FPGA

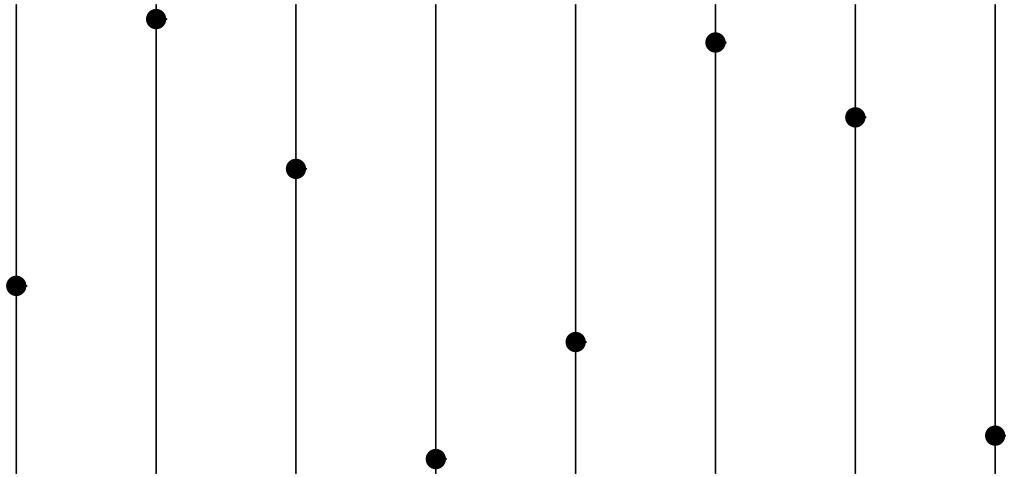


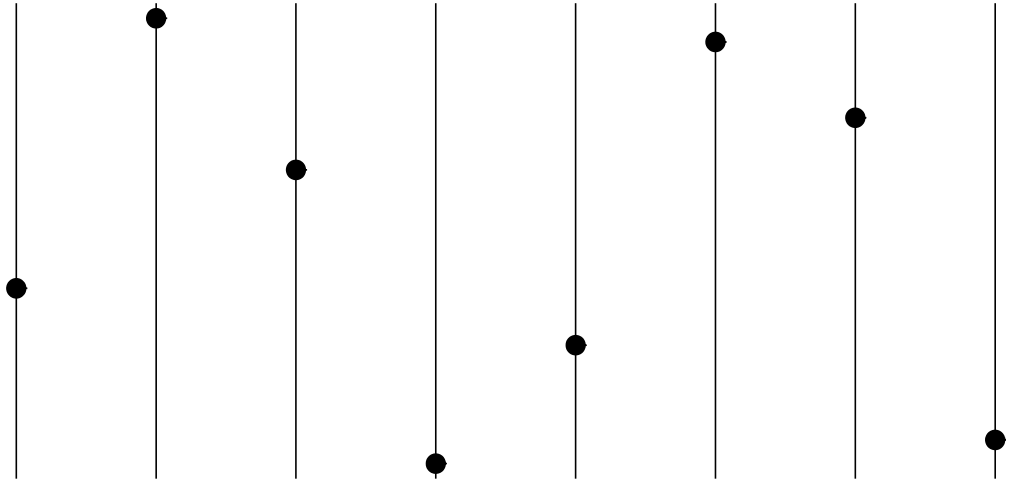



# Nyquist-Shannon Sampling Theorem

$f_{signal} < f_{sampling}/2$

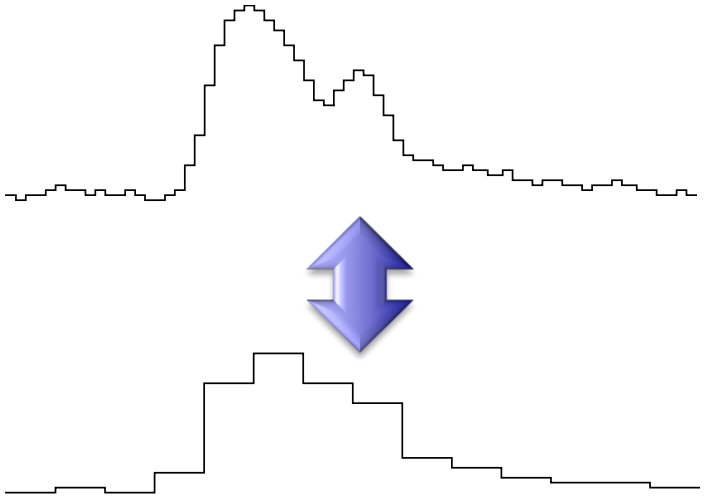


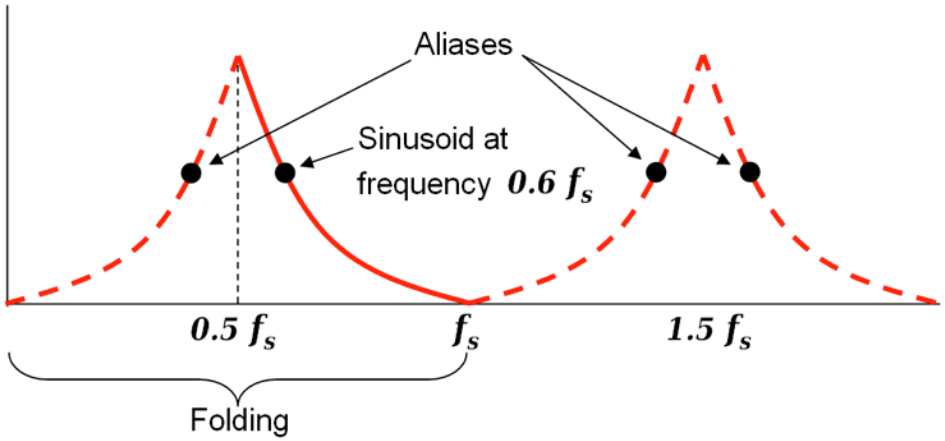
$f_{signal} > f_{sampling}/2$



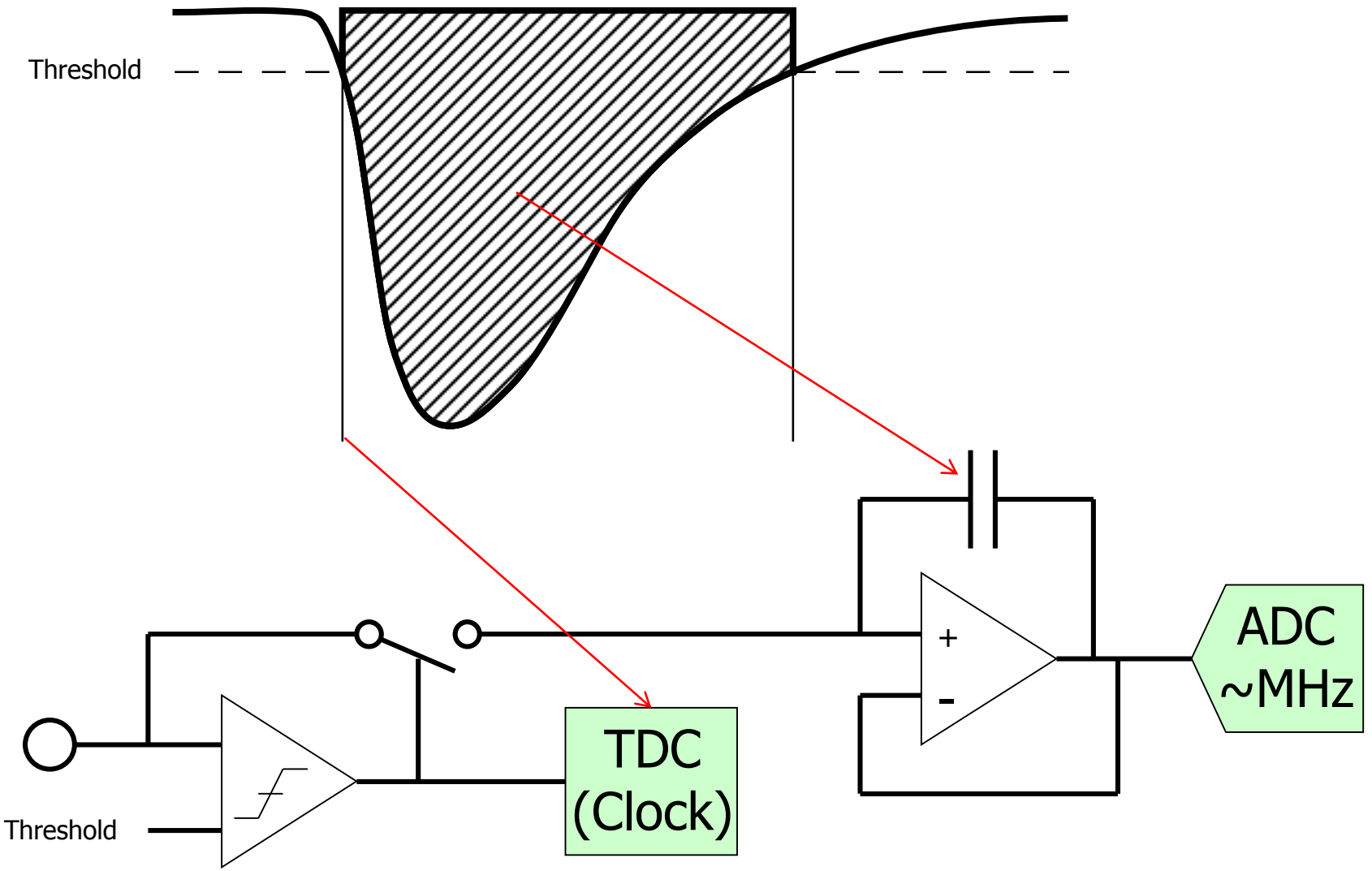
# Limits of waveform digitizing

- Aliasing Occurs if $f_{signal} > 0.5 * f_{sampling}$
- Features of the signal can be lost ("pile-up")
- Measurement of time becomes hard
- ADC resolution limits energy measurement
- Need very fast high resolution ADC

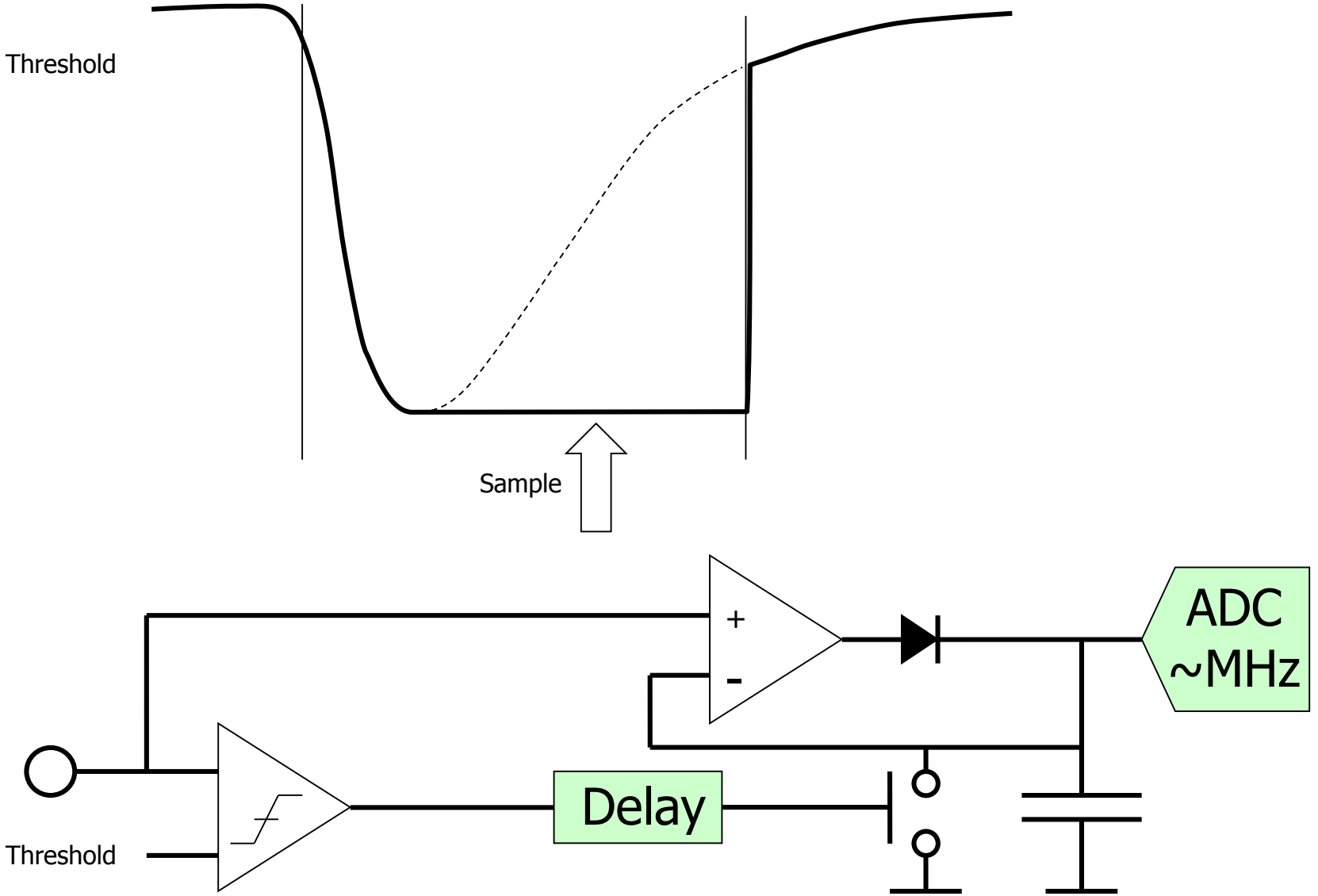




# Charge ADCs (QADC)

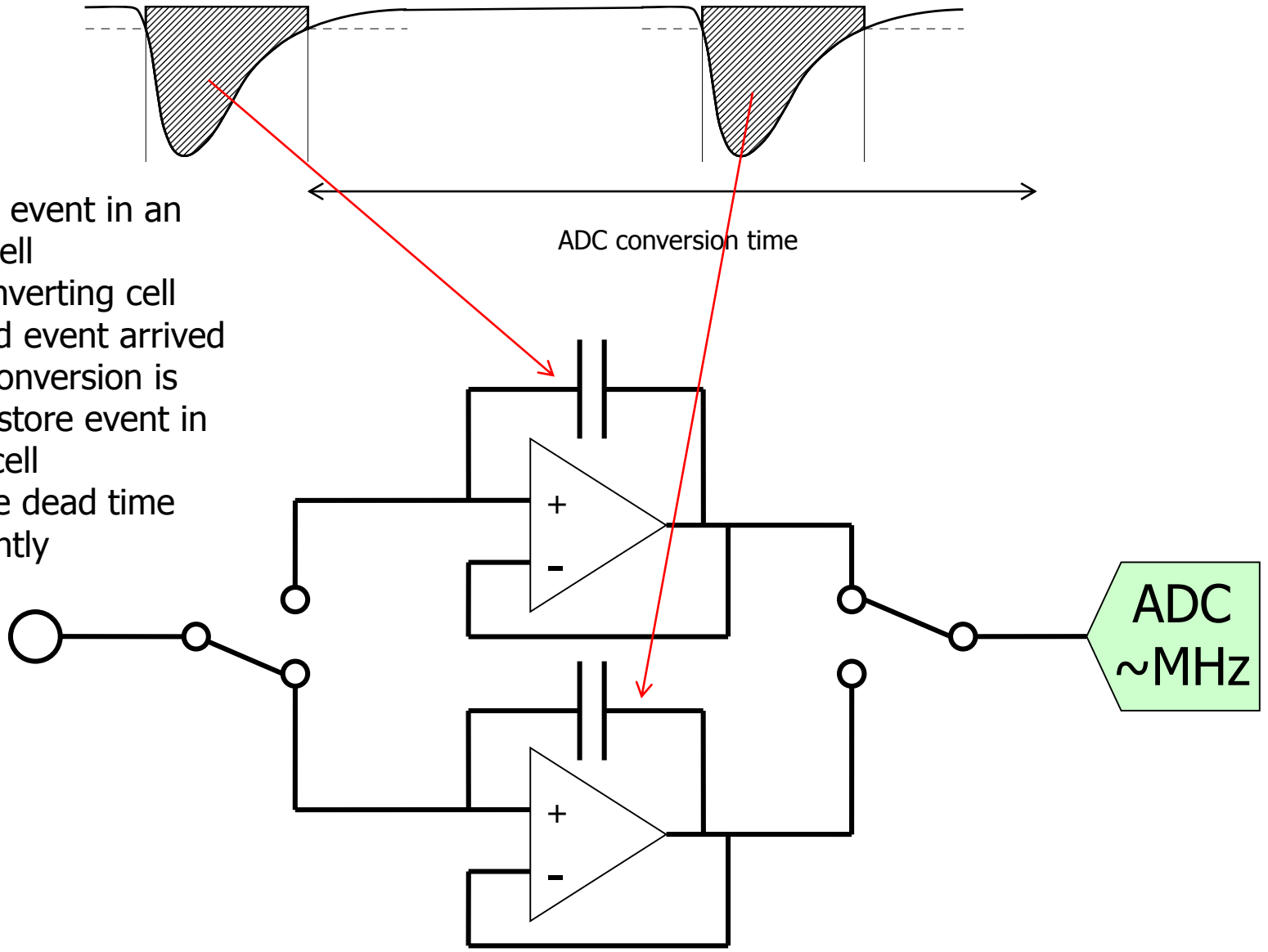


# Peak sensing ADC

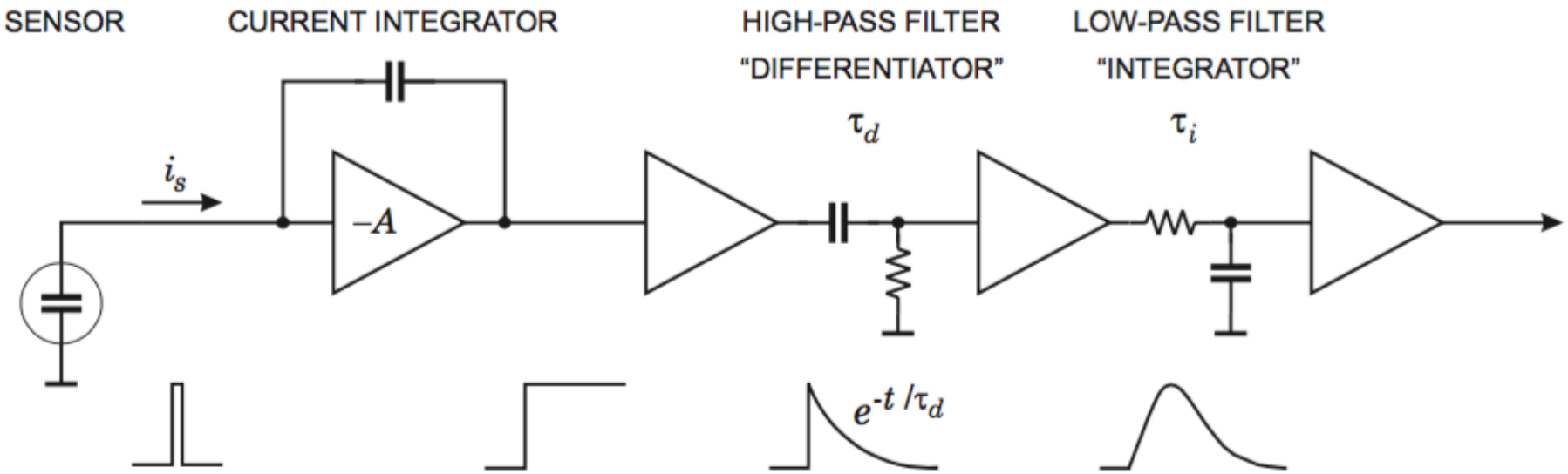


# Double buffering

- Store an event in an analog cell
- Start converting cell
- If second event arrived before conversion is ready – store event in second cell
- Decrease dead time significantly

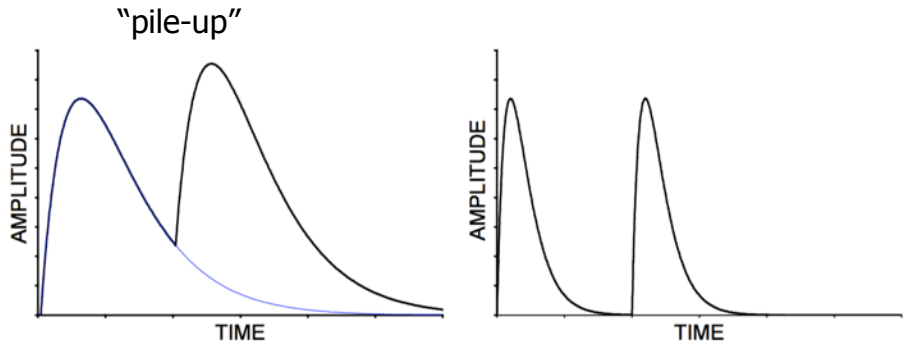


# Analog readout chain

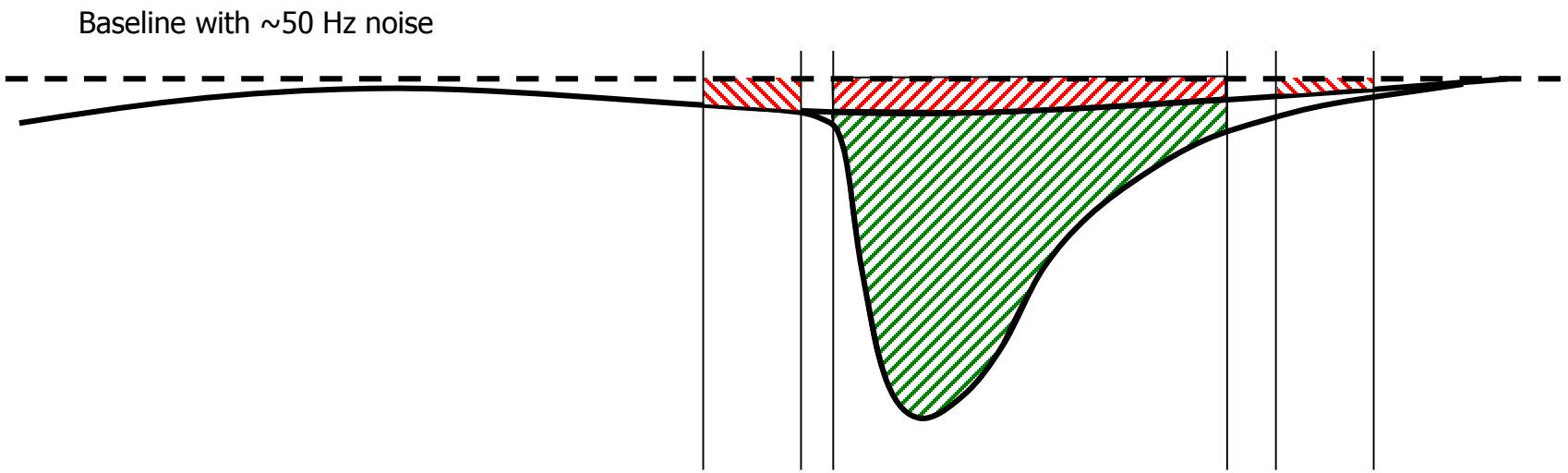



Optimal parameters can greatly improve the signal-to-noise ratio

Effect of slow shaping time:

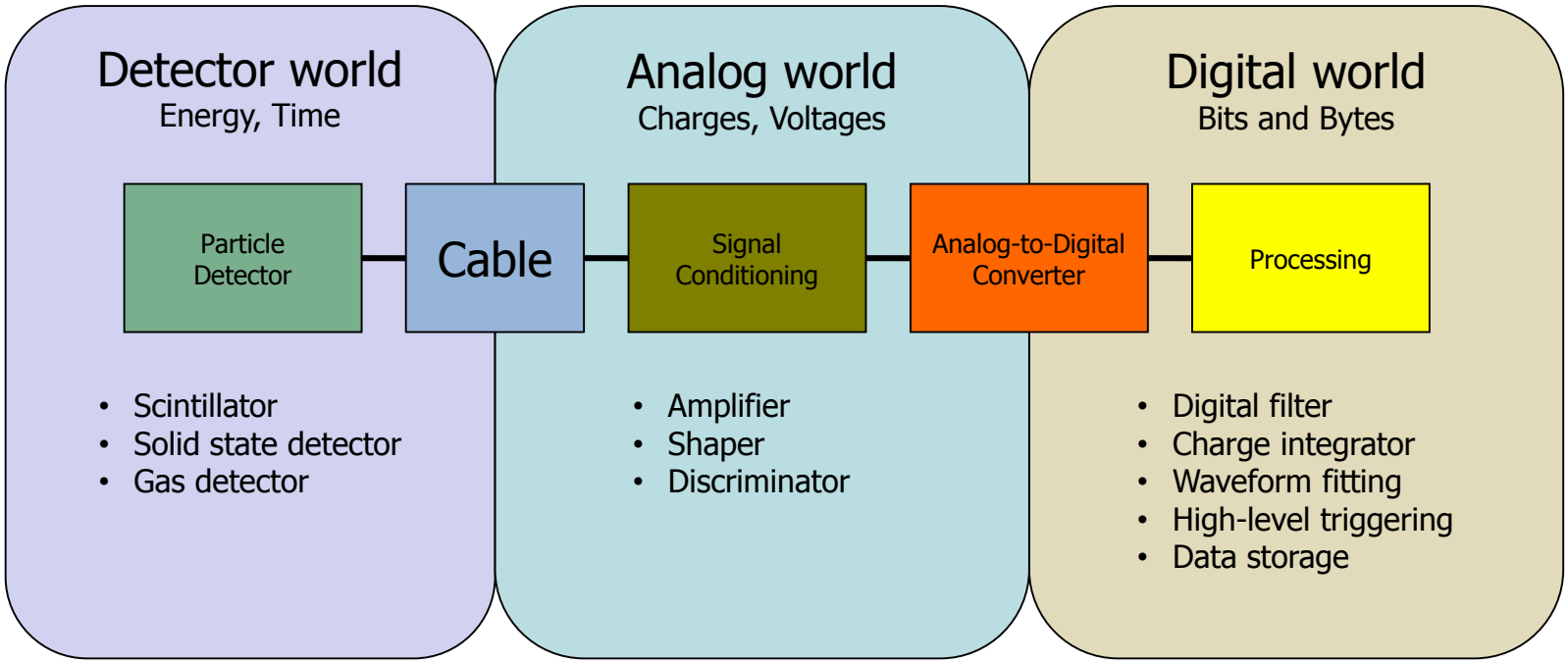


# Baseline noise

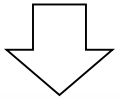



- Charge integration error due to signal "sitting" on fluctuating baseline (e.g. 50 Hz ground loop or artifact of shaper)
- Can be fixed by sampling baseline prior to signal (requires signal delay)
- Sample signal after peak for pile-up recognition

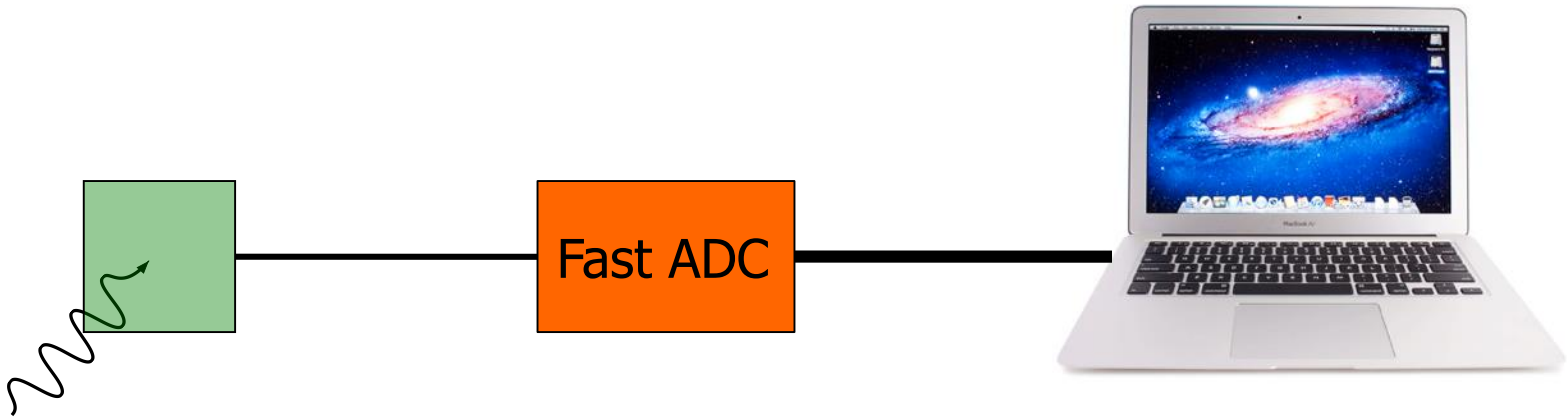
# Conventional DAQ chain



# Let's go a bit faster…



# Ultimate sampling



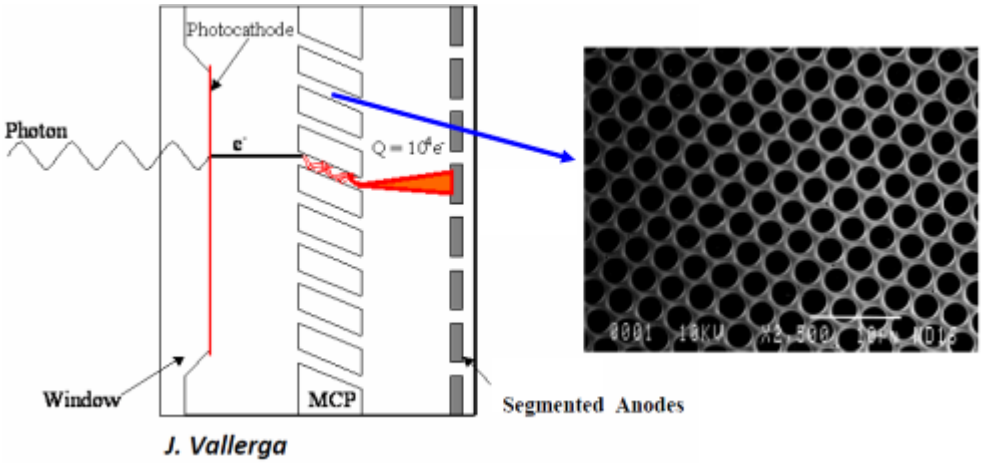

Direct fast sampling without shaping

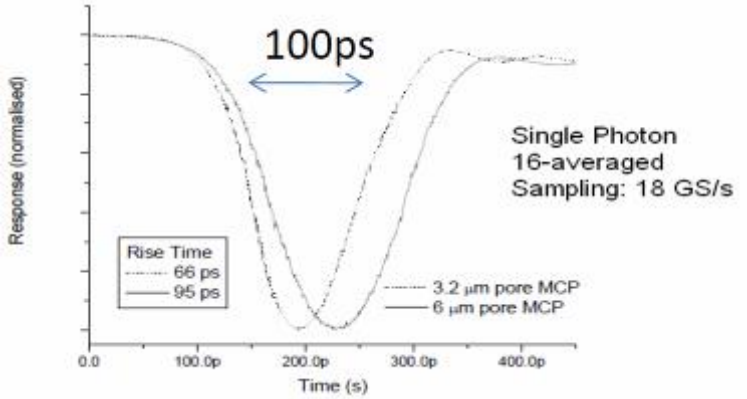
- No shaping artifacts
- Less electronics
- All information if captured if $f_{sampling} > 2*f_{signal}$ and LSB < $V_{noise}$
- Any shaping circuitry can only *remove* information

# What are the fastest detectors?

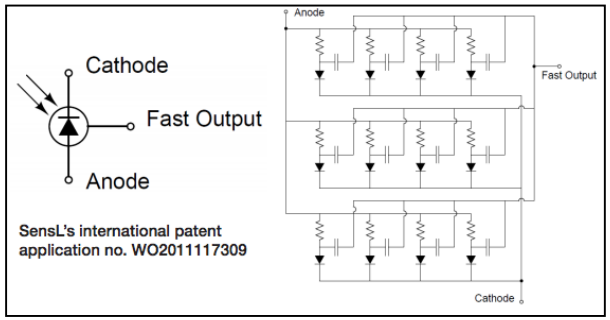


- Micro-Channel-Plates (MCP)
  - Photomultipliers with thousands of tiny channels (3-10 μm)
  - Typical gain of 10,000 per plate
  - Very fast rise time down to 70 ps
- 70 ps rise time → **4-5 GHz BW** → **10 GSPS**
- SiPMs (Silicon PMTs) are also getting < 100 ps

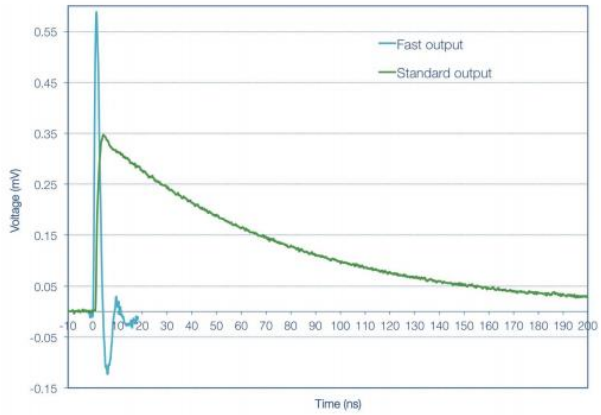



J. Milnes, J. Howoth, Photek

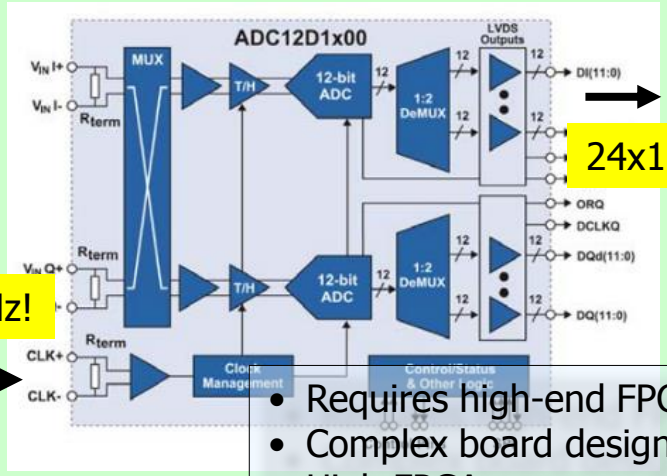



http://sensl.com



# Can it be done with FADCs?

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s




24x1.8 Gbits/s

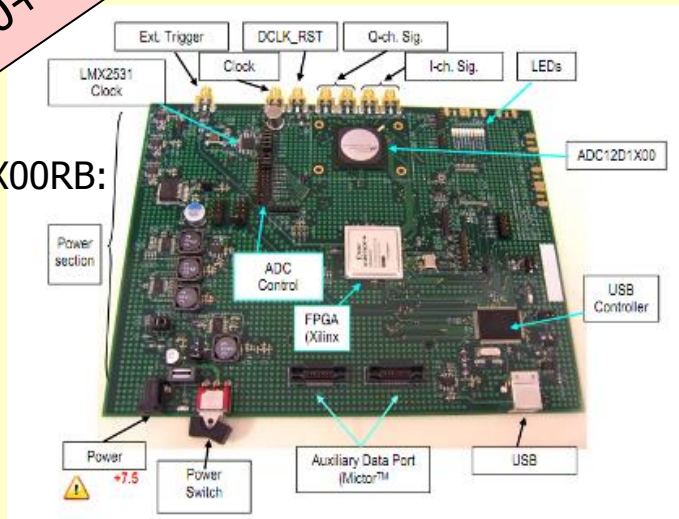
1.8 GHz!

- Requires high-end FPGA
- Complex board design
- High FPGA power

PX1500-4:
2 Channel
3 GS/s
8 bits

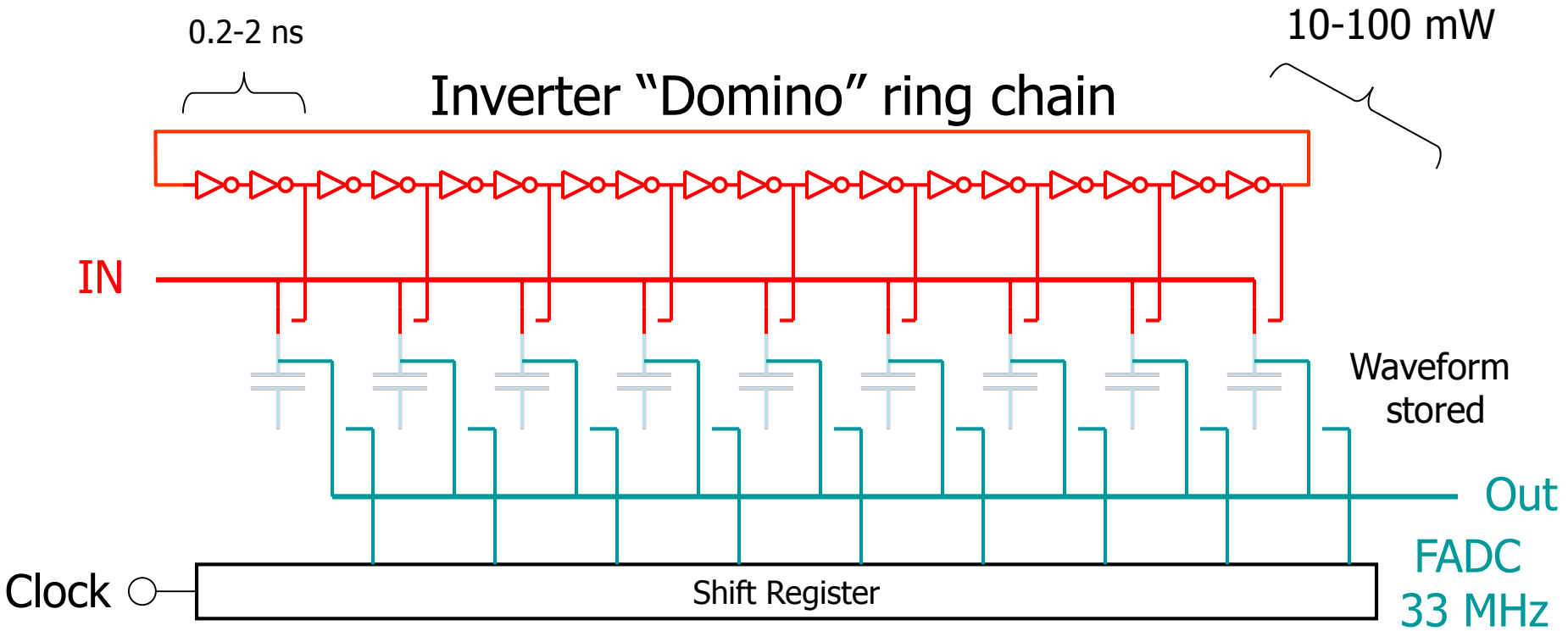

1-10 k$ / channel
What about 1000+ Channels?

ADC12D1X00RB:
1 Channel
1.8 GS/s
12 bits



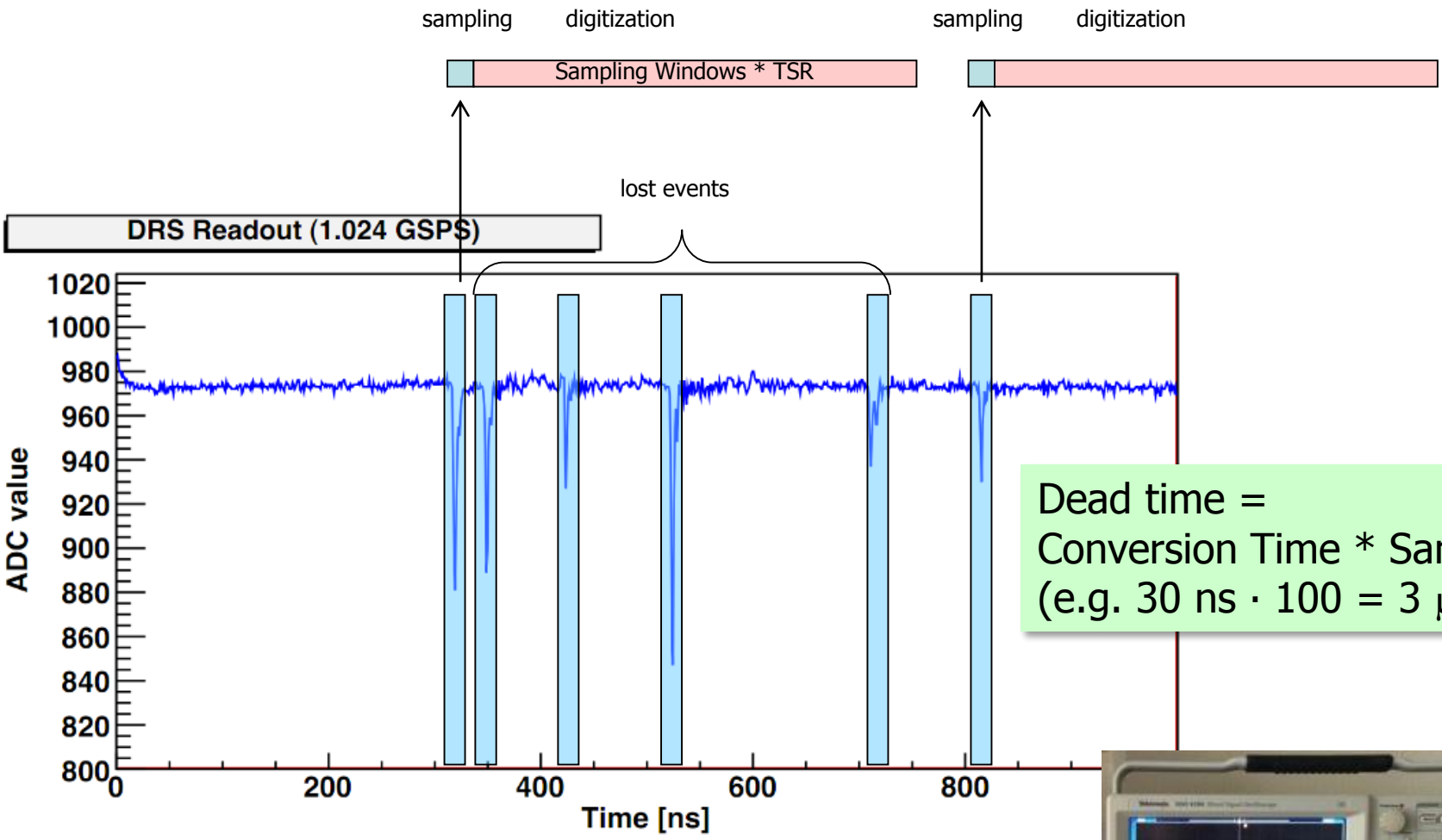

V1761: 2 Channels, 4 GS/s, 10 bits

# Switched Capacitor Array (Analog Memory)

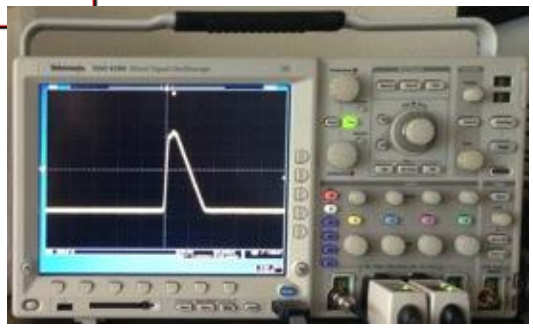



"Time stretcher" GHz → MHz

# Triggered Operation



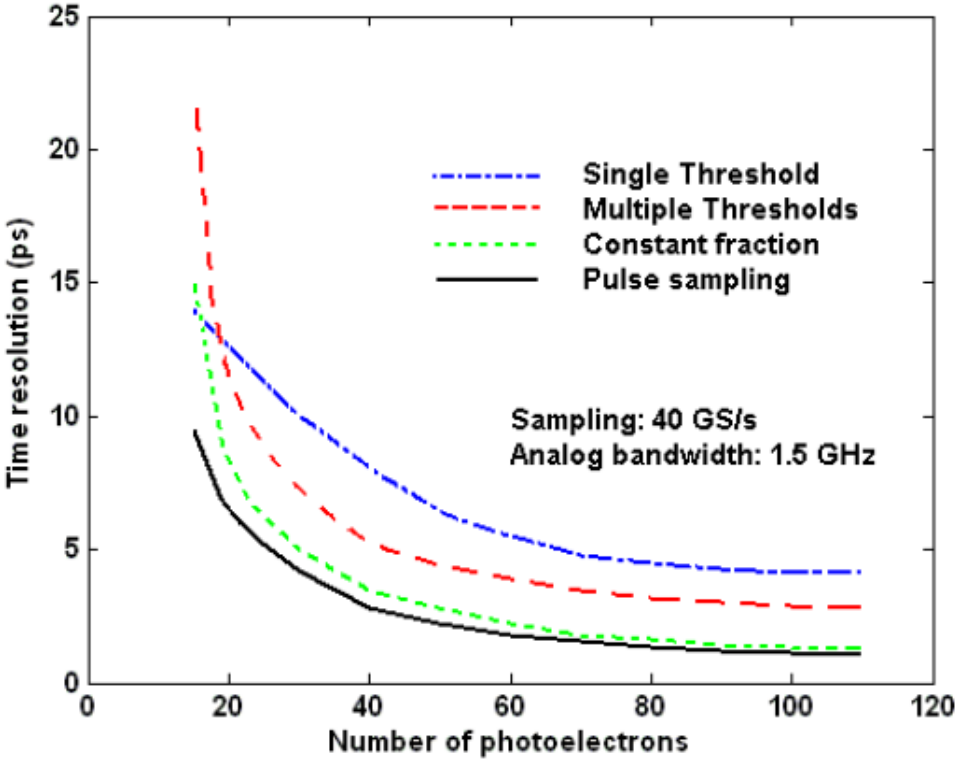

Dead time =
Conversion Time * Samples
(e.g. 30 ns · 100 = 3 μs)



Chips usually cannot sample during readout ⇒ "Dead Time"
Technique only works for "events" and "triggers"

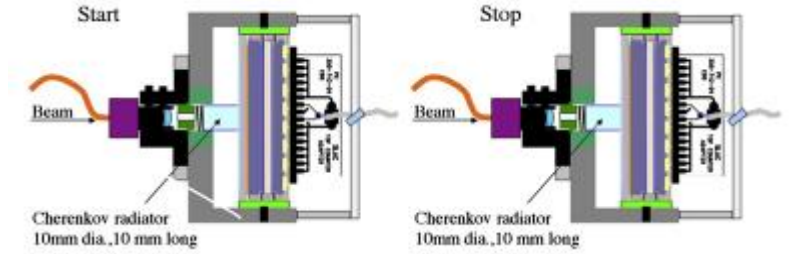
# How to measure best timing?

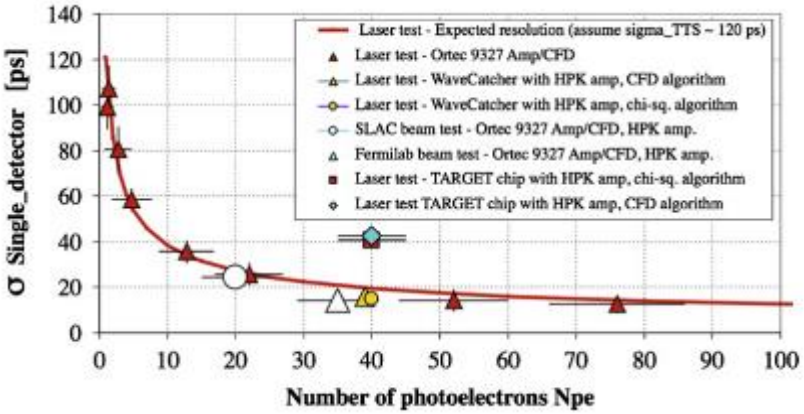
Simulation of MCP with realistic noise and different discriminators




J.-F. Genat et al., arXiv:0810.5590 (2008)

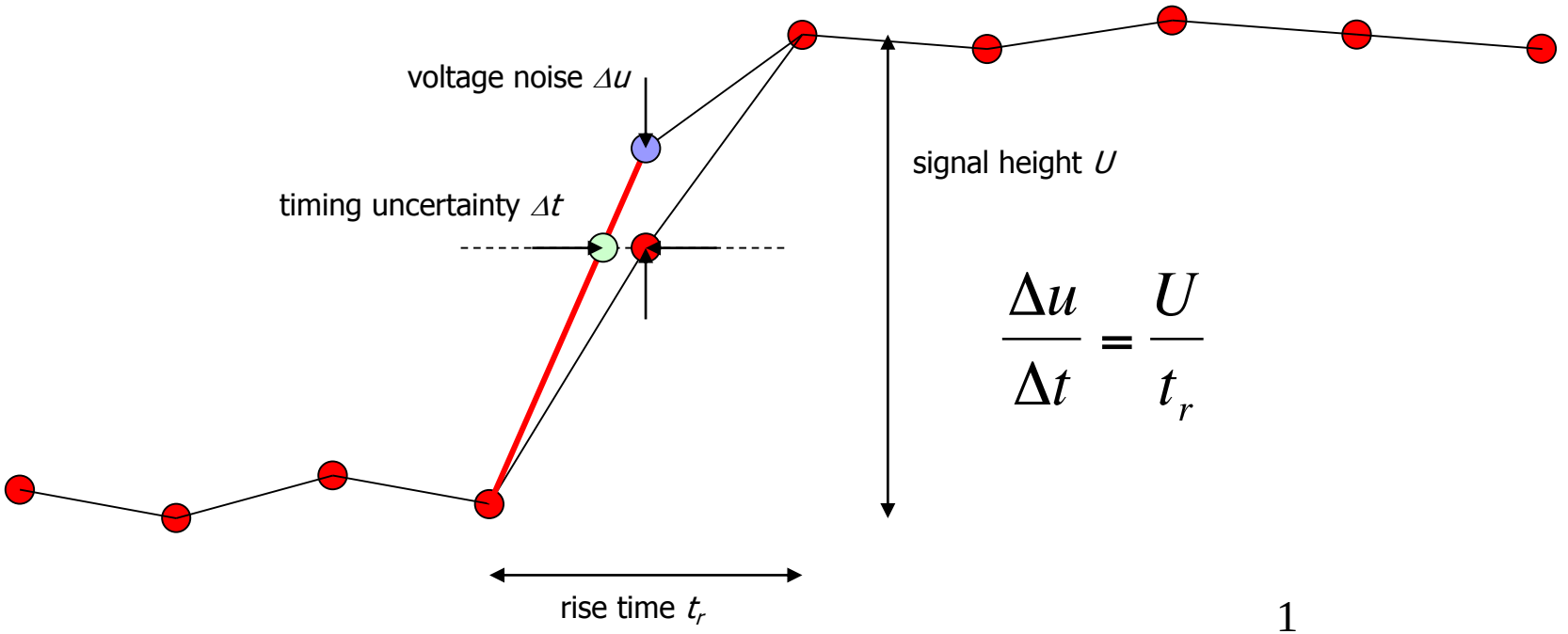
Beam measurement at SLAC & Fermilab




D. Breton et al., NIM **A629**, 123 (2011)

# How is timing resolution affected?




$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

number of samples on slope

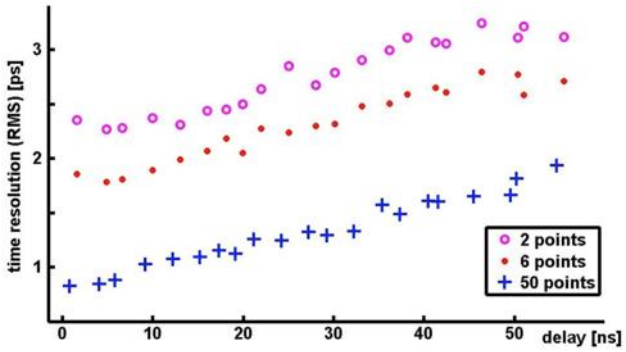
Simplified estimation!

# How is timing resolution affected?

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

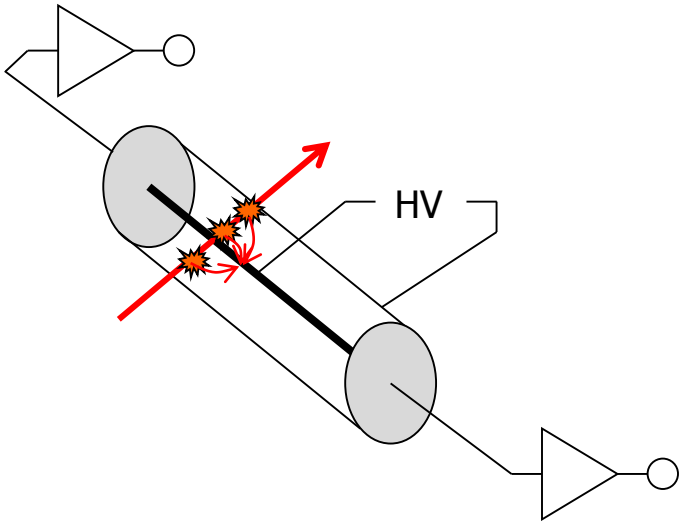
Assumes ideal sampling

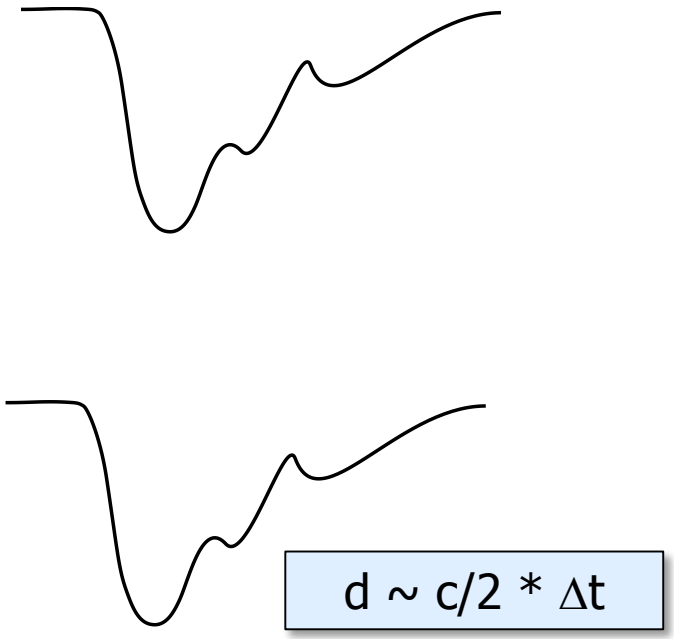
| | $U$ | $\Delta u$ | $f_s$ | $f_{3db}$ | $\Delta$t |
|---|---|---|---|---|---|
| today: | 100 mV | 1 mV | 2 GSPS | 300 MHz | ~10 ps |
| optimized SNR: | 1 V | 1 mV | 2 GSPS | 300 MHz | 1 ps |
| next generation: | 1 V | 1 mV | 10 GSPS | 3 GHz | 0.1 ps |




"Novel Calibration Method for Switched Capacitor Arrays Enables Time Measurements width Sub-Picosecond Resolution", D.A. Stricker-Shaver, S. Ritt, B.J. Pichler, IEEE **TNS 61** (2014), 3607

# Readout of Straw Tubes



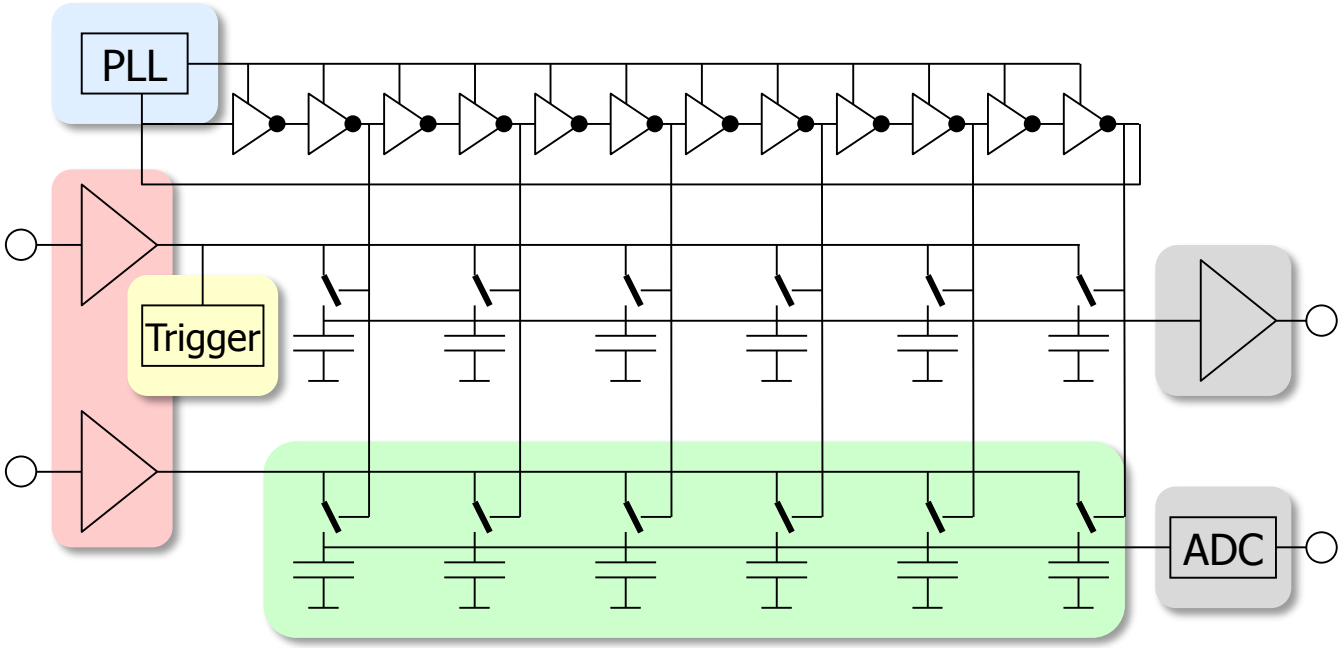



$d \sim c/2 * \Delta t$

- Readout of straw tubes or drift chambers usually with "charge sharing": 1-2 cm resolution
- Readout with fast timing: 10 ps / √10 = 3 ps → 0.5 mm
- Currently ongoing research project at PSI

# Design Options

- CMOS process (typically 0.35 … 0.13 μm) → sampling speed
- Number of channels, sampling depth, differential input
- PLL for frequency stabilization
- Input buffer or passive input
- Analog output or (Wilkinson) ADC
- Internal trigger
- Exact design of sampling cell



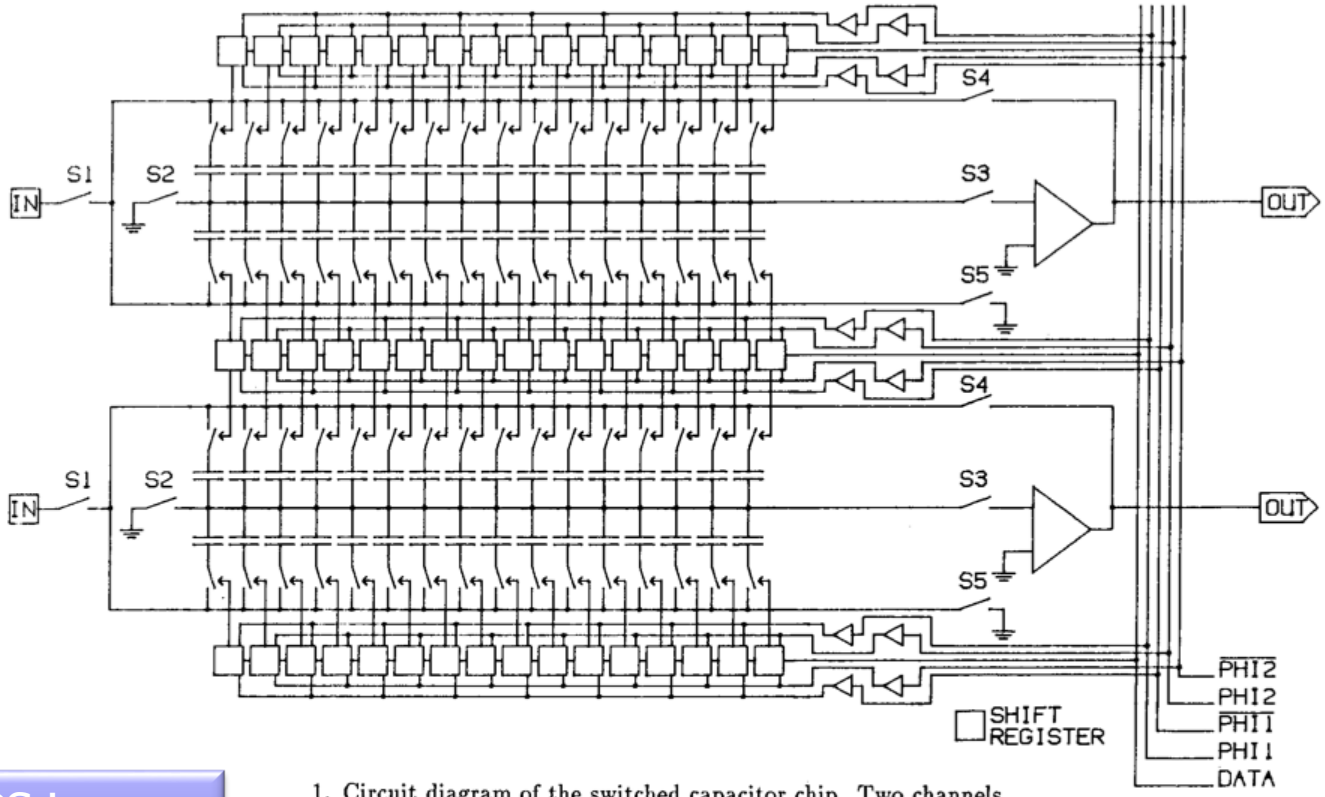
# First Switched Capacitor Arrays

DEVELOPMENT OF A SWITCHED CAPACITOR BASED MULTI-CHANNEL TRANSIENT WAVEFORM RECORDING INTEGRATED CIRCUIT

Stuart A. Kleinfelder

Lawrence Berkeley Laboratory
Berkeley, California 94720

IEEE Transactions on Nuclear Science, Vol. 35, No. 1, Feb. 1988




1. Circuit diagram of the switched capacitor chip. Two channels of 32 sample and hold cells per channel are shown. The I.C. contains 16 channels of 128 cells per channel.

50 MSPS in
3.5 μm CMOS process

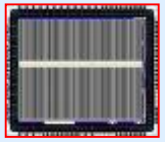
# Switched Capacitor Arrays for Particle Physics

G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

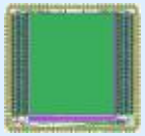
STRAW3 LABRADOR3 TARGET


- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube …)

**www.phys.hawaii.edu/~idlab/**

AFTER SAM NECTAR0




- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

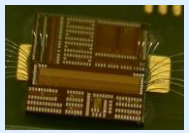
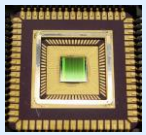
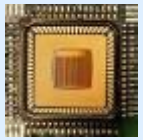
**matacq.free.fr**

PSEC1 - PSEC4

- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

**psec.uchicago.edu**

DRS1 DRS2 DRS3 DRS4


2002 2004 2007 2008

- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET

Poster 15, 106

SR
R. Dinapoli
PSI, Switzerland

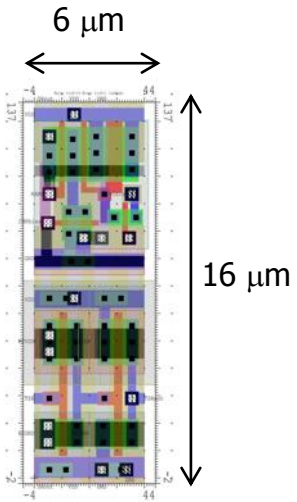
**drs.web.psi.ch**

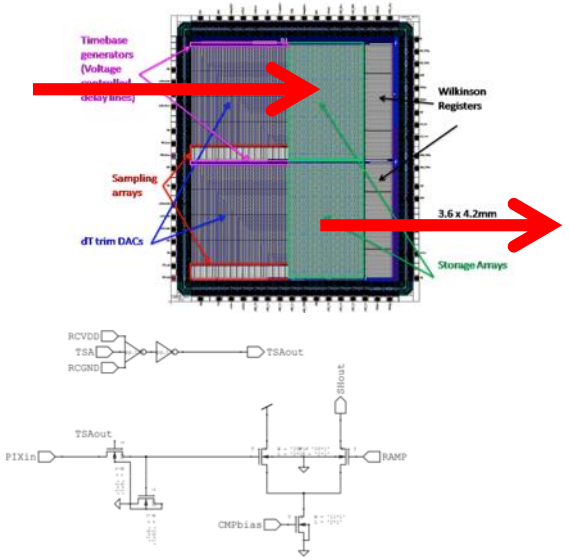
# Some specialities

- LAB Chip Family (G. Varner)
  - Deep buffer (BLAB Chip: 64k)
  - Double buffer readout (LAB4)
  - Wilkinson ADC

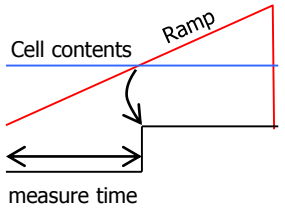
- NECTAR0 Chip (E. Delagnes)
  - Matrix layout (short inverter chain)
  - Input buffer (300-400 MHz)
  - Large storage cell (>12 bit SNR)
  - 20 MHz pipeline ADC on chip

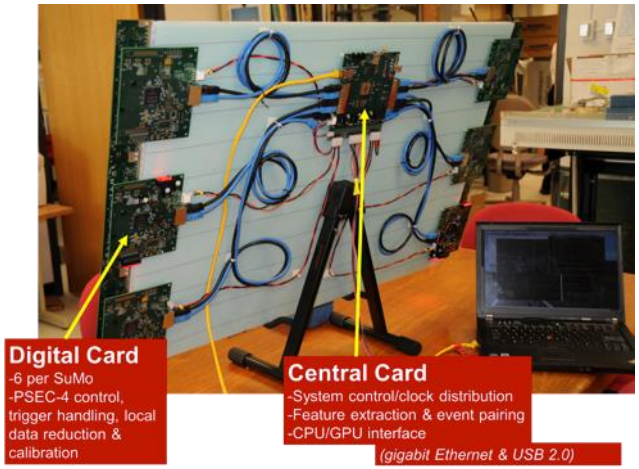
- PSEC4 Chip (E. Oberla, H. Grabas)
  - 15 GSPS
  - 1.6 GHz BW @ 256 cells
  - Wilkinson ADC

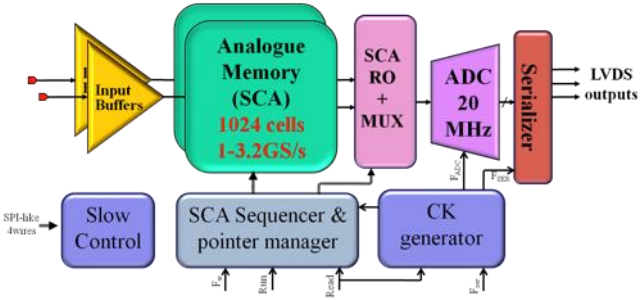


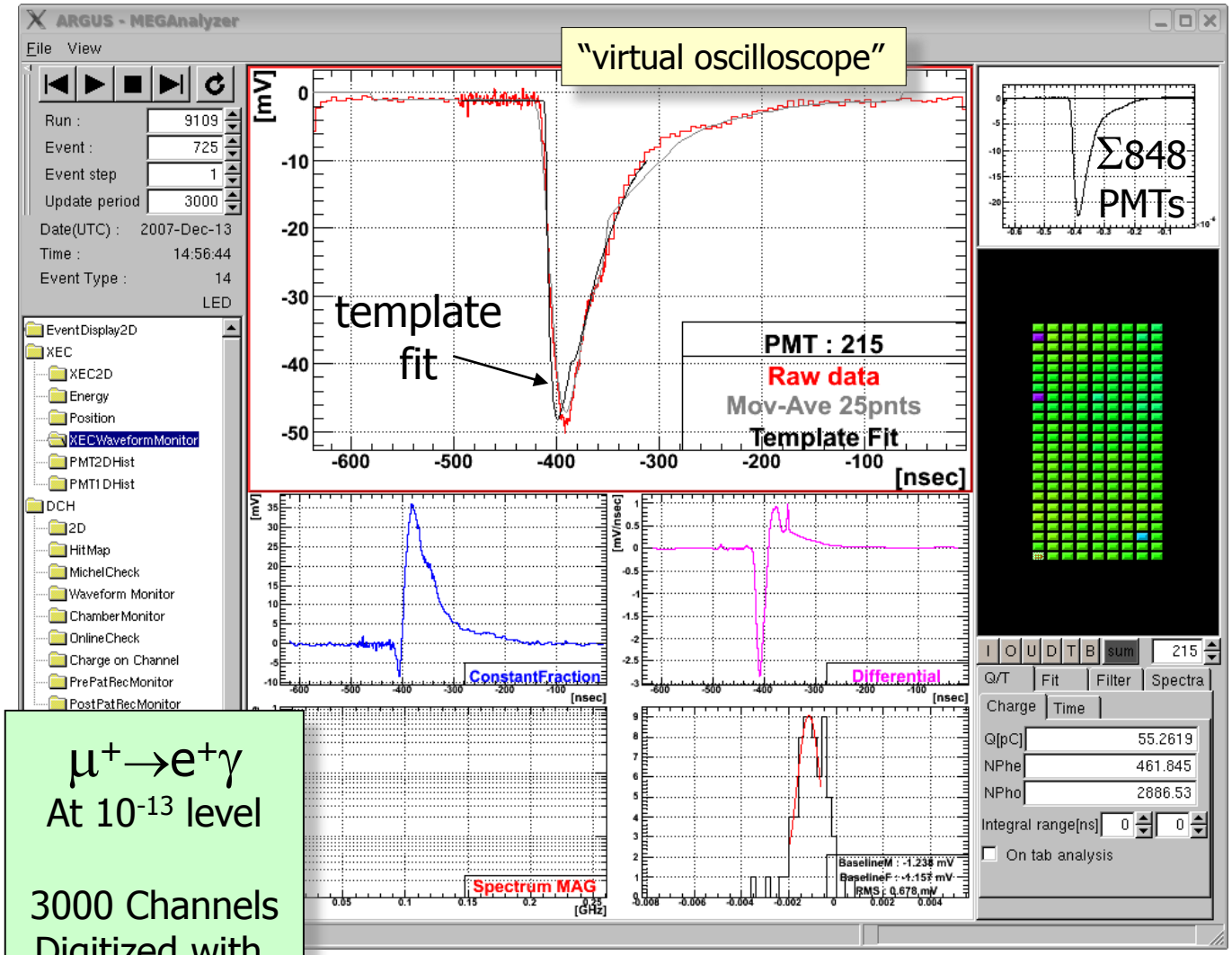

Wilkinson-ADC:

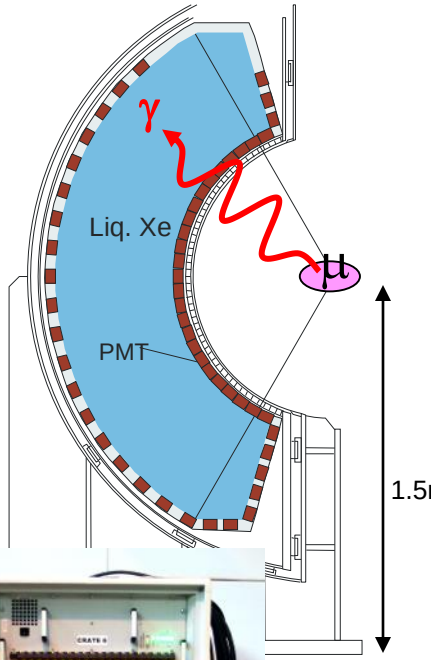


# MEG On-line waveform display



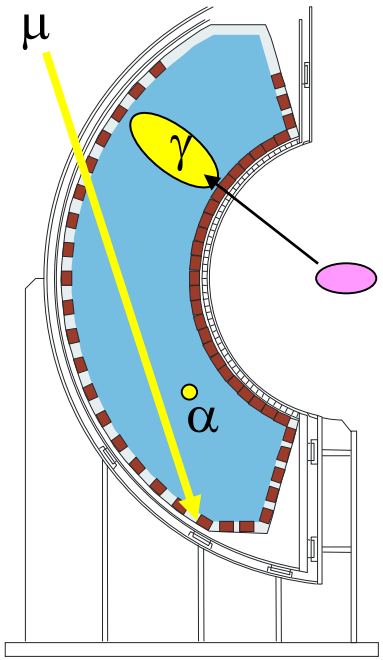


$\mu^+ \rightarrow e^+\gamma$
At $10^{-13}$ level

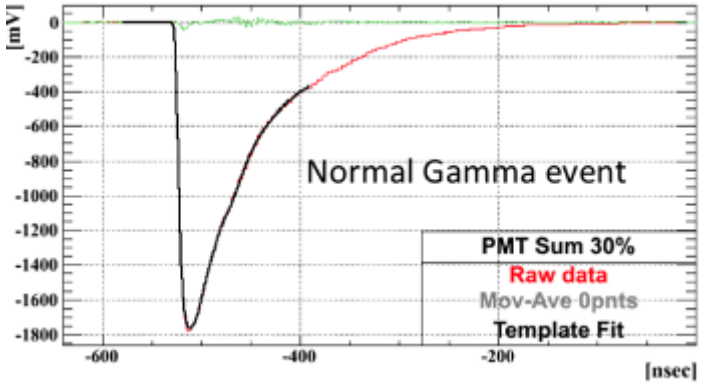
3000 Channels Digitized with **DRS4 chips** at 1.6 GSPS

Drawback: 400 TB data/year

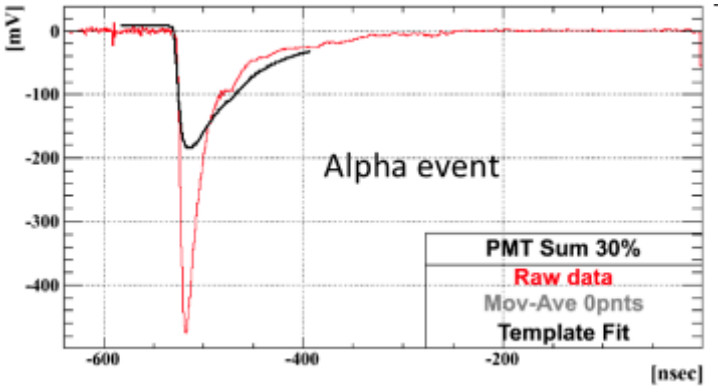
# Pulse shape discrimination



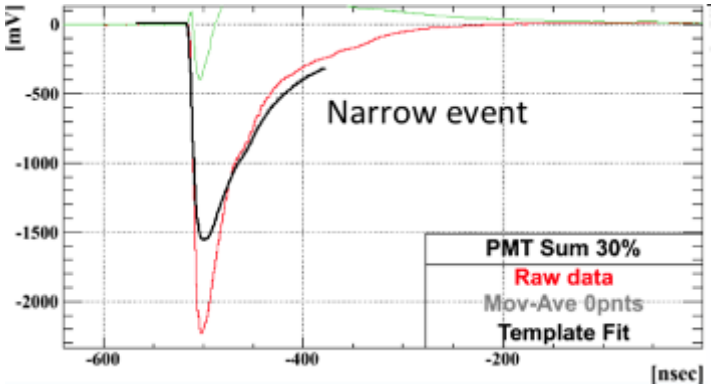

γ




α

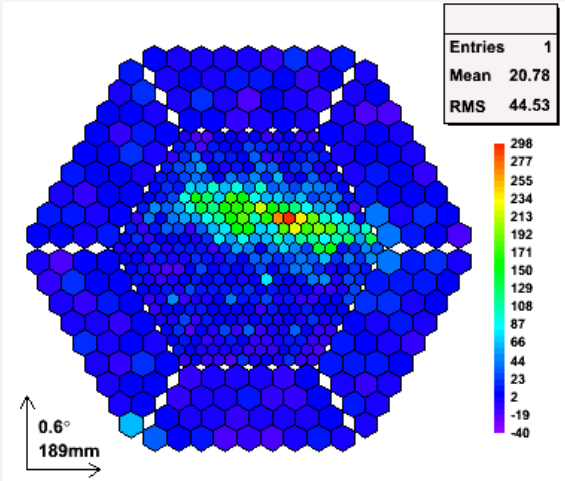


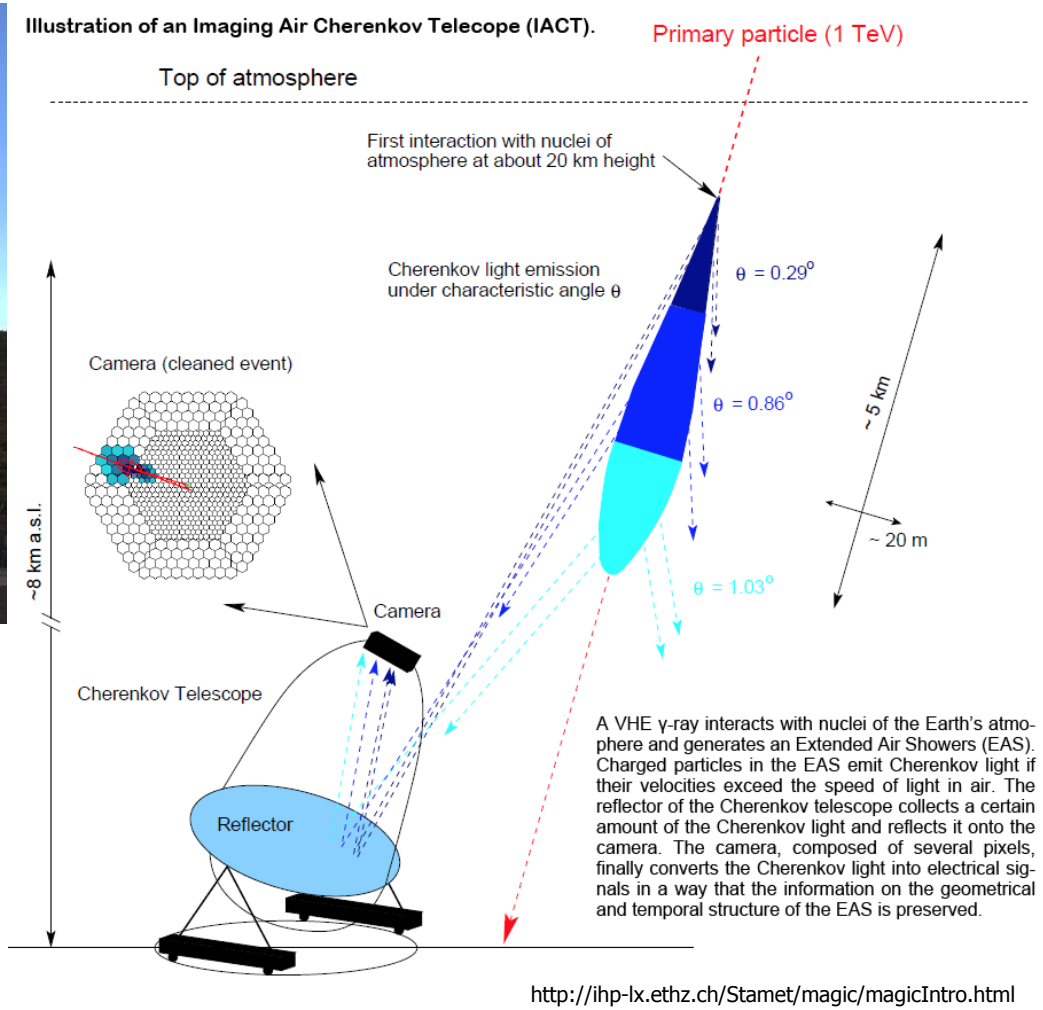

μ




Events found and correctly processed 2 years (!) after the were acquired

# MAGIC Telescope




http://ihp-lx.ethz.ch/Stamet/magic/magicIntro.html

La Palma, Canary Islands, Spain, 2200 m above sea level

https://wwwmagic.mpp.mpg.de/

# MAGIC Readout Electronics

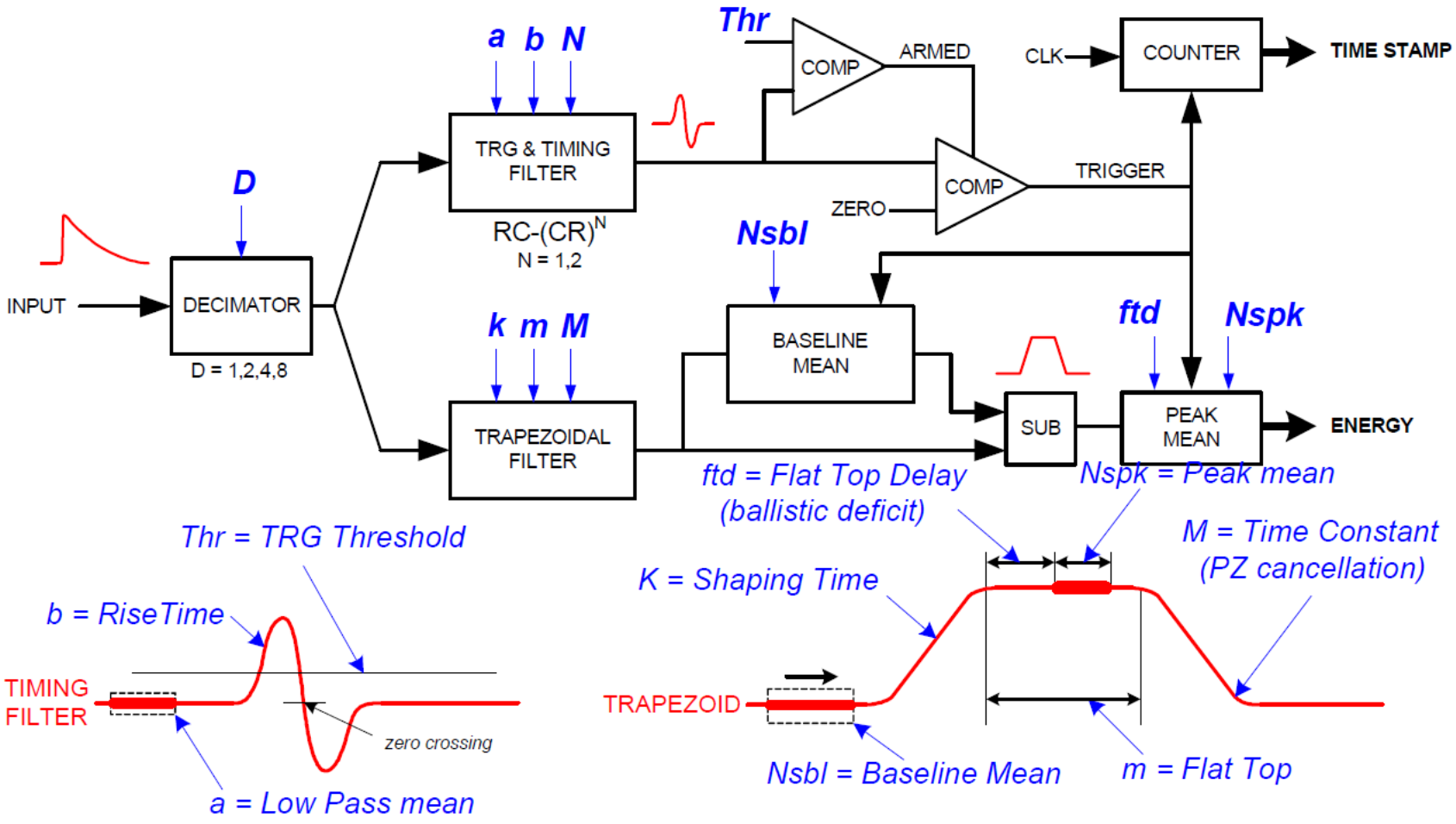
## Old system:

- 2 GHz flash (multiplexed)
- 512 channels
- Total of five racks, ~20 kW

## New system:

- 2 GHz SCA (DRS4 based)
- 2000 channels
- 4 VME crates
- Channel density 10x higher

# Digital Pulse Processing (DPP)

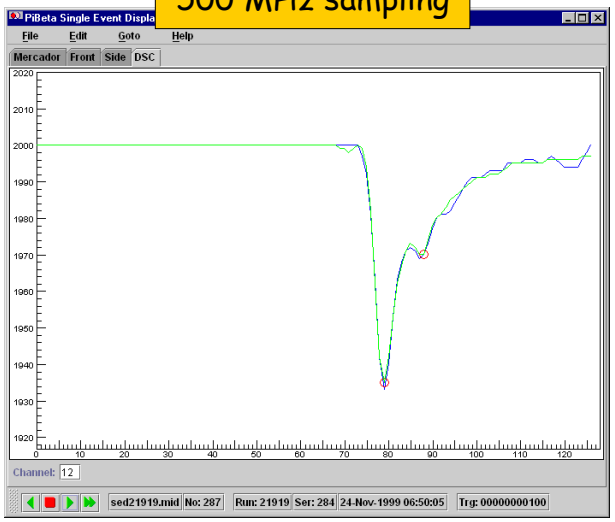



C. Tintori (CAEN)
V. Jordanov *et al.*, NIM **A353**, 261 (1994)

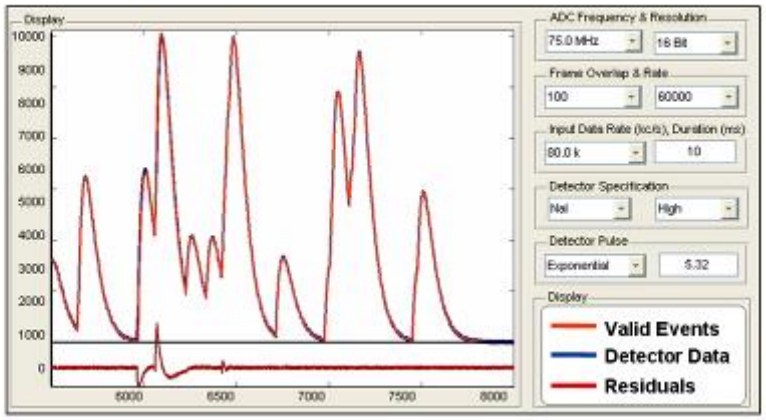
# Template Fit

- Determine "standard" PMT pulse by averaging over many events → "Template"
  - Find hit in waveform
  - Shift ("TDC") and scale ("ADC") template to hit
  - Minimize $\chi^2$
  - Compare fit with waveform
  - Repeat if above threshold
- Store ADC & TDC values

πβ Experiment
500 MHz sampling



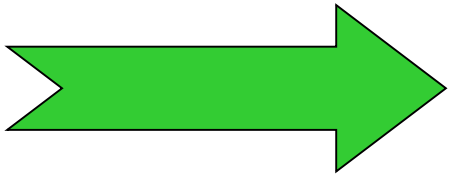

- At 1,000 kc/s less than 10% of events cannot be decoded.



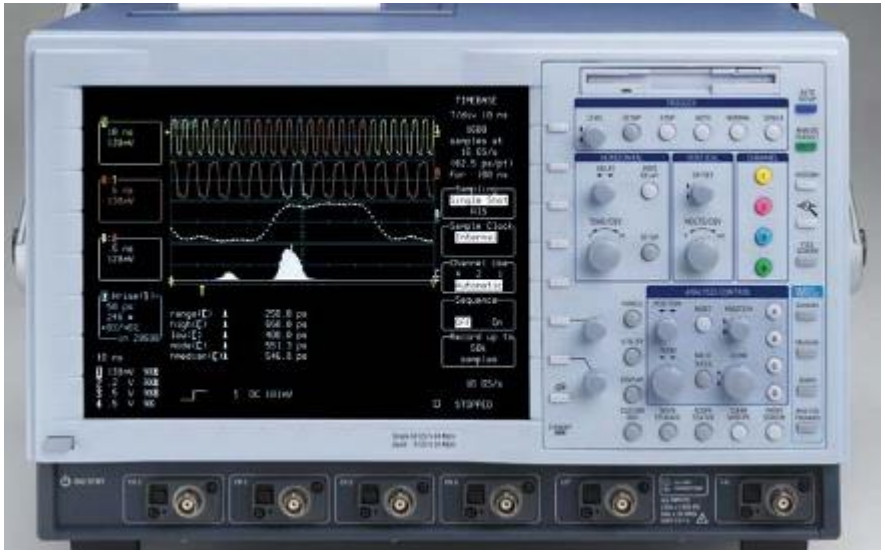

14 bit
60 MHz

# High speed USB oscilloscope

4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15 k€

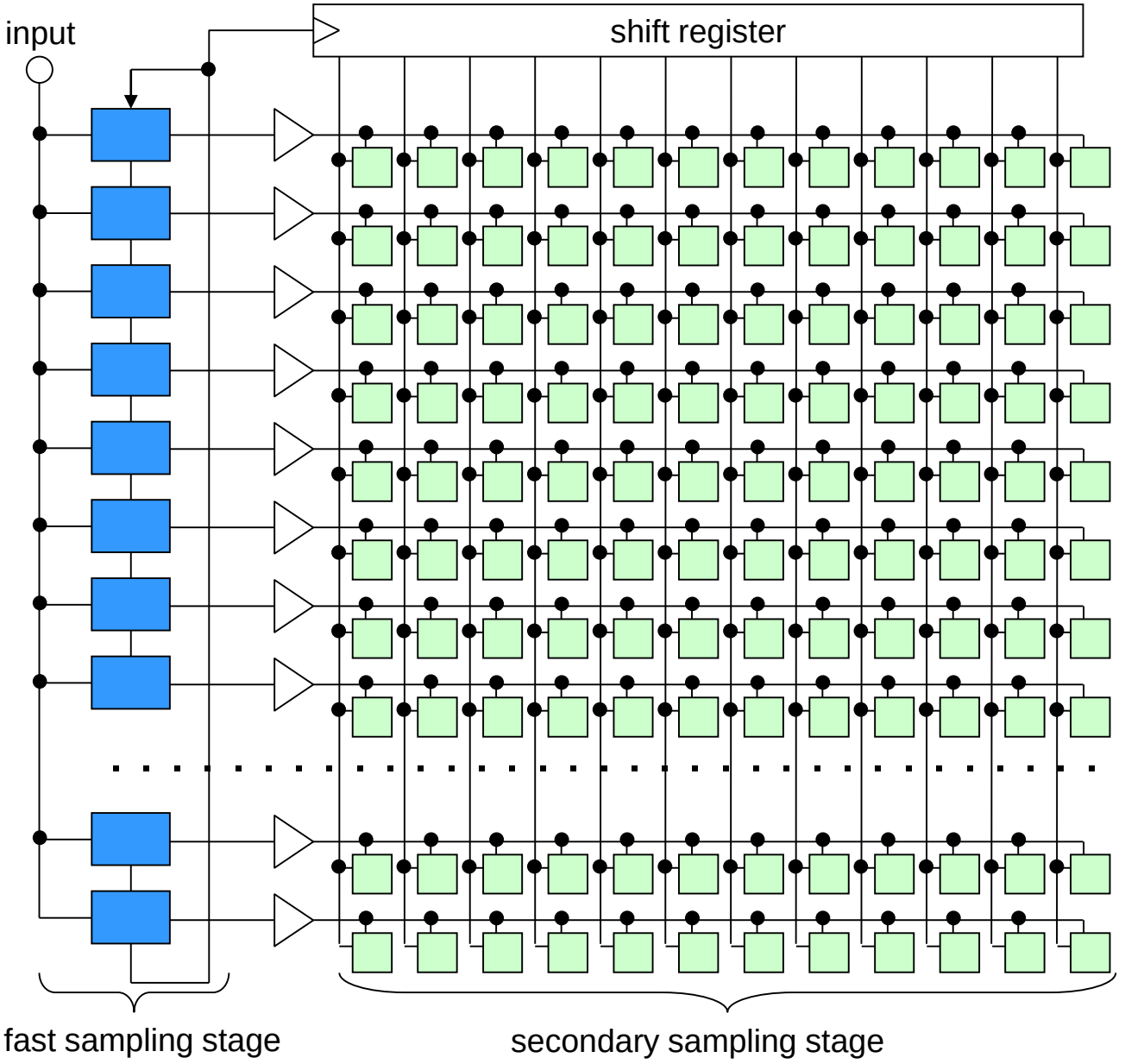


4 channels
5 GSPS
1 GHz BW
11.5 bits
1170 €
USB Power

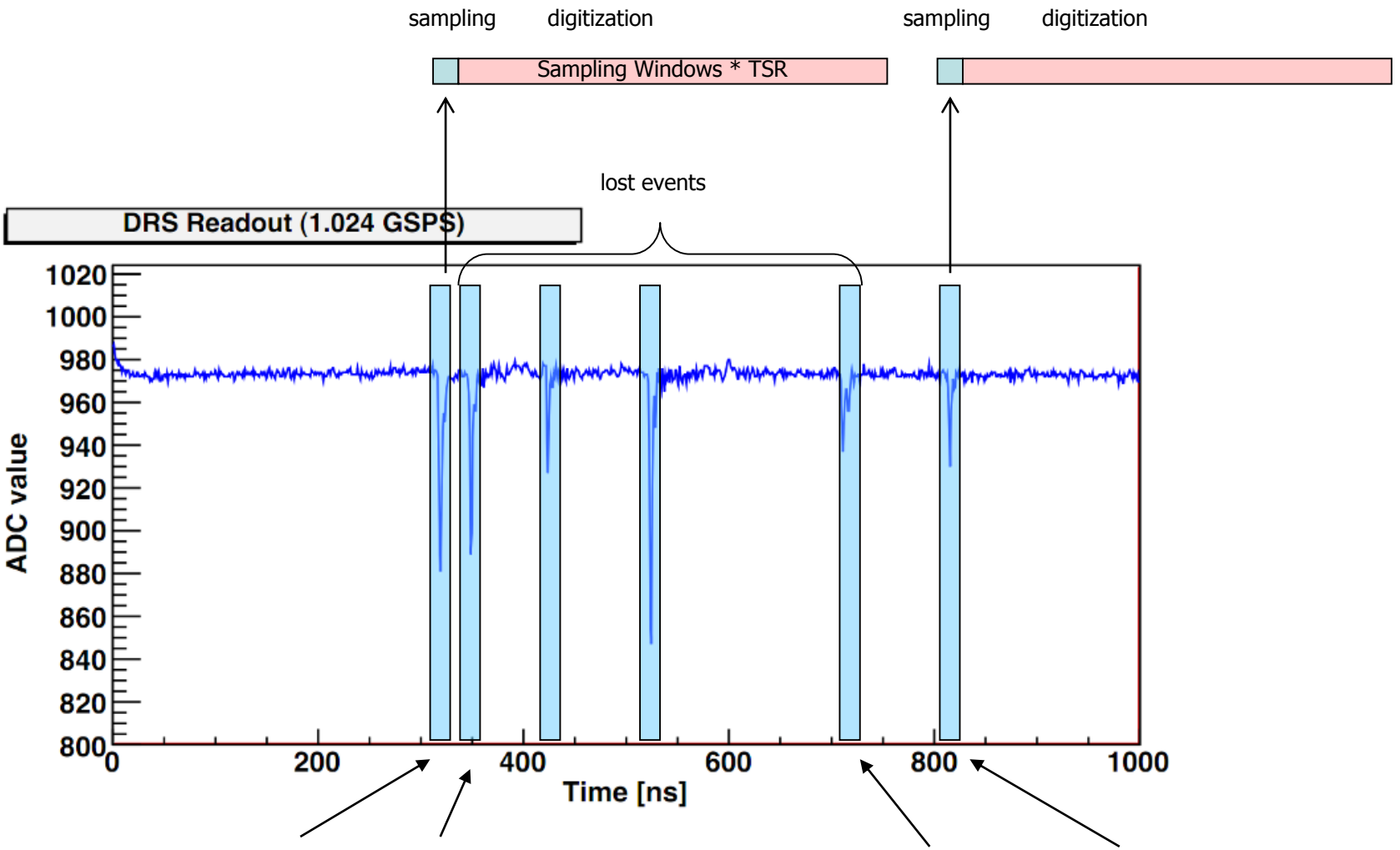


# Cascaded Switched Capacitor Arrays

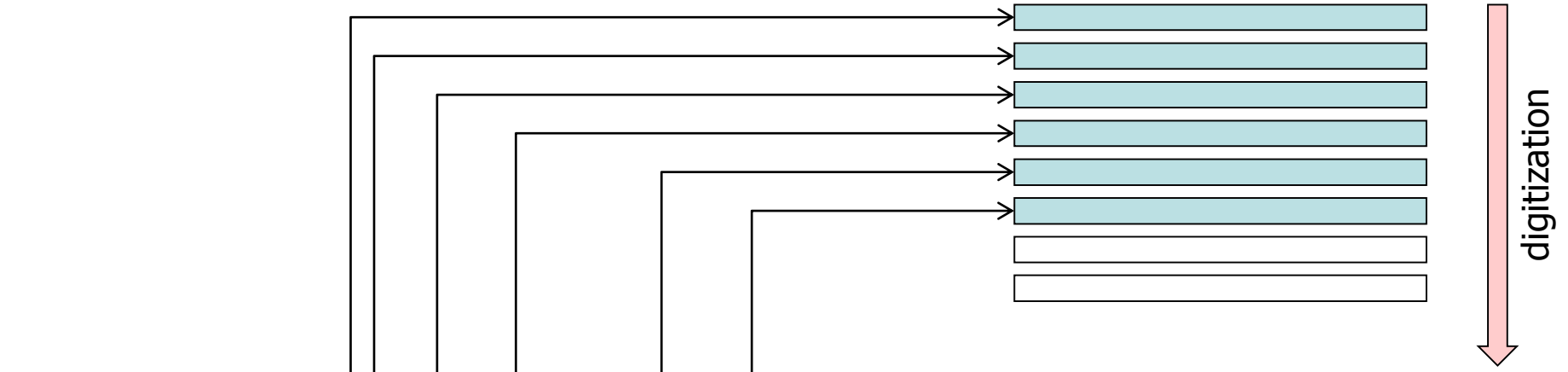
- 32 fast sampling cells (10 GSPS)
- 100 ps sample time, 3.1 ns hold time
- Hold time long enough to transfer voltage to secondary sampling stage with moderately fast buffer (300 MHz)
- Shift register gets clocked by inverter chain from fast sampling stage

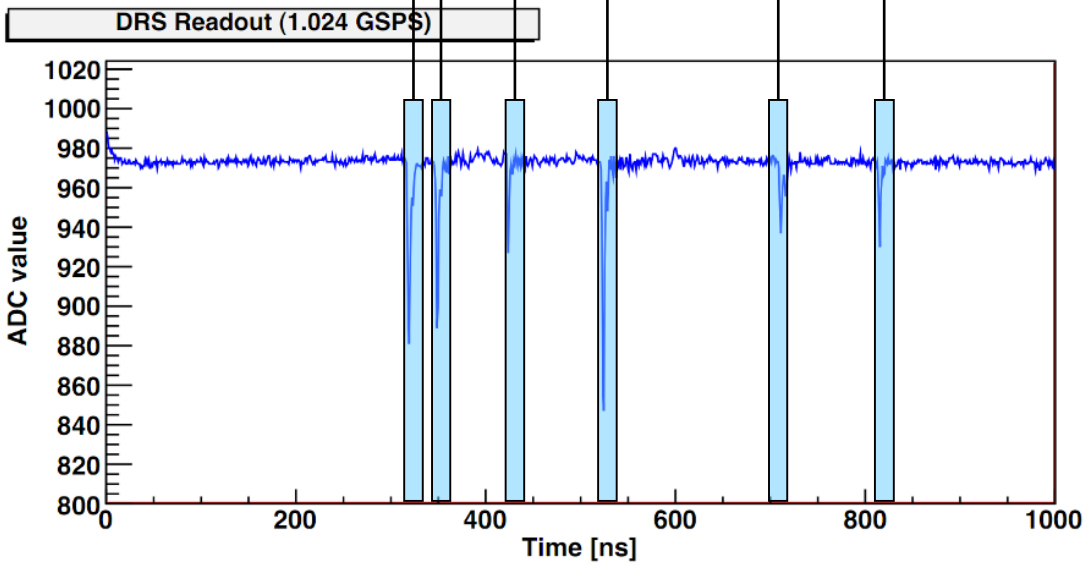


# The dead-time problem



# FIFO-type analog sampler



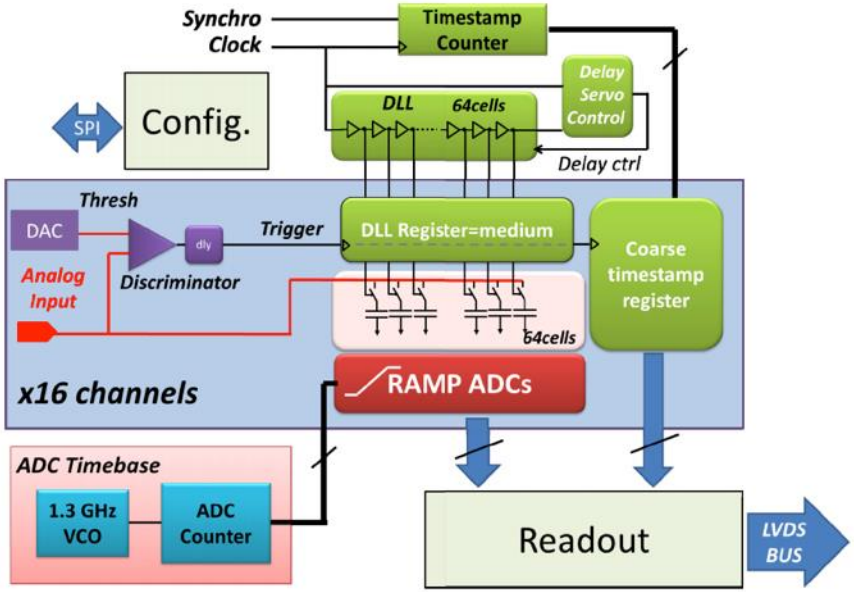




- FIFO sampler becomes immediately active after hit
- Samples are digitized asynchronously
- "De-randomization" of data
- Can work **dead-time less** up to average rate = 1/(window size * TSR)
- Example: 2 GSPS, 10 ns window size, TSR = 60 → rate up to **1.6 MHz**

# New chips

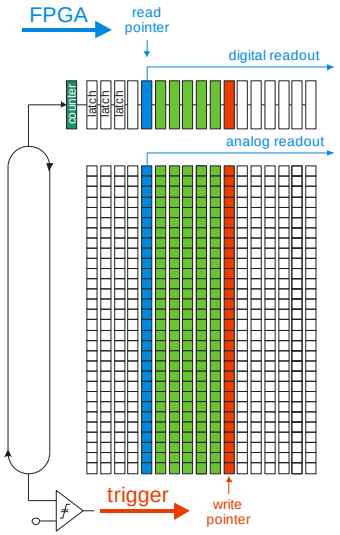
## CEA/Saclay

- SAMPIC Waveform TDC
- Record short (64 bins) waveforms
- Digitize on-chip
- Data-driven read out




## DRS5 (PSI, planned)

- Self-trigger writing of 128 short 32-bin segments (4096 bins total)
- Storage of 128 events
  - Accommodate long trigger latencies
  - Quasi dead time-free up to a few MHz,
  - Possibility to skip segments
    → second level trigger



# Summary

- Digitization is a key element of all particle physics experiments
- General trend to faster digitization and waveform analysis in digital domain (embedded CPUs, FPGAs)
- This talk can only give you a glimpse
- Further information
  - H. Spieler, "Semiconductor Detector Systems", Oxford Univ. Press, 2005
  - G. Knoll, "Radiation Detection and Measurement", Wiley, 2010
  - Conferences (with short courses):
    IEEE Realtime (Padova, Italy, June 2016)
    IEEE NSS-MIC (Strasbourg, France, Nov. 2016)
  - Become IEEE NPSS member

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