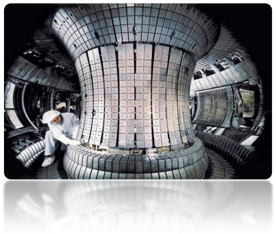
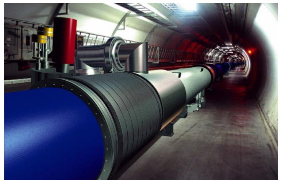
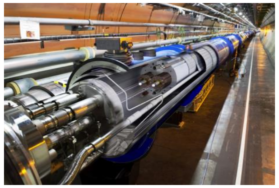
System Design Software Adapting COTS Technology for Scientific Applications for Global use



Eran Castiel, MS

NI Israel Big Physics
Segment Manager

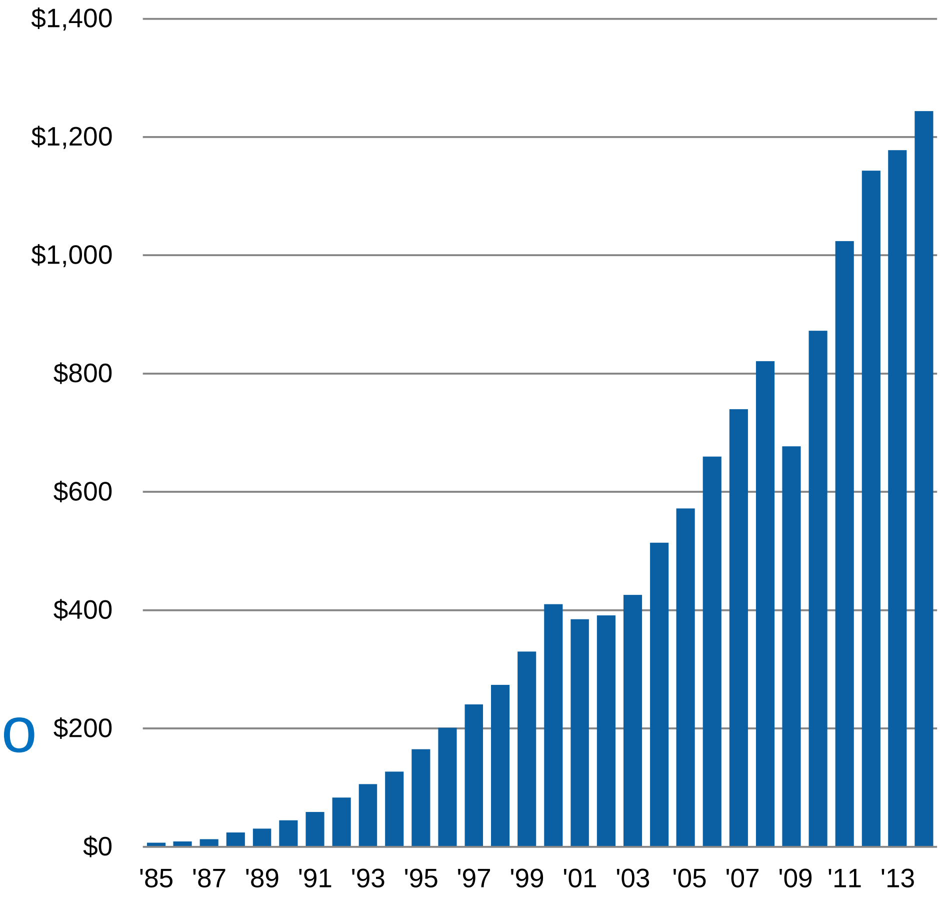
eran.castiel@ni.com

Agenda

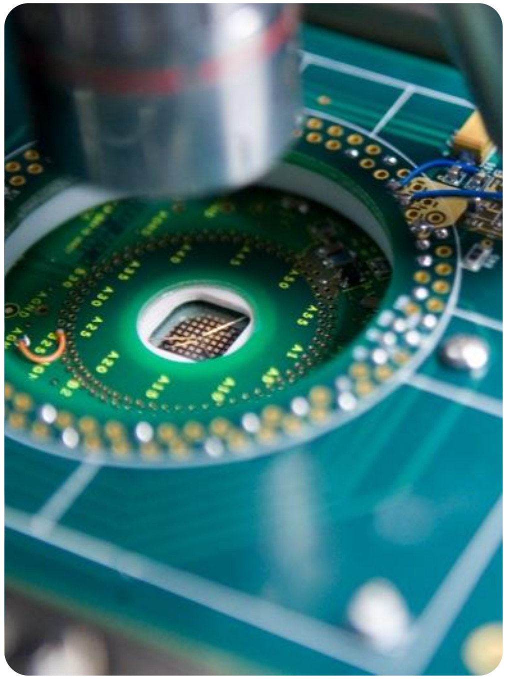
- Introduction to National Instruments (NI)
- Introduction to LabVIEW System Design Software
- Introduction to LabVIEW FPGA and RT
- Involvement in “Big Physics”
- Addressing Big Physics Application Requirements
    - Linux
    - EPICS
    - Radiation and Magnetic Field Testing
    - RASM
    - Lifecycle Management
    - Global Services
- Conclusions

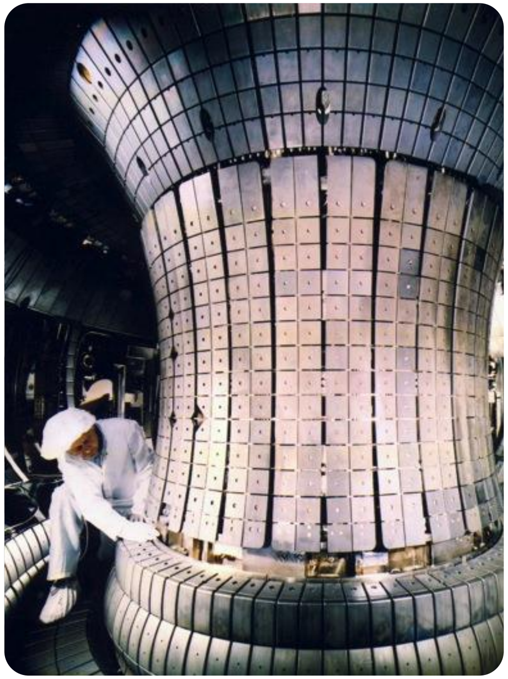
National Instruments Overview

- 35+ years of industry experience
- 1,700+ R&D engineers
- 600+ Field Engineers
- 200+ Application Engineers
- 700+ Alliance Partners
- Broad Customer Base with no industry >15% of revenue



Our Mission





We equip engineers and scientists with tools that accelerate productivity, innovation, and discovery.

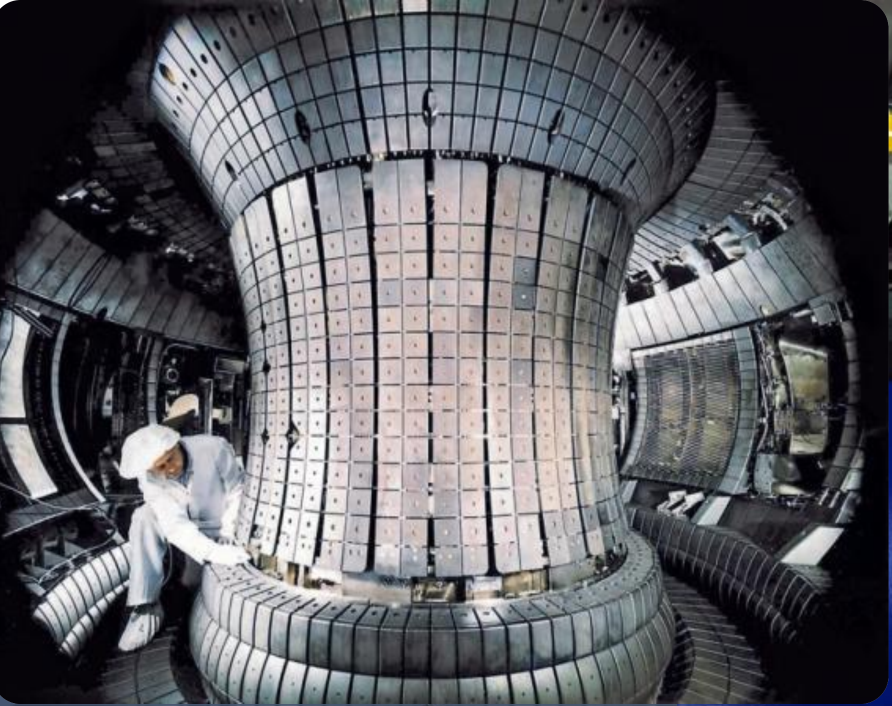
Technology, Innovation, and News
Scientific Research and Big Physics

NATIONAL INSTRUMENTS

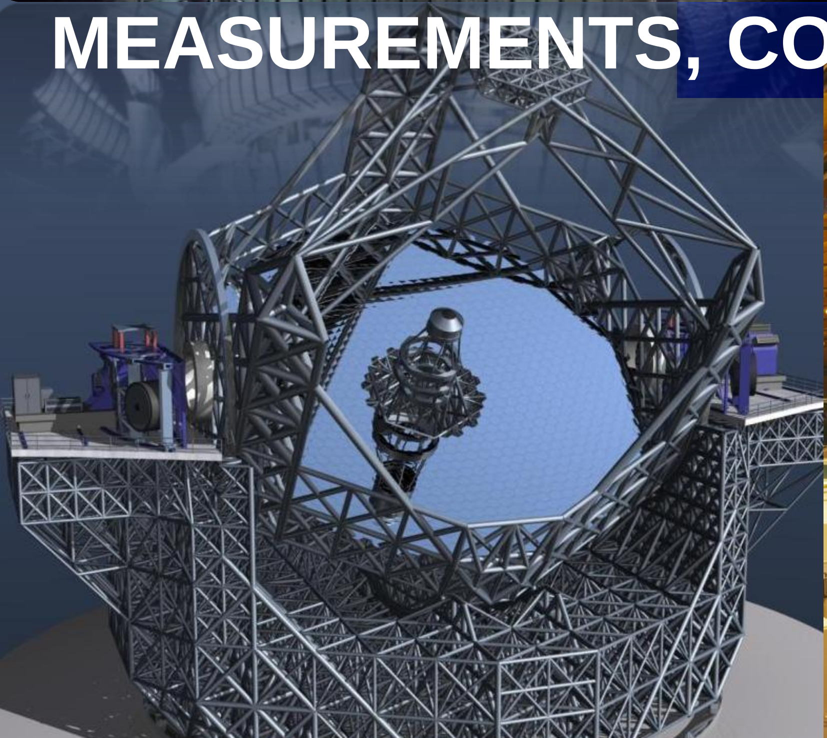
To Equip Engineers and Scientists

To Inspire Future Innovators

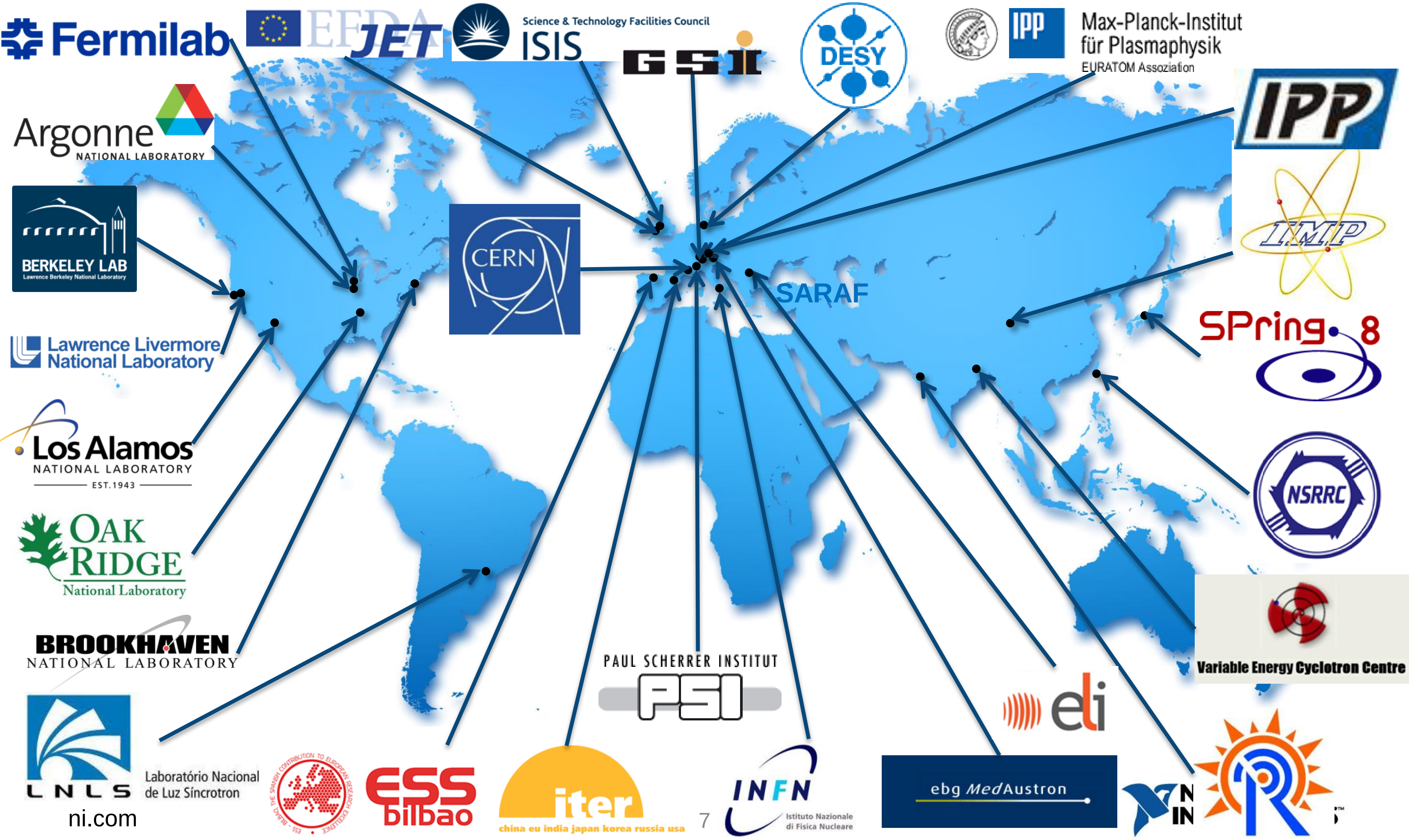
To Solve Grand Challenges



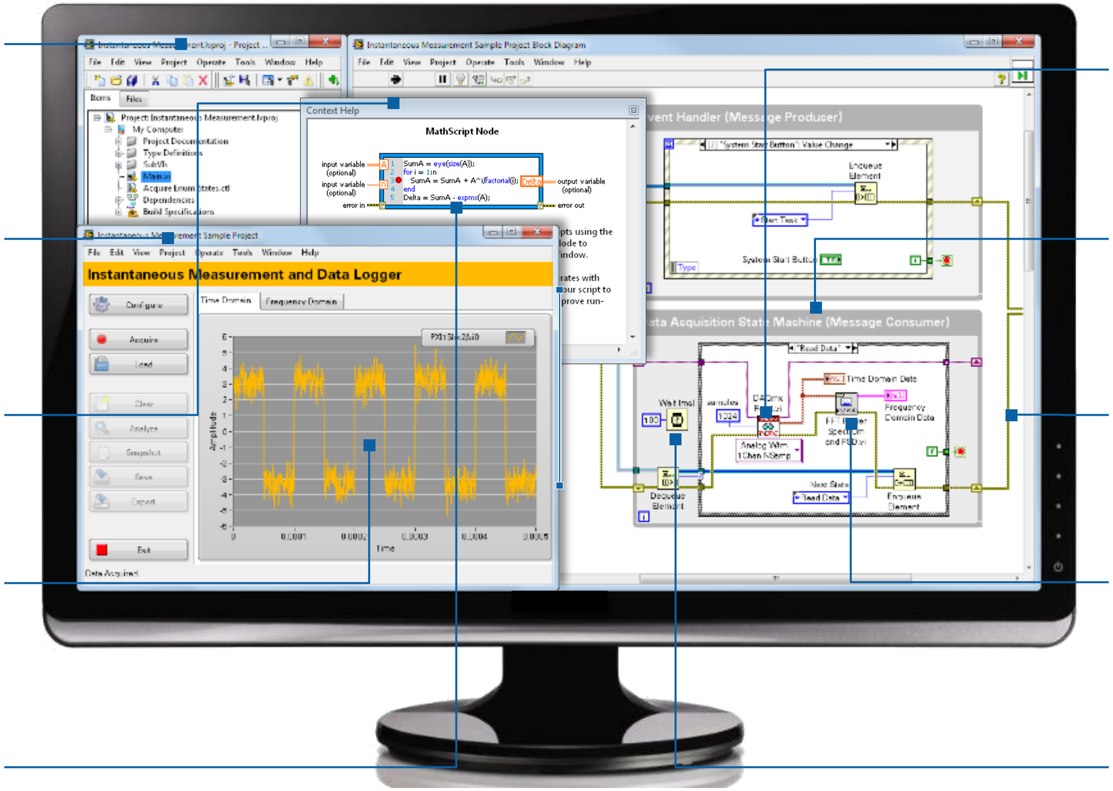
MEASUREMENTS, CONTROL AND DIAGNOSTICS



Worldwide Customers



LabVIEW System Design Software



```
SumA = eye(size(A));
for i = 1:n
  SumA = SumA + A^i/factorial(i);
end
Delta = SumA - expm(A);
```

Project Explorer
Manage and organize all system resources, including I/O and deployment targets

Deployment Targets
Deploy LabVIEW code to the leading desktop, real-time, and FPGA hardware targets

Instant Compilation
See the state of your application at all times, instantly

Front Panel
Create event-driven user interfaces to control systems and display measurements

Models of Computation
Combine and reuse .m files, C code, and HDL with graphical code

Hardware Connectivity
Bring real-world signals into LabVIEW from any I/O on any instrument

Parallel Programming
Create independent loops that automatically execute in parallel

Block Diagram
Define and customize the behavior of your system using graphical programming

Analysis Libraries
Use high-performance analysis libraries designed for engineering and science

Timing
Define explicit execution order and timing with sequential data flow

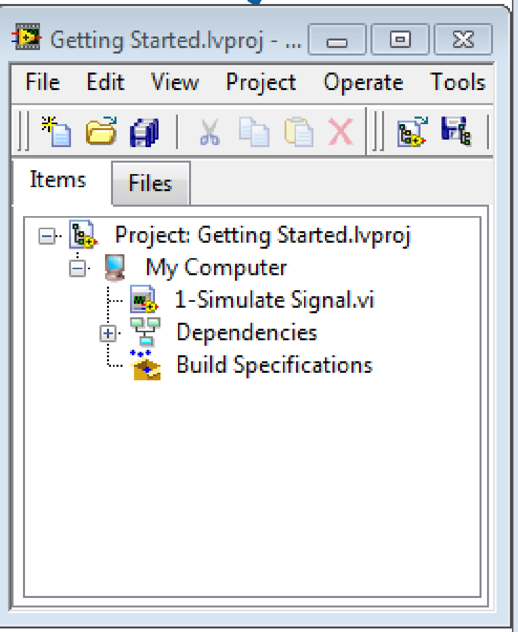
Accelerates Your Success

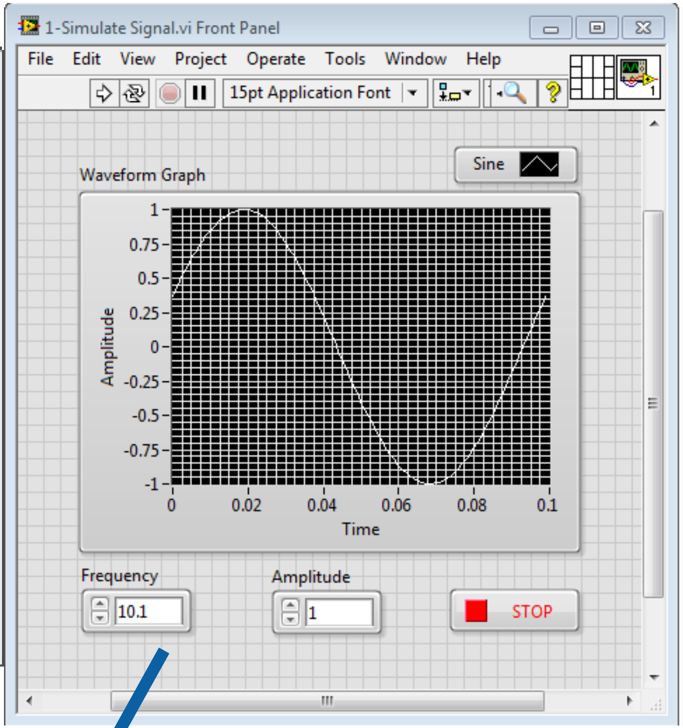
By abstracting low-level complexity and integrating all of the tools you need to build any measurement or control system

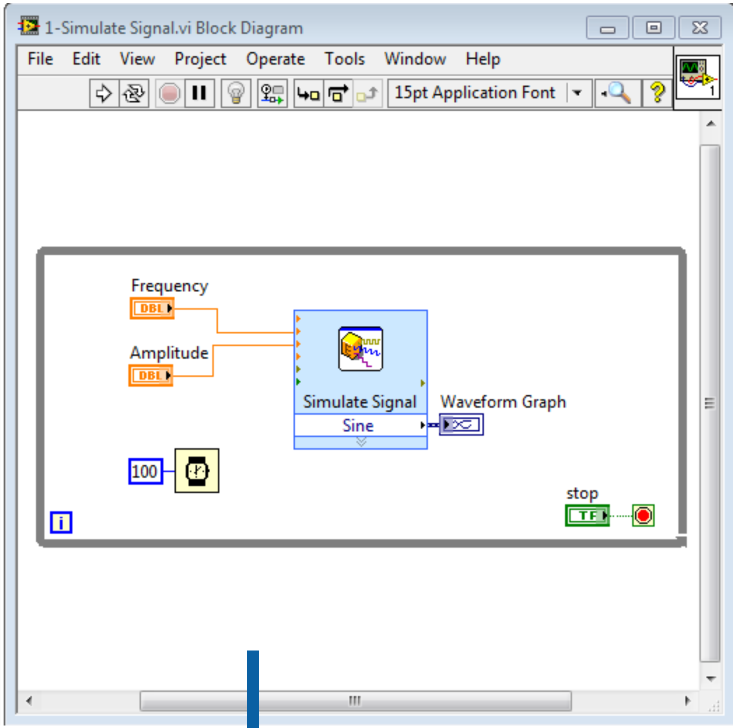
LabVIEW Environment Basics

“Project” = System Configuration

“VI” = Program or Function


Getting Started.lvproj - ...
File Edit View Project Operate Tools
Items
Files
Project: Getting Started.lvproj
My Computer
1-Simulate Signal.vi
Dependencies
Build Specifications





“Front Panel” = User Interface

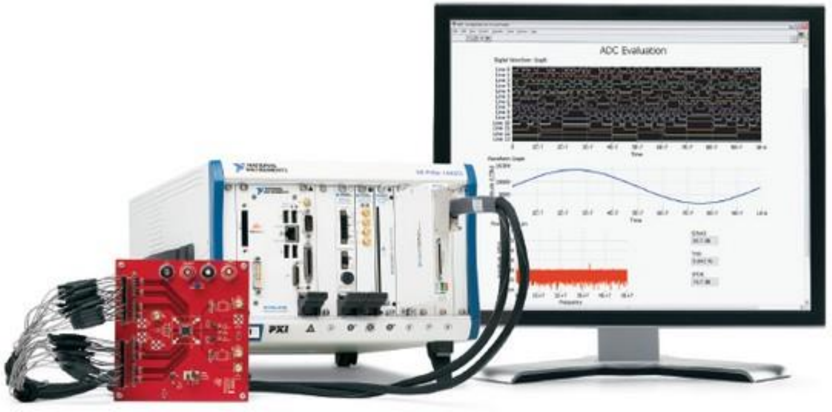
“Block Diagram” = Code

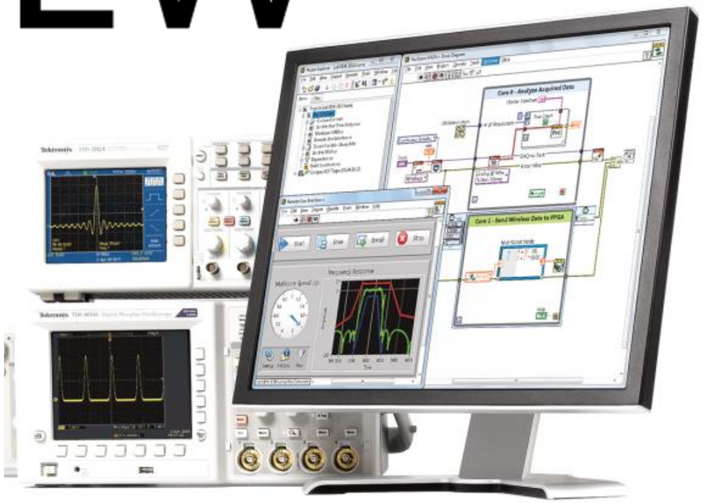
Extend Your LabVIEW Skills

RF

NATIONAL INSTRUMENTS

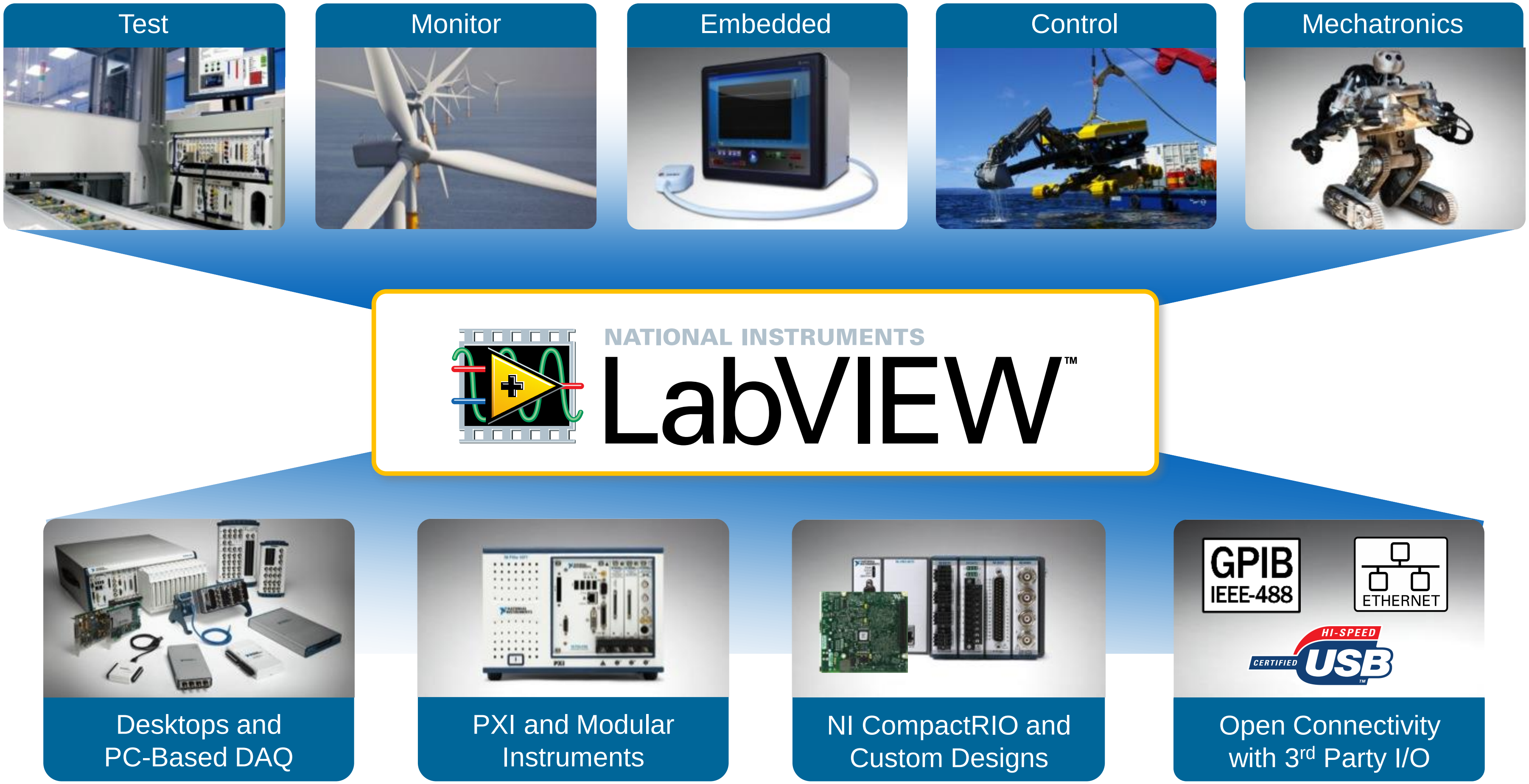
LabVIEW™





Graphical System Design

The Platform Approach to High-Performance Embedded Design



Test

Monitor

Embedded

Control

Mechatronics

NATIONAL INSTRUMENTS LabVIEW™

Desktops and PC-Based DAQ

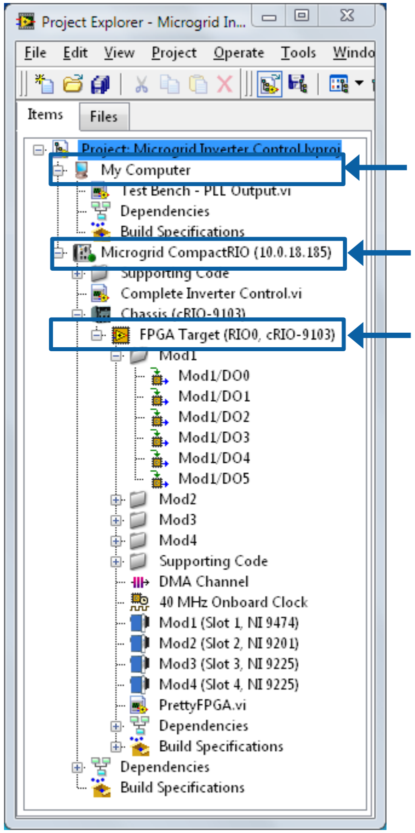
PXI and Modular Instruments

NI CompactRIO and Custom Designs

Open Connectivity with 3rd Party I/O

LabVIEW System Development Environment

Complete System IDE



- Project: Microgrid Inverter Control.lvproj
  - My Computer
    - Test Bench - PLL Output.vi
    - Dependencies
    - Build Specifications
  - Microgrid CompactRIO (10.0.18.185)
    - Supporting Code
    - Complete Inverter Control.vi
    - Chassis (cRIO-9103)
      - FPGA Target (RIO0, cRIO-9103)
        - Mod1
          - Mod1/DO0
          - Mod1/DO1
          - Mod1/DO2
          - Mod1/DO3
          - Mod1/DO4
          - Mod1/DO5
        - Mod2
        - Mod3
        - Mod4
        - Supporting Code
        - DMA Channel
        - 40 MHz Onboard Clock
        - Mod1 (Slot 1, NI 9474)
        - Mod2 (Slot 2, NI 9201)
        - Mod3 (Slot 3, NI 9225)
        - Mod4 (Slot 4, NI 9225)
        - PrettyFPGA.vi
        - Dependencies
        - Build Specifications
    - Dependencies
    - Build Specifications

← Windows + Desktop PC Application

← Real-Time OS + Processor Application

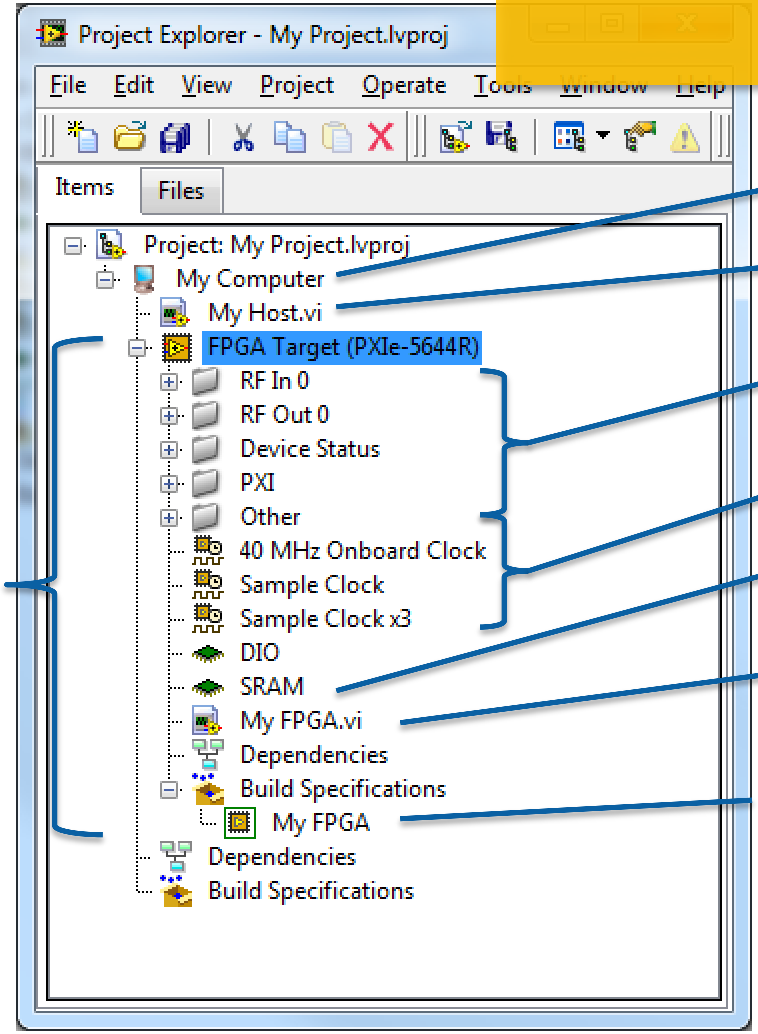
← FPGA Configuration/Application

System Design Tool

Graphical System Design

The LabVIEW Project

One environment for the FPGA, real-time embedded processor, desktop, HMIs, web services, and more…



Project Explorer - My Project.lvproj
File Edit View Project Operate Tools Window Help
Items
Files

```
Project: My Project.lvproj
  My Computer
    My Host.vi
    FPGA Target (PXIe-5644R)
      RF In 0
      RF Out 0
      Device Status
      PXI
      Other
      40 MHz Onboard Clock
      Sample Clock
      Sample Clock x3
      DIO
      SRAM
      My FPGA.vi
      Dependencies
      Build Specifications
        My FPGA
    Dependencies
    Build Specifications
```

FPGA Target

Host (RT/Win/Linux)

Interface code (CPU)

I/O and Synchronization

Clocks

DRAM Interface

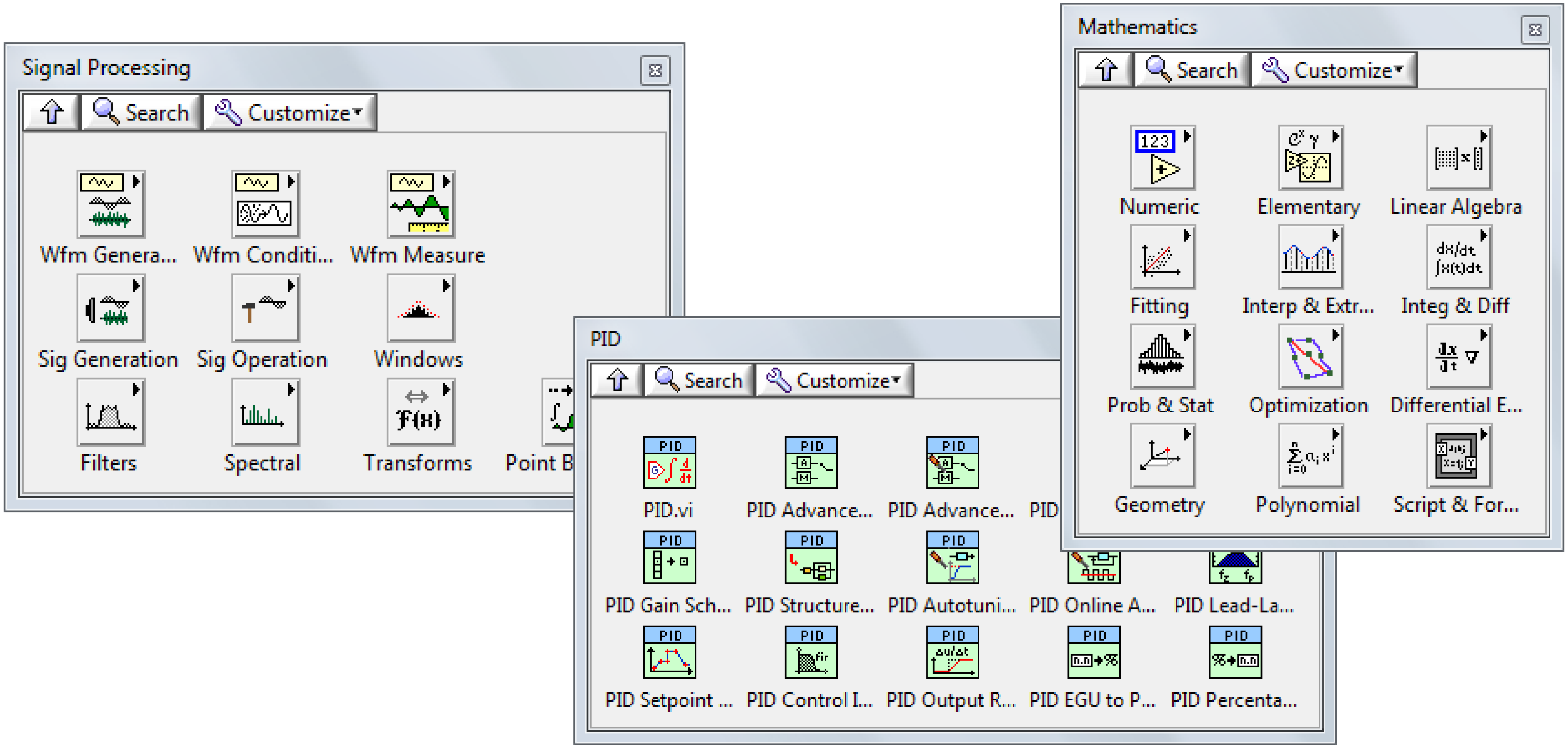
Top-level FPGA VI (compiled to bitstream)

Build settings (passed to Xilinx ISE tool chain)

LabVIEW System Development Environment

Complete System IDE

Math and Analysis

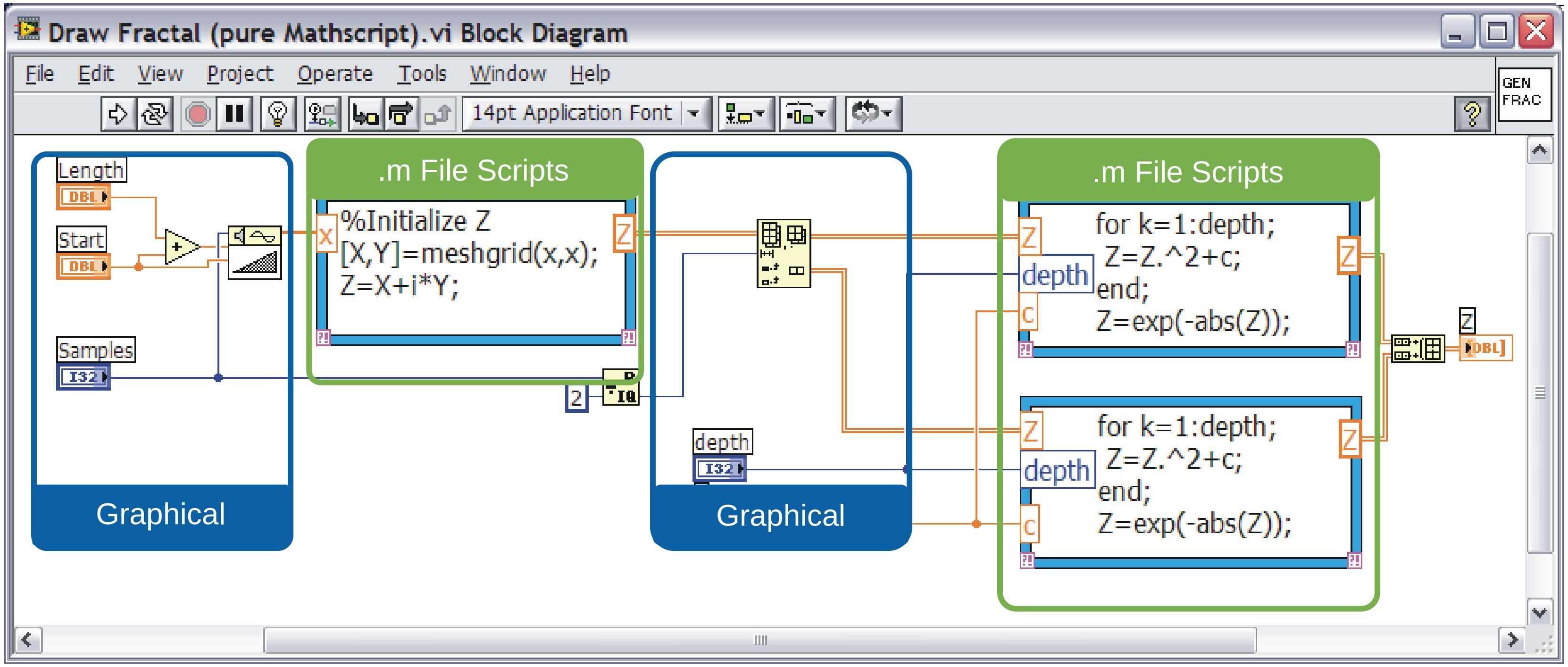


LabVIEW System Development Environment

Complete
System IDE

Math and
Analysis

Reuse of
Existing Code



```
%Initialize Z
[X,Y]=meshgrid(x,x);
Z=X+i*Y;
```

```
for k=1:depth;
 Z=Z.^2+c;
end;
Z=exp(-abs(Z));
```

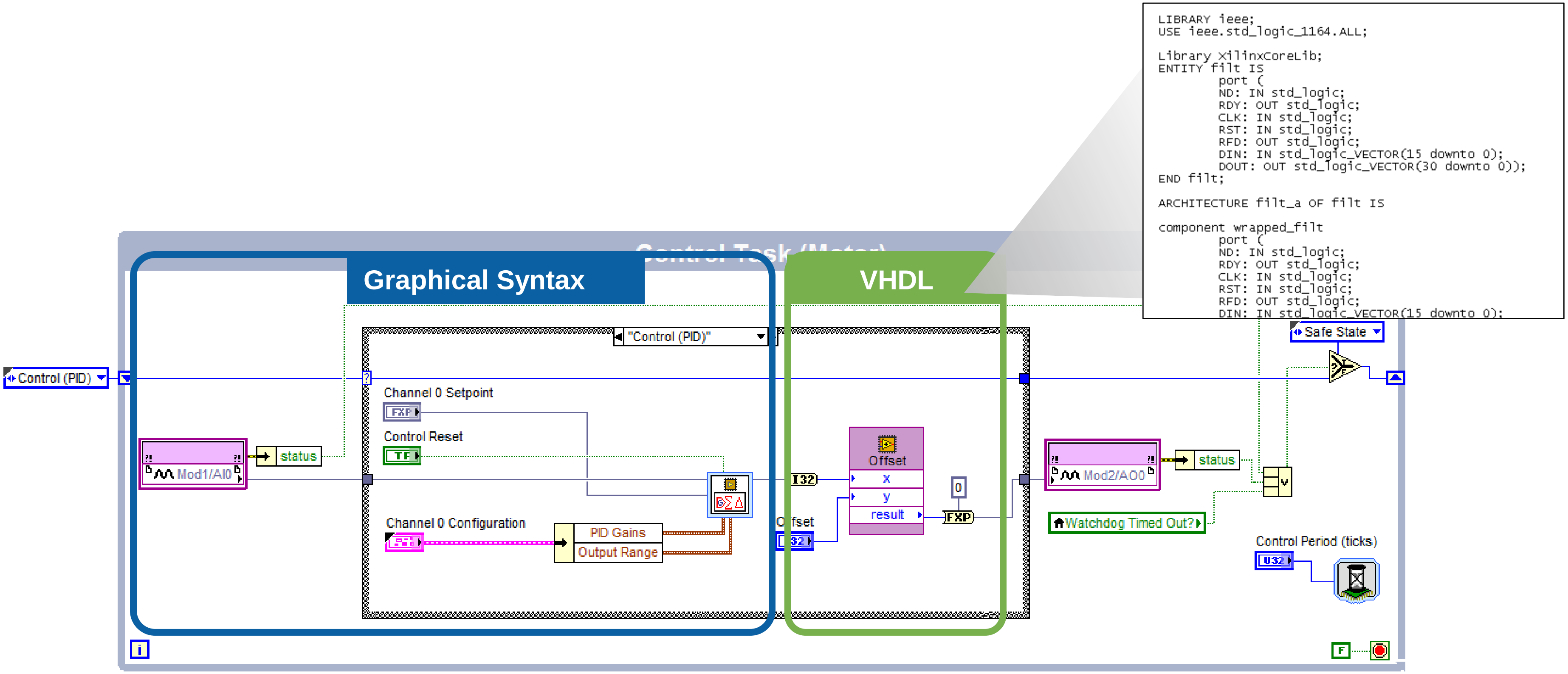
```
for k=1:depth;
 Z=Z.^2+c;
end;
Z=exp(-abs(Z));
```

LabVIEW System Development Environment

Complete System IDE

Math and Analysis

Reuse of Existing Code



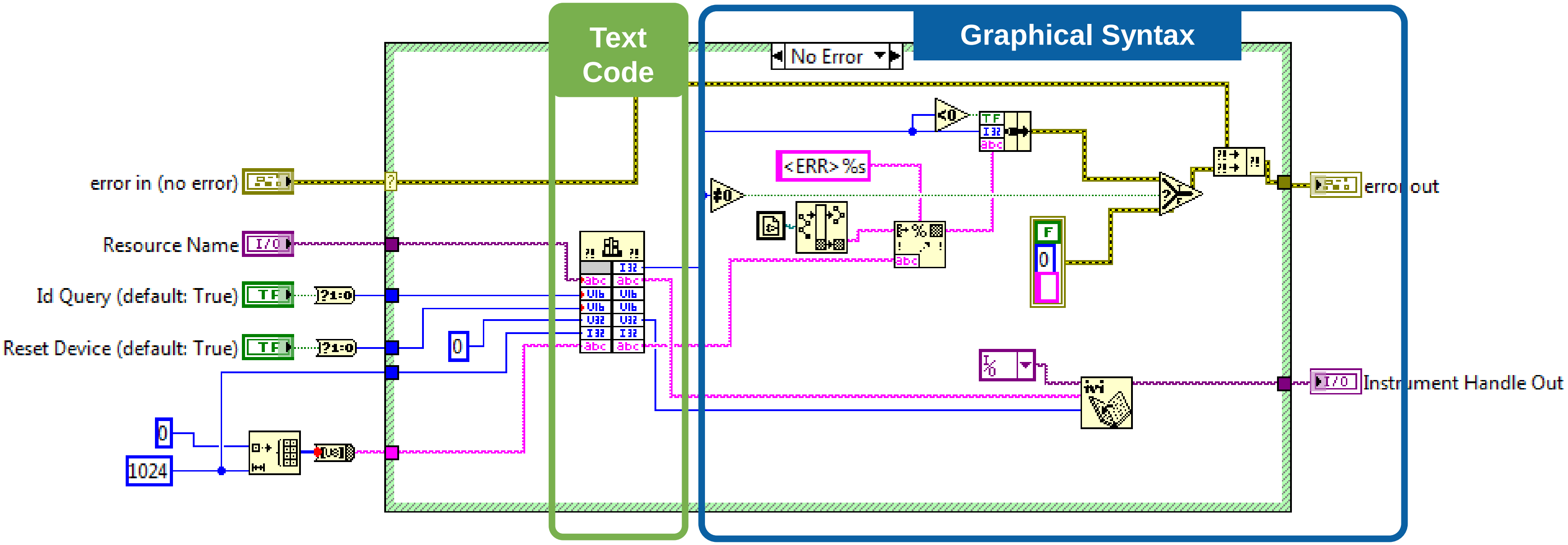
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

Library XilinxCoreLib;
ENTITY filt IS
        port (
        ND: IN std_logic;
        RDY: OUT std_logic;
        CLK: IN std_logic;
        RST: IN std_logic;
        RFD: OUT std_logic;
        DIN: IN std_logic_VECTOR(15 downto 0);
        DOUT: OUT std_logic_VECTOR(30 downto 0));
END filt;

ARCHITECTURE filt_a OF filt IS

component wrapped_filt
        port (
        ND: IN std_logic;
        RDY: OUT std_logic;
        CLK: IN std_logic;
        RST: IN std_logic;
        RFD: OUT std_logic;
        DIN: IN std_logic_VECTOR(15 downto 0);
```

LabVIEW System Development Environment

Complete System IDE

Math and Analysis

Reuse of Existing Code



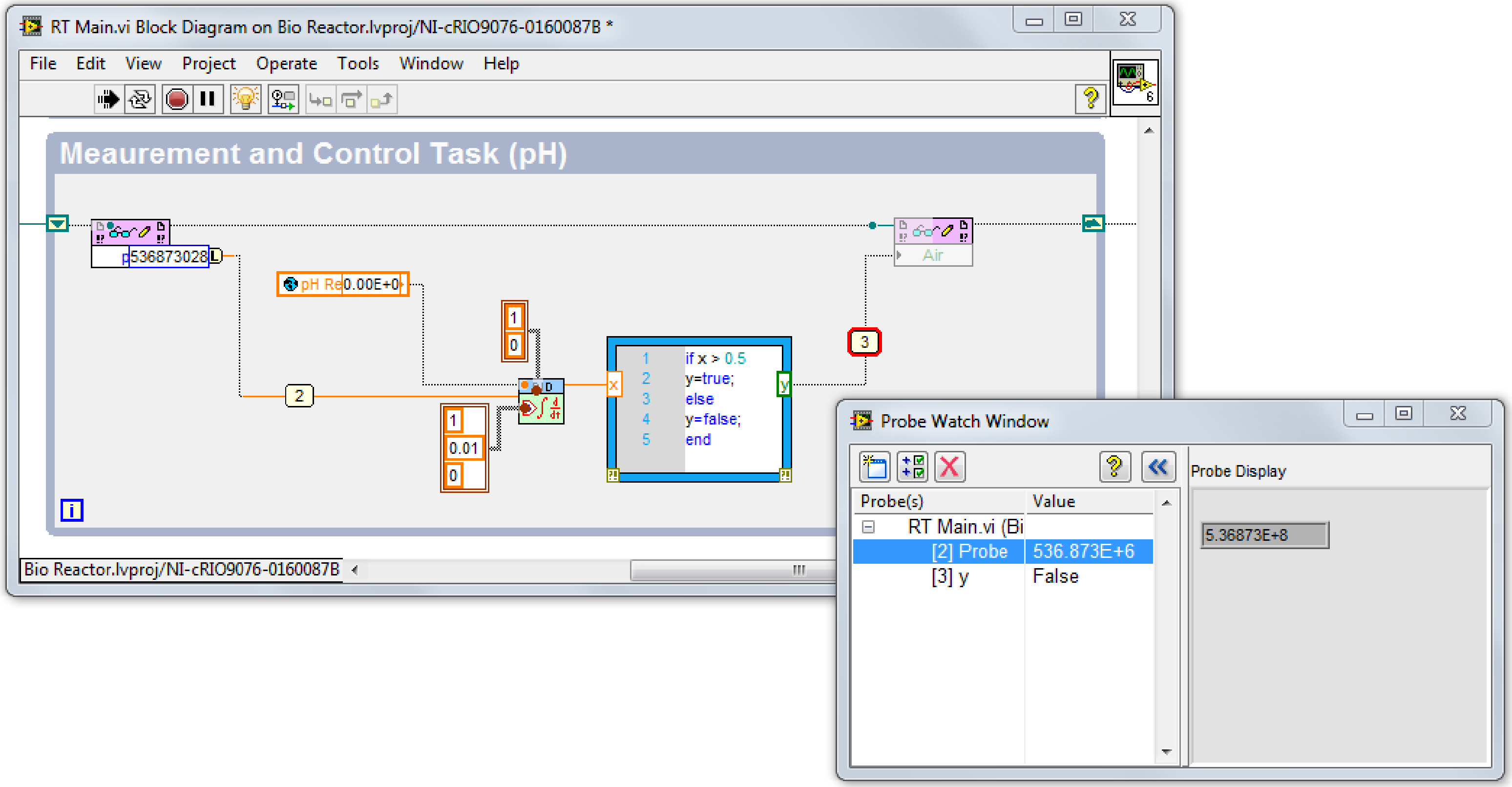
LabVIEW System Development Environment

Complete System IDE

Math and Analysis

Reuse of Existing Code

Graphical Debugging


RT Main.vi Block Diagram on Bio Reactor.lvproj/NI-cRIO9076-0160087B *
File
Edit
View
Project
Operate
Tools
Window
Help
Meaurement and Control Task (pH)
536873028
pH Re
0.00E+0
1
0
2
1
0.01
0
x
y
3
Air
Bio Reactor.lvproj/NI-cRIO9076-0160087B
Probe Watch Window
Probe Display

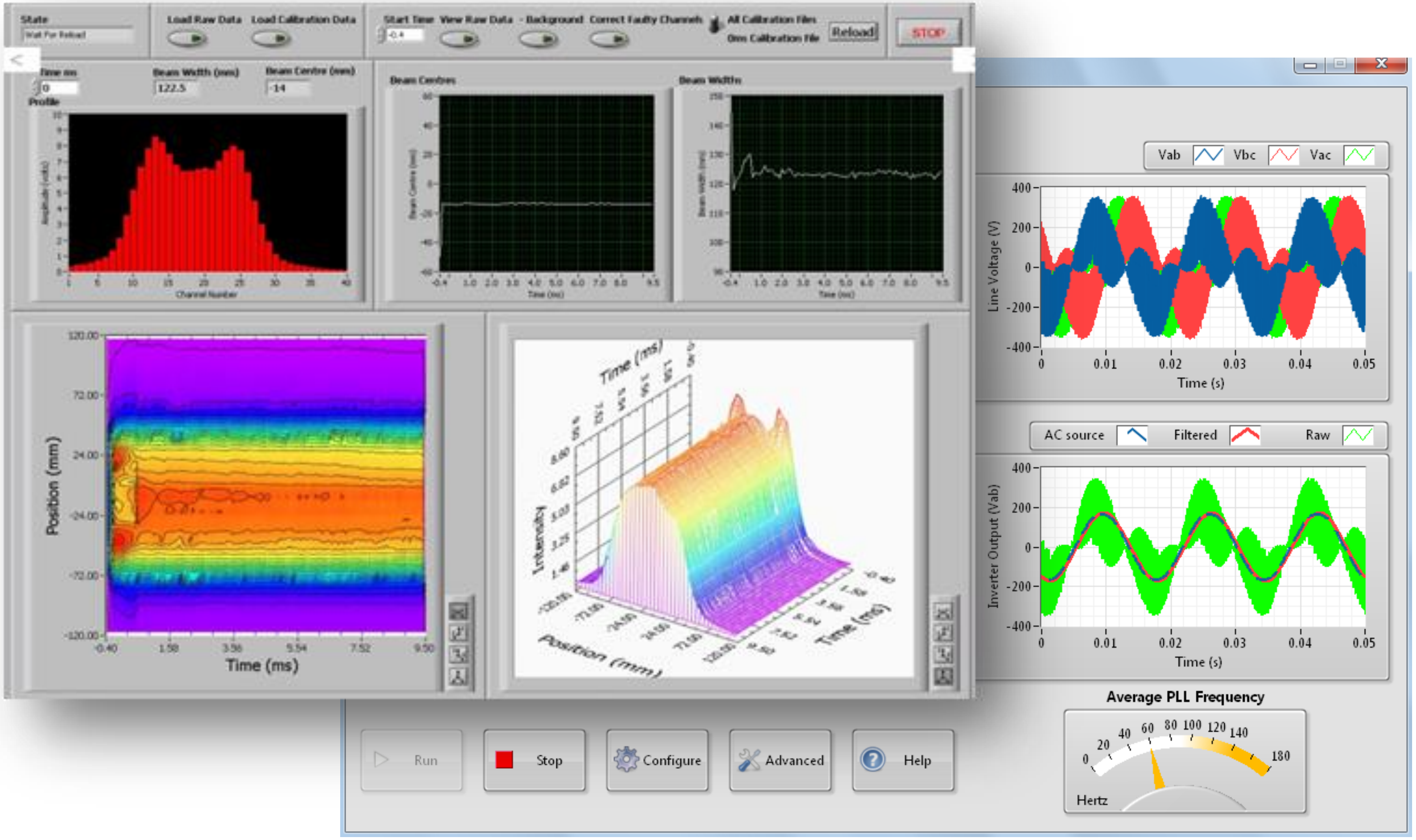
```
if x > 0.5
y=true;
else
y=false;
end
```

Probe(s)	Value
⊟ RT Main.vi (Bi	
[2] Probe	536.873E+6
[3] y	False

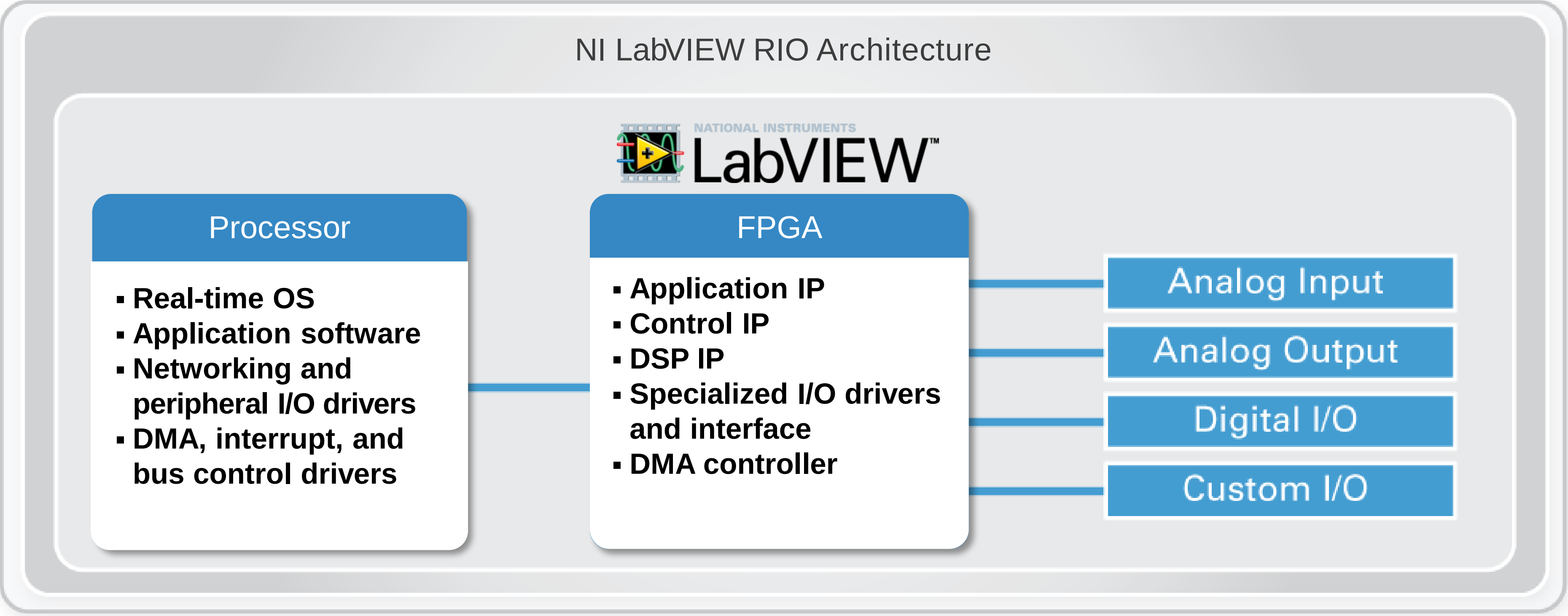
5.36873E+8

LabVIEW System Development Environment

Complete System IDE	Math and Analysis	Reuse of Existing Code	Graphical Debugging	User Interface



The NI Approach to Flexible Hardware



NI LabVIEW RIO Architecture

Processor

- Real-time OS
- Application software
- Networking and peripheral I/O drivers
- DMA, interrupt, and bus control drivers

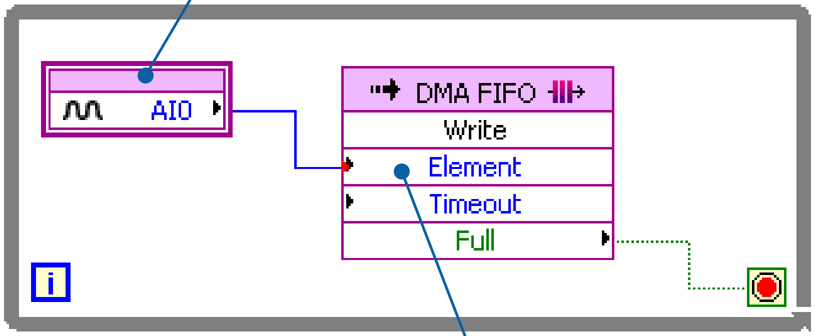
FPGA

- Application IP
- Control IP
- DSP IP
- Specialized I/O drivers and interface
- DMA controller

Highly Productive LabVIEW Graphical Programming Environment for Programming Host, FPGA, I/O, and Bus Interfaces

Abstraction of Hardware Complexities

Acquire analog data point-by-point

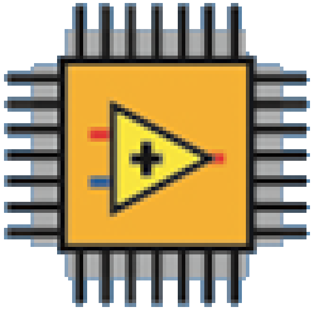


Transfer analog data to host CPU via DMA FIFO for data logging, display, etc.

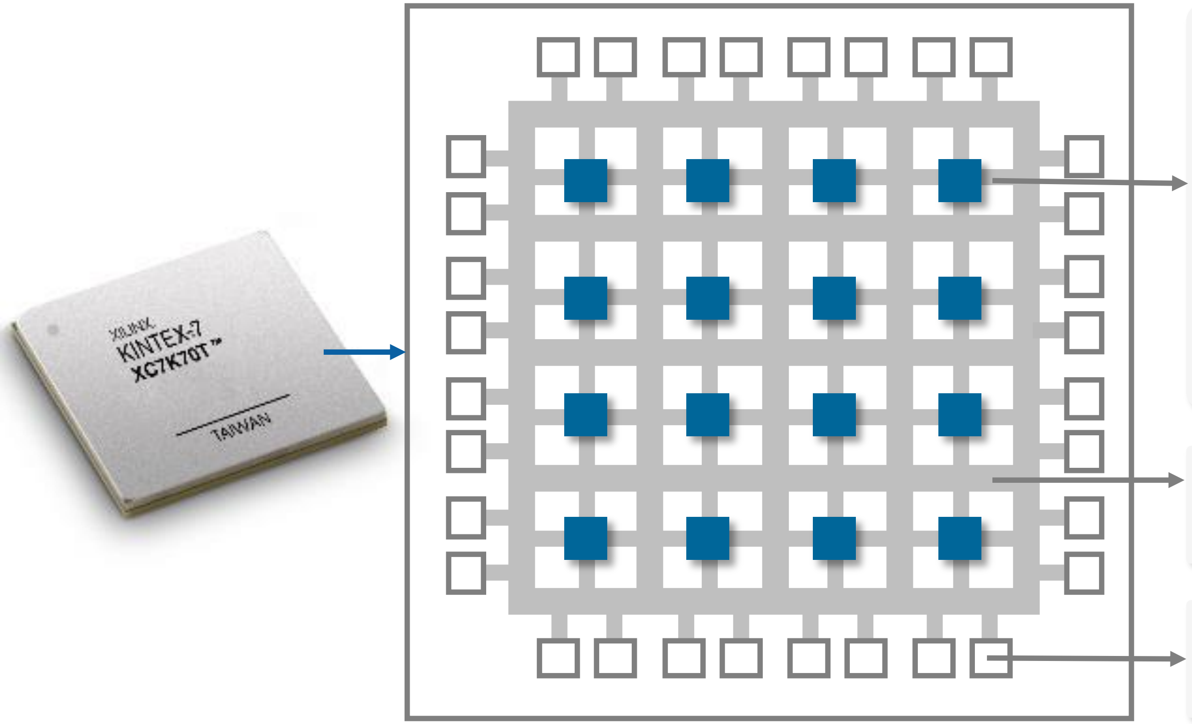
~4000 lines of VHDL

LabVIEW FPGA vs. VHDL

Introduction to LabVIEW FPGA:



Field-Programmable Gate Array (FPGA)



Memory Blocks
Store data sets or values in user defined RAM

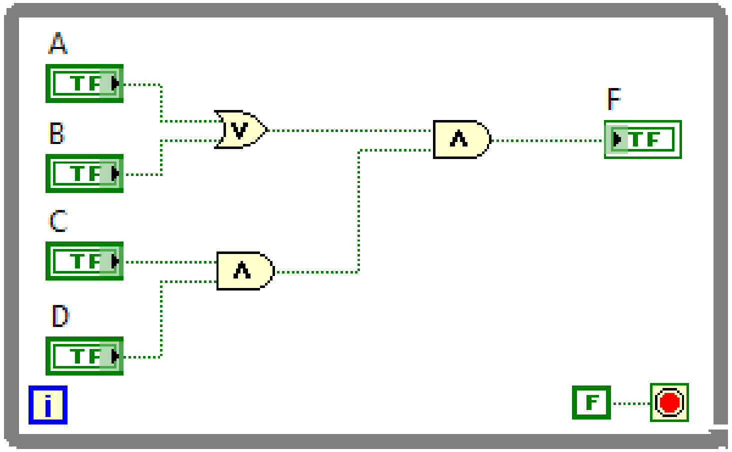
Configurable Logic Blocks (CLBs)
Implement logic using flip-flops and LUTs

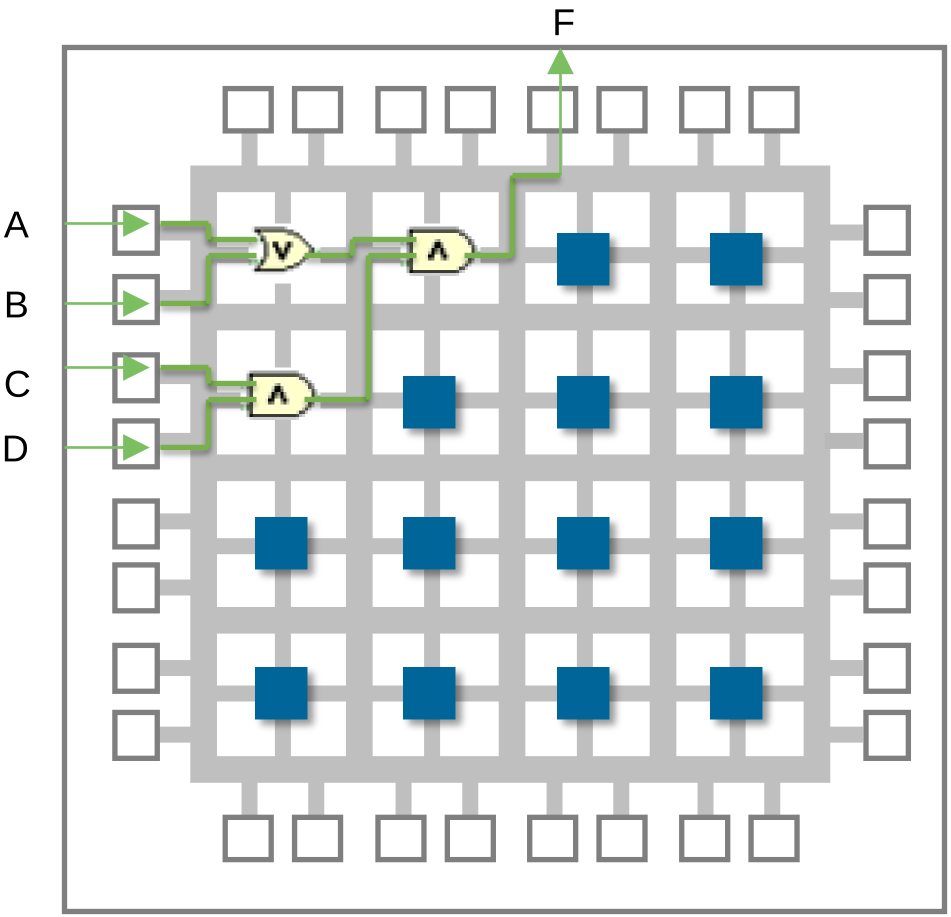
Multipliers and DSPs
Implement signal processing using multiplier and multiplier-accumulate circuitry

Programmable Interconnects
Route signals through the FPGA matrix

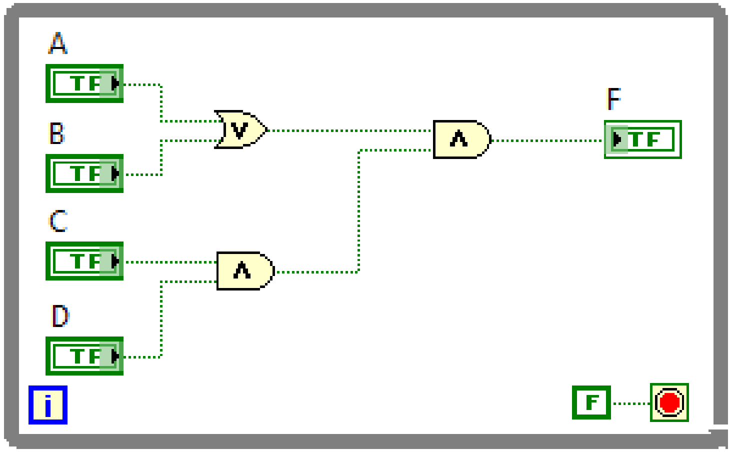
I/O Blocks
Directly access digital and analog I/O

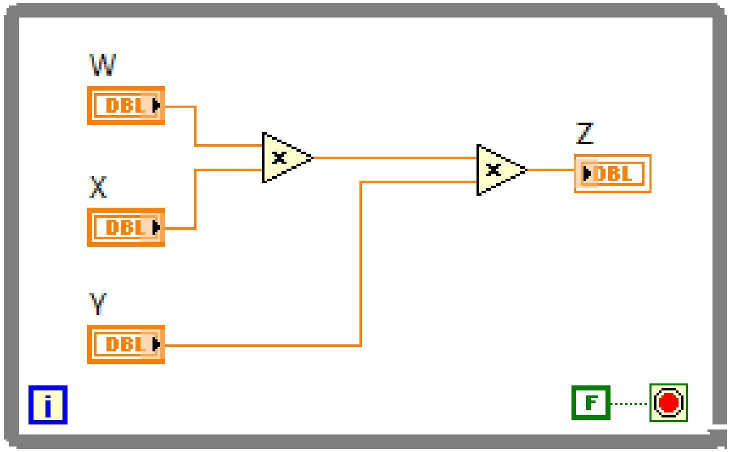
FPGAs Are Dataflow Systems

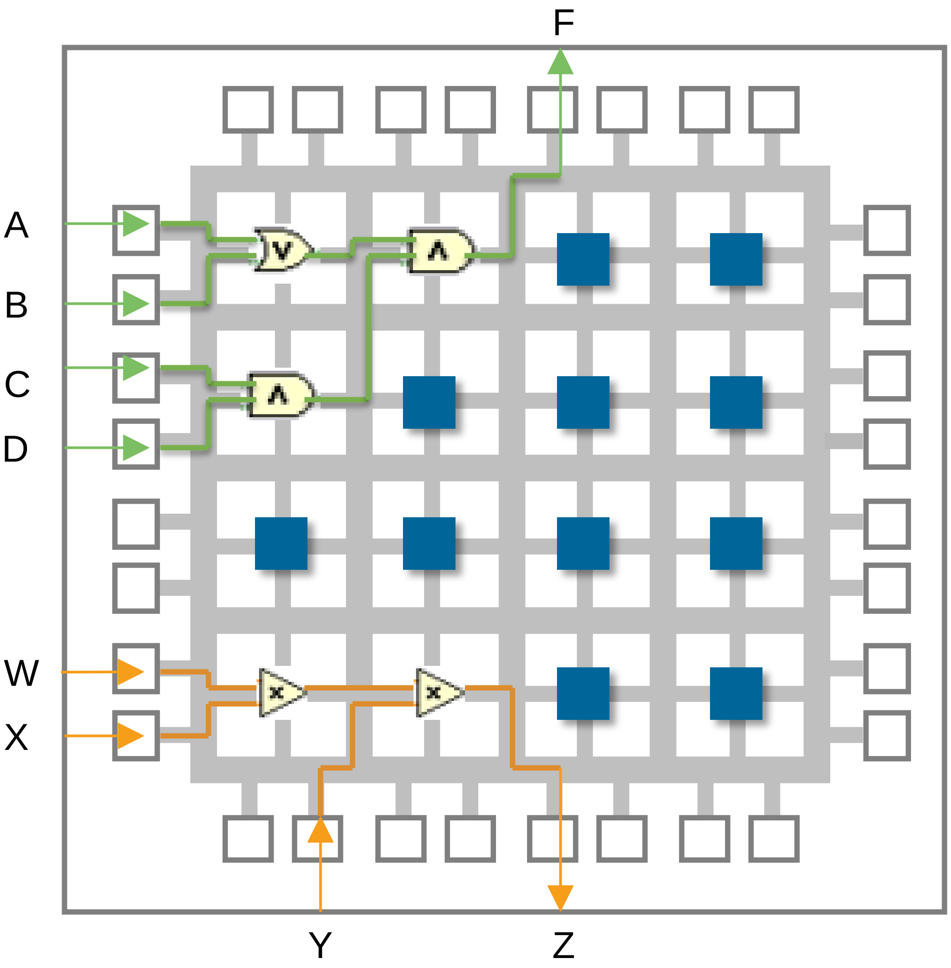




Parallel Processing



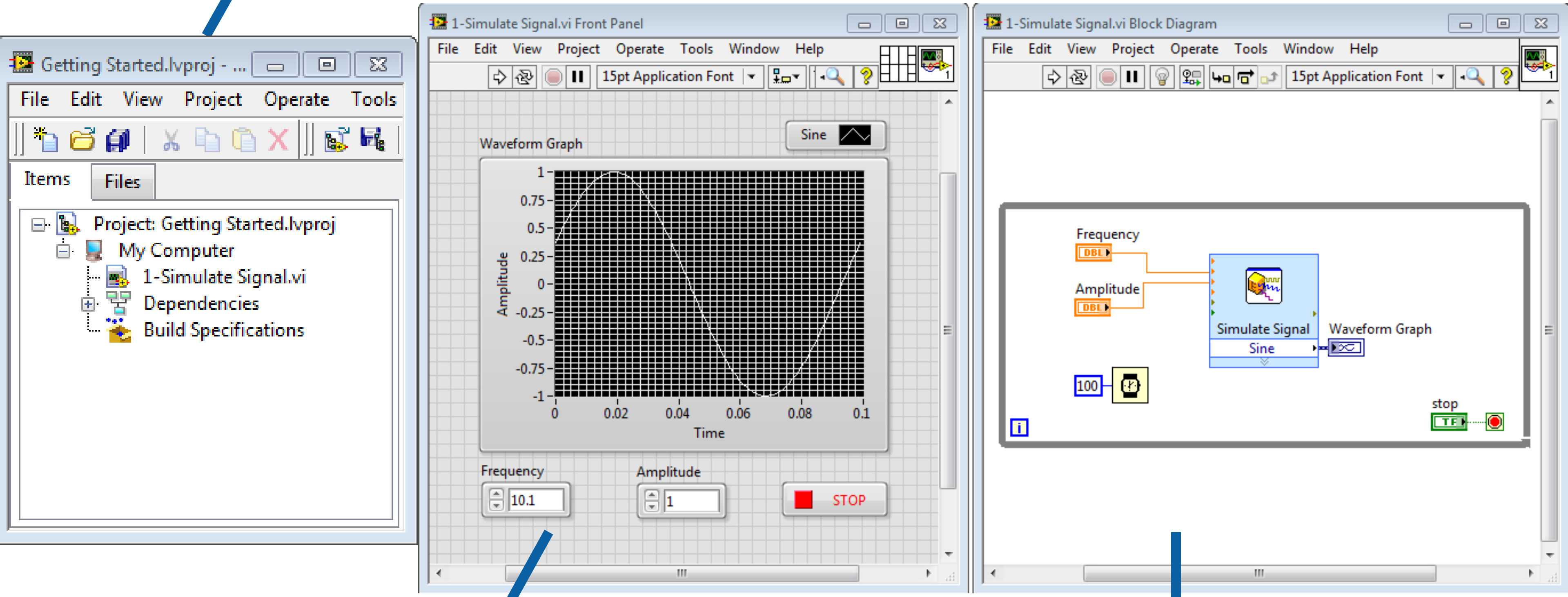




LabVIEW Environment Basics

“Project” = System Configuration

“VI” = Program or Function



“Front Panel” = User Interface

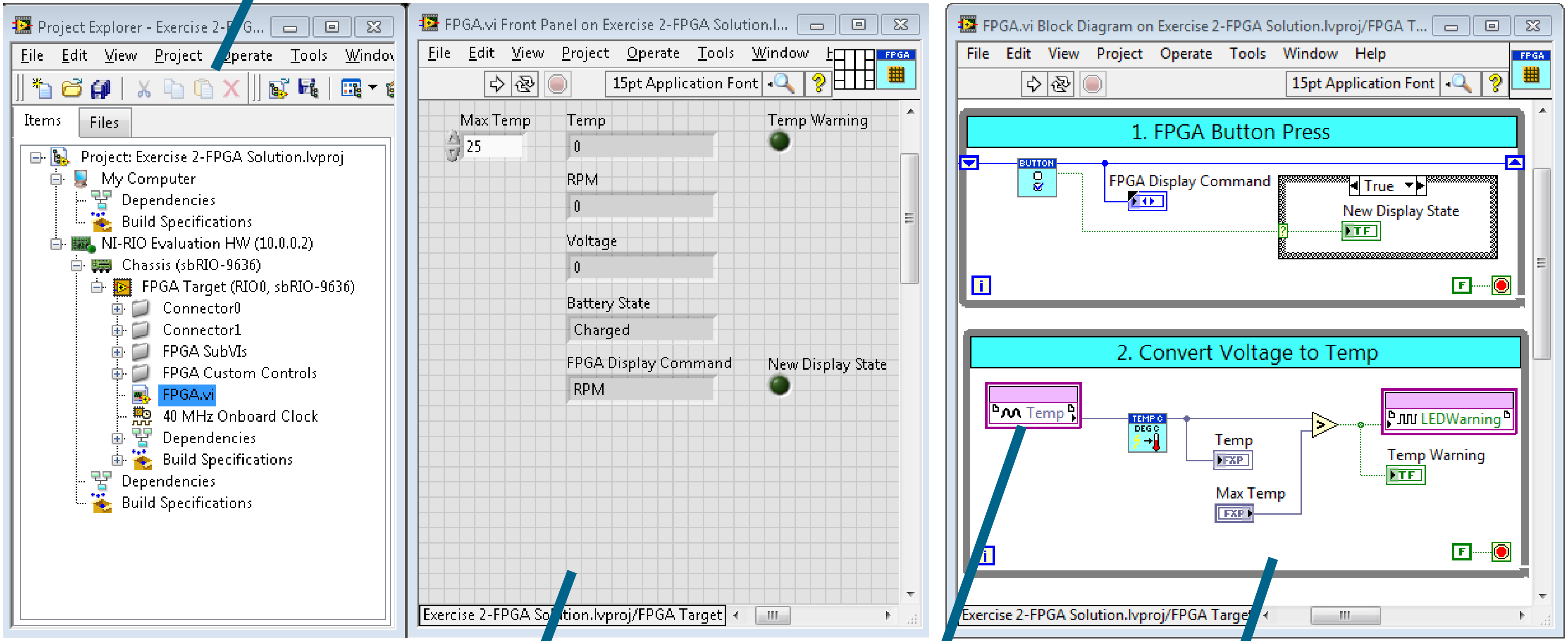
“Block Diagram” = Code

ni.com

LabVIEW FPGA

“Project” = System Configuration

“VI” = Application


Project Explorer - Exercise 2-FPG...
File Edit View Project Operate Tools Window
Items Files
Project: Exercise 2-FPGA Solution.lvproj
My Computer
Dependencies
Build Specifications
NI-RIO Evaluation HW (10.0.0.2)
Chassis (sbRIO-9636)
FPGA Target (RIO0, sbRIO-9636)
Connector0
Connector1
FPGA SubVIs
FPGA Custom Controls
FPGA.vi
40 MHz Onboard Clock
Dependencies
Build Specifications
Dependencies
Build Specifications
FPGA.vi Front Panel on Exercise 2-FPGA Solution.l...
File Edit View Project Operate Tools Window
15pt Application Font
FPGA
Max Temp
25
Temp
0
Temp Warning
RPM
0
Voltage
0
Battery State
Charged
FPGA Display Command
RPM
New Display State
Exercise 2-FPGA Solution.lvproj/FPGA Target
FPGA.vi Block Diagram on Exercise 2-FPGA Solution.lvproj/FPGA T...
File Edit View Project Operate Tools Window Help
15pt Application Font
1. FPGA Button Press
BUTTON
FPGA Display Command
True
New Display State
TF
F
2. Convert Voltage to Temp
Temp
TEMP C DEG C
Temp
FXP
Max Temp
FXP
LEDWarning
Temp Warning
TF
F
Exercise 2-FPGA Solution.lvproj/FPGA Target

“Front Panel”= Interface Elements

I/O Node

“Block Diagram”= Code

LabVIEW FPGA vs. VHDL: Blink an LED

VHDL Implementation

```
begin

  LED <= LED_local;

  process (CLK_50MHZ)
  begin
    if rising_edge(CLK_50MHZ) then
       if ToggleLED then
         LED_local <= not LED_local;
       end if;
    end if;
  end process;

  CounterProc: process (CLK_50MHZ)
  begin
    if rising_edge(CLK_50MHZ) then
      if CounterValue = kCounterTC then
        CounterValue <= (others => '0');
        ToggleLED <= true;
      else
        CounterValue <= CounterValue + 1;
        ToggleLED <= false;
      end if;
    end if;
  end process CounterProc;

end rtl;
```

Physical wire connection to “LED”

LabVIEW FPGA vs. VHDL: Blink an LED

VHDL Implementation

```
begin

  LED <= LED_local;

  process (CLK_50MHZ)
  begin
    if rising_edge(CLK_50MHZ) then
       if ToggleLED then
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    end if;
  end process;

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        CounterValue <= (others => '0');
        ToggleLED <= true;
      else
        CounterValue <= CounterValue + 1;
        ToggleLED <= false;
      end if;
    end if;
  end process CounterProc;

end rtl;
```

Physical wire connection to “LED”

Toggle the physical LED when internal timing signal “ToggleLED” is true. Executes every tick of the 50Mhz clock.

LabVIEW FPGA vs. VHDL: Blink an LED

VHDL Implementation

```
begin

  LED <= LED_local;

  process (CLK_50MHZ)
  begin
    if rising_edge(CLK_50MHZ) then
       if ToggleLED then
         LED_local <= not LED_local;
       end if;
    end if;
  end process;

  CounterProc: process (CLK_50MHZ)
  begin
    if rising_edge(CLK_50MHZ) then
      if CounterValue = kCounterTC then
        CounterValue <= (others => '0');
        ToggleLED <= true;
      else
        CounterValue <= CounterValue + 1;
        ToggleLED <= false;
      end if;
    end if;
  end process CounterProc;

end rtl;
```

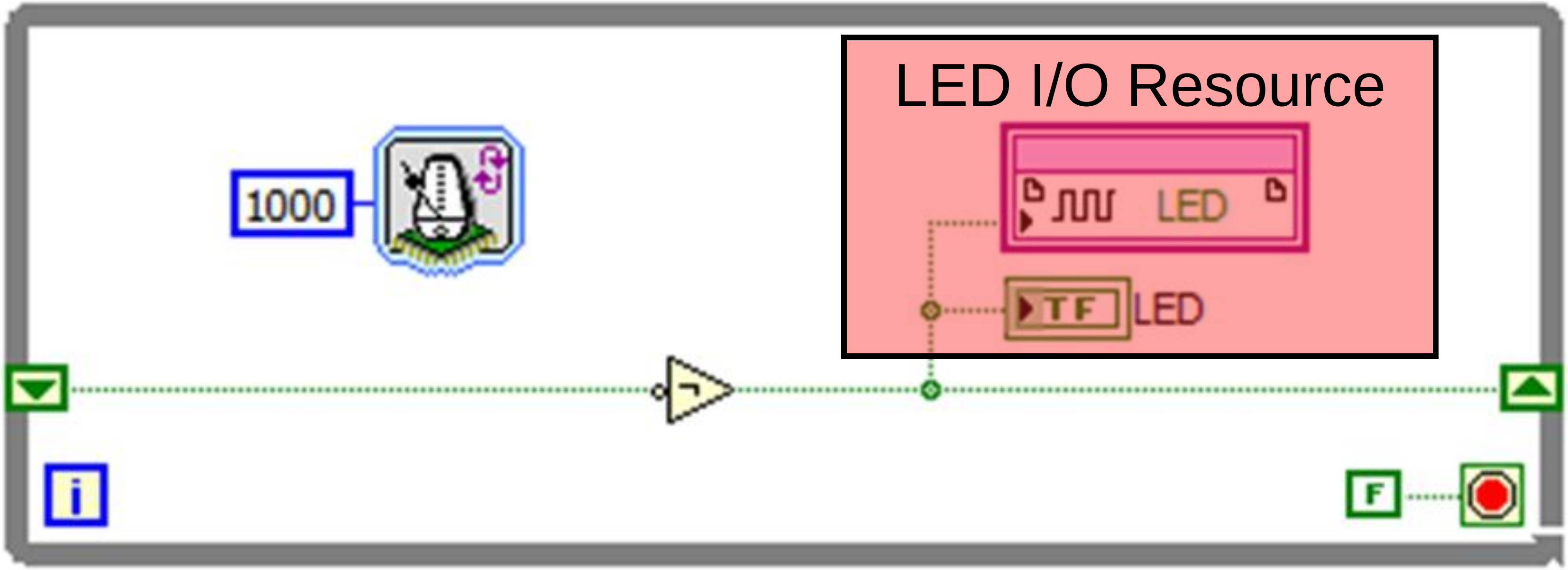
Physical wire connection to “LED”

Toggle the physical LED when internal timing signal “ToggleLED” is true. Executes every tick of the 50Mhz clock.

Counter establishes the timing of the “ToggleLED” signal. Goes “true” when the counter reaches 50,000,000 (1 second) and resets counter.

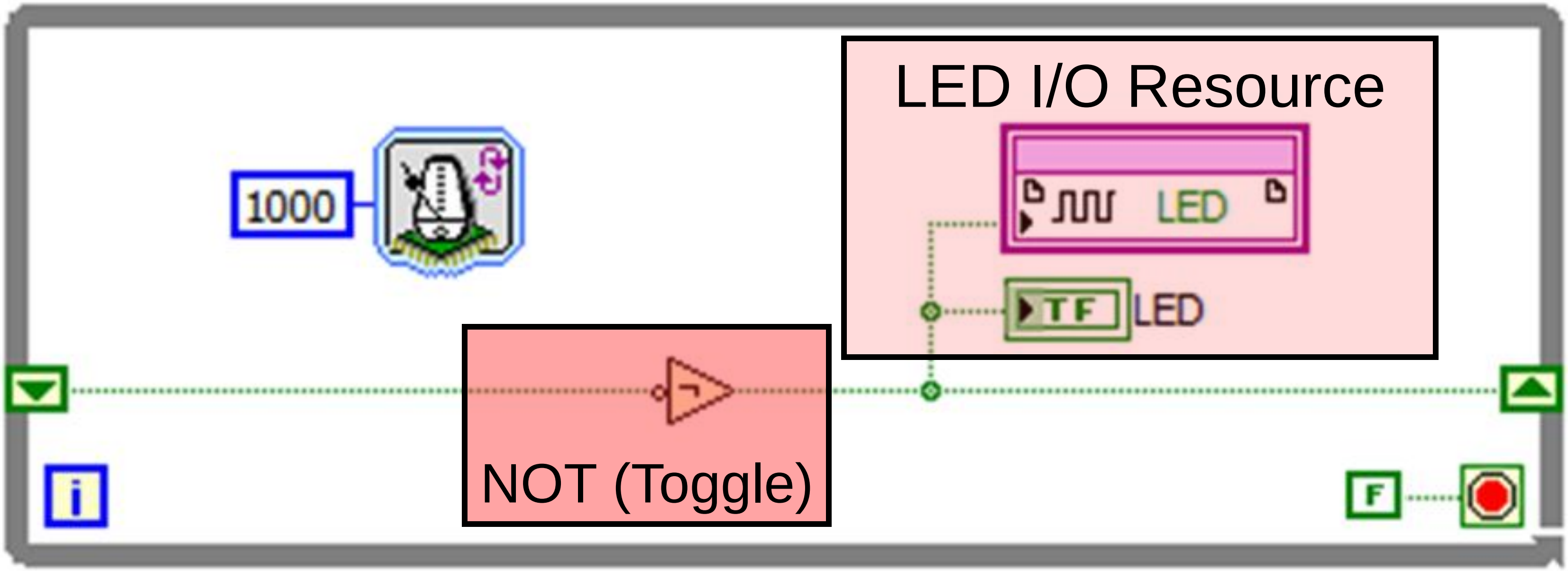
LabVIEW FPGA vs. VHDL: Blink an LED

LabVIEW Implementation



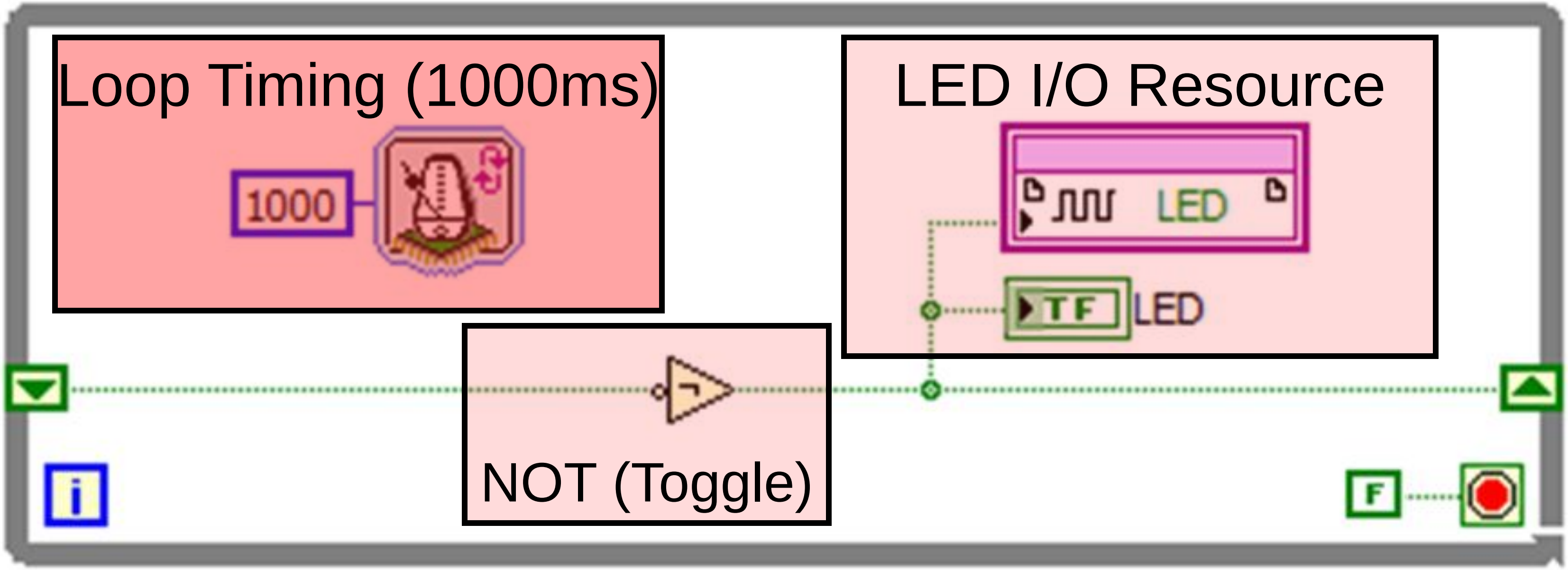
LabVIEW FPGA vs. VHDL: Blink an LED

LabVIEW Implementation

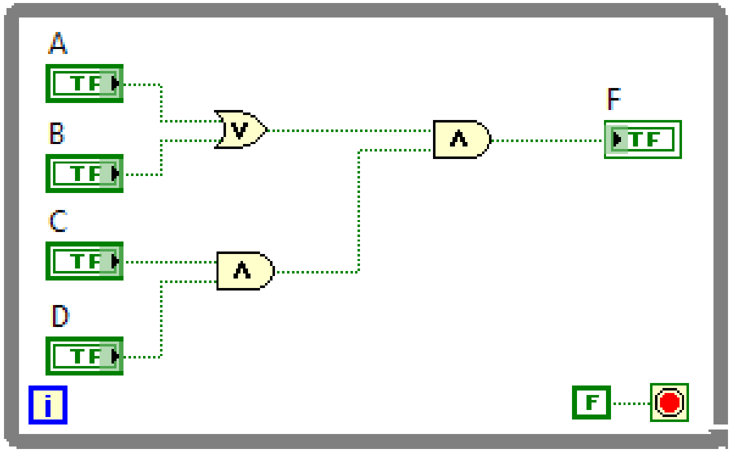


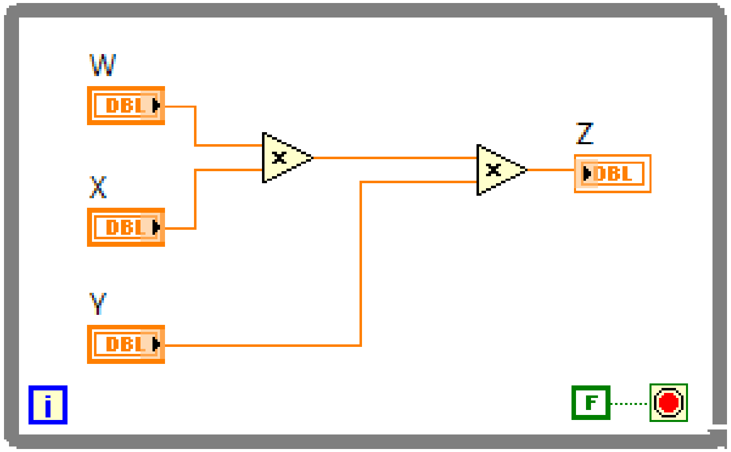
LabVIEW FPGA vs. VHDL: Blink an LED

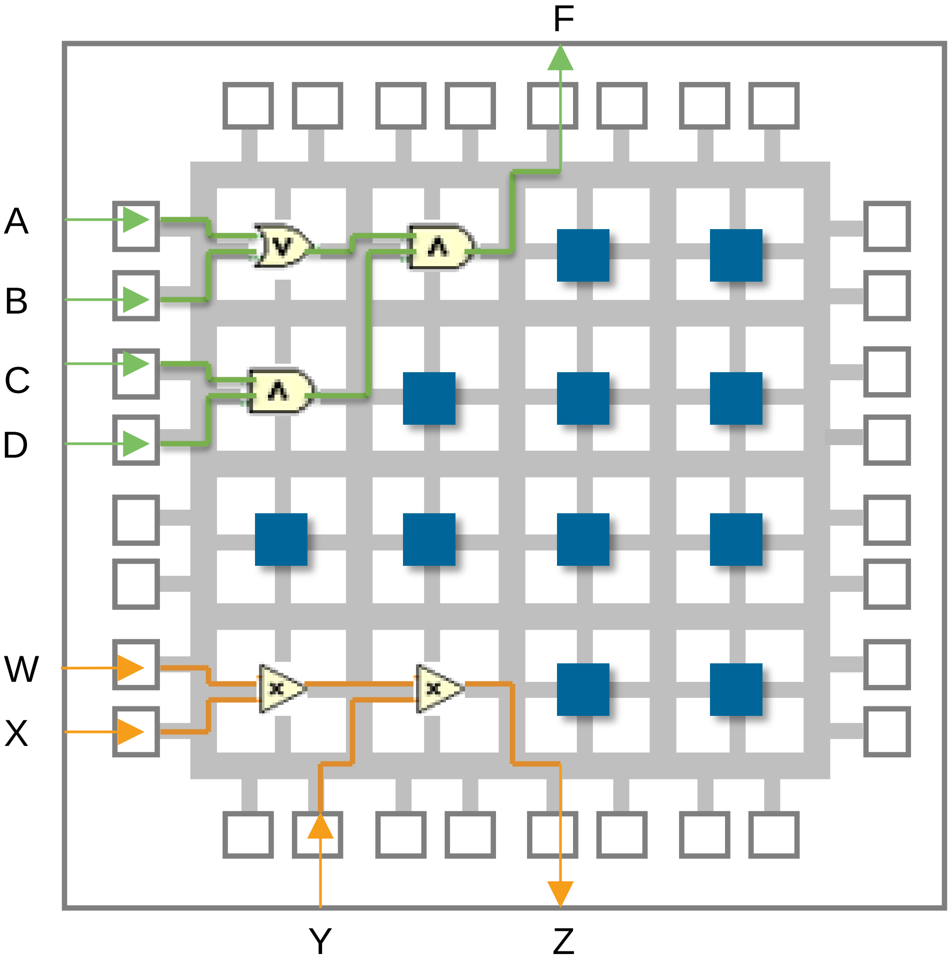
LabVIEW Implementation



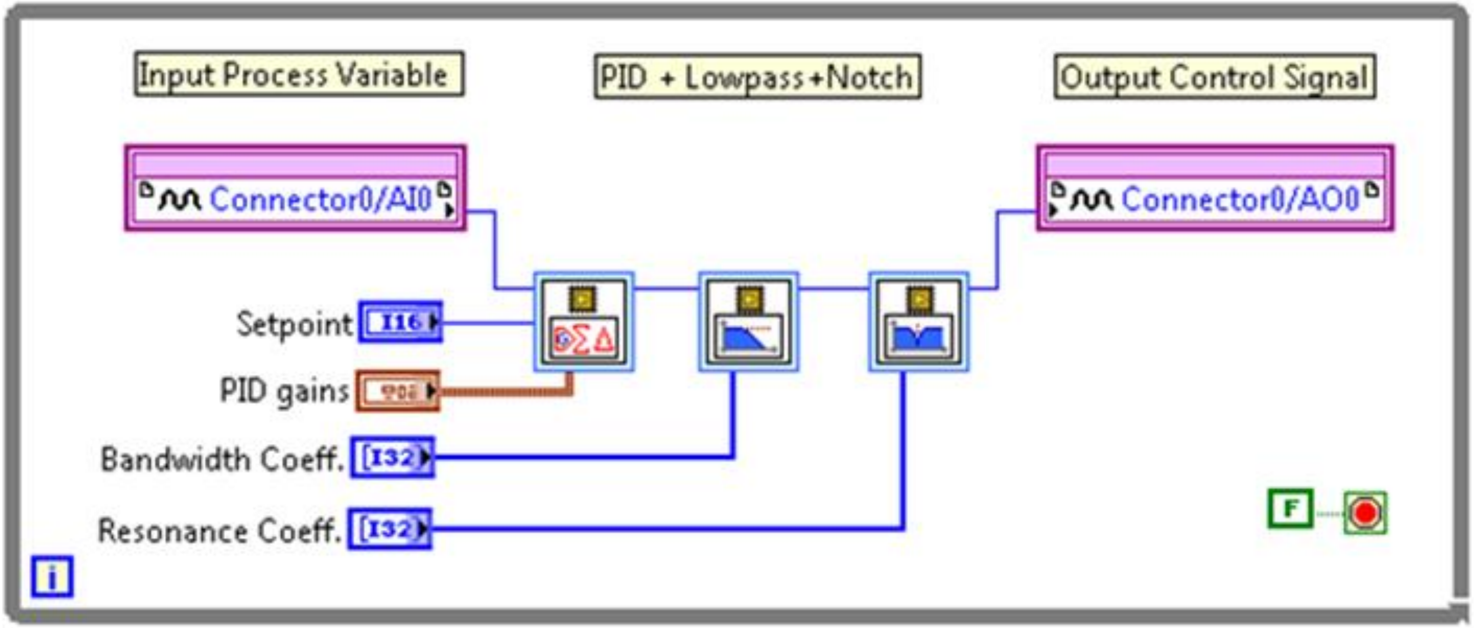
Parallel Processing



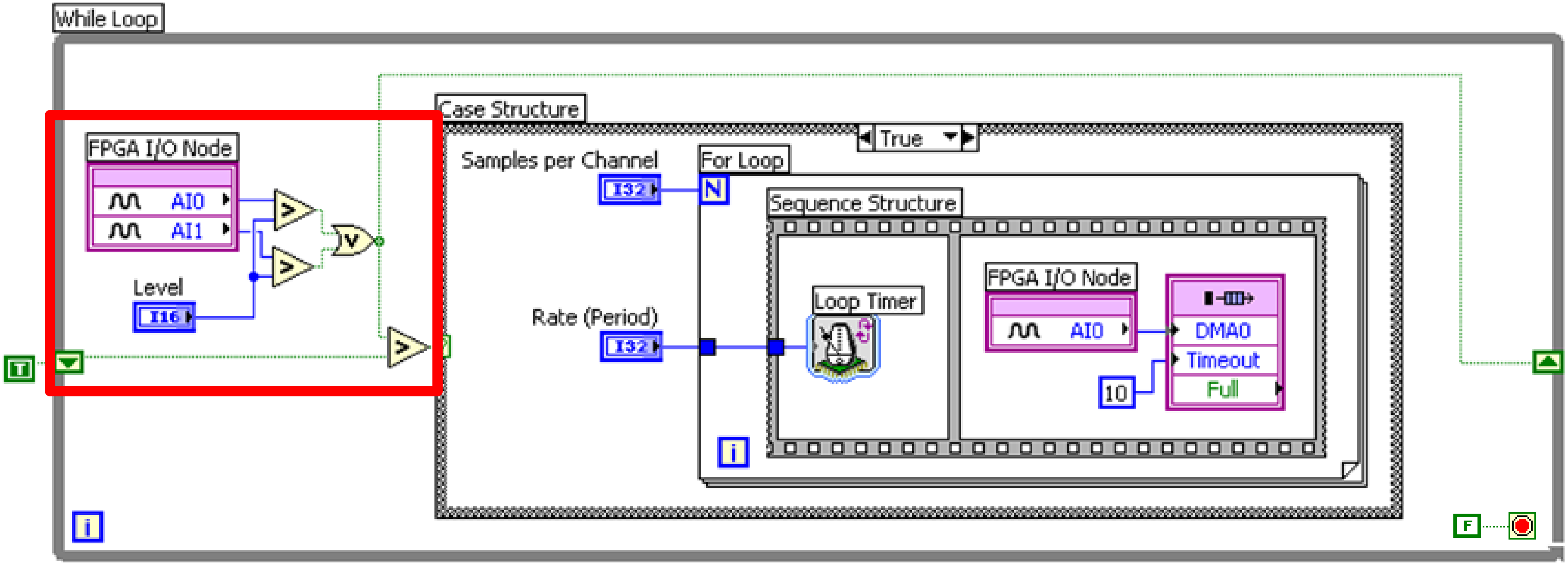




High-Speed Control



Custom Triggered Analog Input



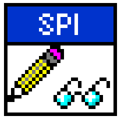
- Custom timing & synchronization
- Multi-rate sampling
- Custom counters
- Flexible PWM
- Flexible encoder interface

Digital Communication Protocol APIs

- SPI:

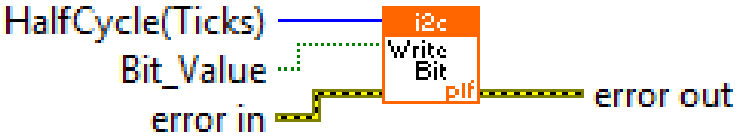
FPGA SPI_Configure.vi

FPGA SPI_Read Write.vi



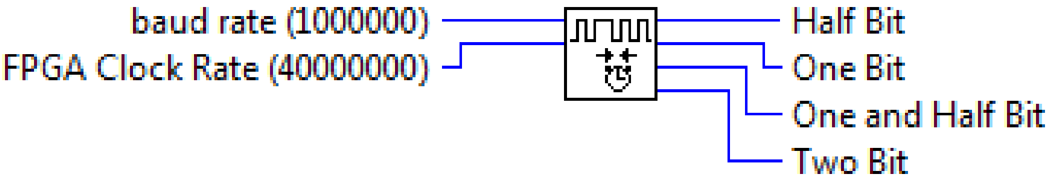
- I2C:

I2C_WriteBitToSlave.vi

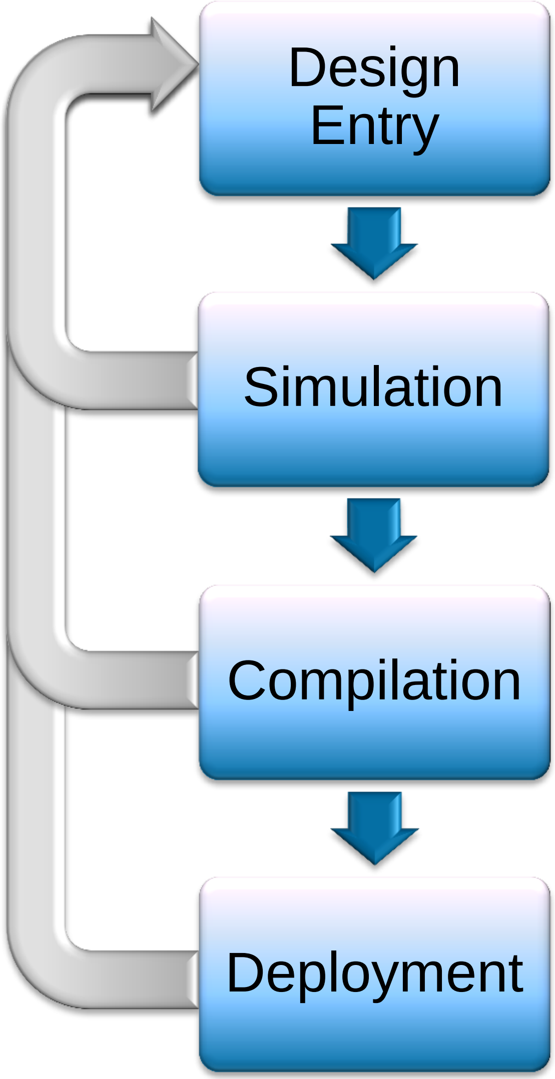


- Serial:

LV FPGA Serial Calc Timing Values.vi



Simplified FPGA Design Flow

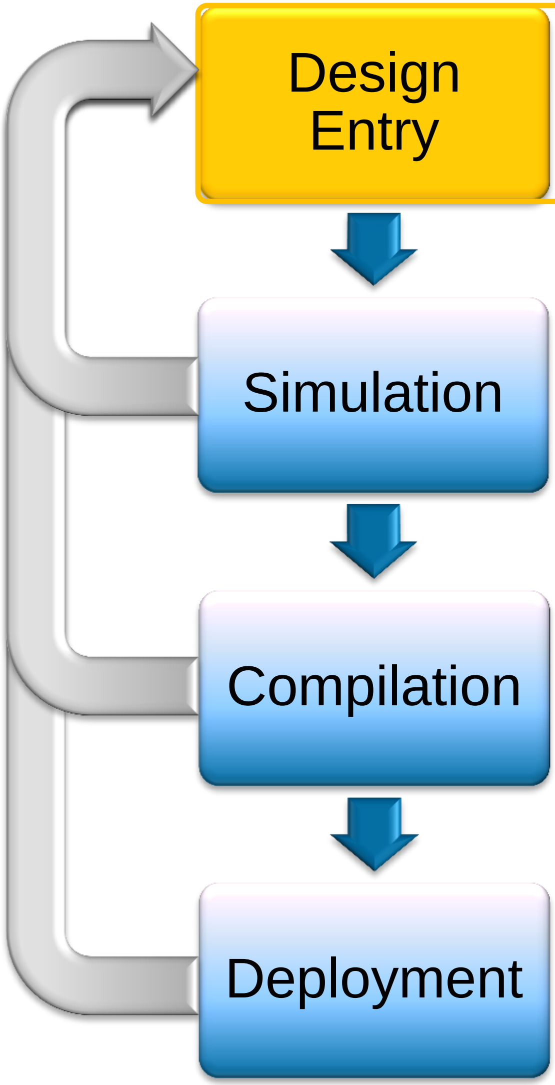

Design Entry

Simulation

Compilation

Deployment

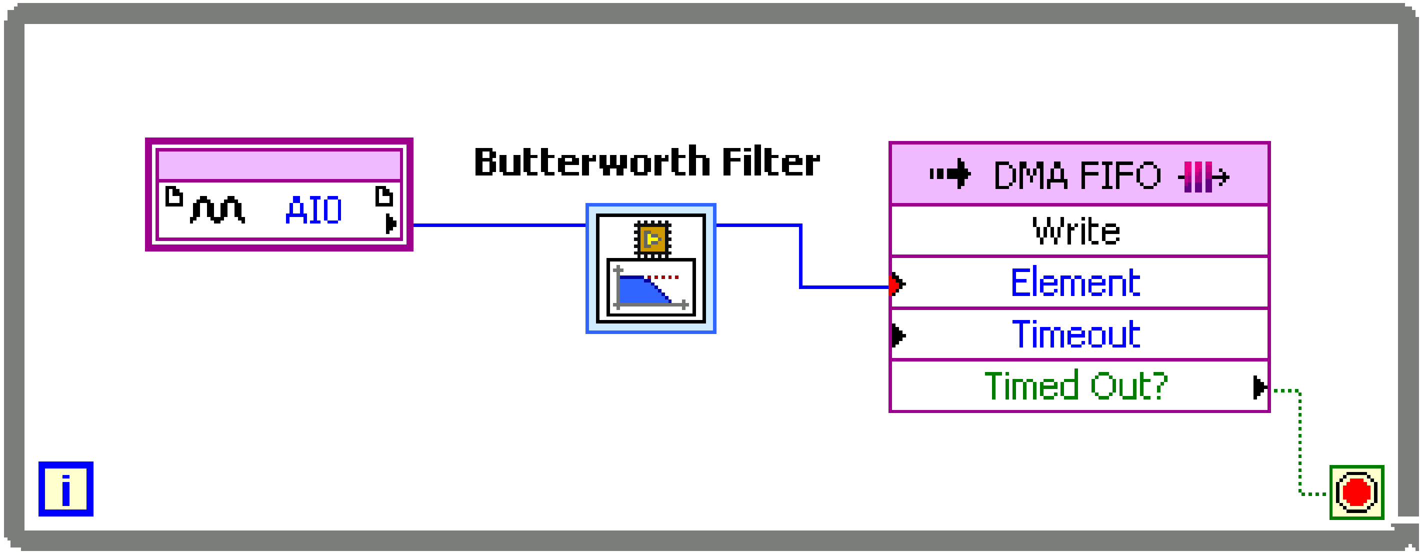
Simplified FPGA Design Flow



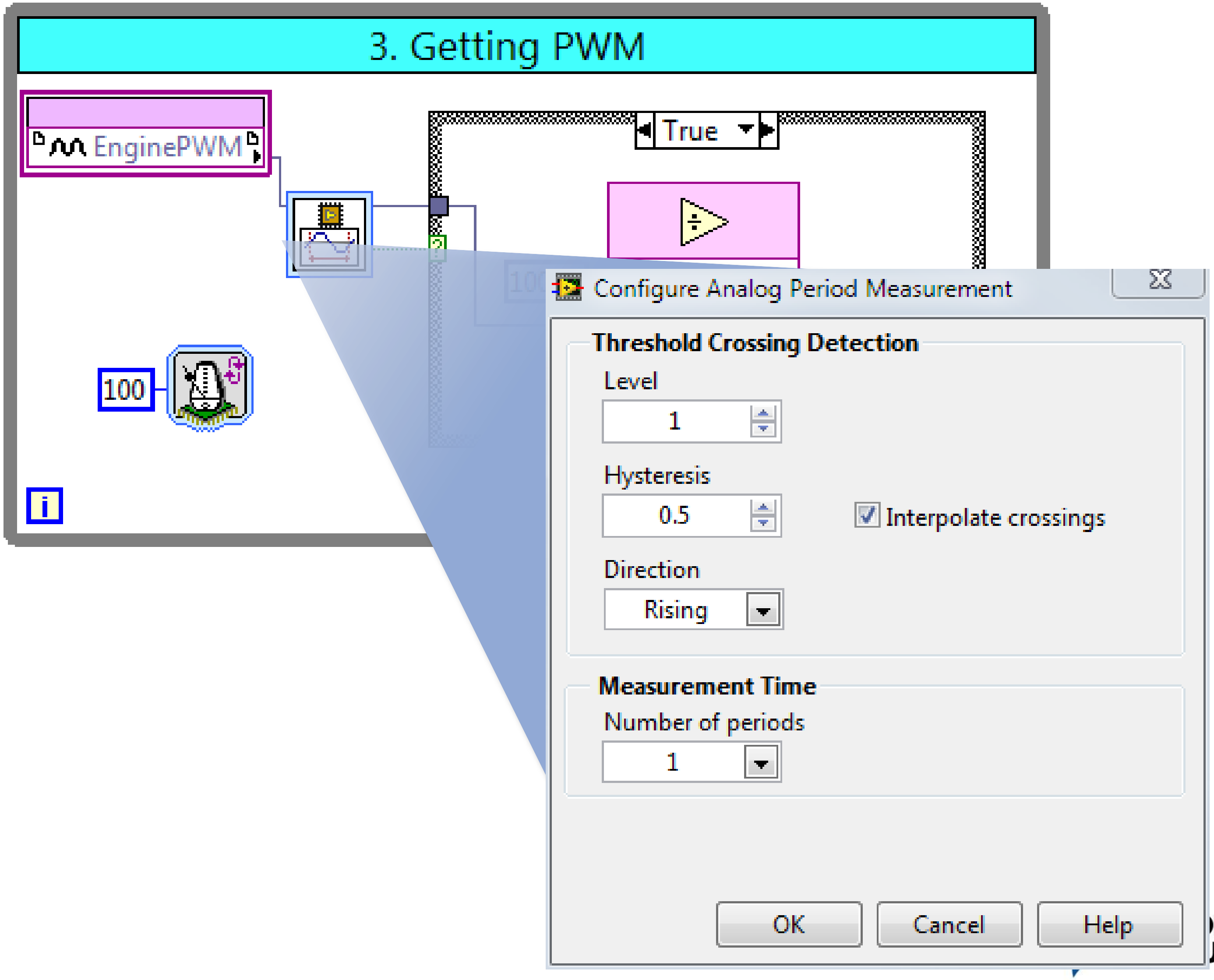
- Interface Abstraction
- HDL/IP Integration
- Configuration-Based

Interface Abstraction

- I/O Interfaces to NI and 3rd party I/O modules
- Built-in DMA FIFO interfaces



Configuration-Based Design



Configure Analog Period Measurement

Threshold Crossing Detection

Level: 1

Hysteresis: 0.5

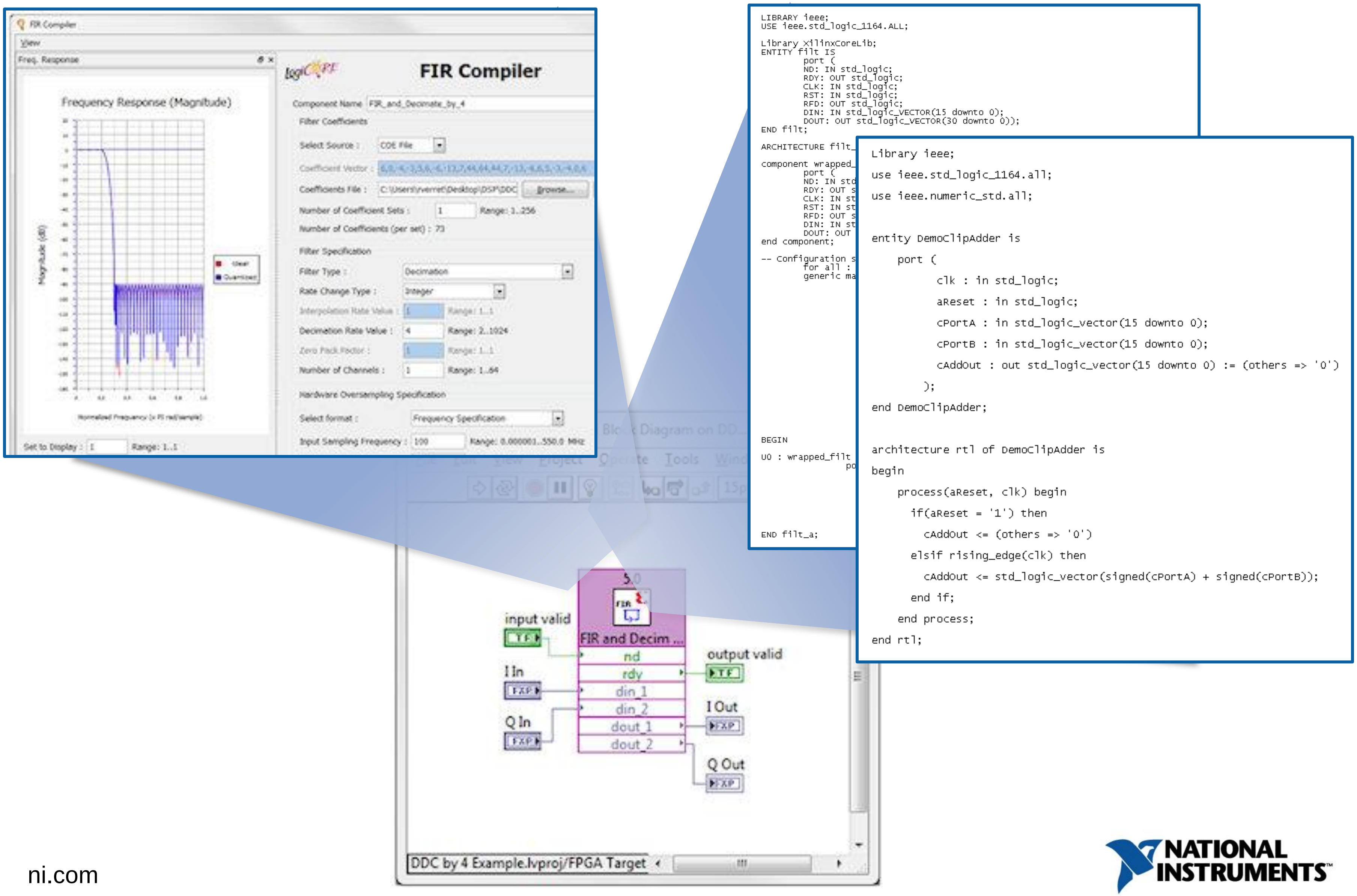
☑ Interpolate crossings

Direction: Rising

Measurement Time

Number of periods: 1

IP Integration in LabVIEW FPGA



FIR Compiler

Component Name FIR_and_Decimate_by_4

Filter Coefficients

Select Source : COE File

Coefficient Vector : 6,0,-6,-3,5,6,-6,-13,7,44,64,44,7,-13,-6,6,5,-3,-6,0,6

Coefficients File : C:\Users\rverret\Desktop\DSP\DDC Browse...

Number of Coefficient Sets : 1 Range: 1..256

Number of Coefficients (per set) : 73

Filter Specification

Filter Type : Decimation

Rate Change Type : Integer

Interpolation Rate Value : 1 Range: 1..1

Decimation Rate Value : 4 Range: 2..1024

Zero Pack Factor : 1 Range: 1..1

Number of Channels : 1 Range: 1..64

Hardware Oversampling Specification

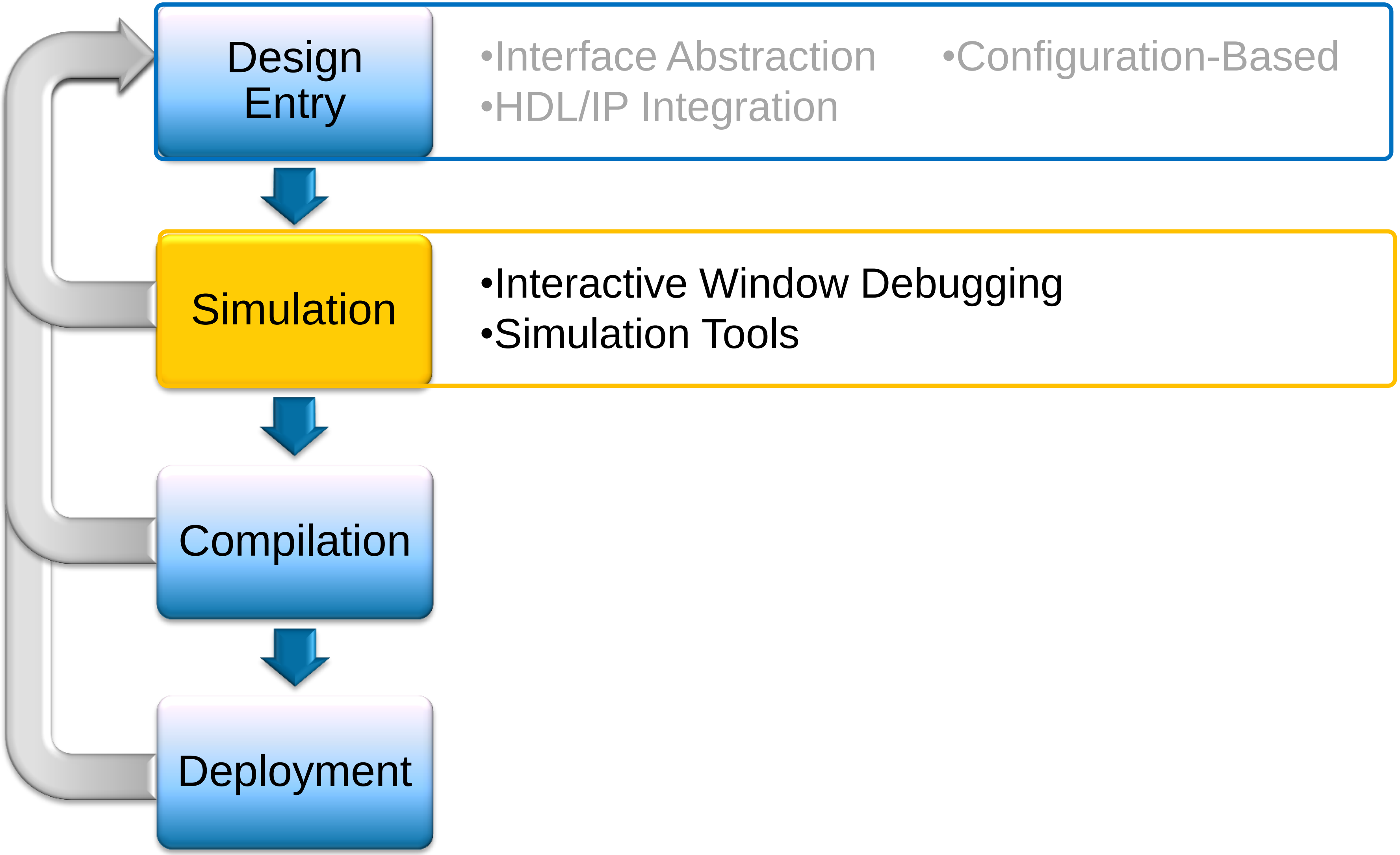
Select format : Frequency Specification

Input Sampling Frequency : 100 Range: 0.000001..550.0 MHz

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

Library XilinxCoreLib;
ENTITY filt IS
        port (
        ND: IN std_logic;
        RDY: OUT std_logic;
        CLK: IN std_logic;
        RST: IN std_logic;
        RFD: OUT std_logic;
        DIN: IN std_logic_VECTOR(15 downto 0);
        DOUT: OUT std_logic_VECTOR(30 downto 0));
END filt;

ARCHITECTURE filt_

component wrapped_
        port (
        ND: IN std
        RDY: OUT s
        CLK: IN st
        RST: IN st
        RFD: OUT s
        DIN: IN st
        DOUT: OUT
end component;

-- Configuration s
        for all :
        generic ma





BEGIN

U0 : wrapped_filt
                   po



END filt_a;
```

```
Library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity DemoClipAdder is
    port (
           clk : in std_logic;
           aReset : in std_logic;
           cPortA : in std_logic_vector(15 downto 0);
           cPortB : in std_logic_vector(15 downto 0);
           cAddOut : out std_logic_vector(15 downto 0) := (others => '0')
         );
end DemoClipAdder;

architecture rtl of DemoClipAdder is
begin
    process(aReset, clk) begin
      if(aReset = '1') then
        cAddOut <= (others => '0')
      elsif rising_edge(clk) then
        cAddOut <= std_logic_vector(signed(cPortA) + signed(cPortB));
      end if;
    end process;
end rtl;
```

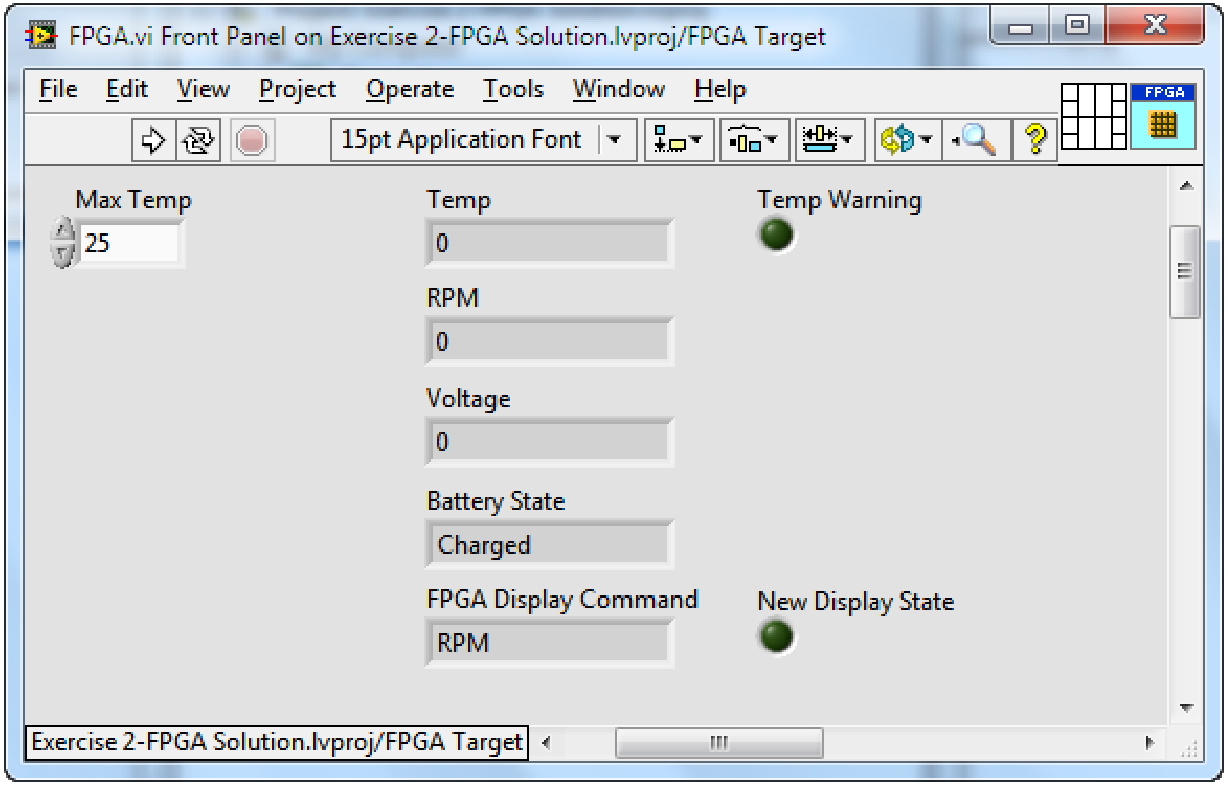
Simplified FPGA Design Flow



- •Interface Abstraction
- •HDL/IP Integration
- •Configuration-Based

- •Interactive Window Debugging
- •Simulation Tools

Interactive “Front Panel” Window



FPGA.vi Front Panel on Exercise 2-FPGA Solution.lvproj/FPGA Target
File Edit View Project Operate Tools Window Help
15pt Application Font
FPGA

Max Temp
25

Temp
0

Temp Warning

RPM
0

Voltage
0

Battery State
Charged

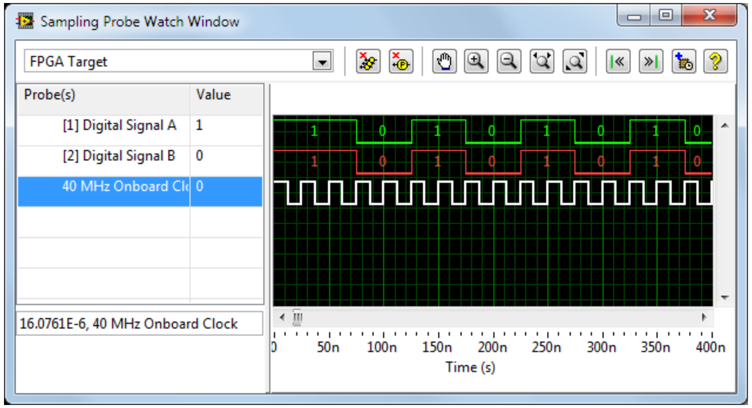
FPGA Display Command
RPM

New Display State

Exercise 2-FPGA Solution.lvproj/FPGA Target

Visual Simulation and Debugging Tools

Debug with standard LabVIEW features in simulation



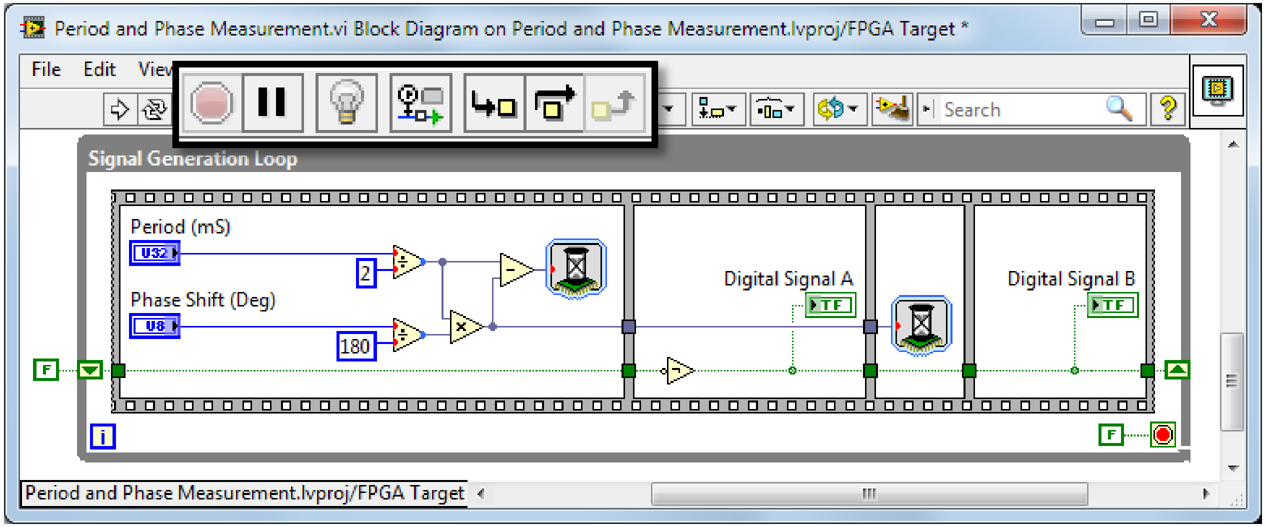
Sampling Probe Watch Window

FPGA Target

Probe(s)	Value
[1] Digital Signal A	1
[2] Digital Signal B	0
40 MHz Onboard Cl(	0

16.0761E-6, 40 MHz Onboard Clock

Verify signal timing with digital waveform probe

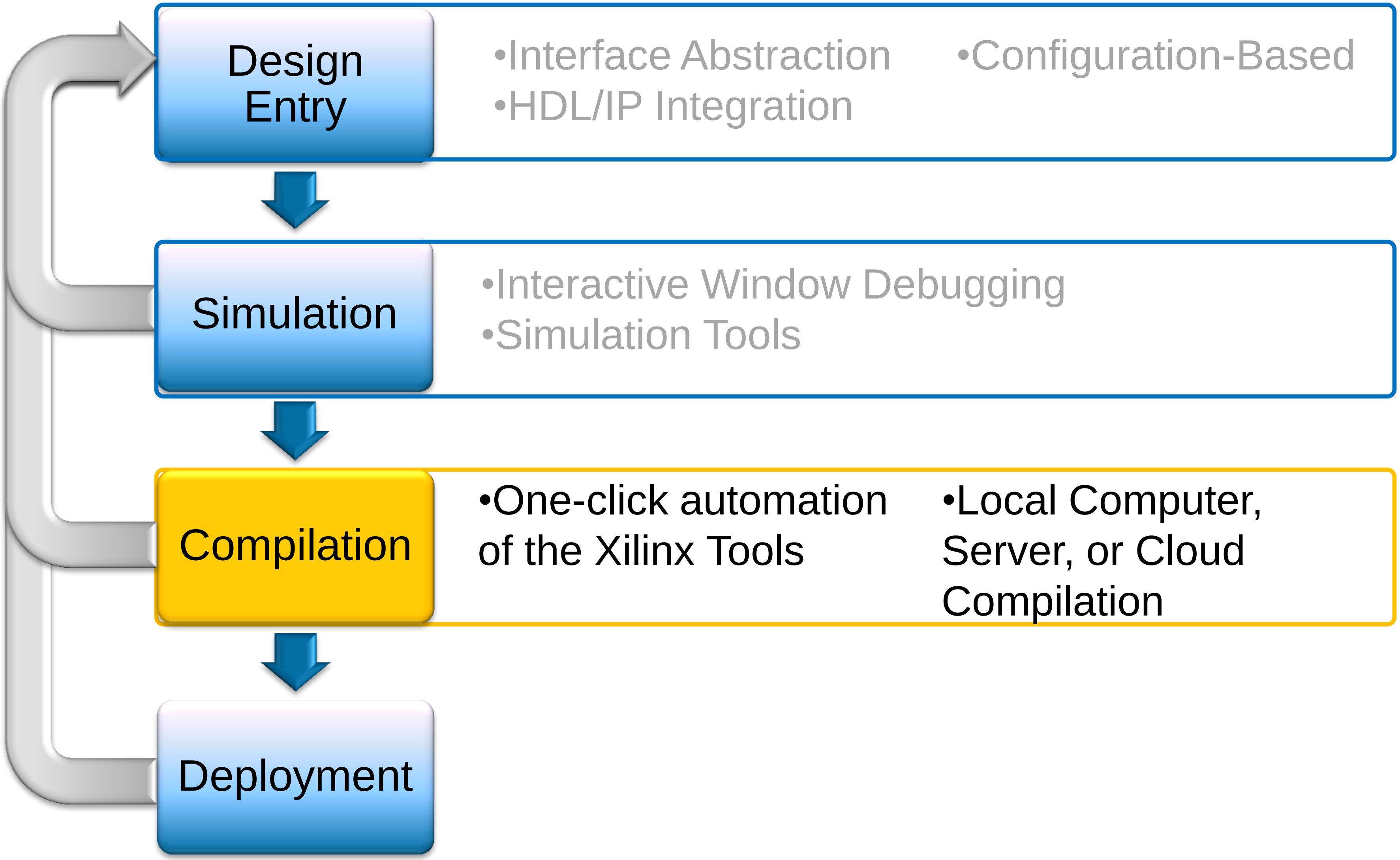


Period and Phase Measurement.vi Block Diagram on Period and Phase Measurement.lvproj/FPGA Target *

Period and Phase Measurement.lvproj/FPGA Target

Simulator offers bit-true simulation

Simplified FPGA Design Flow



Design Entry

- Interface Abstraction
- HDL/IP Integration
- Configuration-Based

Simulation

- Interactive Window Debugging
- Simulation Tools

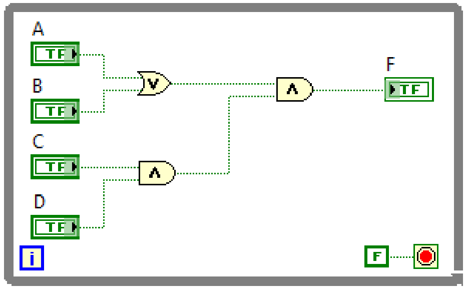
Compilation

- One-click automation of the Xilinx Tools
- Local Computer, Server, or Cloud Compilation

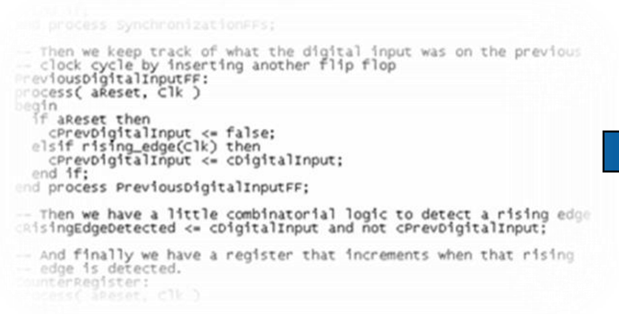
Deployment

Compilation Process

LabVIEW FPGA Code



Compile VHDL through Xilinx

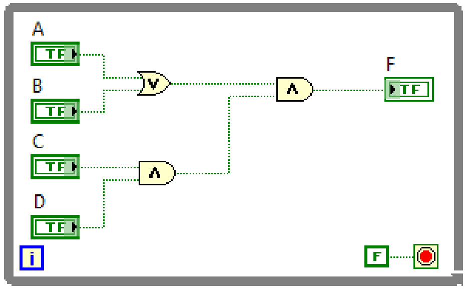


```
end if;
end process SynchronizationFFs;

-- Then we keep track of what the digital input was on the previous
-- clock cycle by inserting another flip flop
PreviousDigitalInputFF:
process( aReset, Clk )
begin
  if aReset then
    cPrevDigitalInput <= false;
  elsif rising_edge(Clk) then
    cPrevDigitalInput <= cDigitalInput;
  end if;
end process PreviousDigitalInputFF;

-- Then we have a little combinatorial logic to detect a rising edge
cRisingEdgeDetected <= cDigitalInput and not cPrevDigitalInput;

-- And finally we have a register that increments when that rising
-- edge is detected.
CounterRegister:
process( aReset, Clk )
```

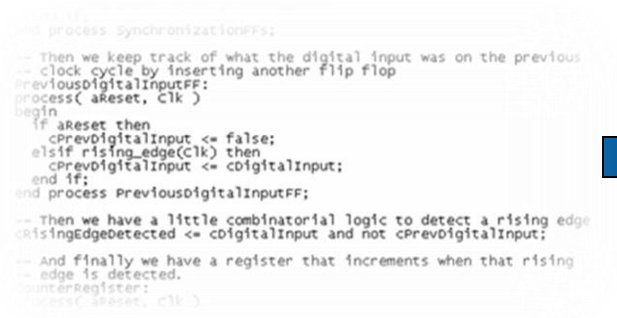
FPGA Logic Implementation

Compilation Process

LabVIEW FPGA Code



Compile VHDL through Xilinx



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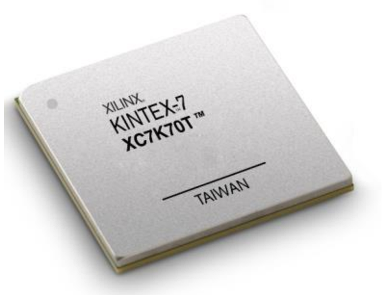
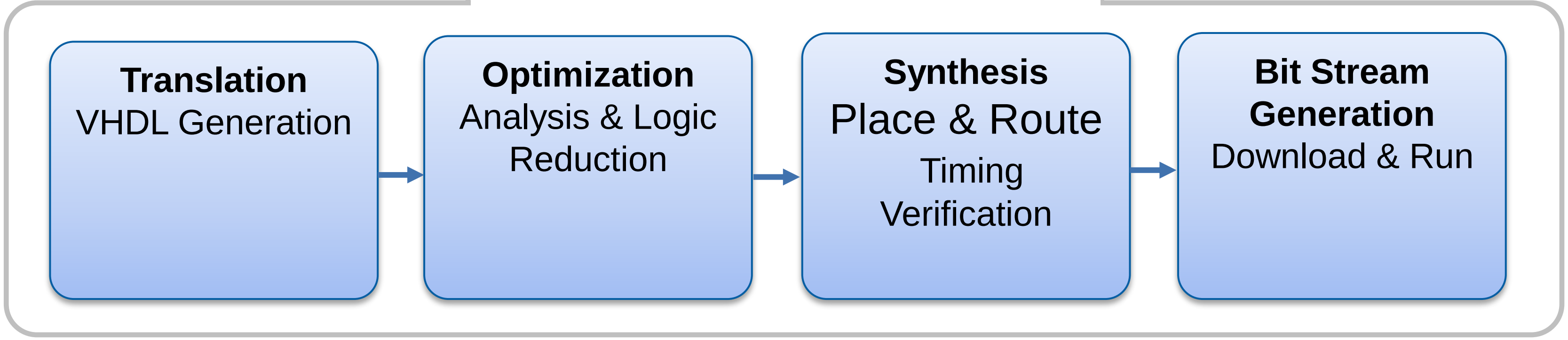
FPGA Logic Implementation





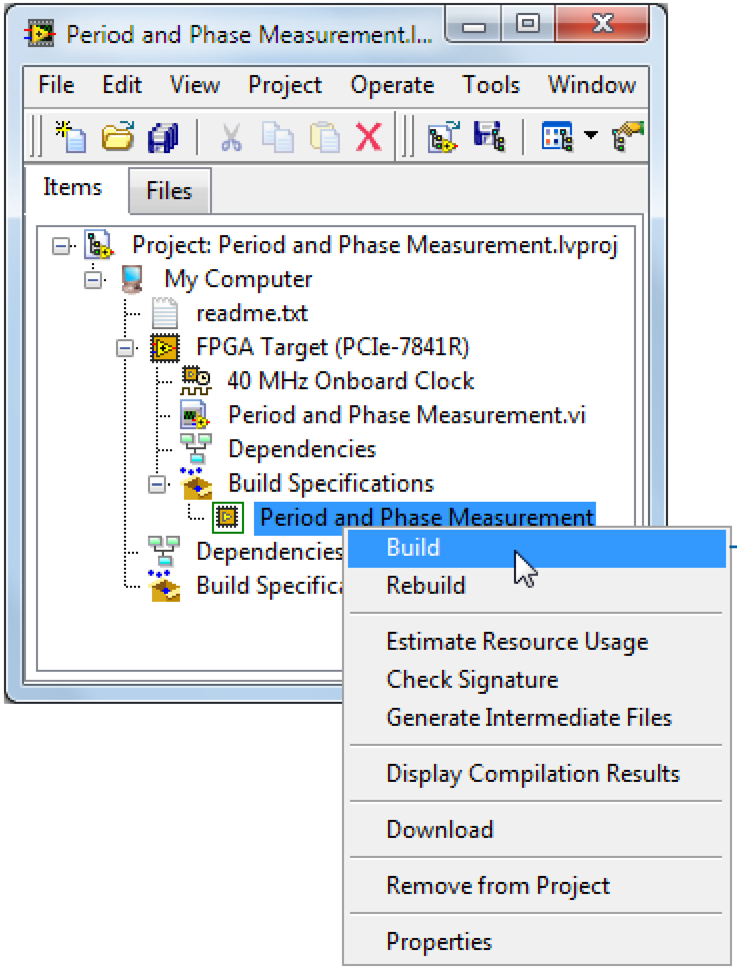
Translation
VHDL Generation

Optimization
Analysis & Logic Reduction

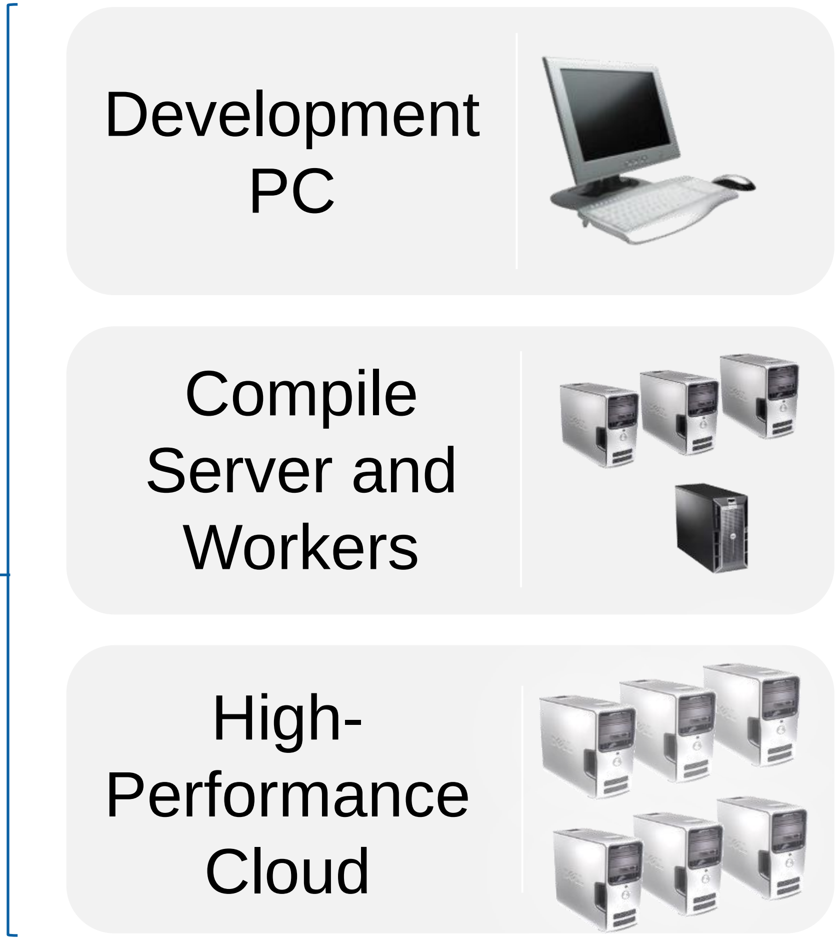
Synthesis
Place & Route
Timing Verification

Bit Stream Generation
Download & Run

One-Click Deployment and Compilation



Project: Period and Phase Measurement.lvproj
My Computer
readme.txt
FPGA Target (PCIe-7841R)
40 MHz Onboard Clock
Period and Phase Measurement.vi
Dependencies
Build Specifications
Period and Phase Measurement
Dependencies
Build Specifica

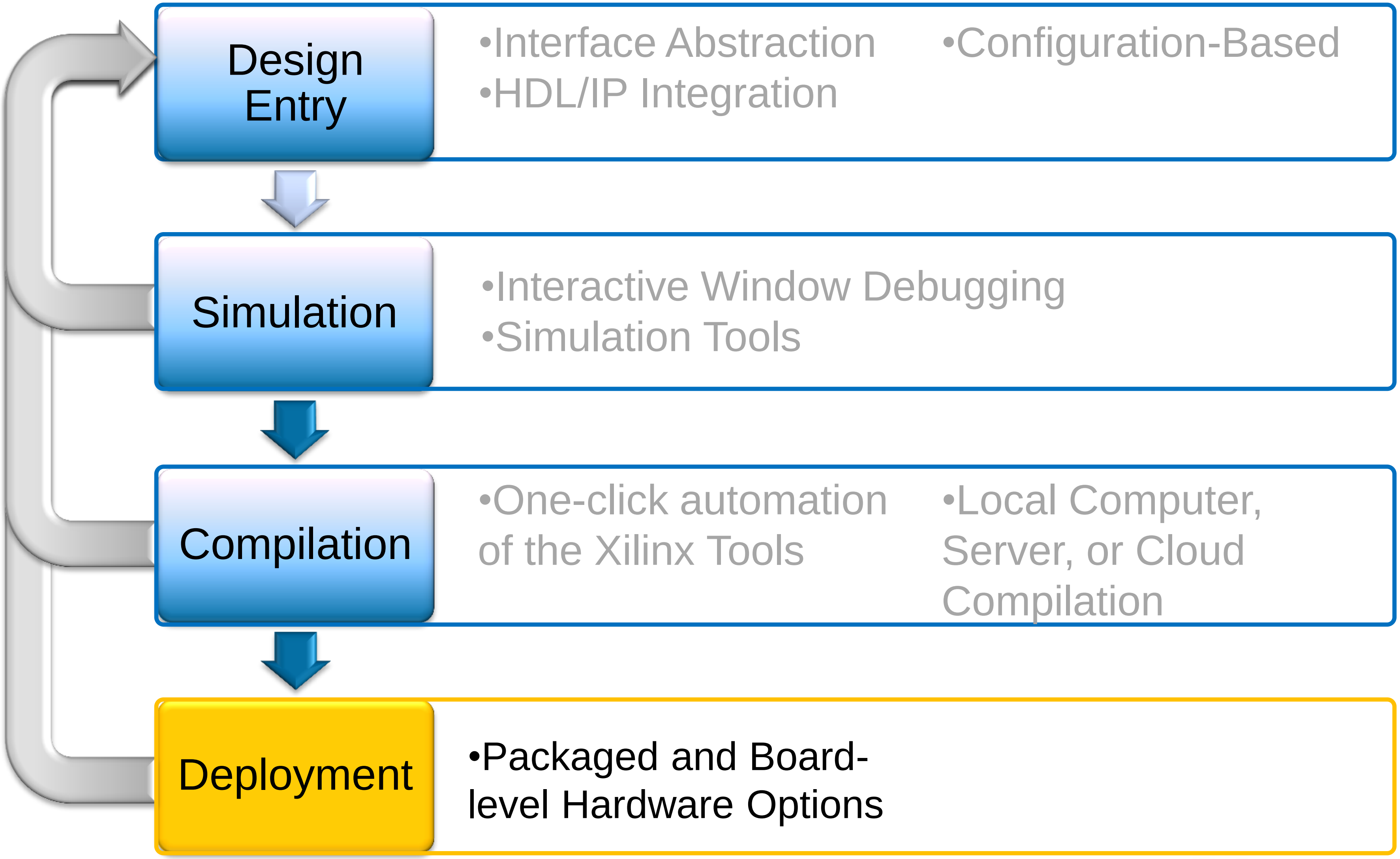


Development PC

Compile Server and Workers

High-Performance Cloud

Simplified FPGA Design Flow



Design Entry

- Interface Abstraction
- HDL/IP Integration
- Configuration-Based

Simulation

- Interactive Window Debugging
- Simulation Tools

Compilation

- One-click automation of the Xilinx Tools
- Local Computer, Server, or Cloud Compilation

Deployment

- Packaged and Board-level Hardware Options

LabVIEW RIO Hardware

CompactRIO and NI Single-Board RIO

Value

Ultra Rugged

Performance

PXI, PC RIO (R Series, NI FlexRIO)

High Performance

Expansion I/O

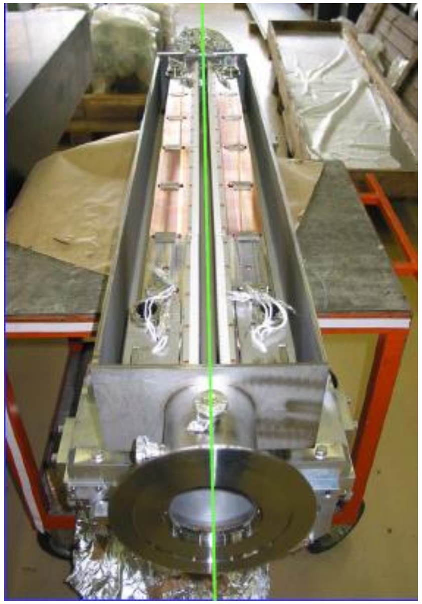
MXI-Express RIO

Ethernet RIO

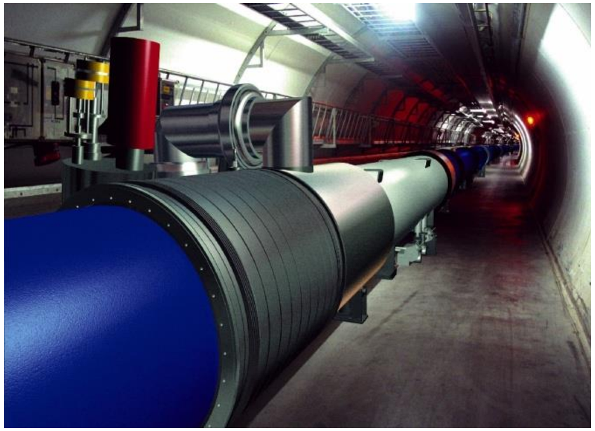
EtherCAT RIO

Wireless

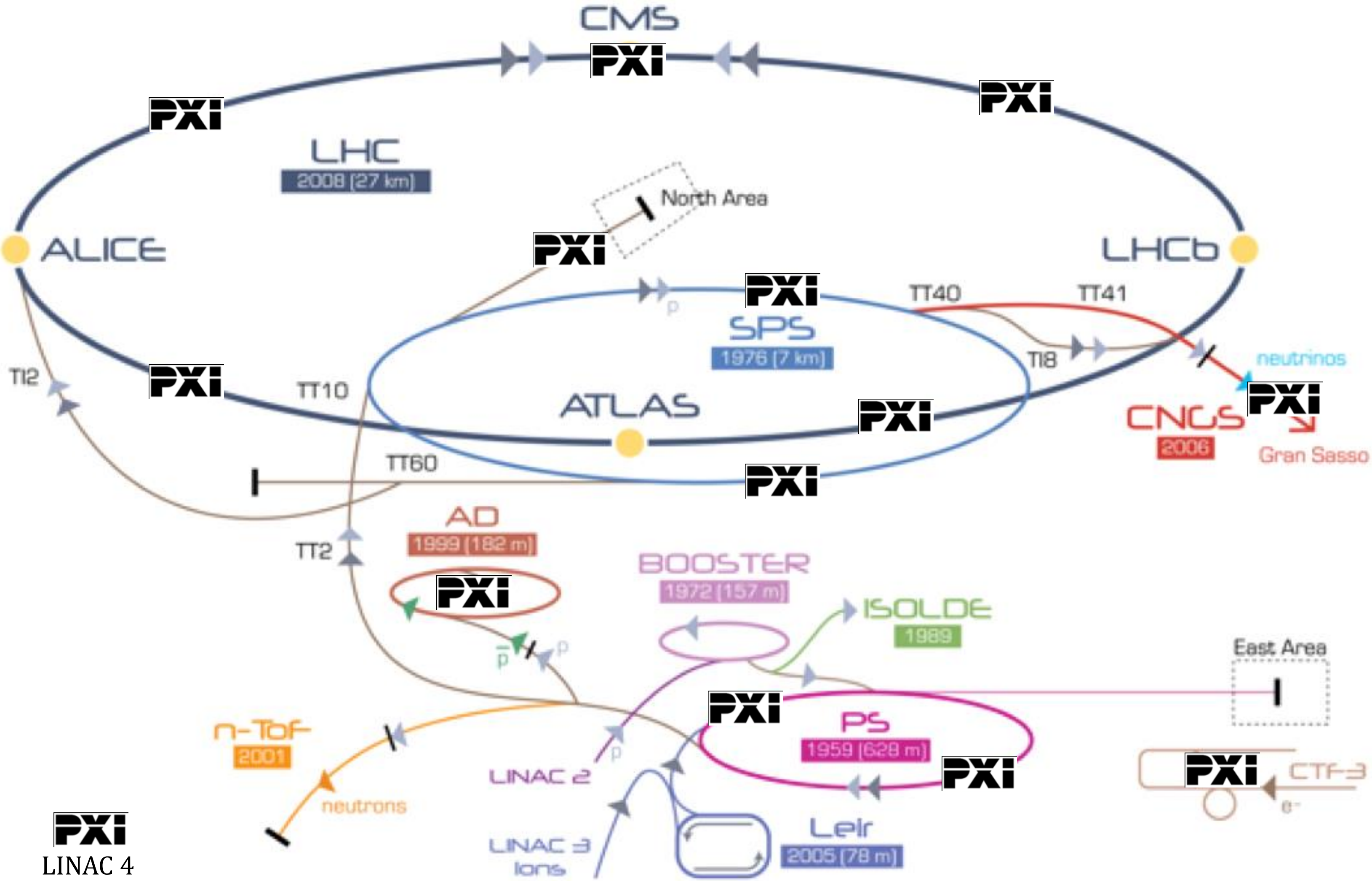
LHC Collimator Control



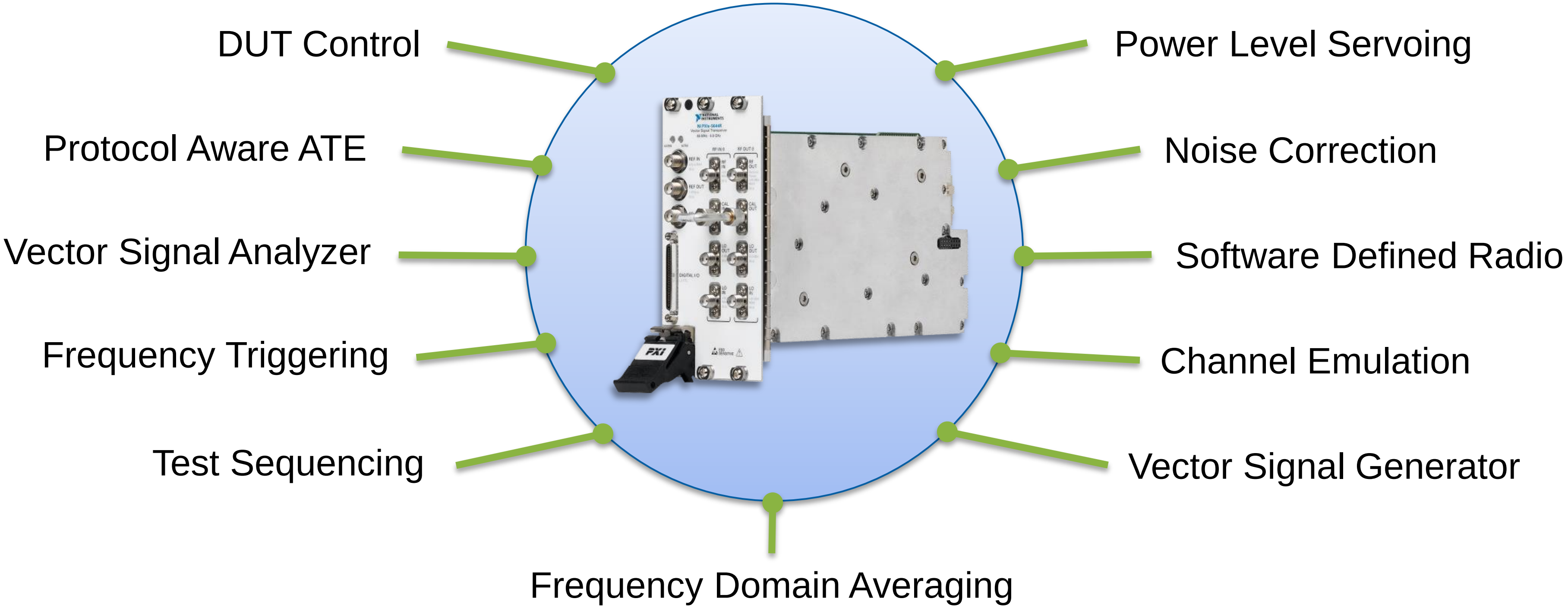
- 550+ axes of motion
- Across 27 km distance
- The jaws have to be positioned with an accuracy which is a fraction of the beam size (200µm)
- Synchronized to
  - < 5ms drift over 15 minutes
  - Maximum jitter in µs



PXI in CERN Accelerator Complex



Software-Designed Instrumentation



DUT Control

Protocol Aware ATE

Vector Signal Analyzer

Frequency Triggering

Test Sequencing

Power Level Servoing

Noise Correction

Software Defined Radio

Channel Emulation

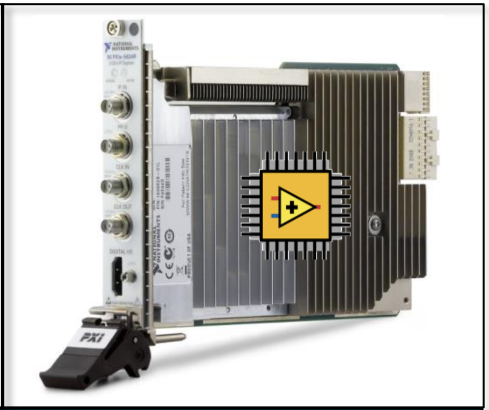
Vector Signal Generator

Frequency Domain Averaging

New Software Designed Instruments

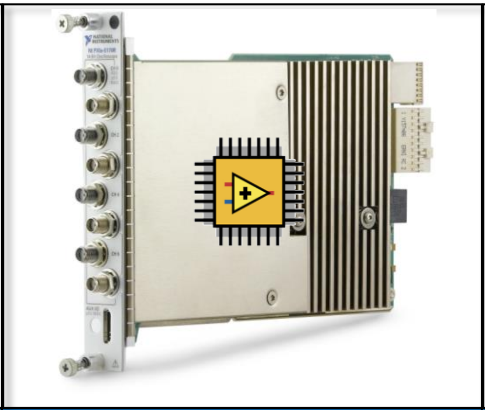
PXIe-5668R
26.5 GHz, >500 MHz
RTBW VSA

PXIe-5654
20 GHz, -110dBm to +20dBm
Signal Source



PXIe-5624R
2 GS/s, 12-bit
IF Digitizer

NI PXIe-6591/92R
12.5 Gbps, 4-8 ch.
High Speed Serial

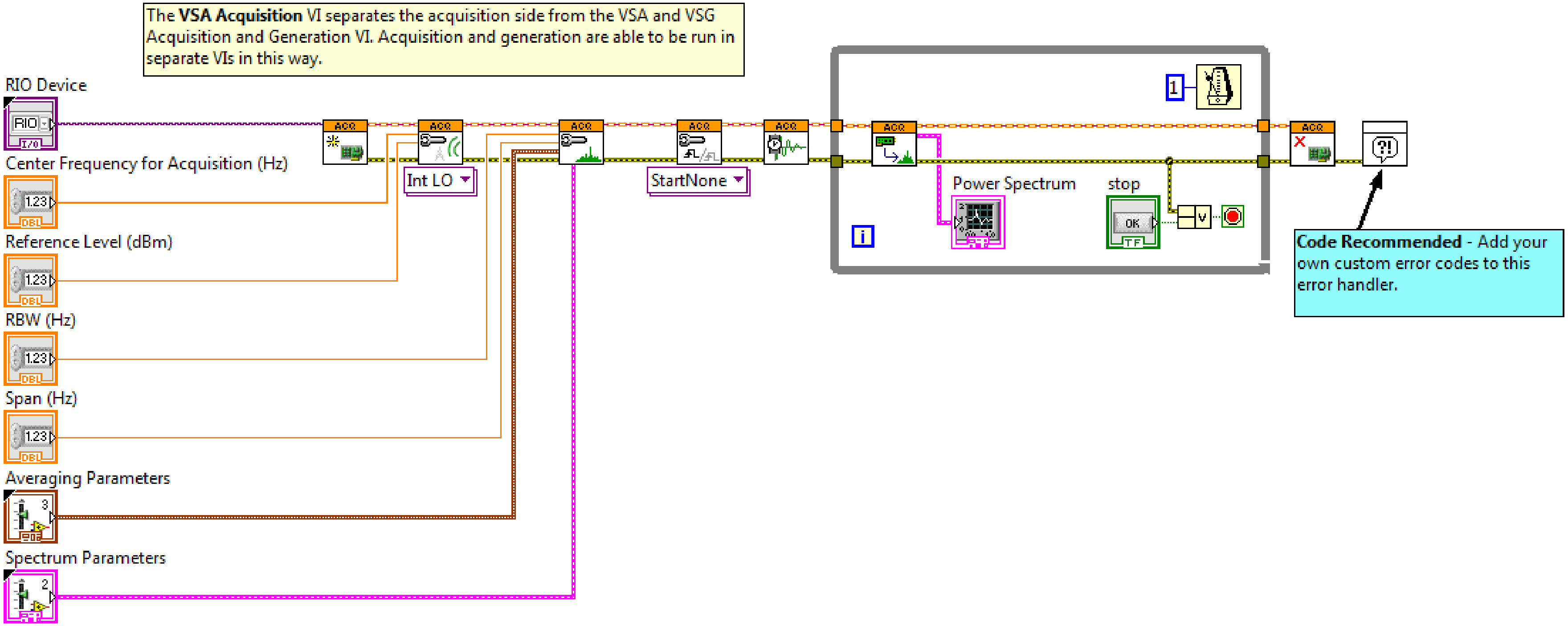


PXIe-5170/71R
250 MS/s, 14-bit, 4-8 ch.
Oscilloscope

PXIe-7976R
3.5GB/s Streaming
K410T K7 FlexRIO

Software-Designed Instrumentation

Completely Open-Source Driver Ensures Ultimate Flexibility

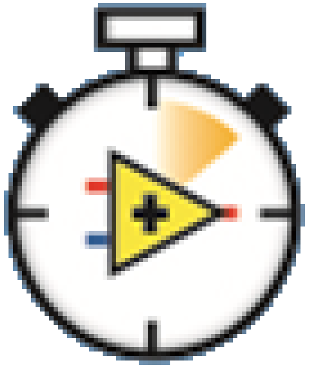


The **VSA Acquisition** VI separates the acquisition side from the VSA and VSG Acquisition and Generation VI. Acquisition and generation are able to run in separate VIs in this way.

Code Recommended - Add your own custom error codes to this error handler.

The vector signal transceiver is ready to run out of the box, but the driver is written entirely in LabVIEW, giving you direct access to the instruments I/O.

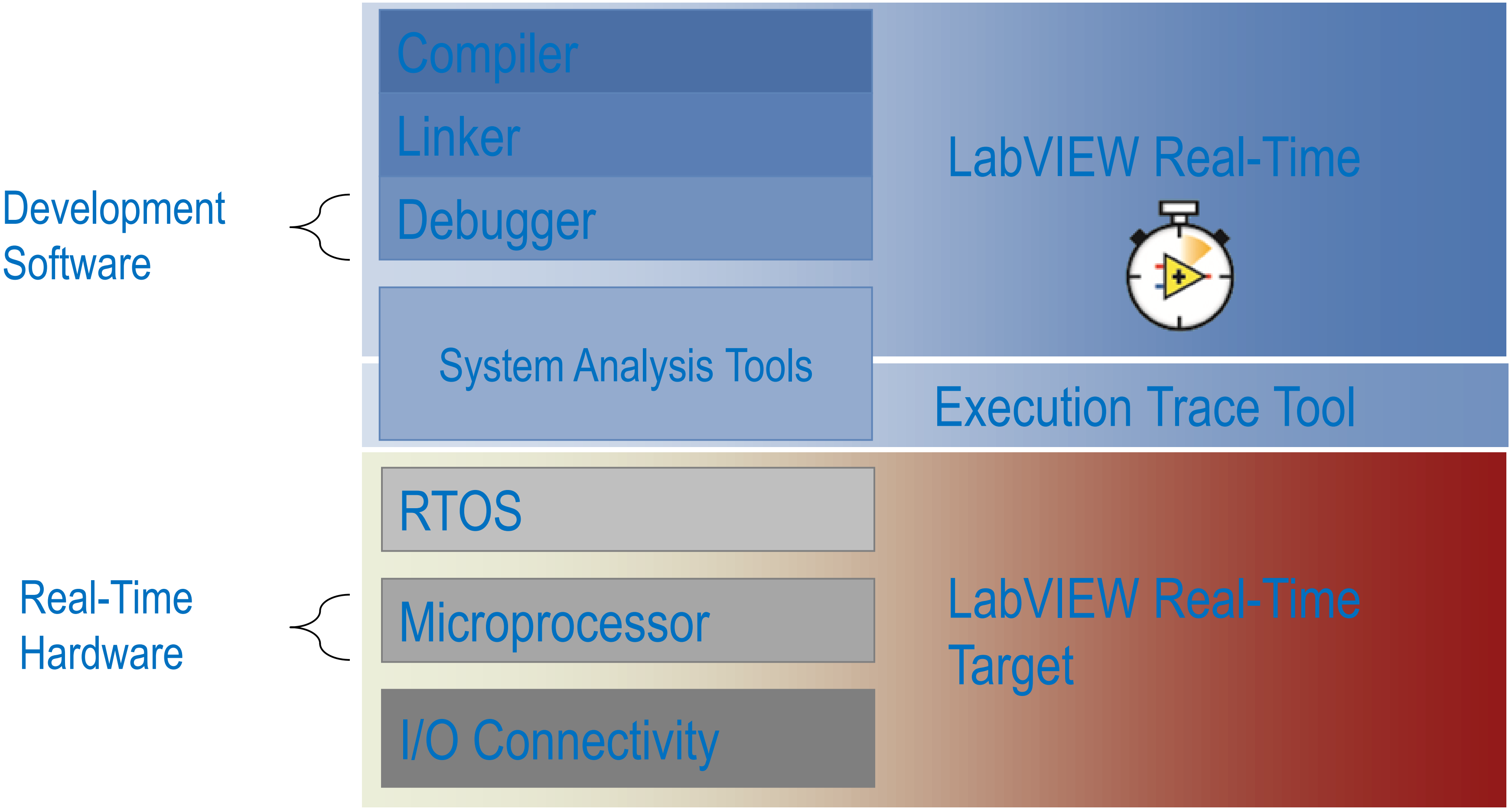
Introduction to LabVIEW Real-Time



What is Real-Time?

- Real-time **does not** always mean really fast
- Real-time means **absolute reliability**
- Real-time systems have timing constraints that must be met to avoid failure
- Determinism is the ability to complete a task within a fixed amount of time

Real-Time Development Tools



Development Software

Compiler

Linker

Debugger

System Analysis Tools

LabVIEW Real-Time

Execution Trace Tool

Real-Time Hardware

RTOS

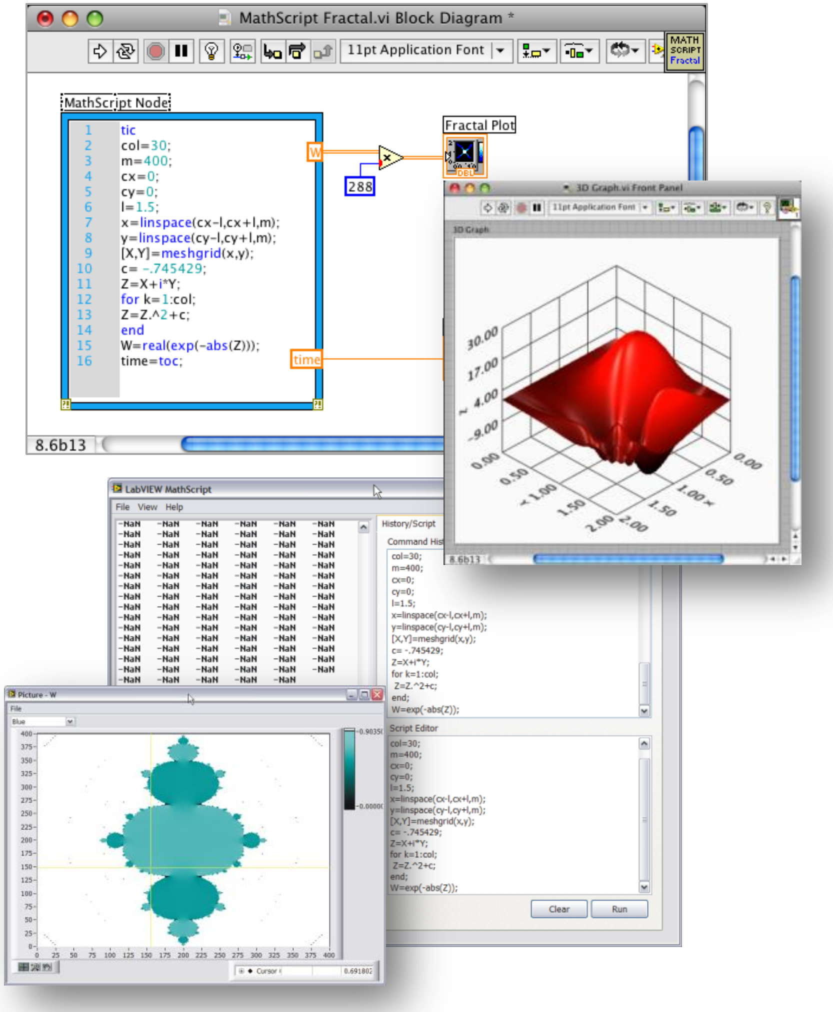
Microprocessor

I/O Connectivity

LabVIEW Real-Time Target

LabVIEW MathScript RT Module

- **Text-based controls, signal processing, analysis, and math**
  - 900 built-in functions / user-defined functions
  - Reuse many of your .m file scripts created with The MathWorks, Inc. MATLAB® software and others
- **A native LabVIEW solution**
  - Interactive and programmatic interfaces
  - Does not require 3rd-party software
  - Enables hybrid programming



```
tic
col=30;
m=400;
cx=0;
cy=0;
l=1.5;
x=linspace(cx-l,cx+l,m);
y=linspace(cy-l,cy+l,m);
[X,Y]=meshgrid(x,y);
c= -.745429;
Z=X+i*Y;
for k=1:col;
Z=Z.^2+c;
end
W=real(exp(-abs(Z)));
time=toc;
```

```
col=30;
m=400;
cx=0;
cy=0;
l=1.5;
x=linspace(cx-l,cx+l,m);
y=linspace(cy-l,cy+l,m);
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Z=X+i*Y;
for k=1:col;
 Z=Z.^2+c;
end;
W=exp(-abs(Z));
```
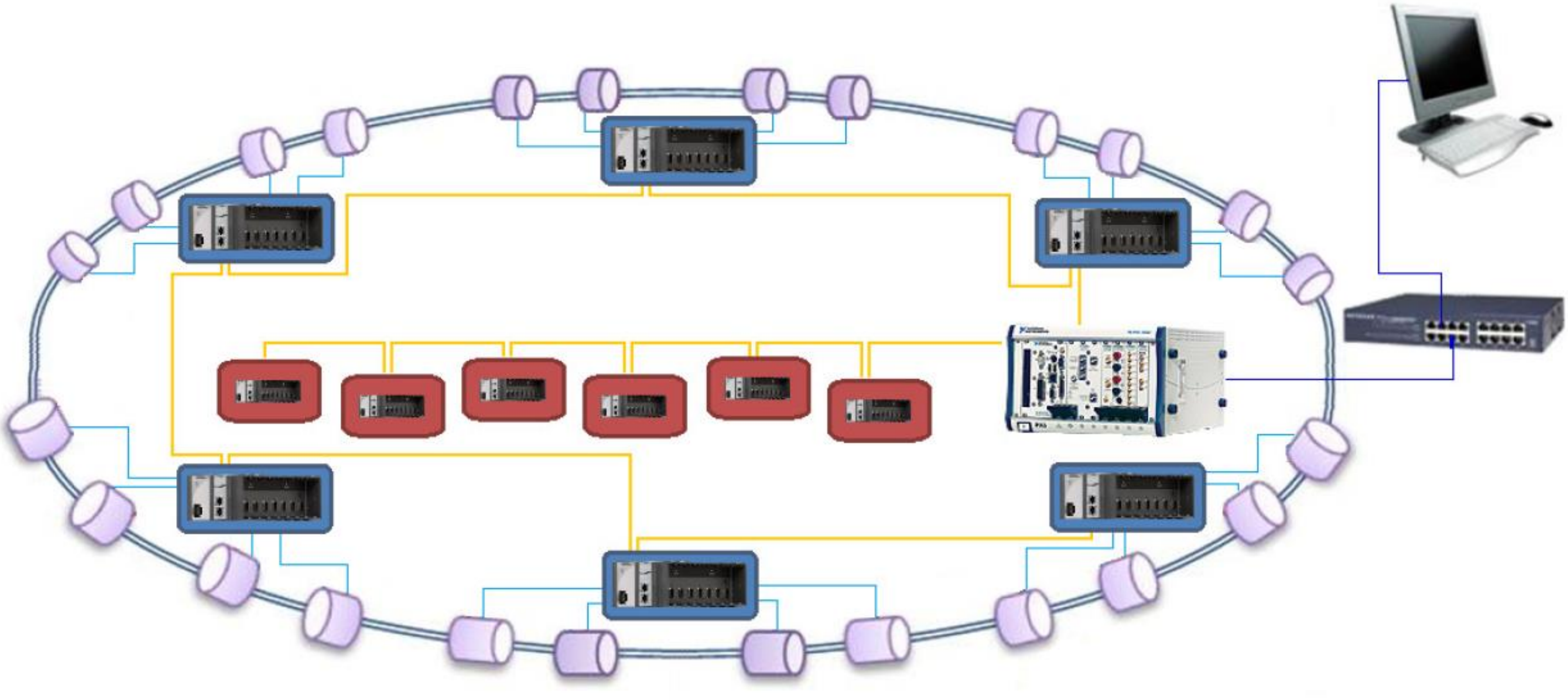

MATLAB® is a registered trademark of The MathWorks, Inc..

CAMAC Systems replaced with by cRIO+EPICS+LabVIEW FPGA

LNLS (Brazil): FOFB Control System

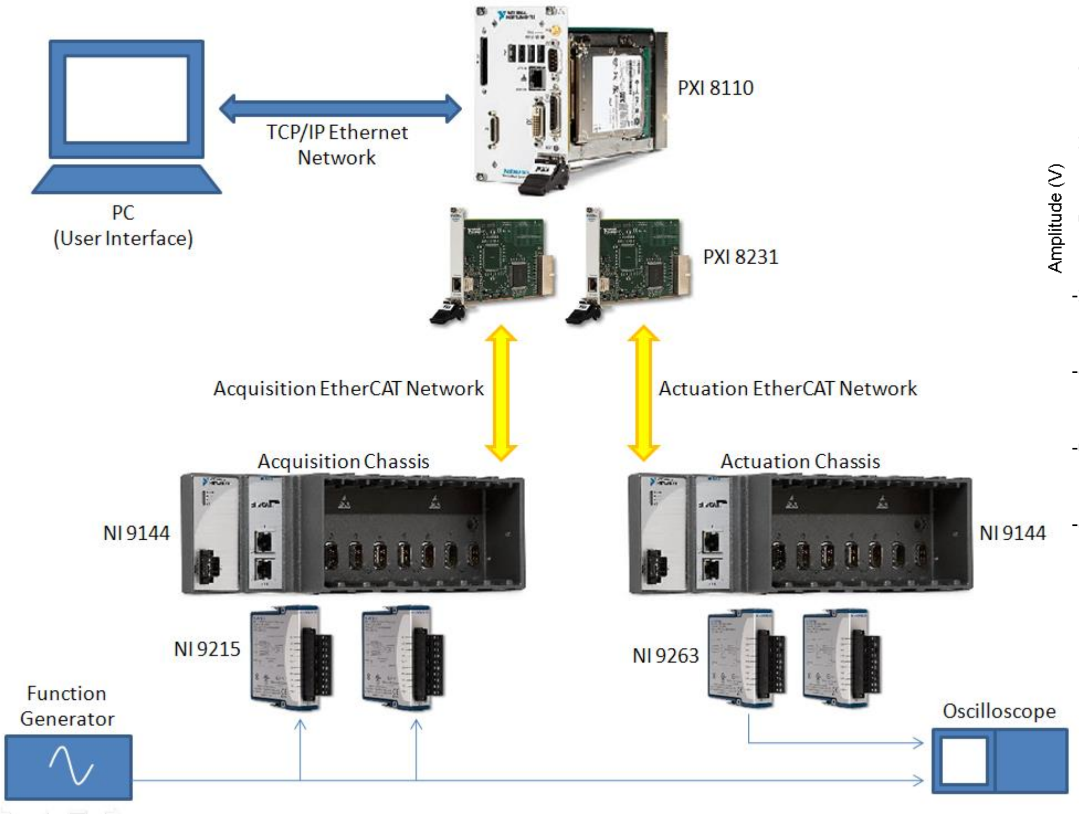


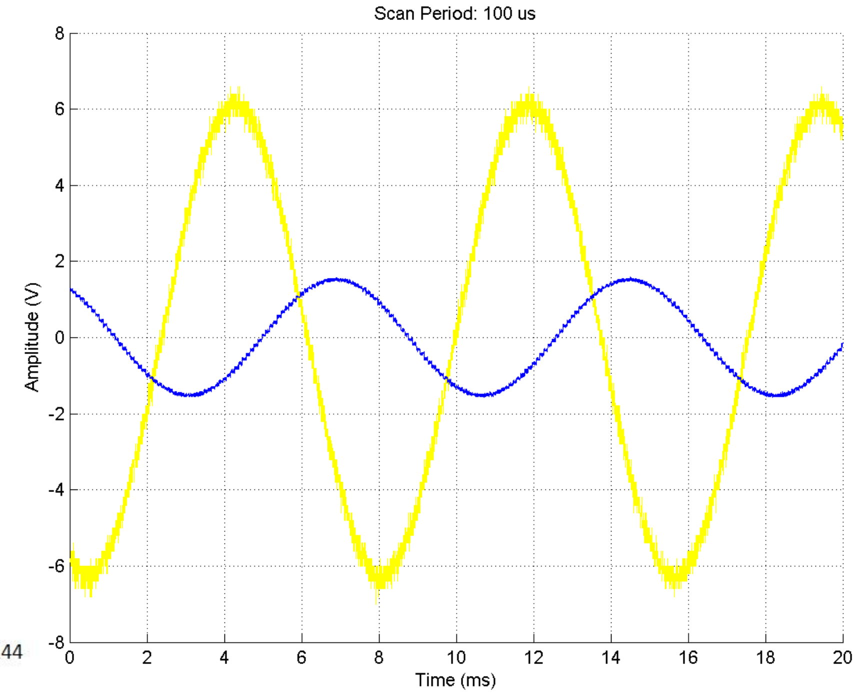
⬭	BPM + Sterring Magnets
🟦	EtherCAT cRIO (AI)
🟥	Steering Magnets Power Supplies + cRIO (AI AO DIO)

─	Conditioned signals
─	Ethernet network
─	EtherCAT network

FOFB Control System

System Validation: Speed

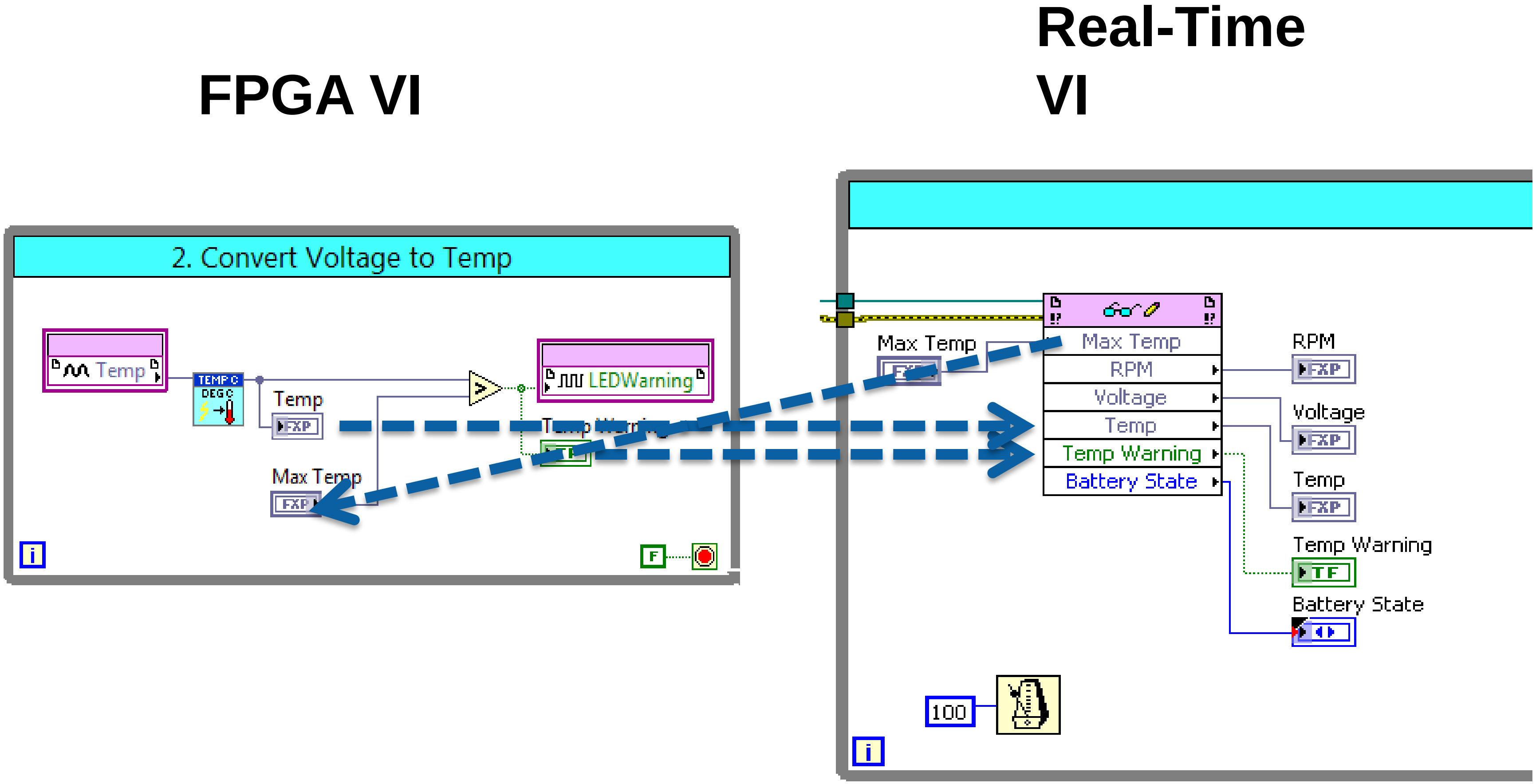




MIMO system @ 5KHz

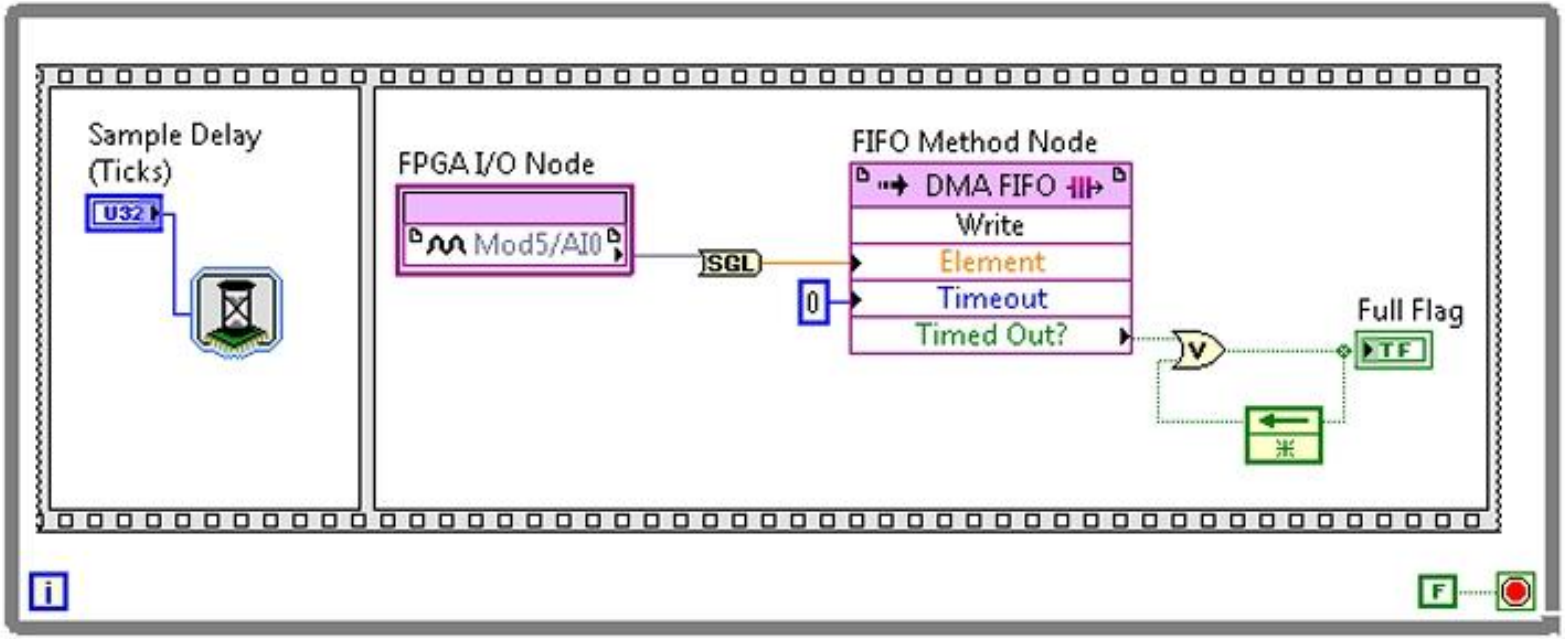
15x improvement !

FPGA ←→ RT: FPGA Read/Write Controls

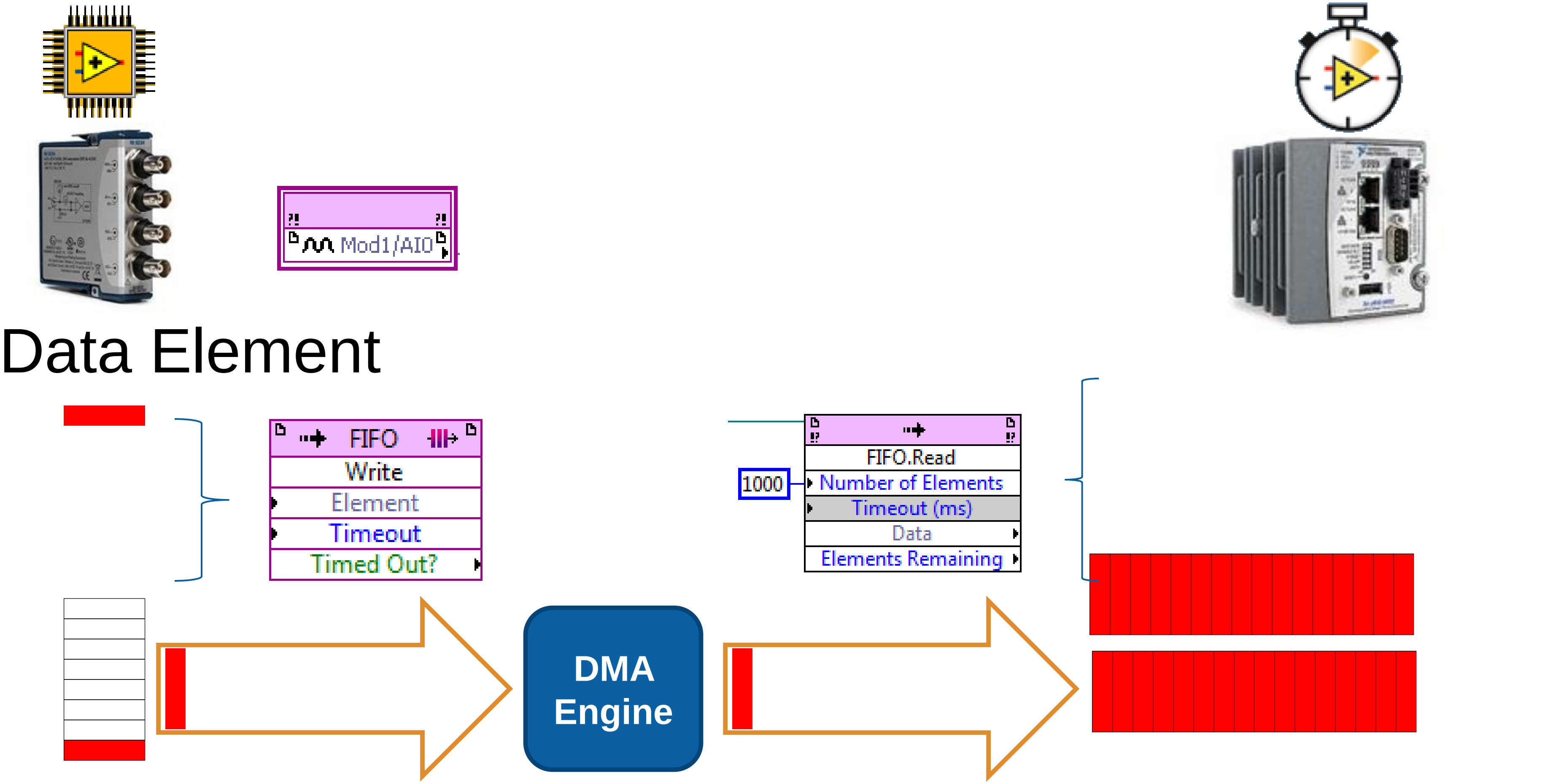


FPGA ←→ RT: Direct Memory Access (DMA) FIFOs

- DMA FIFOs are an efficient mechanism for streaming data from the FPGA to RT Processor
- Most RIO hardware targets have 3 dedicated DMA channels



FPGA ←→ RT: DMA FIFOs



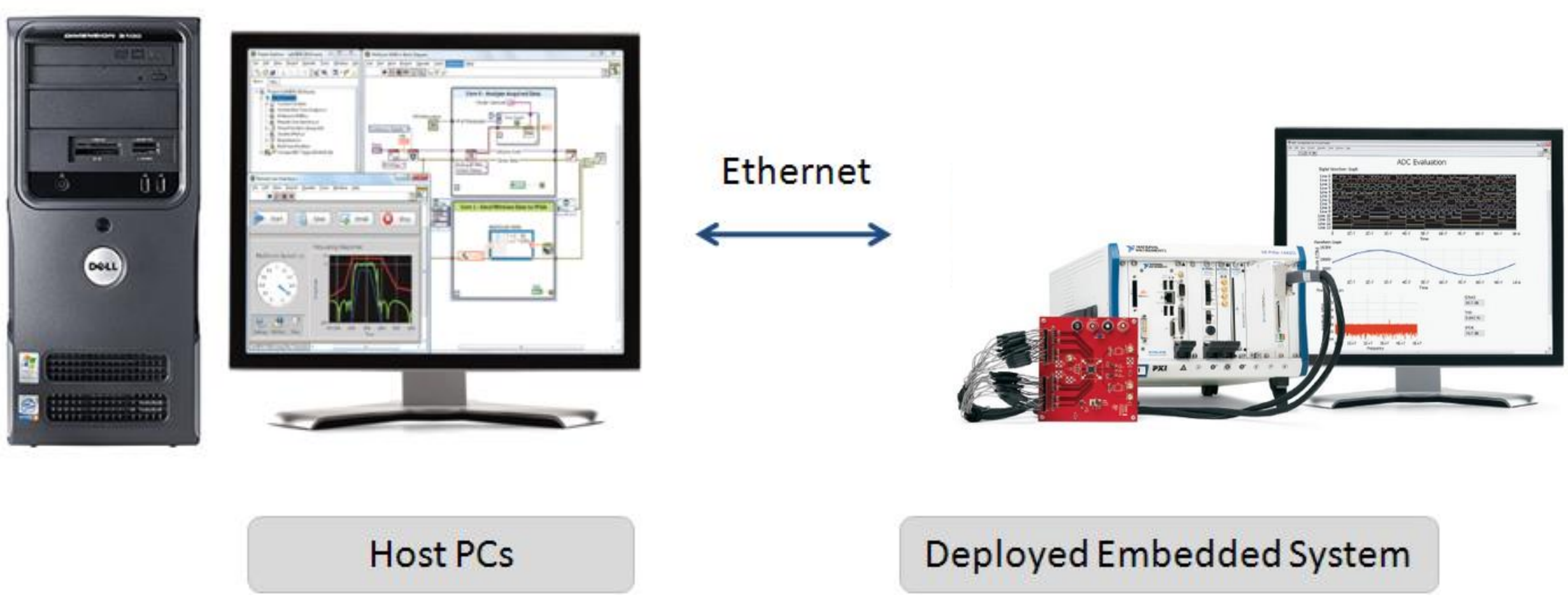
Data Element

FPGA DMA FIFO

Real-Time Buffer

Real-Time Processor ←→ Network

- Communicating with Development PC, distributed targets
- Real-Time VI front panel should only be used for debugging
- Embedded targets are designed to run headlessly
  - Often no graphics support



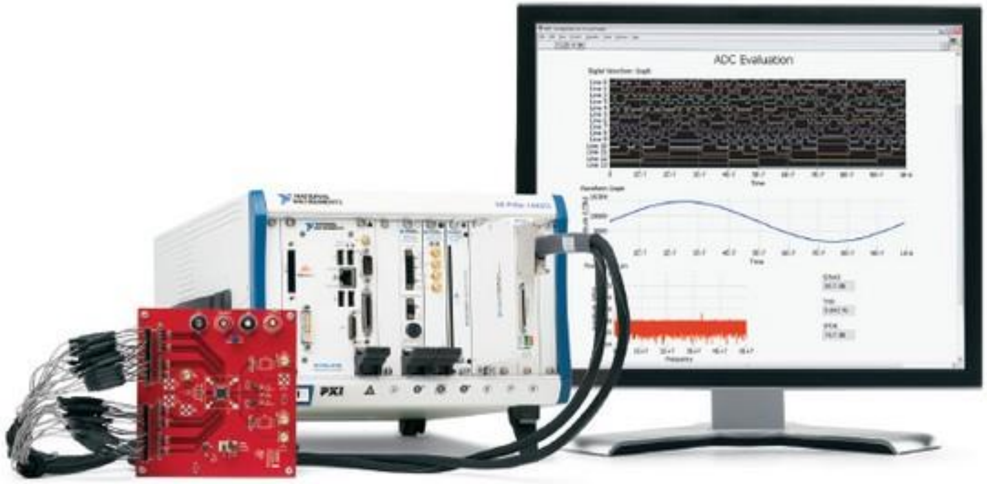
Ethernet

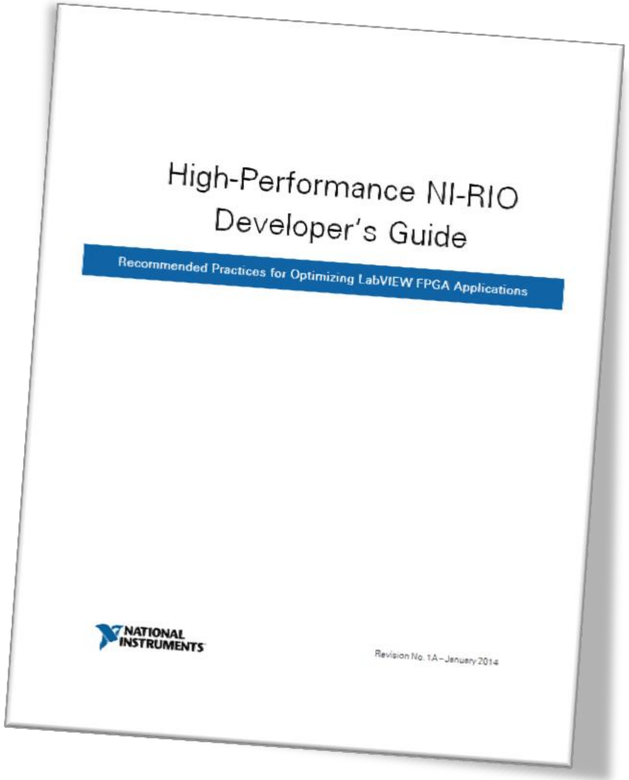
Host PCs

Deployed Embedded System

LabVIEW High-Performance FPGA Developer's Guide

- LabVIEW single-cycle Timed Loop programming
- Throughput, latency, and resource optimization techniques
- HDL and third-party IP integration
- Data transfer mechanisms




High-Performance NI-RIO
Developer's Guide

Recommended Practices for Optimizing LabVIEW FPGA Applications

NATIONAL INSTRUMENTS

Revision No. 1A – January 2014

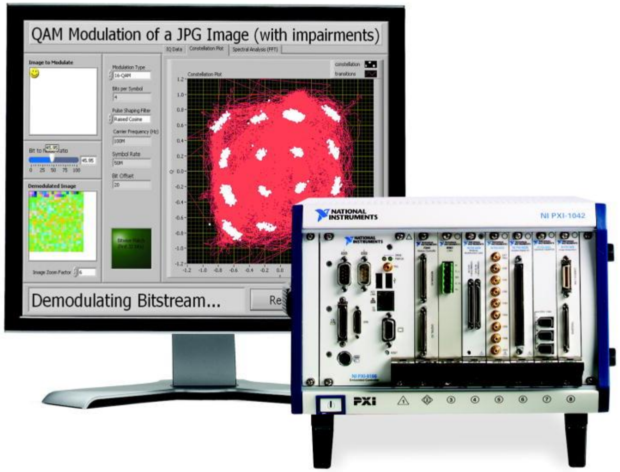
ni.com/hprioguide

Control & Monitoring SuperKEKB Vacuum System

- 300 cold cathode gauges
- Residual gas analyzers
- Vacuum switches
- 300 wheel type flow meters
- 6000 Platinum resistance thermometer sensors
- All measurements every 1 or 2 seconds and data recorded (several minutes) - All above data controlled by EPICS
- All of the above controlled and measured using LabVIEW-FPGA, cRIO & EPICS (in cRIO)
    - Controlled remotely from control room
    - Highly reliable control and alarm system

Addressing Big Physics Application Requirements

Platforms and Standards


QAM Modulation of a JPG Image (with impairments)
Demodulating Bitstream...
NATIONAL INSTRUMENTS
NI PXI-1042
PXI

More than 1,500 PXI Products from More than 70 Vendors

DAQ and Control:

- Multifunction I/O
- FPGA/Reconfigurable I/O
- Digital I/O
- Analog Input/Output
- Vision and Motion
- Counter/Timers

Instruments:

- Oscilloscopes
- Digital Waveform Generator/Analyzers
- Digital Multimeters
- Signal Generators
- Switching
- RF Signal Generation and Analysis

Interfaces:

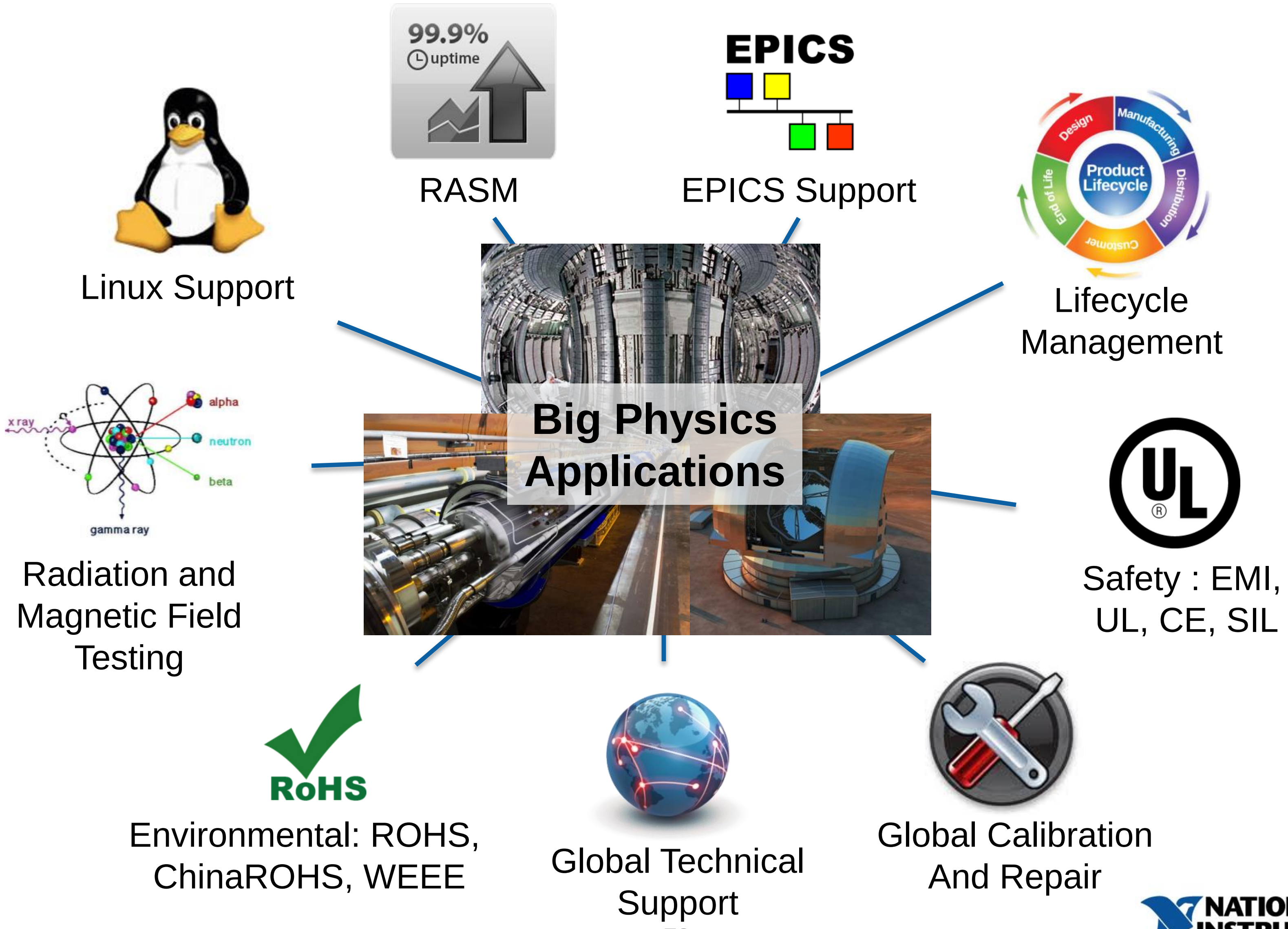
- GPIB, USB, LAN
- SCSI + Enet
- Boundary Scan/JTAG
- CAN + DeviceNet
- RS232/RS485
- VXI/VME

Features and Specifications

- **Analog Input**
  - Up to 250 kS/s, simultaneous sampling
  - 4, 8, 16, and 32-ch options
  - Built-in signal condition for sensors
    - Strain gages, accelerometers, thermocouples, RTDs
  - Up to ± 60 V, ±20 mA
  - 12, 16 and 24-bit resolution
  - Available ch-to-ch isolation
- **Analog Output**
  - Up to100 kS/s simultaneous updating
  - Up to 16-ch per module
  - ±10 V, ±20 mA
  - Isolation

- **Digital I/O**
  - Up to 10 MHz timing
  - Counter/timer, PWM
  - 8 and 32-channel options
  - 5V/TTL, 12/24/48 V logic levels
- **Specialty**
  - 2-port CAN modules
  - Brushed DC servo motor drive
- **Third Party Modules**
  - LIN, Profibus, WLAN 802.11, MIL-1553, ARINC-429, GPS, and more

BP Application Special Requirements



Big Physics Applications

Linux Support

RASM

EPICS Support

Lifecycle Management

Radiation and Magnetic Field Testing

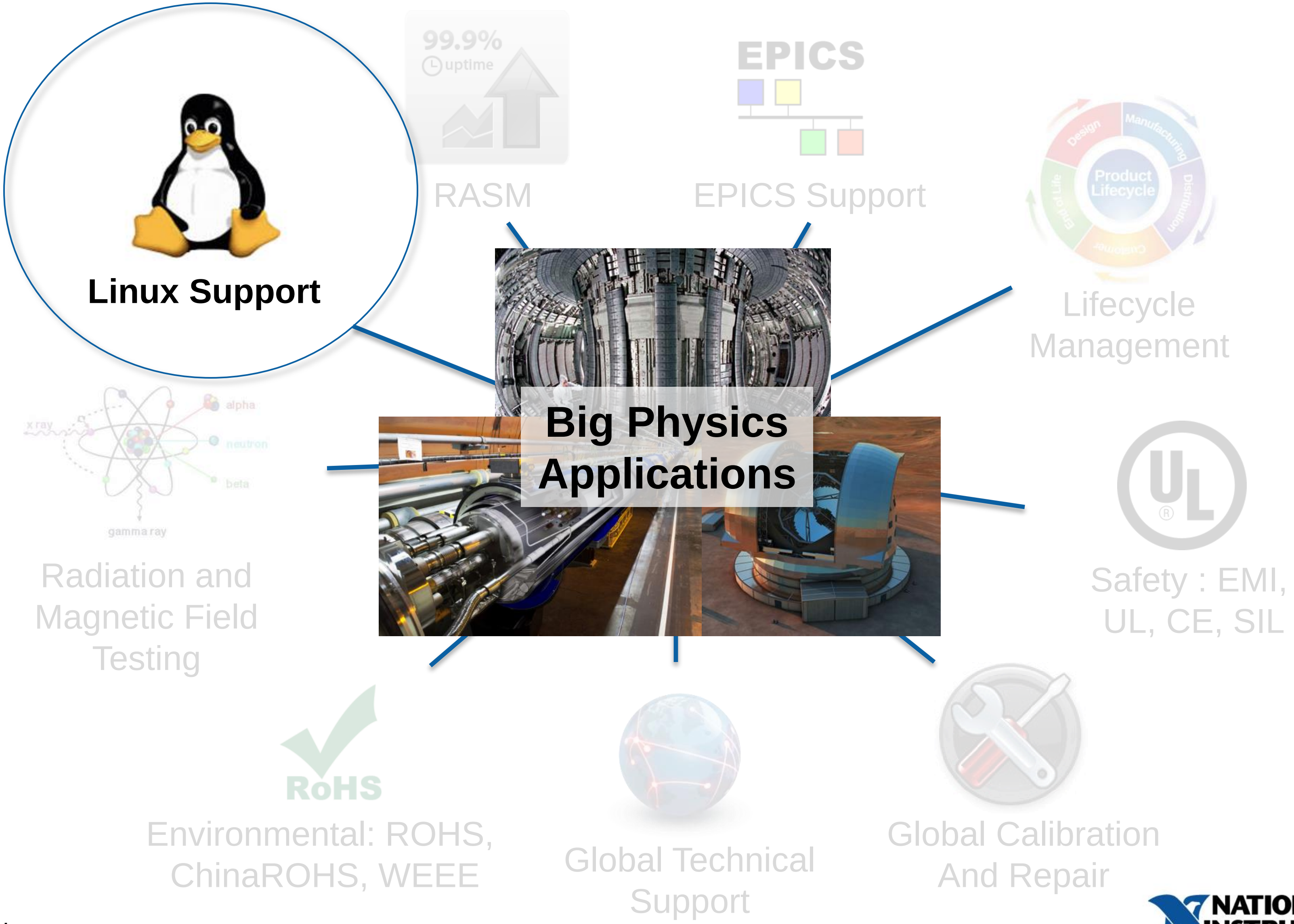
Safety : EMI, UL, CE, SIL

Environmental: ROHS, ChinaROHS, WEEE

Global Technical Support

Global Calibration And Repair

Linux Support



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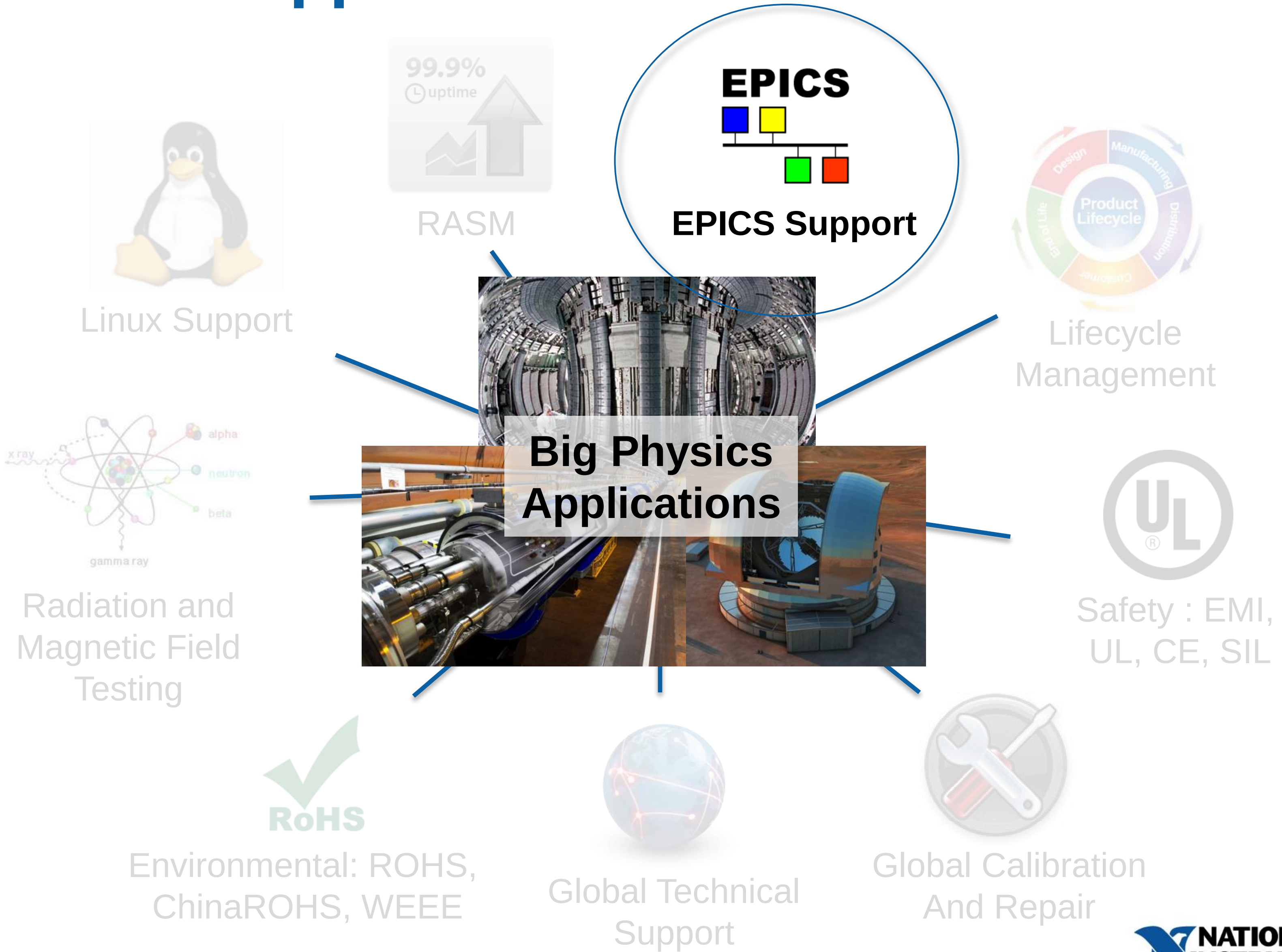
Linux Integration - Summary

Hardware	Customer Custom Driver Development	NI Custom Open Source Driver	Platform Integrated
Measurement HW	MHDDK	ITER	DAQmx Linux, Hypervisor
RIO	FPGA interface C API	ITER	API, Hypervisor

EPICS Support



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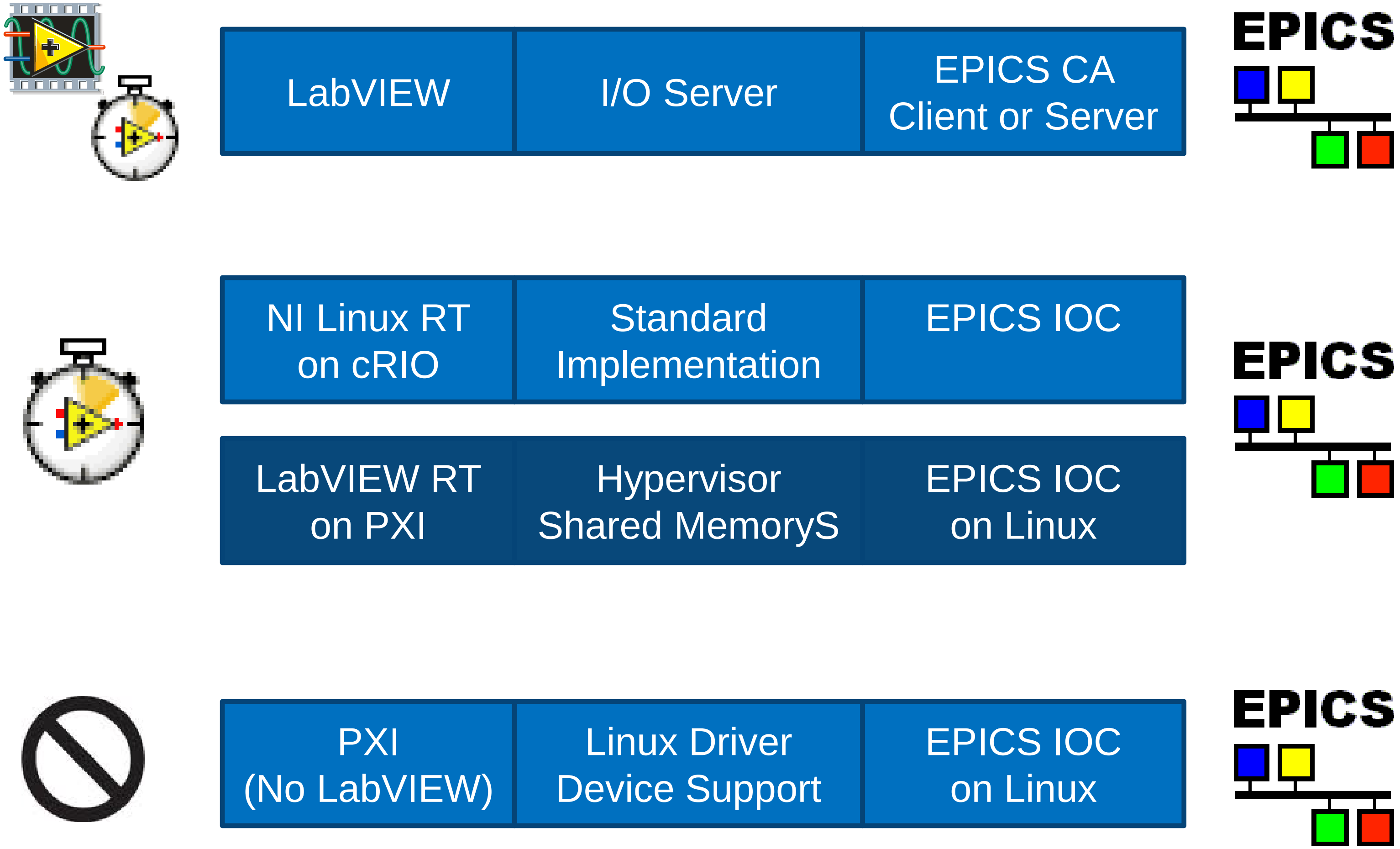
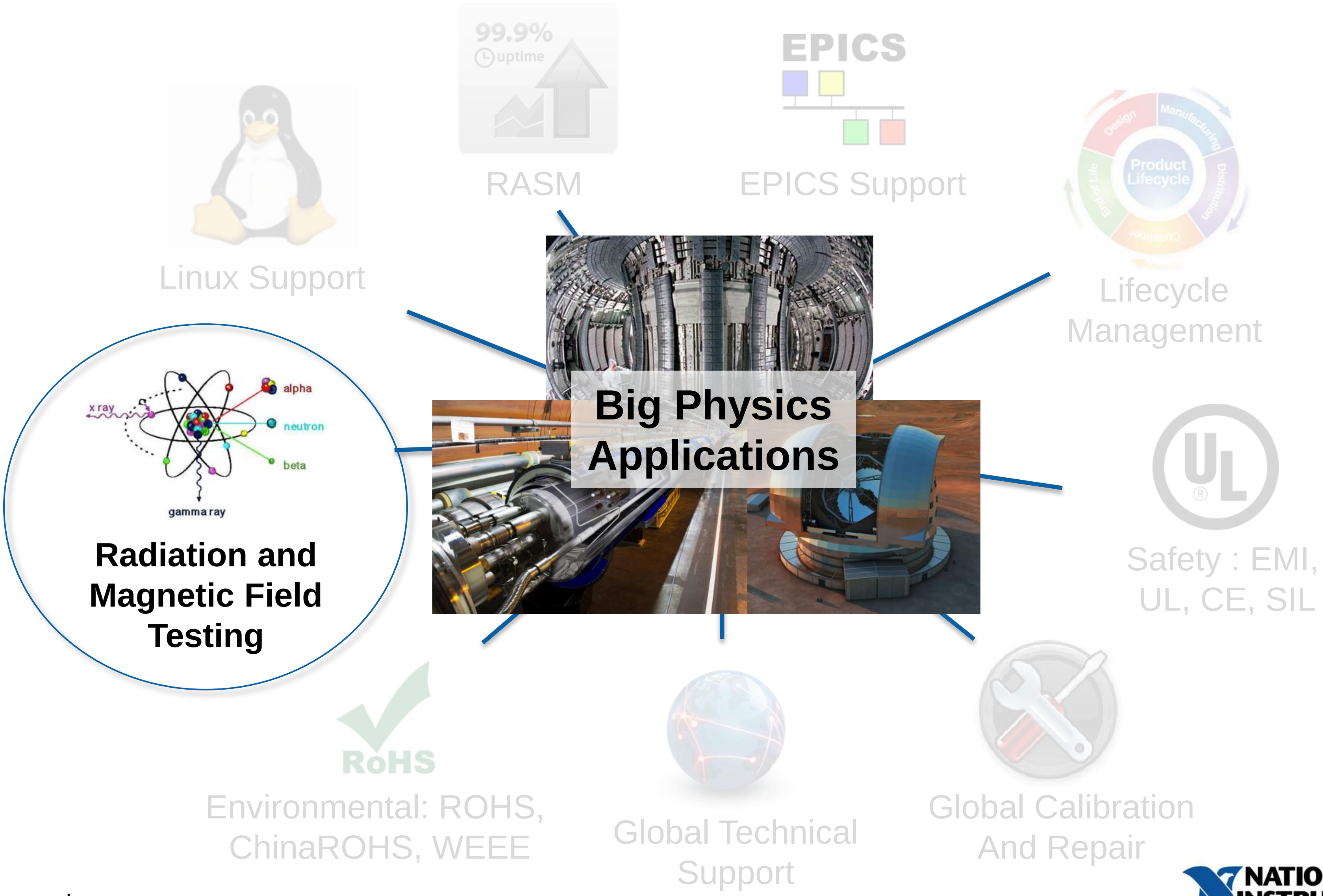
EPICS Integration



LabVIEW	I/O Server	EPICS CA Client or Server
NI Linux RT on cRIO	Standard Implementation	EPICS IOC
LabVIEW RT on PXI	Hypervisor Shared MemoryS	EPICS IOC on Linux
PXI (No LabVIEW)	Linux Driver Device Support	EPICS IOC on Linux

Radiation and Magnetic Field Testing



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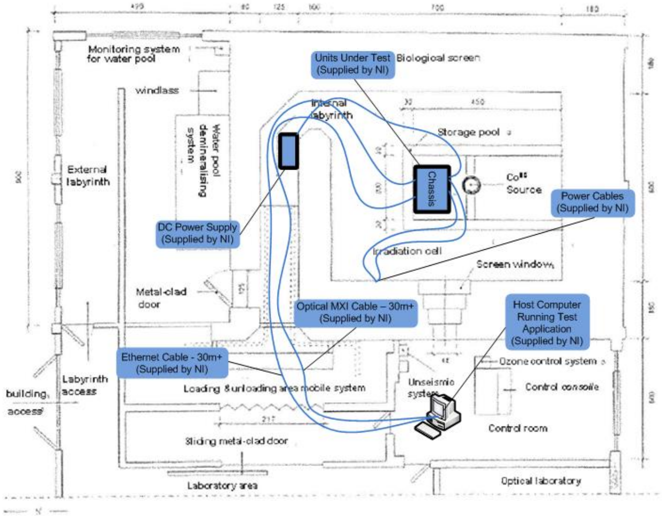
Radiation and Magnetic Field Testing

Calliope Gamma Research Lab at ENEA Casaccia



Units Under Test (Supplied by NI)

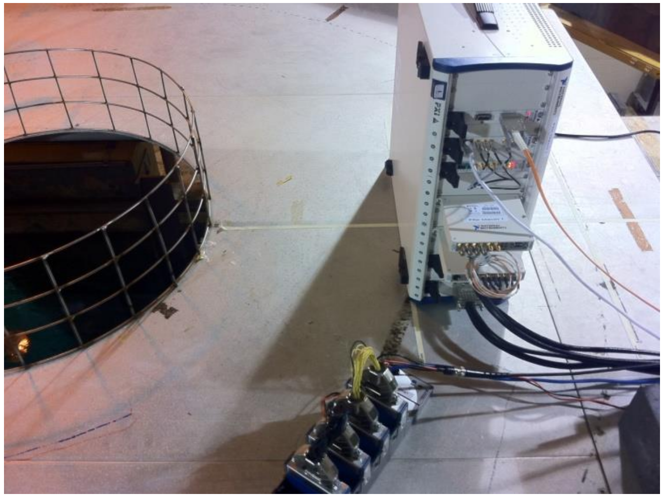
DC Power Supply (Supplied by NI)

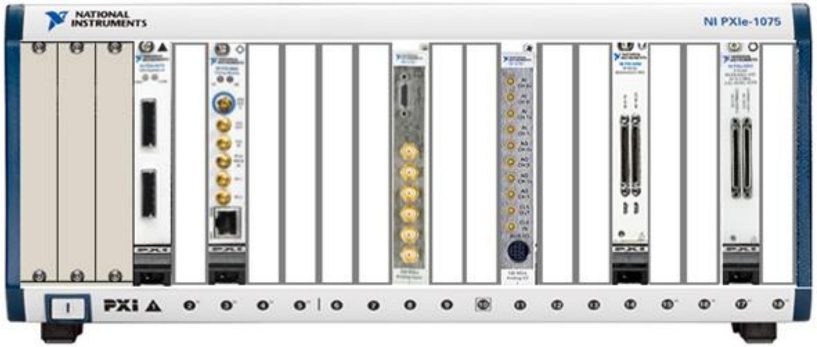
Power Cables (Supplied by NI)

Optical MXI Cable – 30m+ (Supplied by NI)

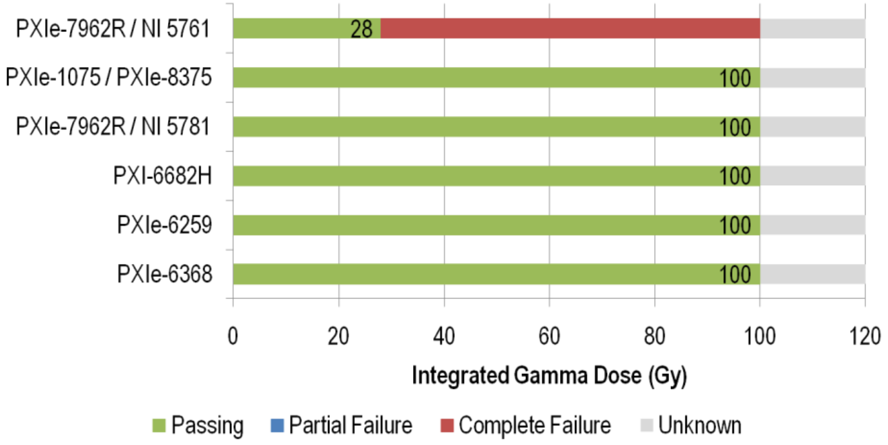
Host Computer Running Test Application (Supplied by NI)

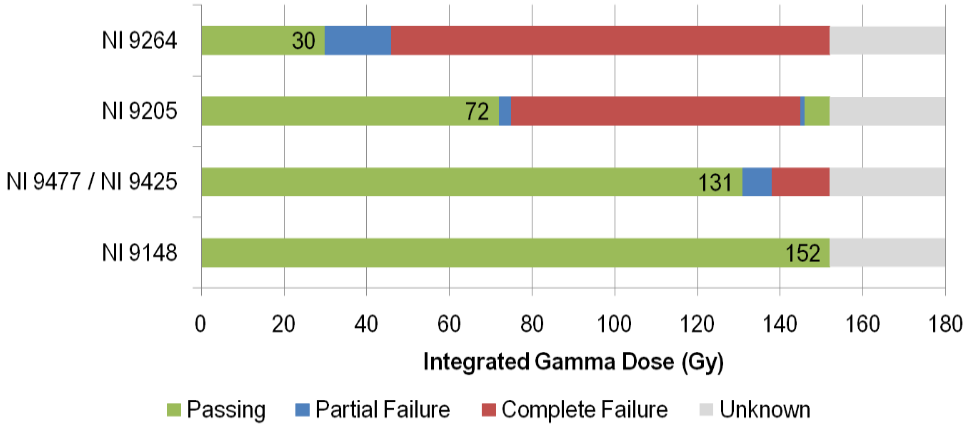
Ethernet Cable - 30m+ (Supplied by NI)





PXIe and cRIO Gamma Testing



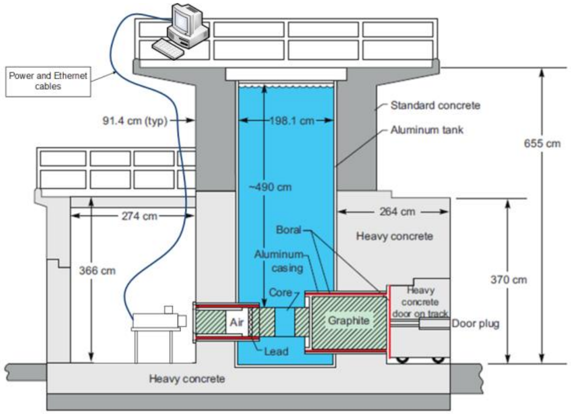


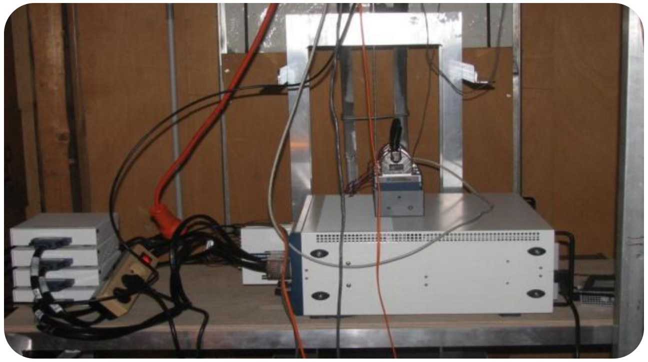
- Cumulative effects are evident in the gamma testing
- Most (1 PXI / 1cRIO) failed devices exceeded expected failure dose of 50Gy
- More than half of the devices exceeded the maximum expected failure dose of 100 Gy

Fast and Thermal Neutron Testing

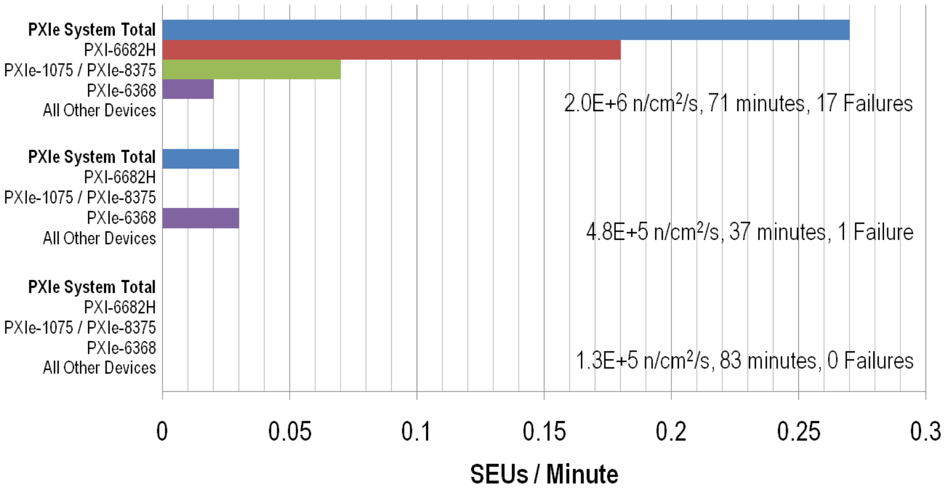
Frascati Neutron Generator, ENEA, Italy (**Fast**)

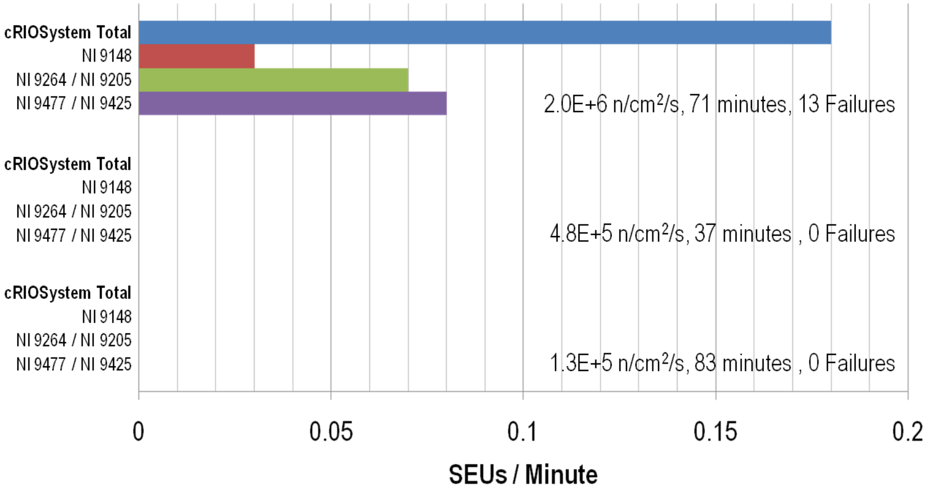
TRIGA Reactor, JSI, Slovenia (**Thermal**)





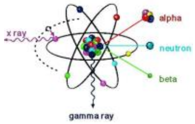
Fast Neutron Results (SEUs/Min)

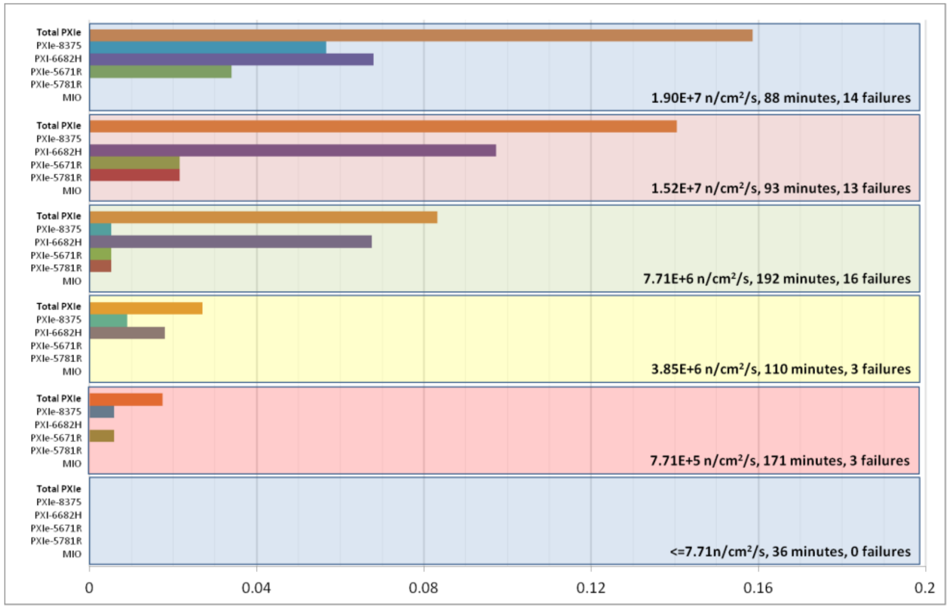


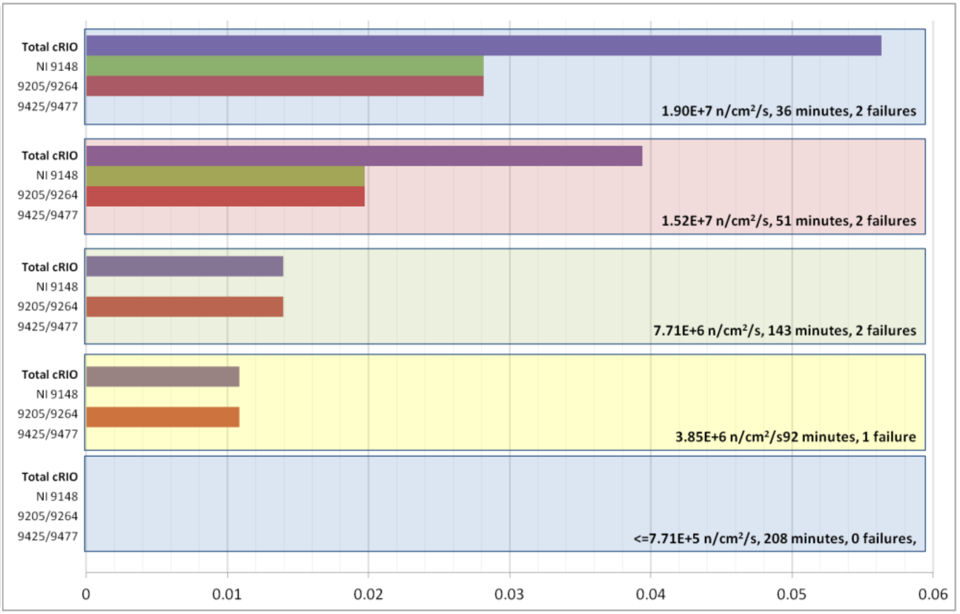


- Single Event Upsets dominated the neutron results generally meeting ITER requirements
- Did not see permanent damage

Thermal Neutron Results (SEUs/Min)

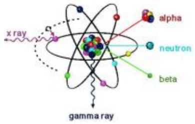






- Where able to test, are almost 1 order of magnitude more flux compared to fast neutrons
- Failure rates were less than or equal to what was seen with fast neutron testing
- MIO hardware handled thermal much better than fast (0 failures)

Radiation Testing Conclusions



- Gamma Testing
  - Most devices exceeded expected failure dose of 50Gy
  - Cumulative effects are evident in the gamma testing
- Fast Neutron Testing
  - Single Event Upsets dominated the neutron results generally meeting ITER requirements
  - Did not see permanent damage
- Thermal Neutron Testing
  - Were able to test are almost 1 order of magnitude more flux compared to fast neutrons
  - Failure rates were less than or equal to what was seen with fast neutron testing
  - MIO hardware handled thermal much better than fast (0 failures)

Magnetic Field Testing at DESY: Phase 1

PXI Chassis

- Fans fail between 15mT - 25 mT
- Investigation to find fans tolerant to higher field continues

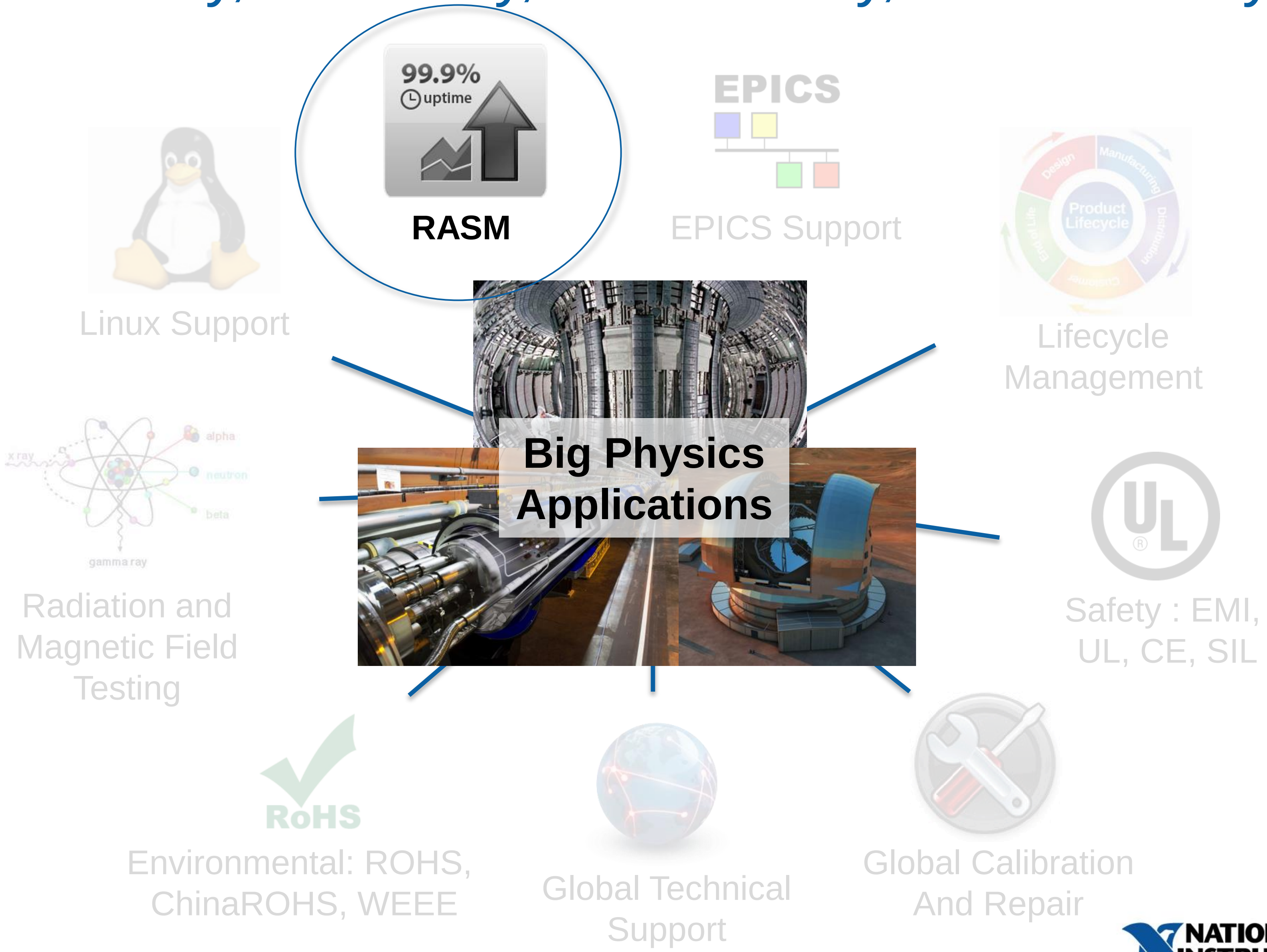
NI 9148 (cRIO Ethernet Chassis)

- Chassis works well up to 60 mT
- Permanent HW damage at 230 mT

cRIO-9205 & cRIO-9263

- Works well up to 40 mT
- Data error between 40 and 50 mT
- Permanent HW failure after several minutes at 50 mT

Reliability, Availability, Serviceability, Maintainability



RASM

EPICS Support

Linux Support

Lifecycle Management

Big Physics Applications

Radiation and Magnetic Field Testing

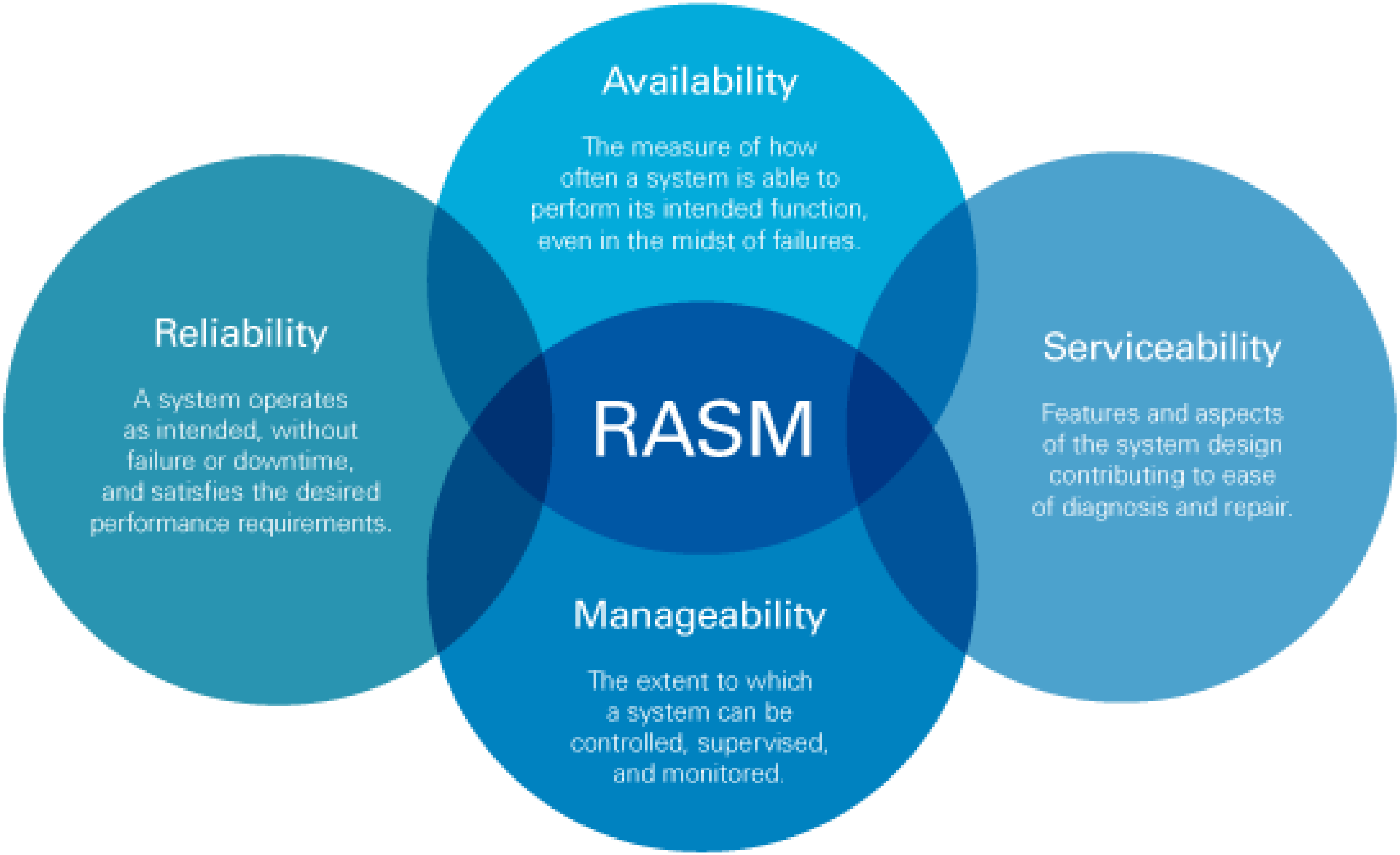
Safety : EMI, UL, CE, SIL

Environmental: ROHS, ChinaROHS, WEEE

Global Technical Support

Global Calibration And Repair

RASM



Availability
The measure of how often a system is able to perform its intended function, even in the midst of failures.
Reliability
A system operates as intended, without failure or downtime, and satisfies the desired performance requirements.
RASM
Serviceability
Features and aspects of the system design contributing to ease of diagnosis and repair.
Manageability
The extent to which a system can be controlled, supervised, and monitored.

System Reliability Lab (SRL)

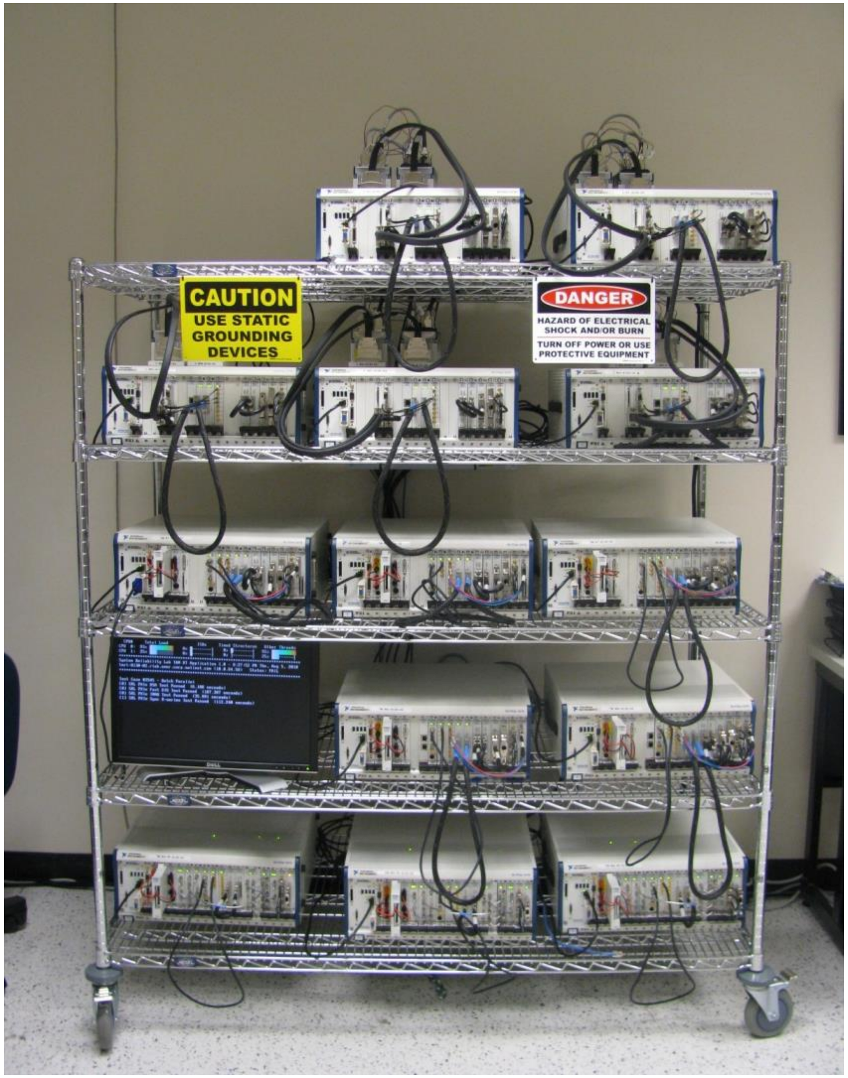
Mission:

Assess the reliability of National Instruments product-based systems and drive product improvements

- Created to focus on system reliability for the:
  - Compact RIO and PXI / PXIe hardware platforms
  - LabVIEW software platform

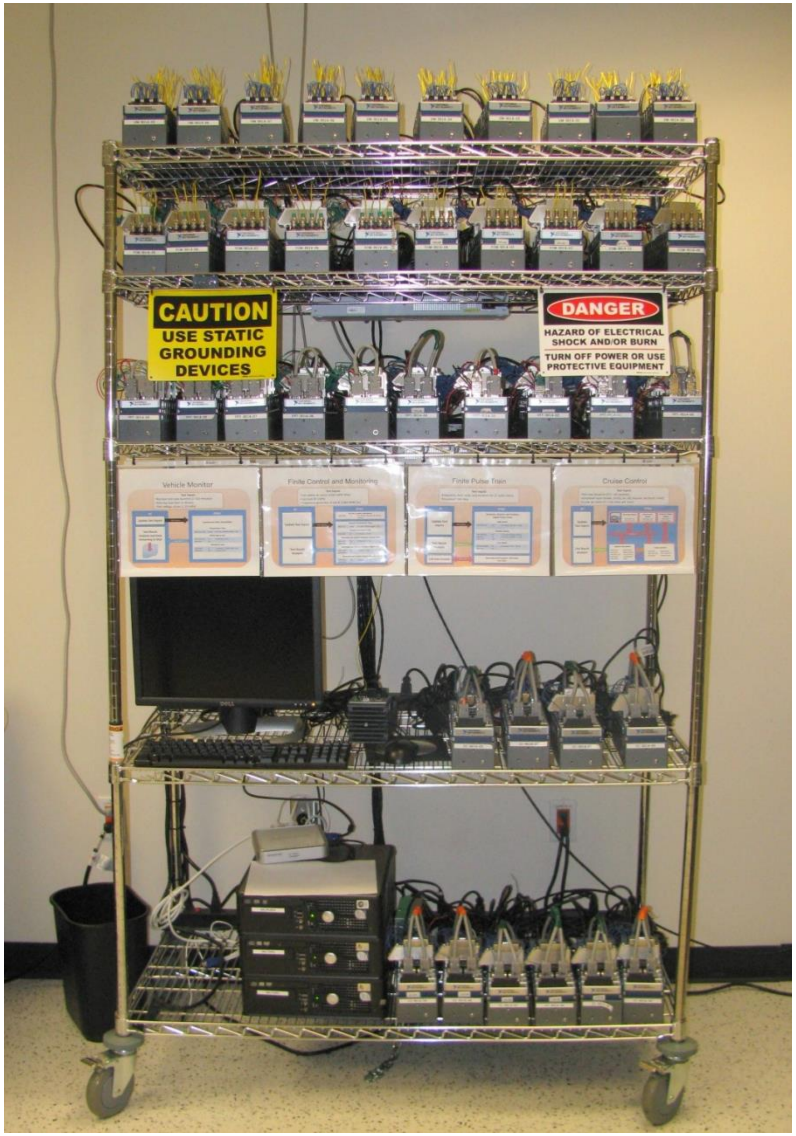
SRL PXI/PXIe Testing

- 20 systems
  - 18 systems at room temperature
  - 2 systems in temperature chamber (cycles between 5°C and 5°C)
  - 5 systems running on dirty power
- 3 different hardware configurations
- 32 test applications
- 24/7 execution during missions


CAUTION
USE STATIC GROUNDING DEVICES
DANGER
HAZARD OF ELECTRICAL SHOCK AND/OR BURN
TURN OFF POWER OR USE PROTECTIVE EQUIPMENT

SRL cRIO Testing

- 40 systems
  - 32 systems at room temperature
  - 8 systems in temperature chamber (cycles between -40 and 70°C three times per day)
  - 8 systems running on dirty power
- 4 unique cRIO applications
- 24/7 execution during mission

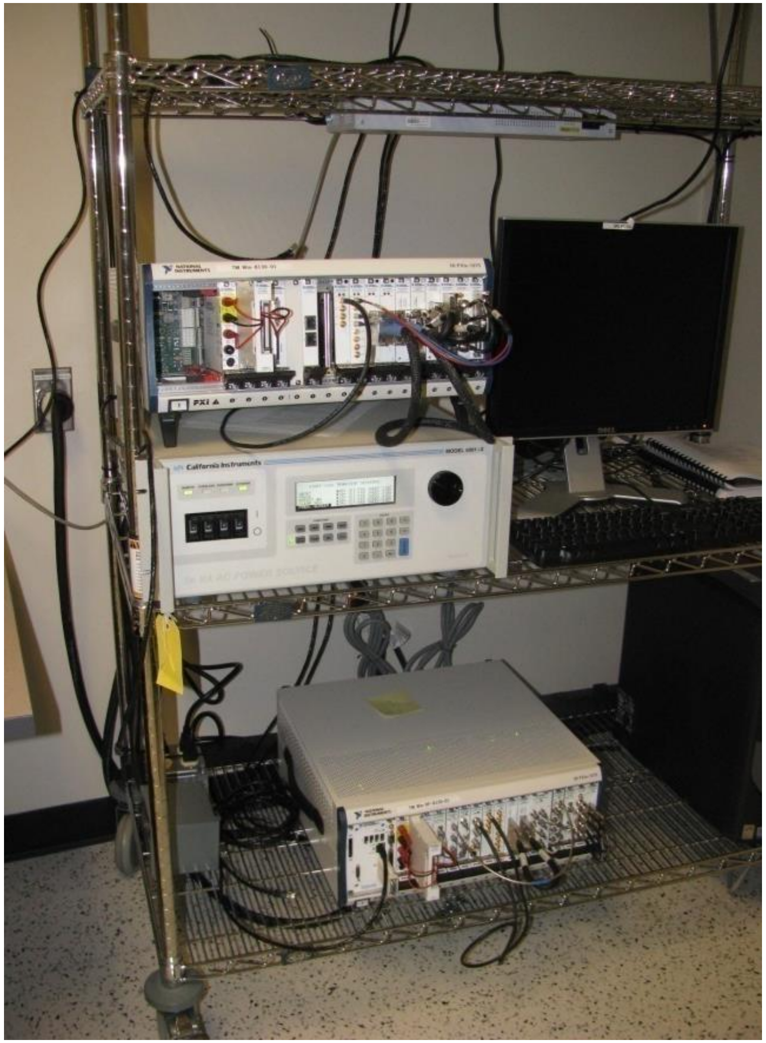

CAUTION
USE STATIC GROUNDING DEVICES
DANGER
HAZARD OF ELECTRICAL SHOCK AND/OR BURN
TURN OFF POWER OR USE PROTECTIVE EQUIPMENT
Vehicle Monitor
Finite Control and Monitoring
Finite Pulse Train
Cruise Control

SRL Temperature Chamber

- Cycle Temperature three times per day for months
- 2 to 8 Systems run for months at time in this environment
- PXI / PXIe: 5°C to 50°C
- cRIO: - 40°C to 70°C

SRL Dirty Power Test Station

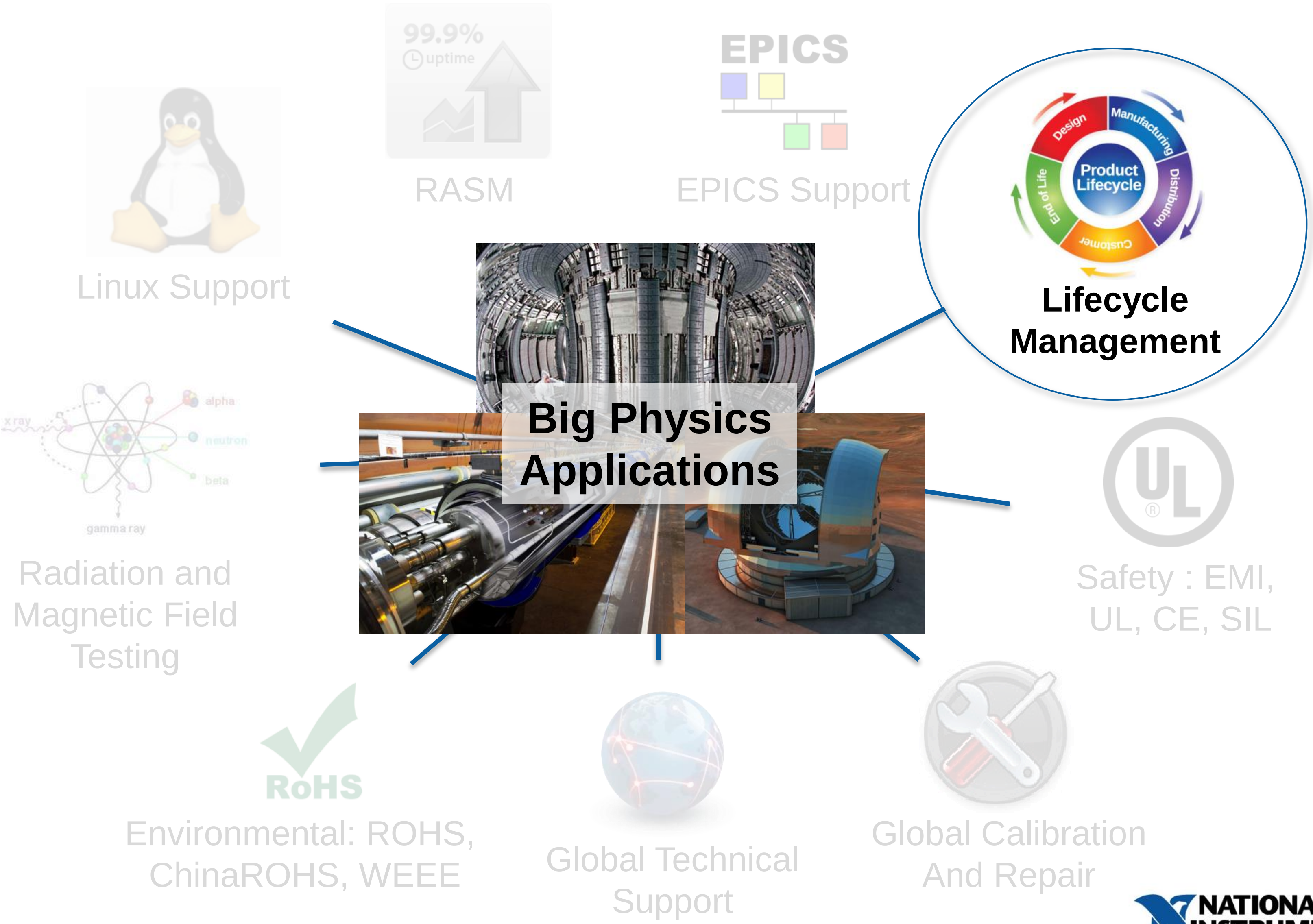
- Simulates a bad power grid
- 5 to 8 Systems run for months at time in this environment
- Vary frequency from 47 to 63 Hz
- Vary voltage level from 90 to 264 V



CERN High Availability Chassis

- Redesigned to mechanically fit into a custom rack
- Independently powered, redundant hot swap power supplies and fans
- Remote Monitoring : Chassis Temperature, Fan Status, Power Supplies

Lifecycle Management



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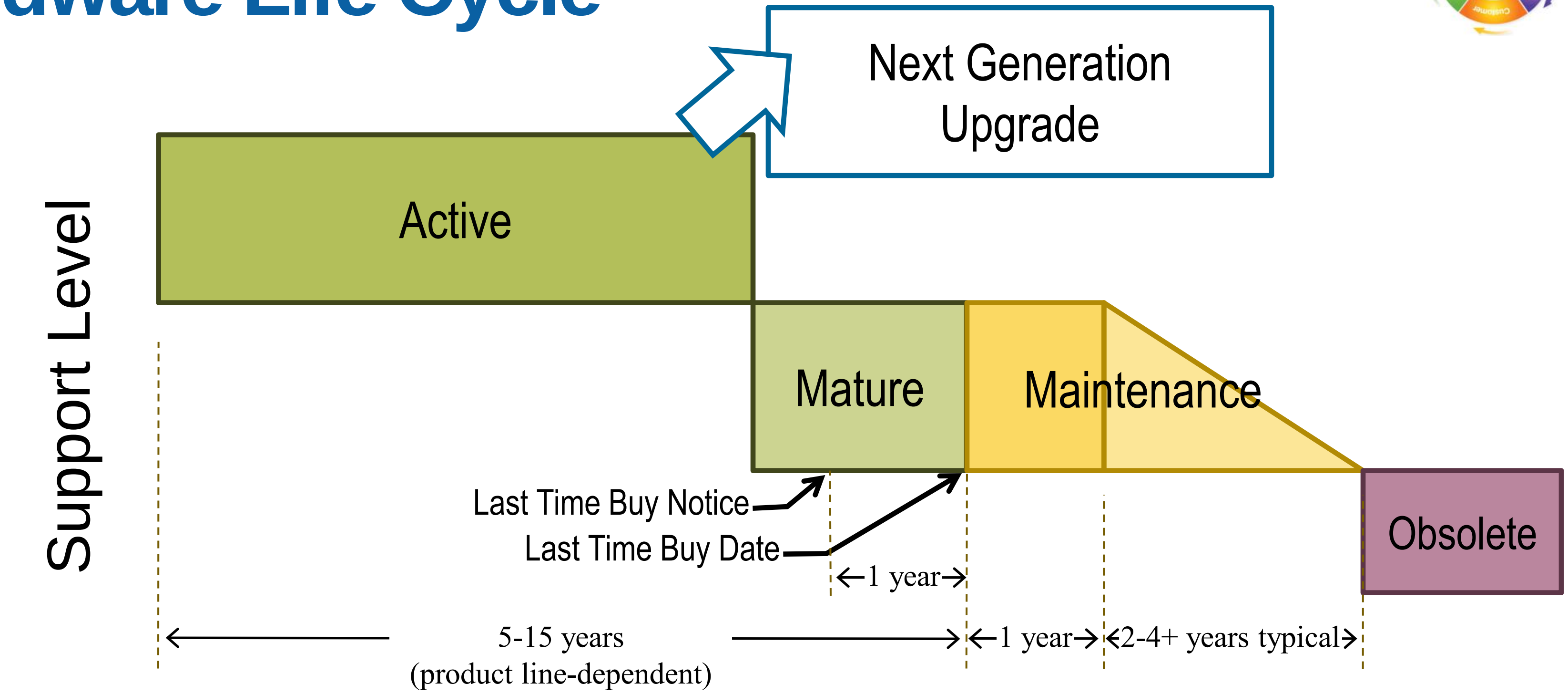
Hardware Life Cycle



	Active	Mature	Maintenance		Obsolete
Purchase new	Yes	Yes	No	No	No
Repair	Yes	Yes	Yes	Reasonable effort	No
Calibration	Yes	Yes	Yes	Reasonable effort	No
Service Agreements	Yes	Yes	Yes	Yes	Yes

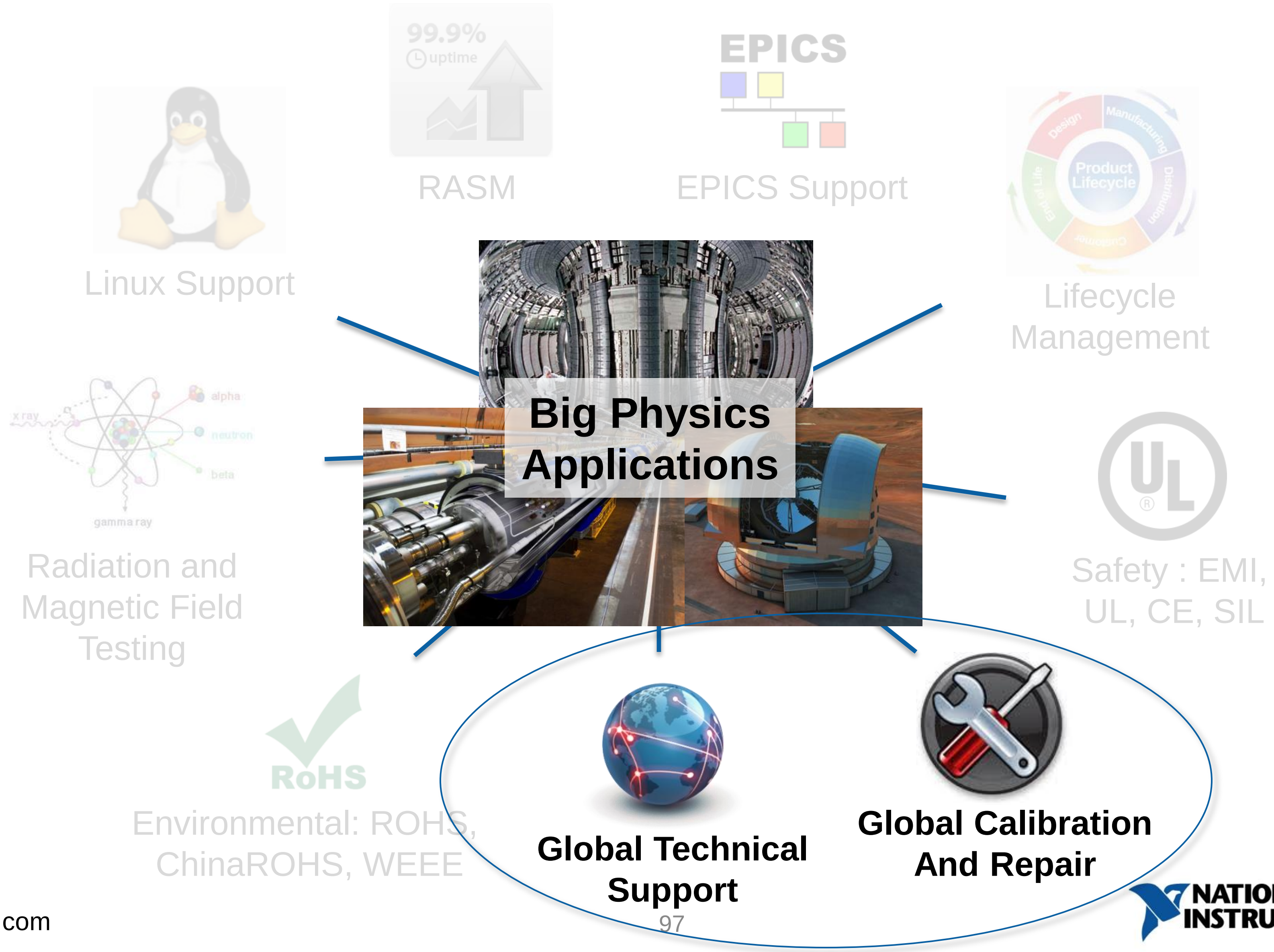
Lifecycle Planning: Examples

Product	Part Number	Released	Active	Mature	Maintenance	Obsolete
cRIO-9072	779998-01	Nov-2007	Nov 2007 - Nov 2012	Nov 2012 - Nov 2017	Nov 2017 - Nov 2022	Nov-2022
cRIO-9073	780471-01	Nov-2007	Nov 2007 - Nov 2012	Nov 2012 - Nov 2017	Nov 2017 - Nov 2022	Nov-2022
cRIO-9074	779999-01	Nov-2007	Nov 2007 - Nov 2012	Nov 2012 - Nov 2017	Nov 2017 - Nov 2022	Nov-2022
cRIO-9002	779000-01	Aug-2004	Aug 2004 - Aug 2010	Aug 2010 - Aug 2014	Aug 2014 - Aug 2019	Aug-2019
cRIO-9004	779055-01	Aug-2004	Aug 2004 - Aug 2010	Aug 2010 - Aug 2014	Aug 2014 - Aug 2019	Aug-2019
cRIO-9012	779563-01	Nov-2006	Nov 2006 - Nov 2011	Nov 2011 - Nov 2016	Nov 2016 - Nov 2021	Nov-2021
cRIO-9014	779564-01	May-2007	May 2007 - May 2012	May 2012 - May 2017	May 2017 - May 2022	May-2022
cRIO-9022	780718-01	Feb-2009	Feb 2009 - Feb 2014	Feb 2014 - Feb 2019	Feb 2019 - Feb 2024	Feb-2024
cRIO-9023	781173-01	Feb-2010	Feb 2010 - Feb 2015	Feb 2015 - Feb 2020	Feb 2019 - Feb 2024	Feb-2024
cRIO-9024	781174-01	Aug-2009	Aug 2009 - Aug 2014	Aug 2014 - Aug 2019	Aug 2019 - Feb 2024	Feb-2024
cRIO-9025	781313-01	Jan-2010	Jan 2010 - Jan 2015	Jan 2015 - Jan 2020	Jan 2020 - Jan 2025	Jan-2025

Product	Part Number	Released	Active	Mature	Maintenance	Obsolete
cRIO-9101	779052-01	Aug-2004	Aug 2004 - Aug 2010	Aug 2010 - Aug 2014	Aug 2014 - Aug 2019	Aug-2019
cRIO-9102	779007-01	Aug-2004	Aug 2004 - Aug 2010	Aug 2010 - Aug 2014	Aug 2014 - Aug 2019	Aug-2019
cRIO-9103	779053-01	Aug-2004	Aug 2004 - Aug 2010	Aug 2010 - Aug 2014	Aug 2014 - Aug 2019	Aug-2019
cRIO-9104	779054-01	Aug-2004	Aug 2004 - Aug 2010	Aug 2010 - Aug 2014	Aug 2014 - Aug 2019	Aug-2019
cRIO-9111	780915-01	Feb-2009	Feb 2009 - Feb 2014	Feb 2014 - Feb 2019	Feb 2019 - Feb 2024	Feb-2024
cRIO-9112	780916-01	Feb-2009	Feb 2009 - Feb 2014	Feb 2014 - Feb 2019	Feb 2019 - Feb 2024	Feb-2024
cRIO-9113	780917-01	Feb-2009	Feb 2009 - Feb 2014	Feb 2014 - Feb 2019	Feb 2019 - Feb 2024	Feb-2024
cRIO-9114	780918-01	Feb-2009	Feb 2009 - Feb 2014	Feb 2014 - Feb 2019	Feb 2019 - Feb 2024	Feb-2024
cRIO-9116	780919-01	Feb-2009	Feb 2009 - Feb 2014	Feb 2014 - Feb 2019	Feb 2019 - Feb 2024	Feb-2024
cRIO-9118	780920-01	Aug-2009	Aug 2009 - Aug 2014	Aug 2014 - Aug 2019	Aug 2019 - Feb 2024	Feb-2024

🟩	First 1/3 of phase
🟨	Second 1/3 of phase
🟥	Third 1/3 of phase

Global Services



Linux Support

RASM

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Lifecycle Management

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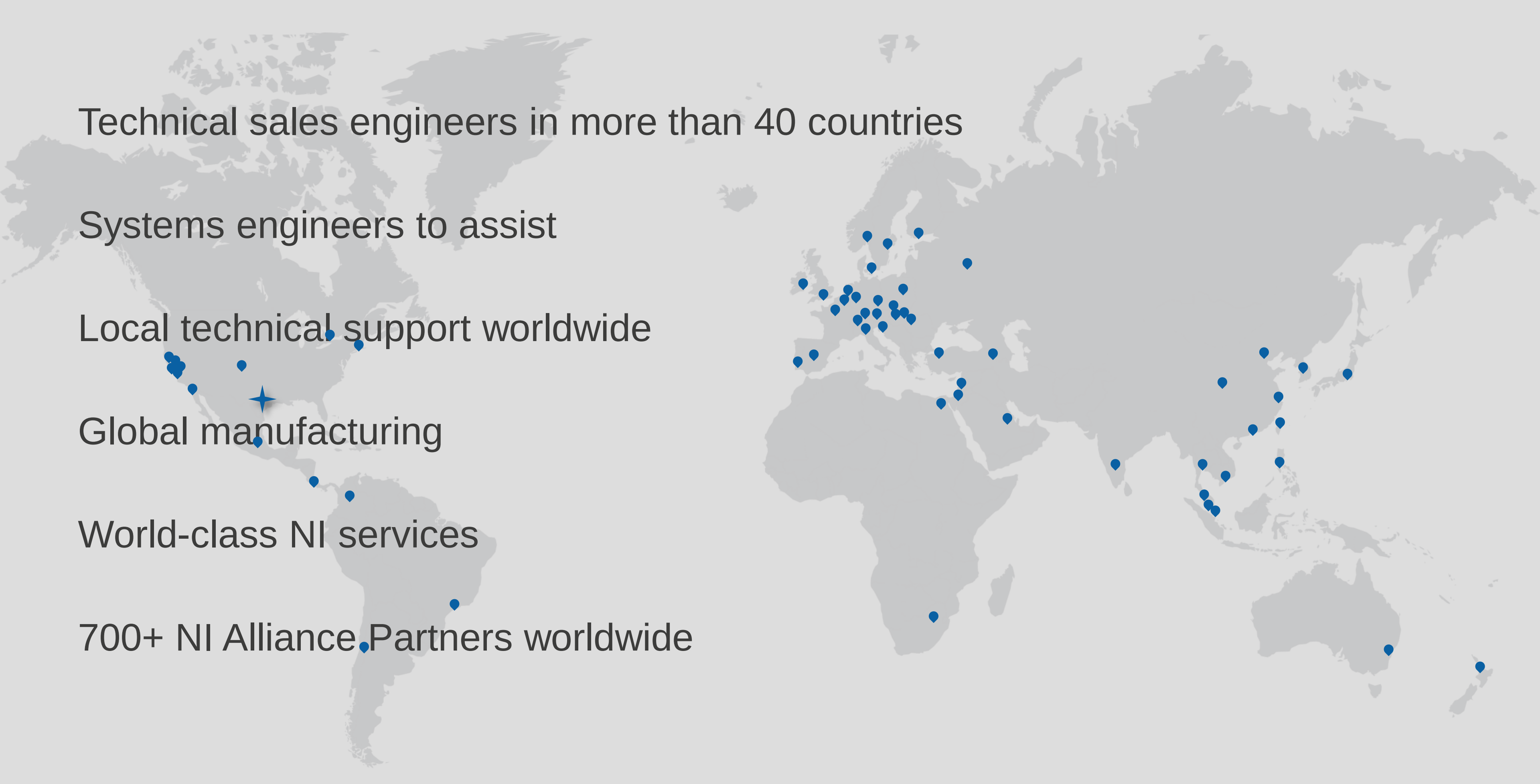
Global Technical Support

Global Calibration And Repair

Committed to Your Success



Technical sales engineers in more than 40 countries

Systems engineers to assist

Local technical support worldwide

Global manufacturing

World-class NI services

700+ NI Alliance Partners worldwide

Calibration Services

NI Flexible Calibration Options Reduce Maintenance Expenses

Perform verification and adjustment of NI products in your own metrology lab

NI Calibration Executive

Your existing service providers can verify and adjust NI products

Calibration Support

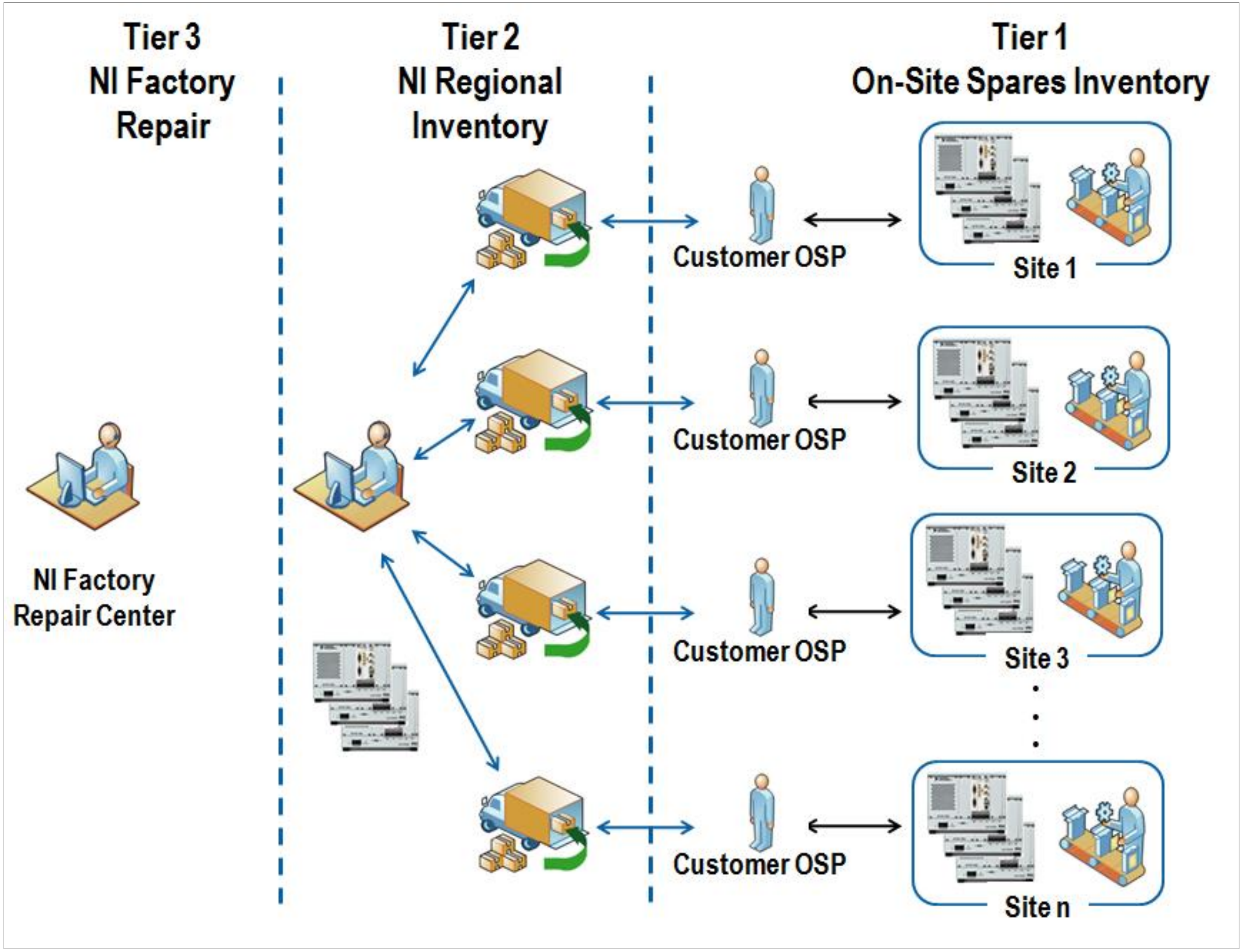
NI can calibrate your device at the NI service center in your region

Regional Calibration

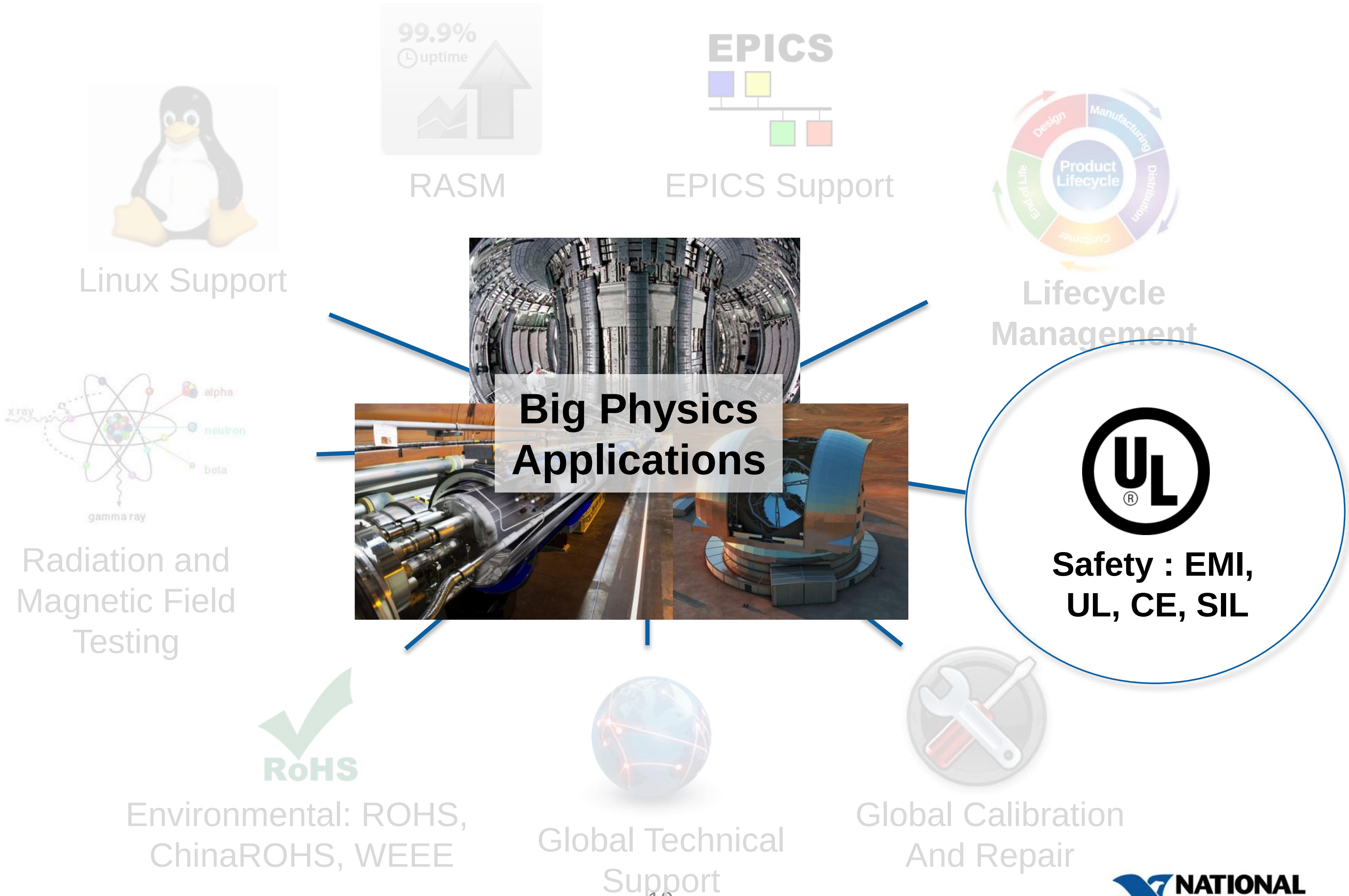
NI can provide calibration service at your facility

Onsite Calibration

Global Sparing and Rapid Replacement for High Availability Requirements



Safety Certifications



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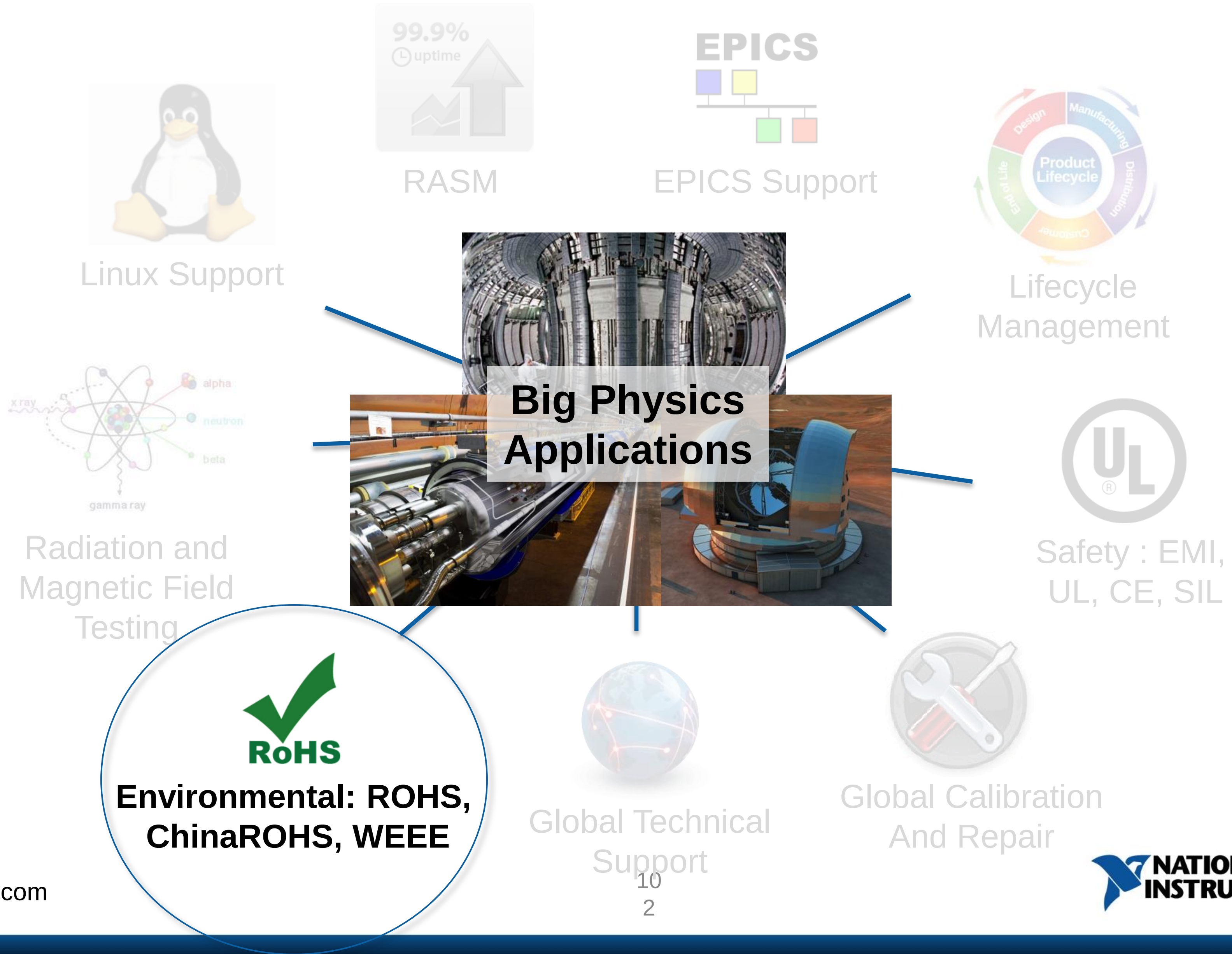
Environmental Certifications



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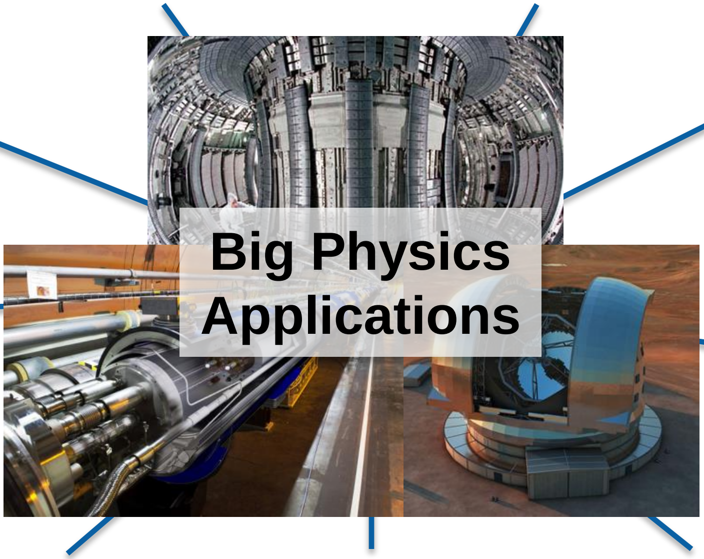
Addressing Big Physics Requirements: Recap


Big Physics Applications

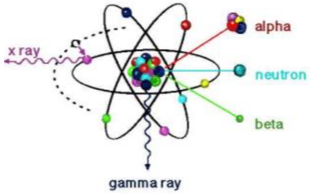
Linux Support

RASM

EPICS Support

Product Lifecycle
Design
Manufacturing
Distribution
Customer
End of Life

Lifecycle Management



Radiation and Magnetic Field Testing

Safety : EMI, UL, CE, SIL

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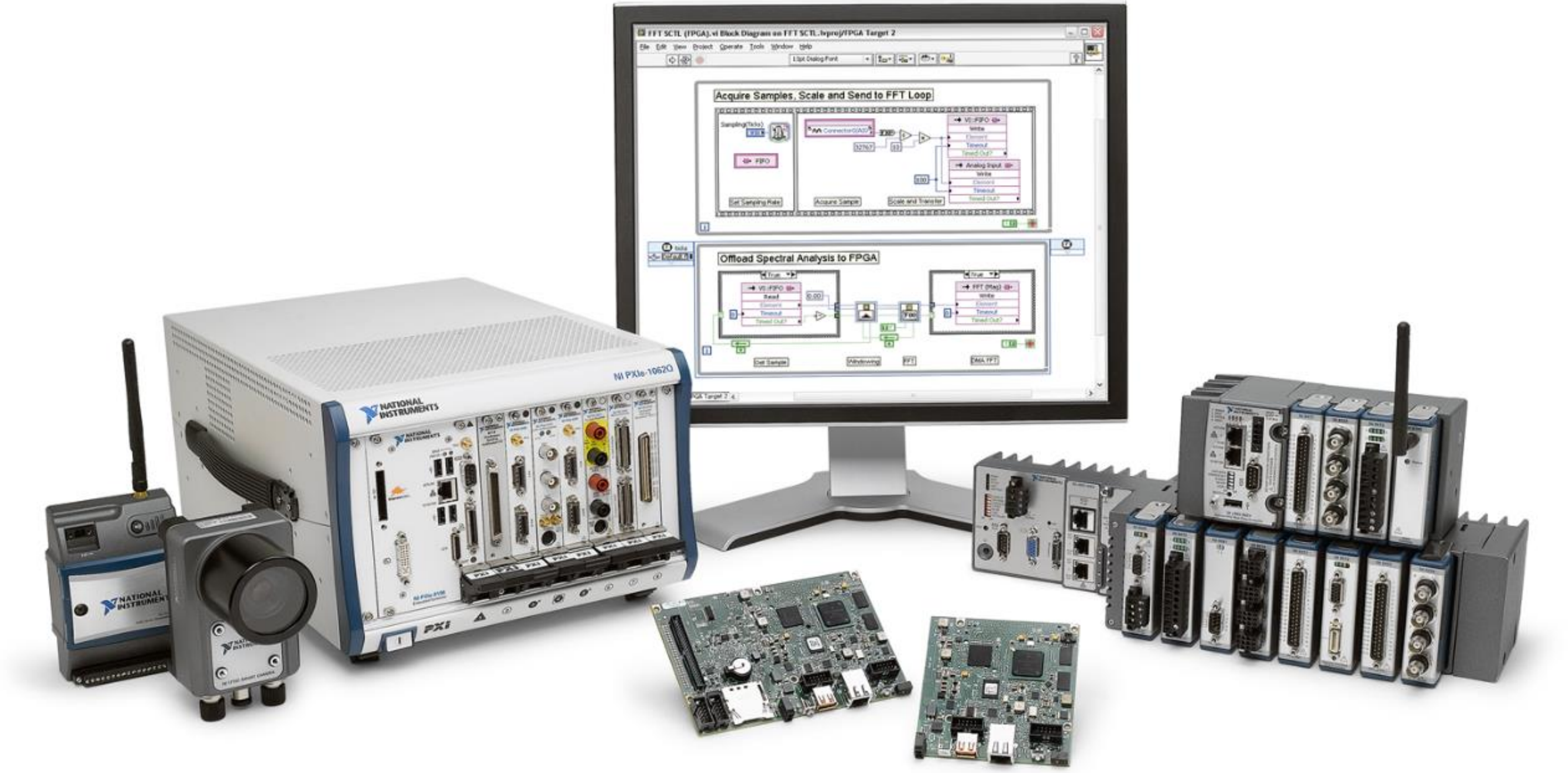
Global Technical Support

Global Calibration And Repair

The Benefits of Off-the-Shelf Technology With the Flexibility of Custom Design


FFT SCTL (FPGA).vi Block Diagram on FFT SCTL.lvproj/FPGA Target 2
Acquire Samples, Scale and Send to FFT Loop
Offload Spectral Analysis to FPGA
NI PXIe-1062Q
NATIONAL INSTRUMENTS
PXI

Conclusions

- **Measurement and Control products must meet technical specifications and features requirements**
- Big Physics applications have additional requirements
- NI adapts COTS products to meet such requirements
- NI globally offers accompanying services to be successful over long term

Thank You

Contact

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Scientific Research & Big Physics

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Eran Castiel, MS

NI Israel Big Physics
Segment Manager

eran.castiel@ni.com