#### The TDAQ System of the MEG Experiment and its upgrade

- The MEG experiment
- requirements for the TDAQ from physics
  - DAQ choice
  - requirements for the trigger
- An FPGA based trigger
  - algorithm implementation
- TDAQ efficiency considerations
- The MEG II case
  - upgrade design
  - the upgraded TDAQ system

ISOTDAQ 2015



מכוז ויצמז למדע



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### Very few words about the MEG experiment





- "Tiny" collaboration
- Search μ->eγ with 5x10<sup>(-13)</sup> sensitivity on the process @Paul Scherrer Institut, Villigen Switzerland
  - CERN recognised experiment in the intensity frontier
  - prohibited in SM -> new physics?/! (SUSY?)
- positive μ-beam stopped in a thin target (3x10<sup>^</sup>7 μ/sec)
  - positron detector
    - non-uniform magnetic field COBRA to bend positrons
    - · tracking with segmented wire drift chambers
    - timing with plastic scintillator bars read by PMTs (Timing Counter)
  - photon detector
    - Liquid Xenon calorimeter read with PMTs

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# Requirements to the TDAQ



- An experiment in the intensity frontier demands for:
  - statistics -> high beam intensity (and associated raw event rate and detector occupancy)
    - electronics to resolve any possible pile-up within few ns in detectors
      - use of GSPS waveform digitisers, no TDC and QDC
  - resolution -> background suppression
    - development of detector with unprecedented resolutions at signal energy (52.8 MeV)
      - high precision electronics for charge and time measurements
  - stability -> systematics under control
    - the detector stability measured with a redundant set of calibration methods (evolving year by year)
      - trigger system flexible to cope with any experimental requests

# Readout choice: the DRS chip

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- The Domino Ring Sampler
  - waveform digitiser developed at Paul Scherrer Institut
  - capacitor array to store the charge from detector signals, each capacitor is a "bin" in our waveform
    - read out with external ADC
  - sampling speed tuneable from 800 MSPS to 5 GSPS
  - waveform width = 1024 bins (from 12.8 μs to 200 ns)
    - time resolution demands for sampling speed greater that 1.5 GSPS - 600 ns memory depth
      - requirement on trigger latency!



Shift Register



Waveform stored

> — Out FADC

33 MHz



## DAQ electronics

- DRS chips in VME boards
  - 32 channel per board
- 5 crates
  - 20 boards per crate
- Introduction to VME bus M. Joos
- 640 channels per crate
- Boards read-out with 32 bit 2eVME protocol
  - 80 MB/s transfer speed









## Trigger too early



| **N F N** 

## Right trigger time



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- The DRS is continuously recording detector signals
  - (1) a pulse is generated on the sensor
  - (2) the pulse is well centred in the recording memory, the ADC bins in from of pulse are needed for waveform analysis!
    - it is time to fire the trigger (if "good" event)
  - (3) the pulse is being overwritten in the memory
    - the trigger would be to late, the event could not be reconstructed
- The trigger latency is defined by ADC memory size
  - is it possible to extend the memory? NO... it is defined by chip design
  - is it possible to delay signals? If possible NO... may spoil time resolution

# Trigger technology choice

- The trigger will be a separate system
- Latency requirements
  - DRS with 1.6 GSPS (600ns waveform width)
  - ~50 ns are required before the pulse in DRS waveforms for offline processing
  - ~50 ns is a conservative estimate for the trigger signal distribution from the trigger to the DAQ
  - the decision must be taken as fast as 500 ns after the event occurrence
    - at trigger level only fast detectors are used: LXe calorimeter and Timing Counter (plastic scintillator detector)
- Flexibility requirements
  - the system have to cope with any possible experimental needs
    - ...and there are really a lot of!
- FPGA based trigger
  - Xilinx Virtex-II pro FPGA (bought in 2004)
    - algorithm execution frequency to be 100 MHz
  - VME boards
    - used for board configuration and monitoring @trigger level
  - Multi layer system
    - transmission with LVDS serialiser-deserialiser, 4.8Gbit/s per connection





#### Introduction to FPGAs Hannes Sakulin

# Overview of the trigger system

- Three layers system
  - Type1 board
    - 6U VME board
    - receiving detector data
    - equipped with FADC 100MHz - 10 bit
  - Type2 board
    - data processing and transmission to next level
      - the master performs last algorithm steps and fires the trigger signal





Type1-6U



Type2-9U



# Some pictures... trigger boards

#### Type1-6U



#### Used in exercise 4:

A Type-I as a (simple) TDAQ system to select cosmic muons tracks through a scintillator pair



# The trigger system at PSI

### Type1 6U crate

### Type2 9U crate

### Type1 6U crate



LAYER

FINAL TYPES

# Trigger bus and event building

- The raw data are scattered over several VME crate
  - each crate is read-out after any trigger by dedicated CPU that create a fragment
  - all the fragments sent to the main CPU
    - what happens if at a certain point a fragment is loss??
      - fragment belonging different events are mixed
      - data useless!!



- The solution is the trigger bus: from the trigger to the DAQ crates
  - event number + event code (trigger type)
  - connected via the VME transition boards on the backplane



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A zero-suppression example INFN





- DAQ efficiency is defined as
  - DAQLiveTime x Trigger Efficiency

Introduction to trigger F. Pastore slide 13

• This quantity has to be as large as possible in any TDAQ system



- Compromise...
  - milestones! let's start from dead time...

### Read-out dead time

- As a first attempt let's try with a single buffer read-out
  - the system is in dead time during the read-out of a crate through VME
  - the dead time is dictated by the heaviest crate

 $t_d = \underset{\# \text{ mezzanines/crate}}{40} \times (\underset{\# \text{ DMA setup time}}{0.125 \text{ ms}} \times \underset{\# \text{ data transfer time}}{40960 \text{ B}/83000 \text{ MB/ms}}) = 24.7 \text{ ms}$ 

 the associated DAQ live time is given by the probability to have 0 event during the readout (trigger rate = 7 Hz, Poisson event distribution)

 $LT = \exp(-R_{trg} \cdot t_d) \simeq 84\%$ 

- Requirement for the trigger rate
  - which trigger algorithms can we use?
  - what about the rejection power?



## Considerations about trigger algorithms

- Goal: DAQ rate of about 7 Hz
- Use of prompt response detectors
  - LXe calorimeter (photon energy, time and direction)
  - Timing Counter (positron time and hit position)
- Synchronous processing with FPGA
  - algorithms to use 1 CLK cycle per operation (if possible)
    - · registers, adders, subtracters, comparators for simple operations
    - · Look Up Tables for more complex operations, for example products
- Online observables
  - photon energy
  - photon-positron timing
  - photon-positron space correlation
- The discrimination on photon energy has the largest background rejection power
  - take care about it!



This choice is driven by physics and your detector!



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- Synchronous sum of the LXe waveform samples
  - the peak of the obtained waveform is the online energy estimate



- the baseline value may differ from channel to channel (remember QDC in lab4)
  - refer the waveform to a common value (0 ADC counts) before the sum stage
- channel calibration with Look Up Table
  - for example in case of PhotoMulTipliers gain and Quantum Efficiency calibration

# Raw waveforms from ADC



### ...online pedestal subtraction...



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Firmware for online pedestal subtraction



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### ...again pedestal subtracted wfms..

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### ... channel calibration...

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# Reconstruction calibration!

- By applying a refined calibration reconstruction improves!
  - better reconstruction -> higher threshold with same efficiency on signal -> lower trigger rate
    -> higher DAQ Live Time with the same trigger efficiency
    - improvement of the DAQ efficiency



• It is important to get the best from the system with the available techniques!

# ...and finally coherent sum



# Run configuration and monitoring

- The trigger system provides the DAQ with 32 different selection algorithms
  - the trigger type are order by priority
  - pre-scaling factors
    - programmable fraction of minimum bias selection in the data stream
      - trigger efficiency studies
      - · detector calibration and monitoring
      - physics analysis, normalisation evaluation
- This flexibility is crucial to take under control the detector
  - the run configuration is store in a database
    - give access to the shift crew
    - default run configuration available
    - metadata for analysis (as discussed in lab 4)
- GUI to check data quality online
  - events "pictures"
    - · not so precise but sensitive to major problems
- Automatic analysis right after the acquisition to check further the data quality
  - histograms for detector debugging
    - · dead channels, electronic noise...



electromagnetic calorimeter picture



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DAQ efficiency: measurement and optimisation

- First run in 2008: DAQ efficiency = 55%
  - "preliminary" trigger system configuration
    - · first run with a complete detector
    - · calibration not optimised yet
- The DAQ (trigger) efficiency measured at the end of data taking
  - the selection has to be trained with data
  - the higher Live Time is NOT the experimental working point
    - but the Live Time is measured online...
- How to find the best working point?
  - trigger "simulation" with real data
    - modify selection and predict the trigger rate and efficiency with no algorithm improvement
  - improve the selection algorithms
    - for example improve calibrations!
- By algorithm refinement we reached 75% DAQ efficiency



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# Is it possible to improve further?

- Many possibilities
  - reduce dead time read out
    - zero-suppression of FPGA to neglect the read-out of "empty" channels
      - this is dangerous with an homogeneous calorimeter...
    - Use 2eVME D64 read-out (160 MB/s instead of 80 MB/s)
      - you have to foreseen it at design phase...

#### Lab. 1 VME bus

- unfortunately you usually miss something in your original design
- more complex selection algorithms
  - current latency of the order of 500 ns, DRS running at 1.6GSPS
    - a more complex algorithm (charge instead of pulse height) would lead to a larger latency...
- Multiple-buffer read-out!
  - data stored in circular memories on VME boards
    - during a buffer read-out the next buffer is filled (if free...)
    - busy released immediately!
      - this can be implanted in FPGA in any time... if you have enough resources!













- Read-out when one of the buffer busy is 1
- The system is busy when all the 3 buffers are full

are reading the read out time is unchanged ~25ms

 the LiveTime fraction can be evaluated

$$LT = e^{-R_{trg} \cdot t_d} \cdot \left[1 + R_{trg} \cdot t_d + (R_{trg} \cdot t_d)^2 / 2!\right]$$

- it is close to 99% even with a trigger rate close to 14 Hz
  - there is room to relax the trigger condition and improve also the trigger efficiency!



And DAQ Live Time?

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# Conclusions - part 1

- A TDAQ system to be designed on top of an experiment
  - the experimental needs drive the choice of the technology
- Even when the technology is decided a lot of compromise, in this case
  - Waveform digitiser with lat least 1.6 GSPS sampling speed
    - background rejection requires the best timing possible
    - trigger latency to be least than 500 ns
  - trigger based FPGA
    - system flexibility, for example detector calibration
      - calibration procedures may changes during the run... and you do want to be the reason why a new calibration procedure will not be used ;)
- Once your TDAQ is built you have to get the best performance
  - use all the accessible handles
    - this is just an example but can help
- What happens in case of a experiment upgrade?
  - let's study the implications of the upgrade

# The MEG II experiment



- 1. Increasing µ<sup>\*</sup>-stop on target
- Reducing target thickness to minimize e<sup>+</sup> MS & bremsstrahlung (or replace it with an active target)
- 3. Replacing the e<sup>+</sup> tracker reducing its radiation length and improving its granularity and resolution
- 4. Improving the timing counter granularity for better timing and reconstruction
- Improving the e<sup>+</sup> tracking-timing integration by measuring the e<sup>+</sup> trajectory up to the TC interface
- 6. Extending y-ray detector acceptance
- Improving the γ-ray energy and position resolution for shallow events
- Integrating splitter, trigger and DAQ maintaining high bandwidth
- Number of channels increased by almost a factor of 4
  - high density TDAQ to fit in the experimental area
- Doubled beam rate
  - trigger rate increased by a factor four (~40 Hz)
    - VME read out not not enough to sustain that value



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## TDAQ integrated board • Shaper-amplifier circuit for input signals

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- DRS4 in bypass mode to forward signals to ADC for trigger
  - sampling speed = 100 MHz .
  - Bandwidth on signals = 50 MHz .
    - this follow the Nyquist prescription
- Data processing by FPGA

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- programmable memory size for 100MHz sampled waveforms
- SiPM biasing with dedicated and programmable HV regulators
- Stand alone use through ethernet connection and PoE
  - 16 channels TDAQ system
- 8Gb/s serial connection to TCB (trigger) and 2 Gb/s to DCB (memory read out)





### Serial connections



### 2-STAR topology

### Gbit/s read out links embedded in FPGA fabric

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# R&D on HW: check performance!



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• Event read out:

WDB to the DCB

*time included)* 

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#### We moved the bottleneck to storage • capability...

#### we are working then for a second level trigger



- a factor 25 smaller than in MEG
- the data transmission is not the bottleneck until ~1 kHz

performed in broadcast from all the

- - well above the MEGII foreseen rate

. OLive Time full (board) event size ~60kB -> event read out in ~1 ms (DRS4 conversion 0.8 0.7



Improvements with Gbit links!

# The first working crate!



#### Step by step

| **N F N** 





#### One circuit each detector



N F N



## Conclusions



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- Even when the technology is decided a lot of compromise, in this case
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    - trigger latency to be least than 500 ns
  - trigger based FPGA
    - system flexibility, for example detector calibration
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- Once your TDAQ is built you have to get the best performance
  - use all the accessible handles
    - · this is just an example but can help
- The new TDAQ system for the MEG II experiment
  - · keep the good features of the previous design and point to the critical points
    - Trigger and DAQ merged in one (custom) board
      - supported by a concentrating trigger crate
    - new serial data transmission scheme to speed up event read out and transmission inside the trigger system
    - improve timing algorithm to improve background rejection