Introduction to the Design of Full-Custom Front-End & Data Transmission ASICs*

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* *Application Specific Integrated Circuit*

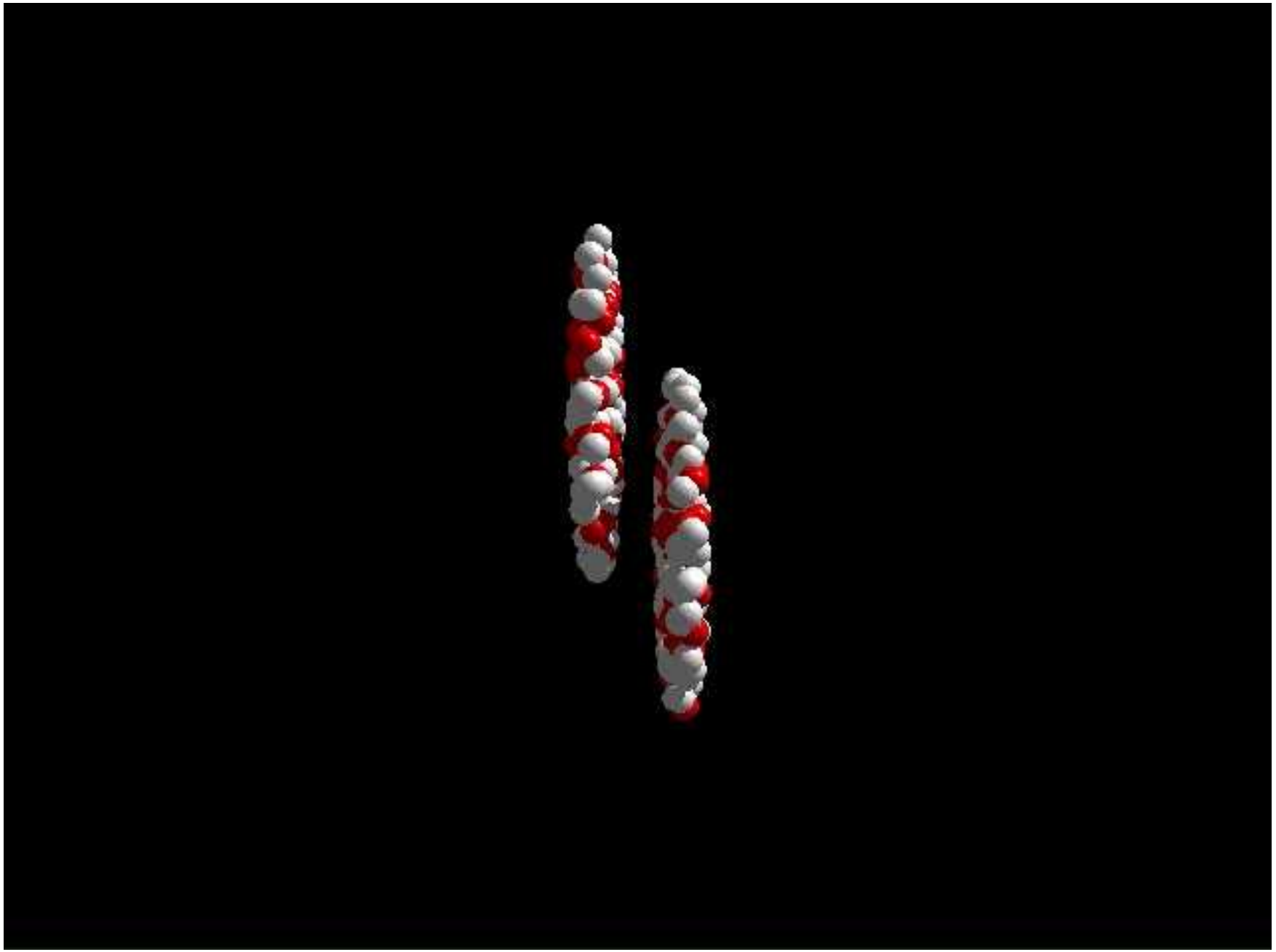
Motivation for the TOC

Composition within the ISOTDAQ curriculum

- One of the ***official goals*** of the school is to "***expose the participants to a maximum variety of topics***"
- What comes just after the "detector" is the ***first link*** of the ***DAQ chain***
- Therefore this lecture will try to deliver:
  - an ***intuitive approach*** to what is listed in the ***TOC***
  - ***without*** providing "***dry and ugly***" math ***phrases***
- This lecture will have ***no specific hands-on laboratory session*** in the current program of the school
  - However it will ***always*** be there at the lowest level of all the laboratory sessions you will attend
- The pages will contain ***enough amount of text*** necessary for you ***NOT*** to need a lecturer in order to understand the slides at home (naively assuming that you will refer to this lecture in near future)
  - Therefore please be aware of the above fact, in case you start feeling that the pages are a little bit ***overloaded***

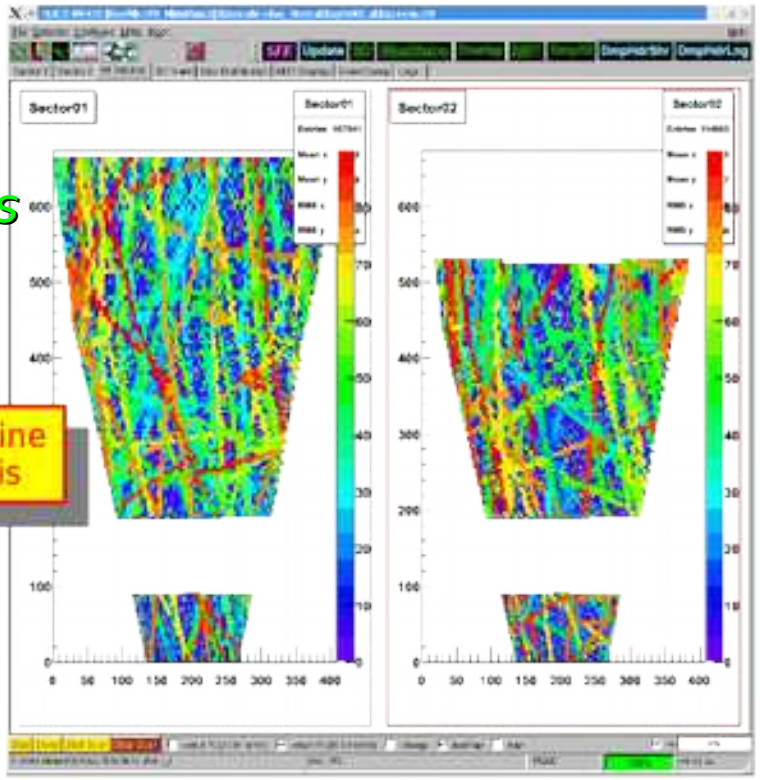
An Ordinary Heavy Ion Collusion

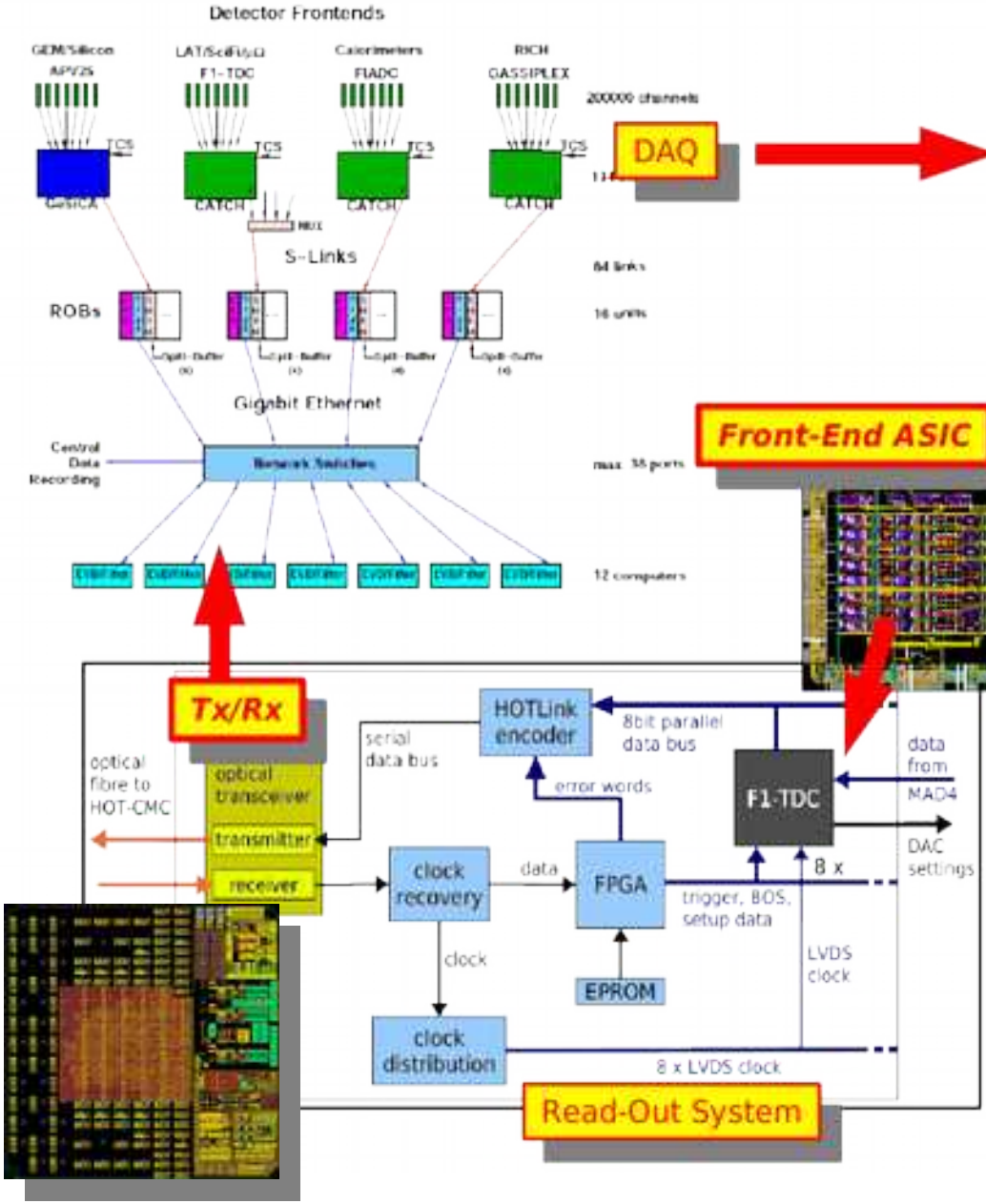
Heavy ions at the center of ALICE detector; a short movie of 5 ns

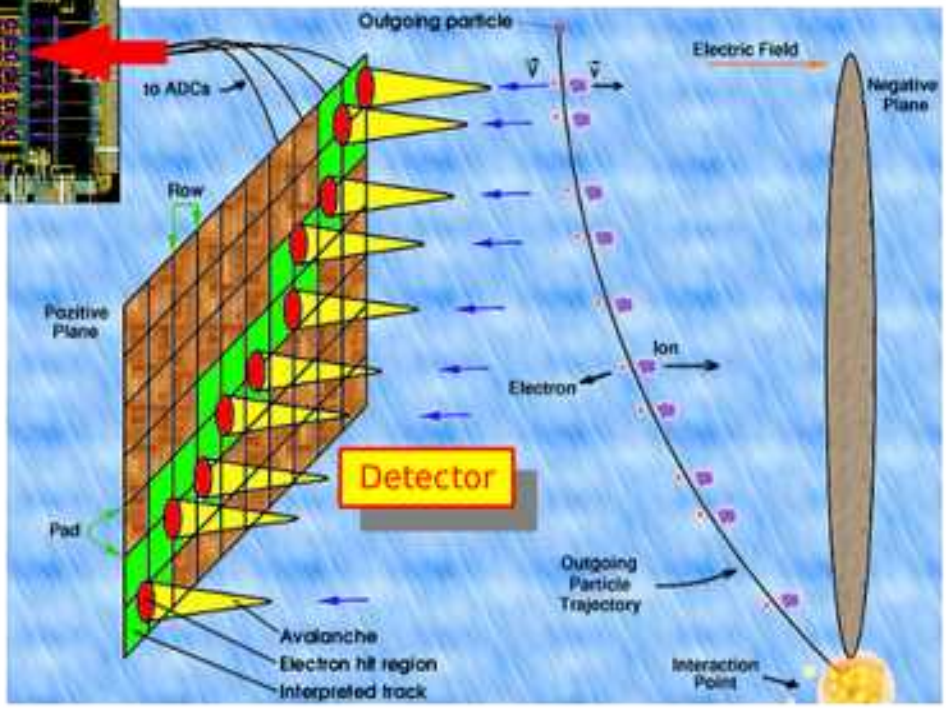


The Big (but Brief) Picture

From colliding particles at the interaction point
to the generation of meaningful data for analysis







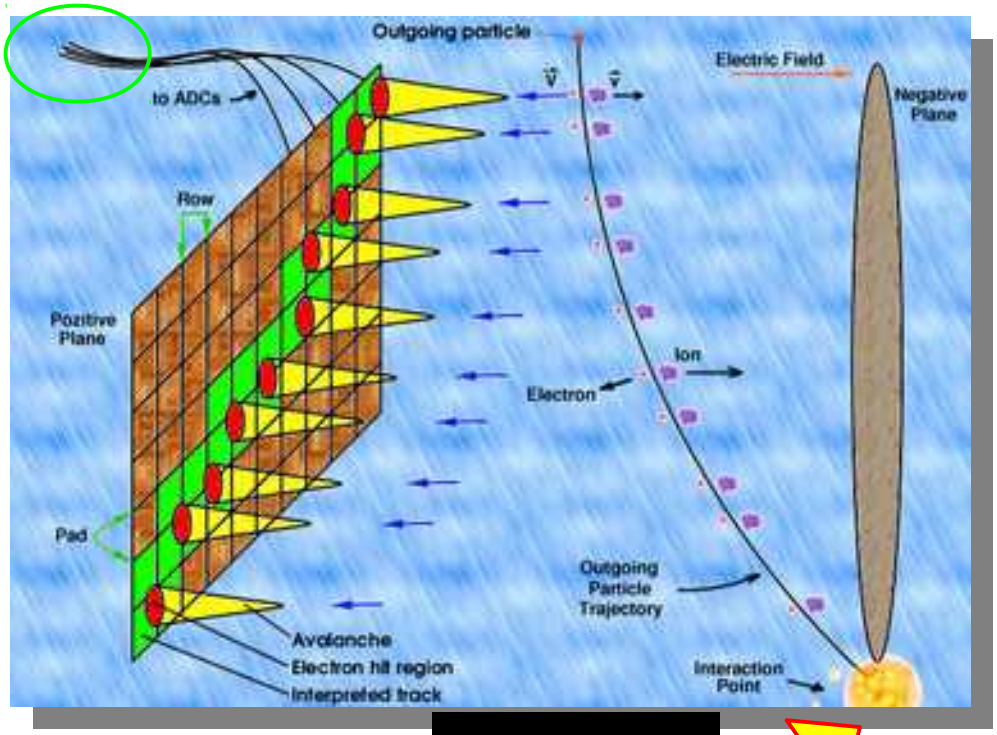
Briefly Front-End

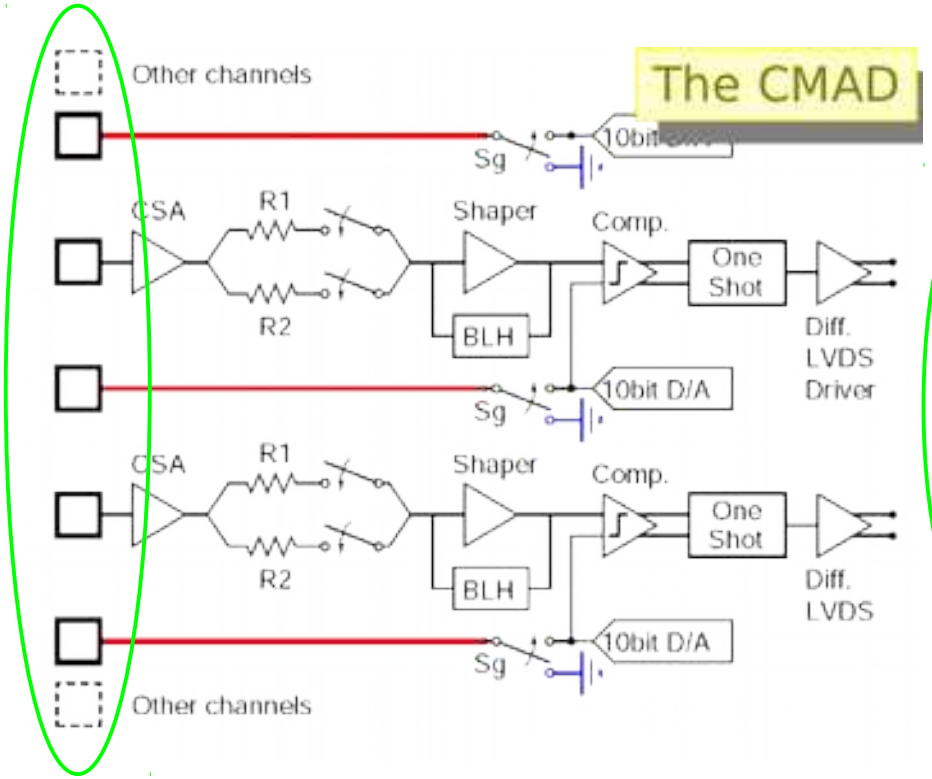
First interpretation of detector data

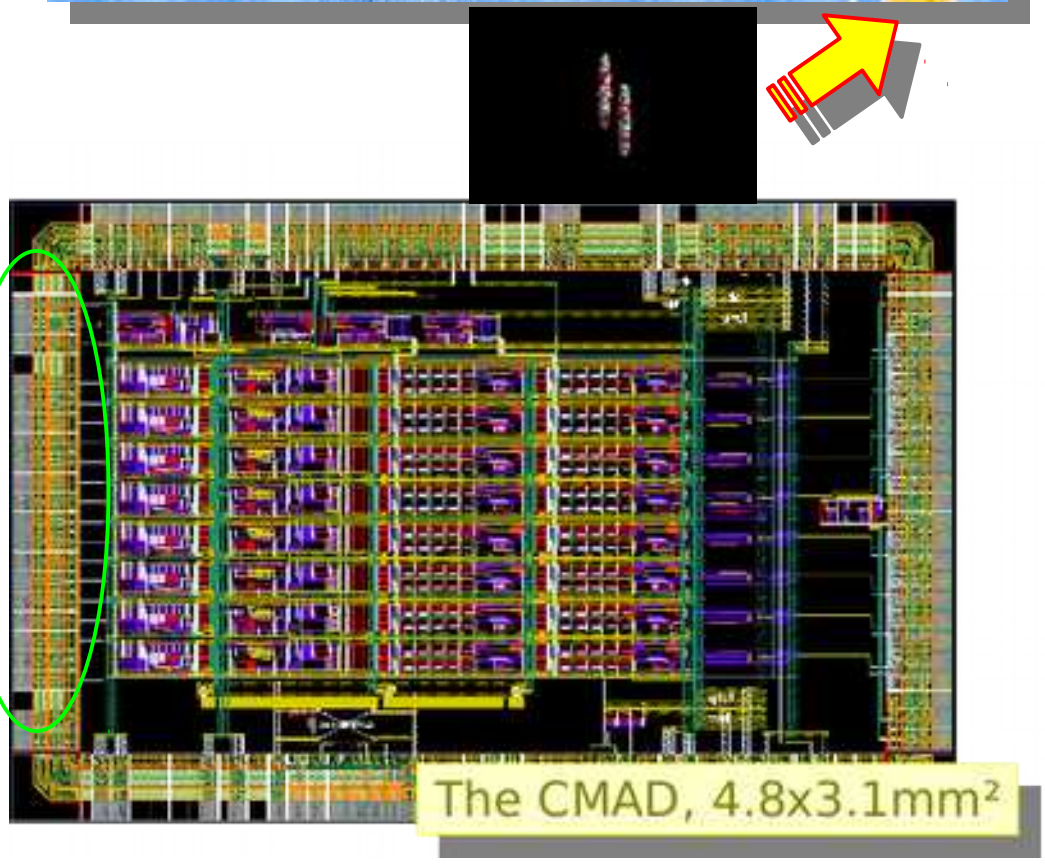
- **Integrate** the **charge** as a **pulse**
- **Shape** this **pulse**

1) **Compare** pulse height to a threshold
   - Higher **?** Yes **:** No
2) **Digitize** the pulse for further processing
   - Digital filters, corrections, etc.

- **Send** the result to **read-out**

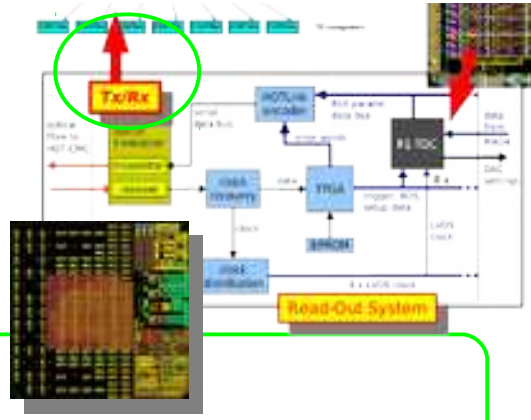




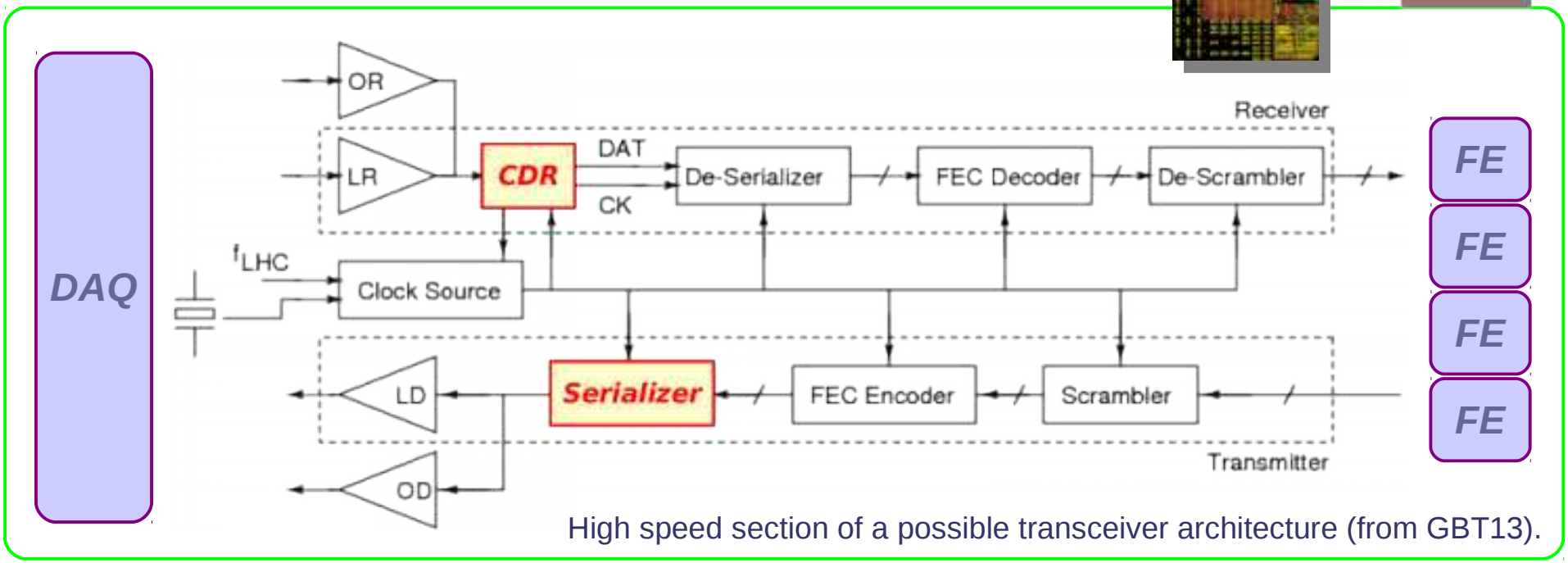


Briefly Read-Out

How to get data from FE and deliver to DAQ



- Add ***header/trailer*** to the data created by the detector FEs
- Combine payload fragments into ***frames*** to be transmitted to DAQ

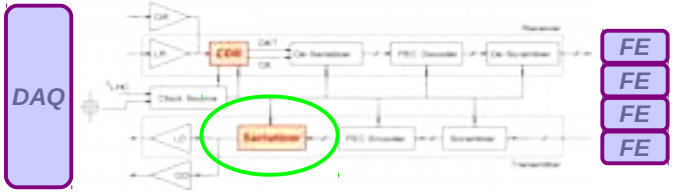


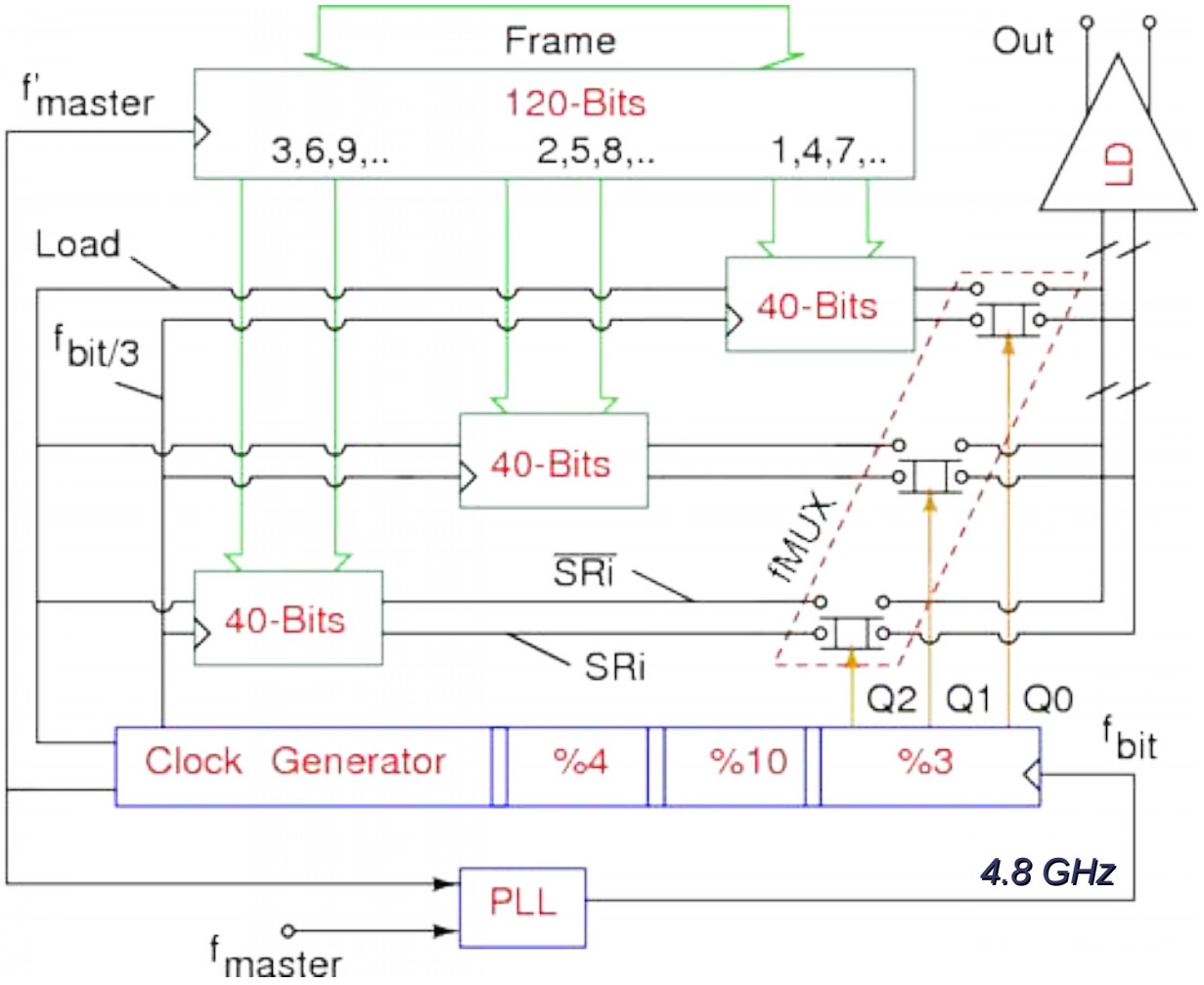
High speed section of a possible transceiver architecture (from GBT13).

- *Receiver*
  - ***Receive*** *laser light representing* ***serial data*** *from fiber*
  - *Check* ***FEC*** *code and* ***correct*** *errors (if possible)*
  - ***Parallelize*** *data*
  - ***Deliver*** *data to the next stage e.g. FE*
- *Transmitter:*
  - *Get data* ***from FE***
  - ***Calculate*** *FEC and* ***add*** *to frame, increasing resistance against transmission errors*
  - ***Serialize*** *parallel data*
  - *Drive a* ***laser diode*** *over fiber to DAQ*

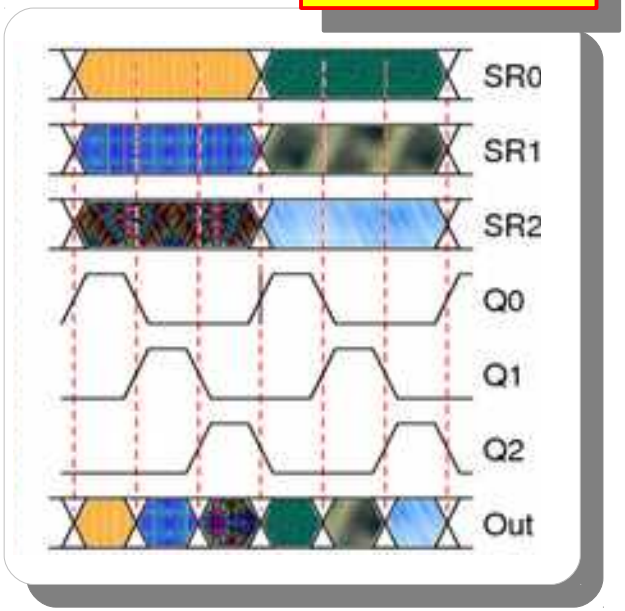
Briefly SER

Parallel → Serial





Timing Diagram



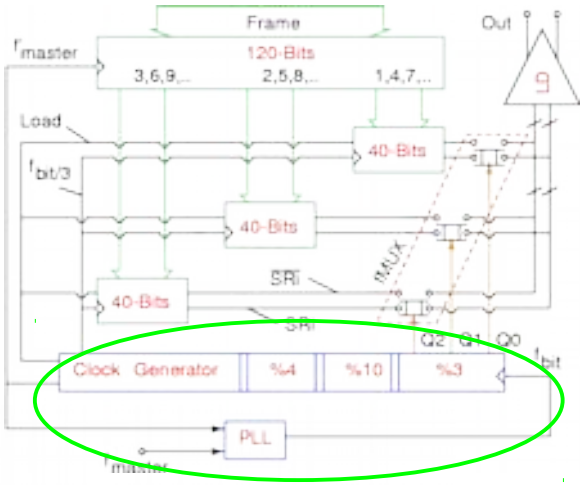
Eye Diagram

Operation:

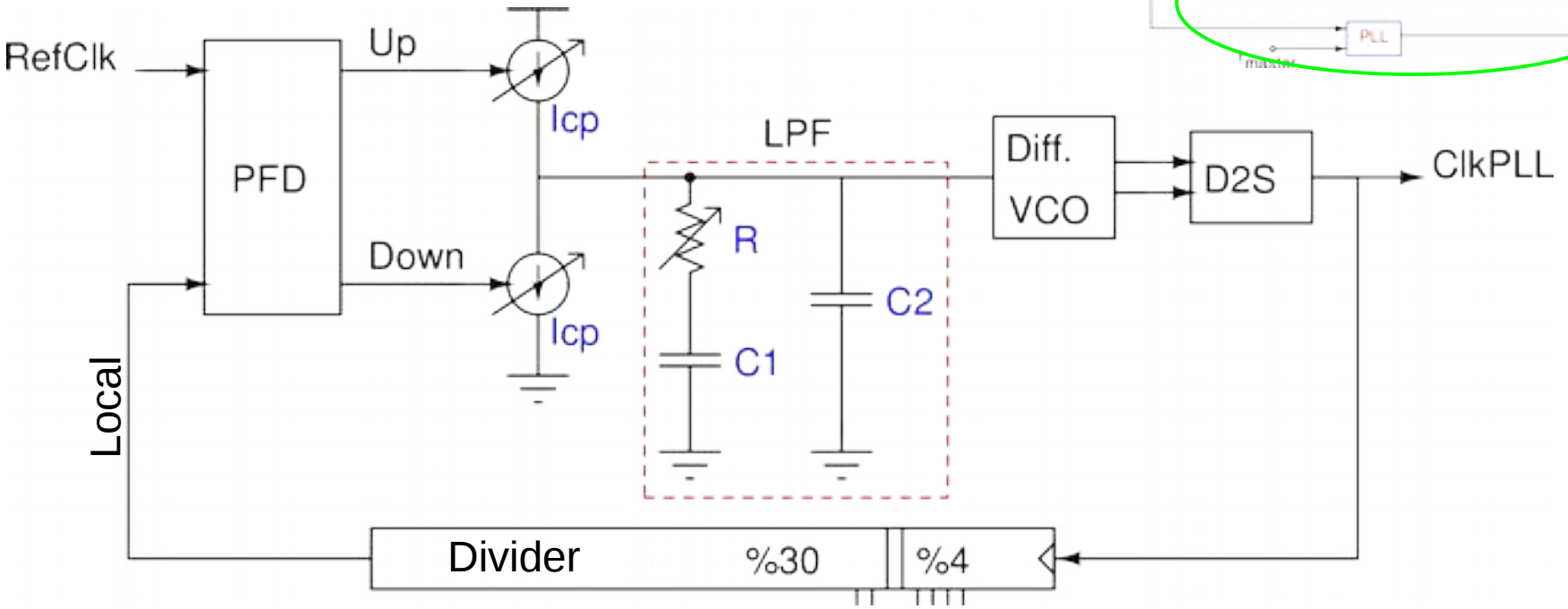
- *@ rising edge of f_{MASTER}, **load** 120-bit-wide **frame** into input register (**40 MHz**)*
- *@ rising edge of Load, **divide** the frame into 3 **40-bit-wide** words (**40 MHz**)*
- *@ rising edge of $f_{BIT/3}$, **right shift** 30-bit-wide words **sequentially** (**1.6 GHz**)*
- *After every shifting, **multiplex** the right bit **to output** (**4.8 GHz**)*

Briefly PLL

Phase-lock loop



- *Locking a clock to a (pseudo) periodic signal*
- *ClkPLL is what we we generate locally and RefClk is the reference to be tracked or to be locked to*



- ***Measure** the rising instant **timing difference** between **RefClk** and **ClkPLL** by the phase-frequency detector (PFD)*
  - ***Generate** correction commands depending on this measurement (**Up**, **Down**)*

- *Correction commands control the charge pump (Icp) **pumping/sinking current** into/from the filter capacitor, varying the **control voltage** for the Voltage Controlled Oscillator (VCO)*
  - *Gradually, the **timing error** of the two signals at the inputs of the PFD would **vanish** (ideal locked condition)*

* Please refer to Phaselock Techniques by F. M. Gardner

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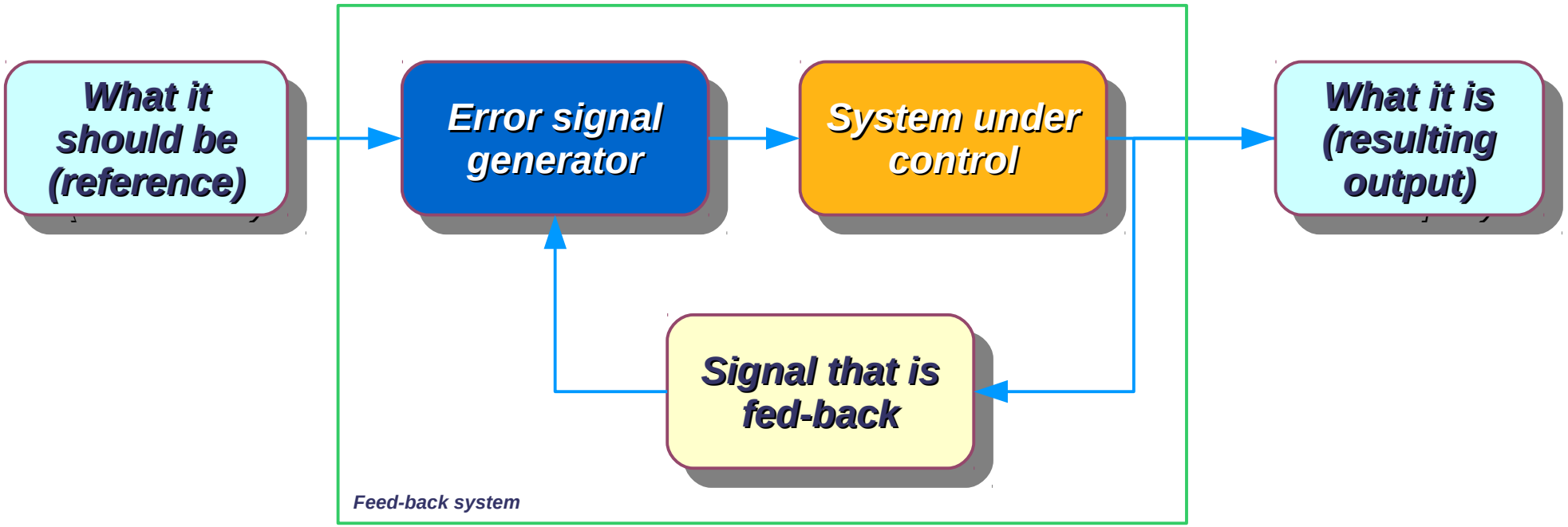
* *Application Specific Integrated Circuit*

Feed-Back

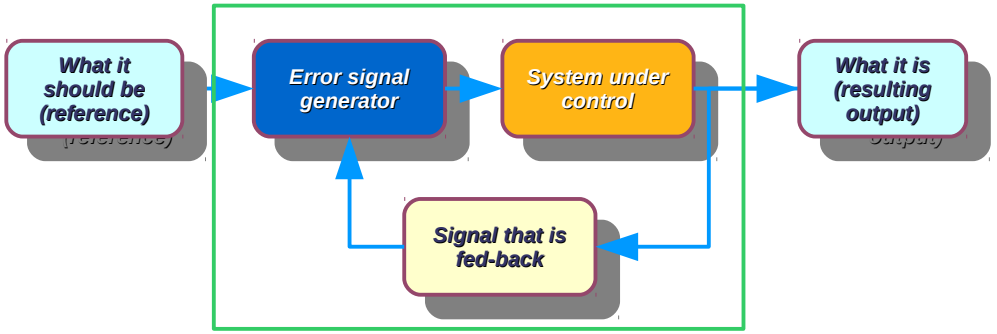
Actually a very familiar concept from daily life



- ***Aim**, is decreasing the **difference** (the error signal) between the **reference** and the **output***
- ***How ?** For each cycle:*
  - *A **portion of the output** is fed-back. Make the system be **sensitive** to a portion of what it outputs*
  - ***Measure** the difference between the reference and what is fed-back (only a portion of the output)*
  - *Depending on the difference, an **error signal** is generated which in turn causes a **correction step** to be taken **controlling the system** under control*
  - ***Repeat** the cycle*

Feed-Back

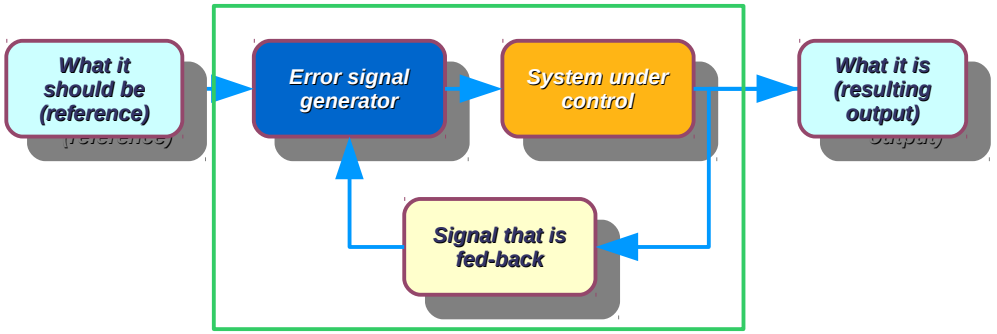
Actually a very familiar concept from daily life

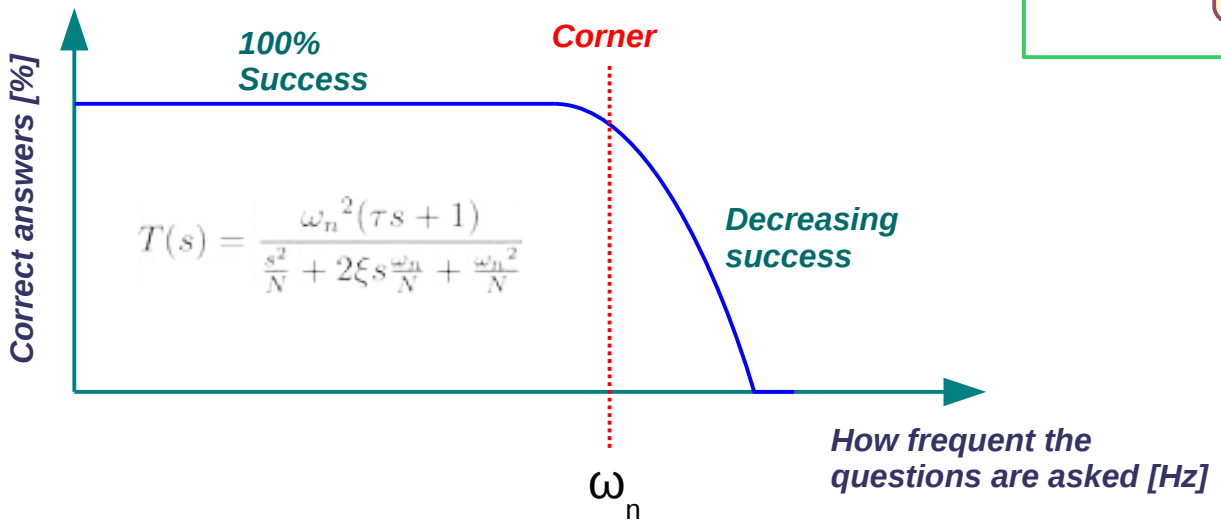


- *Whistling or playing an instrument ?*
  - *How do I **know** what I play is "**Do**" but not "**Re**" ?*
  - *Does it make sense to say "I whistle **better** than you" ?*
  - *What happens when I try **to find the right** guitar solo for an existing song ?*
- *Drinking a glass of water ?*
  - ***Adjust** the angle & position of the glass accordingly **to keep** the water flow as it is **necessary** ?*
  - *Remember the childhood: sometimes the water gets dropped to the ground accidentally (What is the **failure mechanism** ?)*
- *Walking and biking ?*
  - *How do I **decide the frequency** of my steps **not to** fall down or **to be able to** reach somewhere ?*
  - *What about walking or biking **when drunk** ? (What is the **failure mechanism** ?)*
- *Ruling a country ?*
  - *Can "**referendum**" be a term borrowed from the **control theory** ?*
  - *How come politicians of the same ideology can **decide** in substantially different manners ? < Questionably ignoring corruption :D >*

Feed-Back

Natural frequency concept



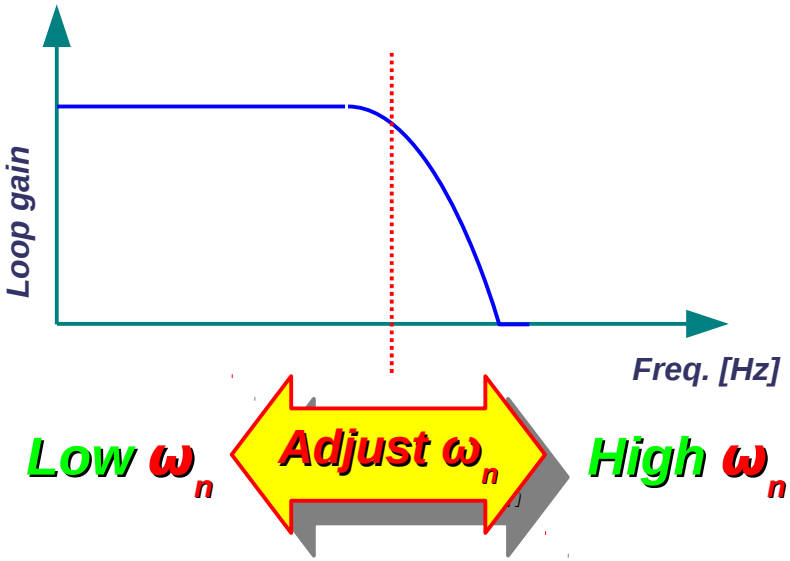


- *An imaginary **system answering questions** asked continuously*
- ***Plot*** (both logarithmic scale) the ***success*** *level within a certain time window as a function of **frequency** of questions asked (transfer function)*
- *If the questions are asked **slow enough**, the system answers **all**, thus 100% success level*
- *Once the questions start to be asked **faster**, the system **starts failing** answering all, thus transfer function begins going down*
- ***Corner** is **at the natural frequency** of the control loop where the system **starts impairing significantly***

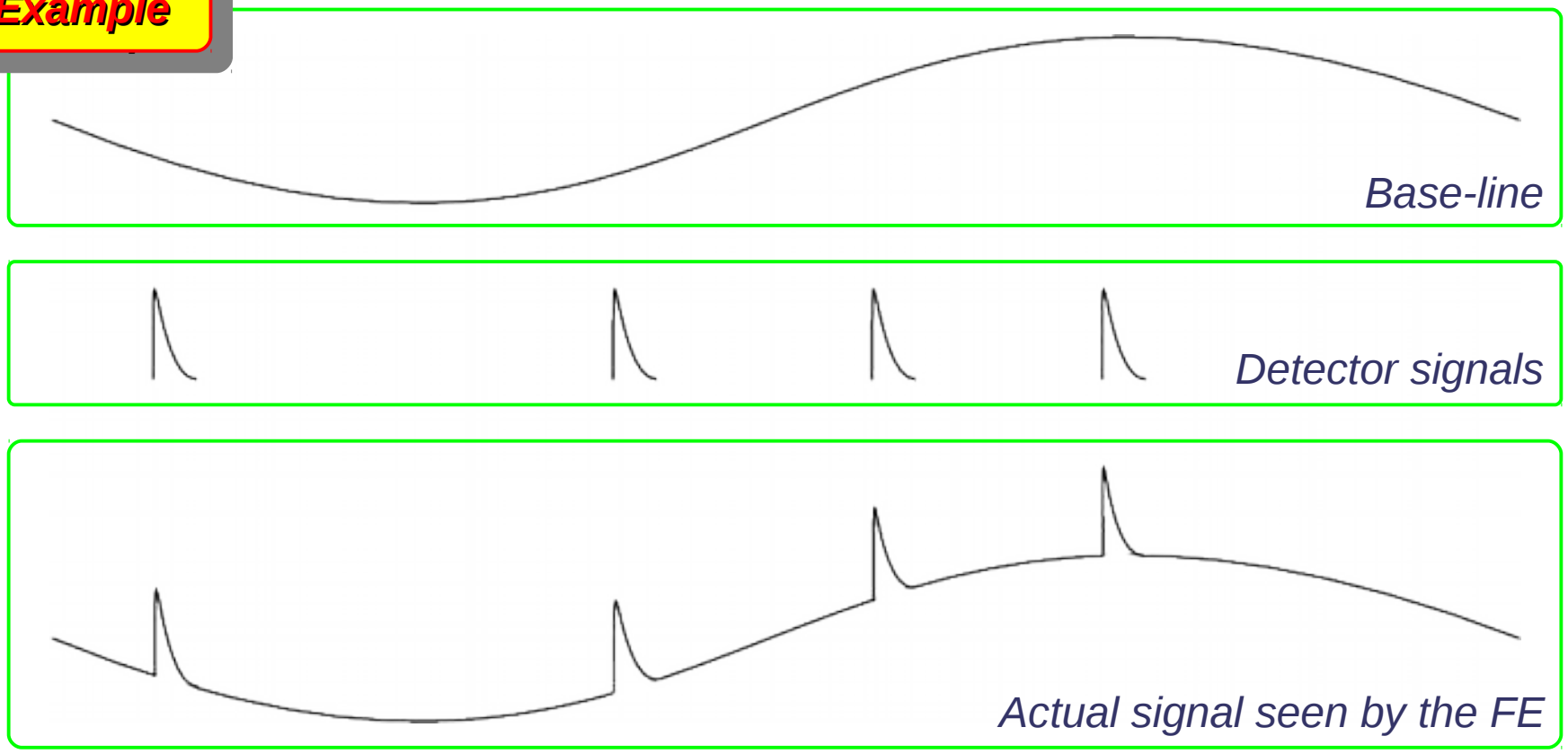
Feed-Back

Choosing for what to be sensitive

- **Low ω_n** → Sense **slow variations**
  - Loop **acts** on **slowly varying** signals
  - Narrow bandwidth – slow loop
- **High ω_n** → Sense **fast variations**
  - Loop **acts** on **rapidly varying** signals
  - Wide bandwidth – fast loop



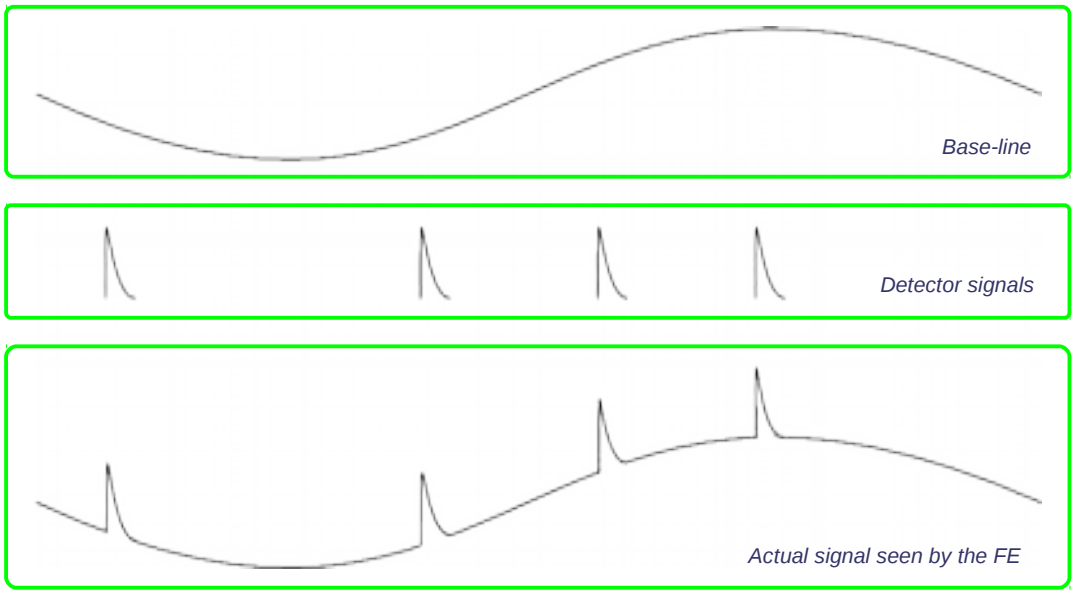
Example

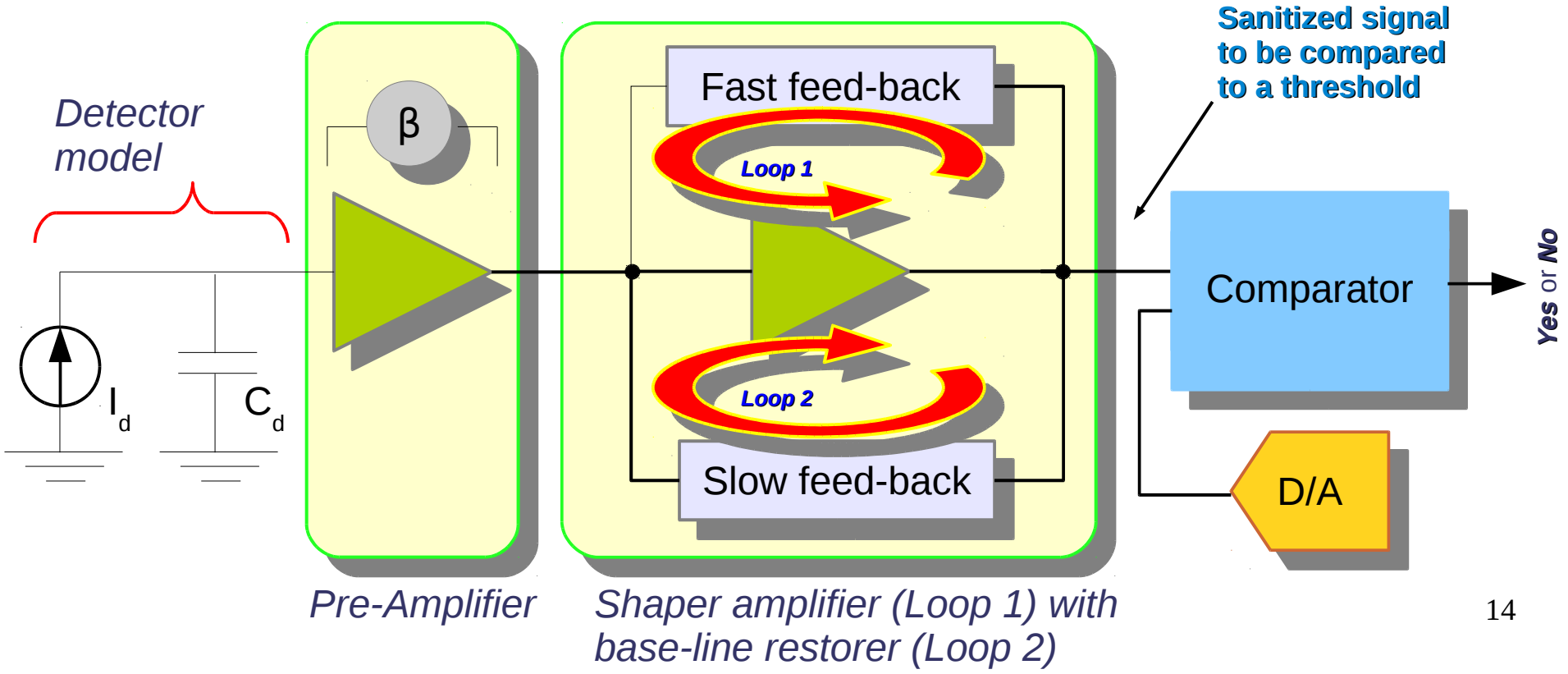


Example

Binary read-out

- Requires stable ***base-line***
  - Which varies slowly
  - A ***narrow*** loop bandwidth is needed ***(Loop 2)***
- Requires a fast signal ***shaper***
  - Which varies rapidly
  - A ***wide*** bandwidth is needed ***(Loop 1)***



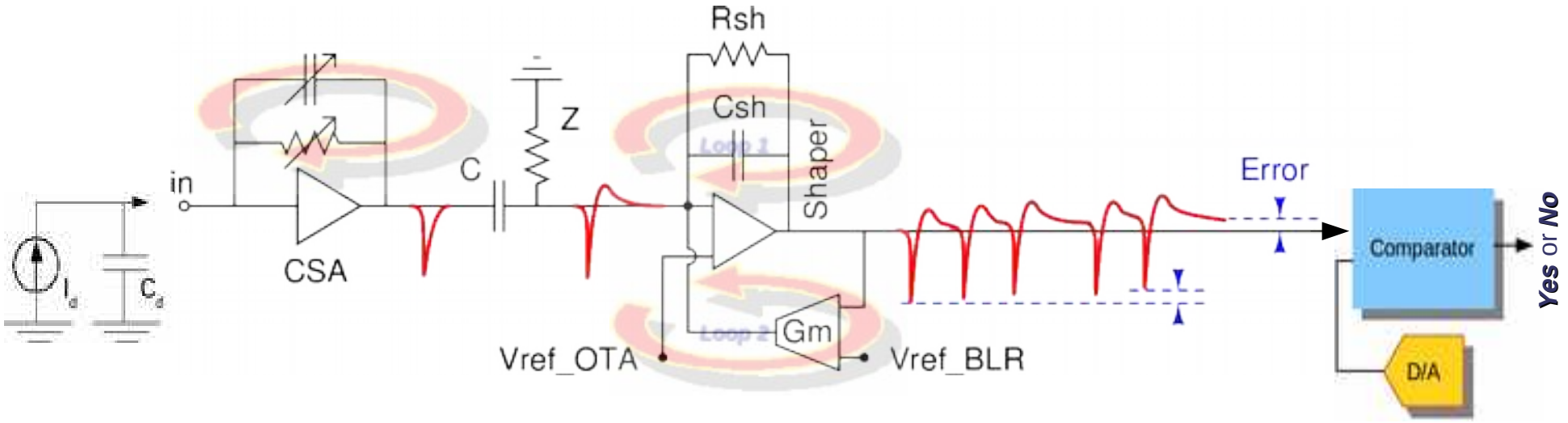


Real-World Example

Binary read-out for time-over threshold measurement

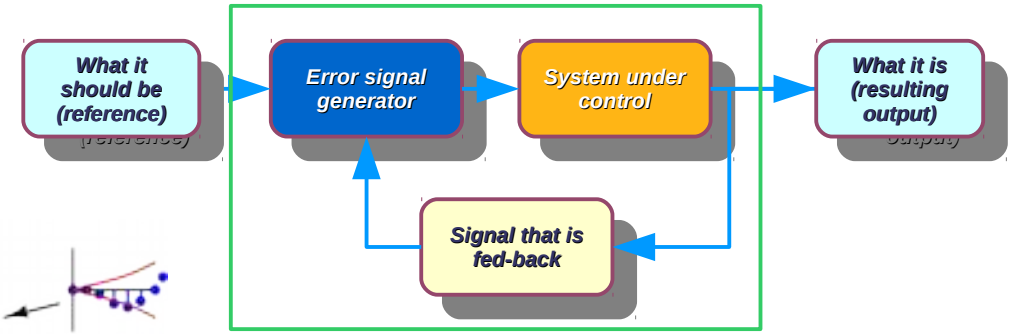
- ***Random*** detector ***pulses*** with ***a few MHz*** frequency; then...
  - ***How fast*** is the ***fast loop*** ?
  - ***How slow*** is the ***slow loop*** ?

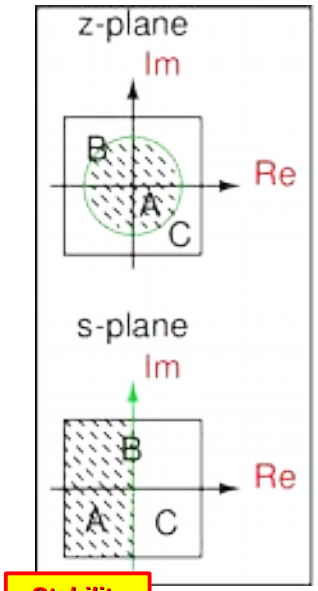
- Depending on the read-out ***speed*** and the operating ***environment***, parameters are ***optimized***
  - *Natural frequencies and gains of the loops, rise/fall-times,* ***etc****.*
  - *Settling behavior, radiation tolerance, damping ratio, power,* ***etc****.*
  - *Circuit footprint, robustness, redundancy, channel efficiency,* ***etc****.*



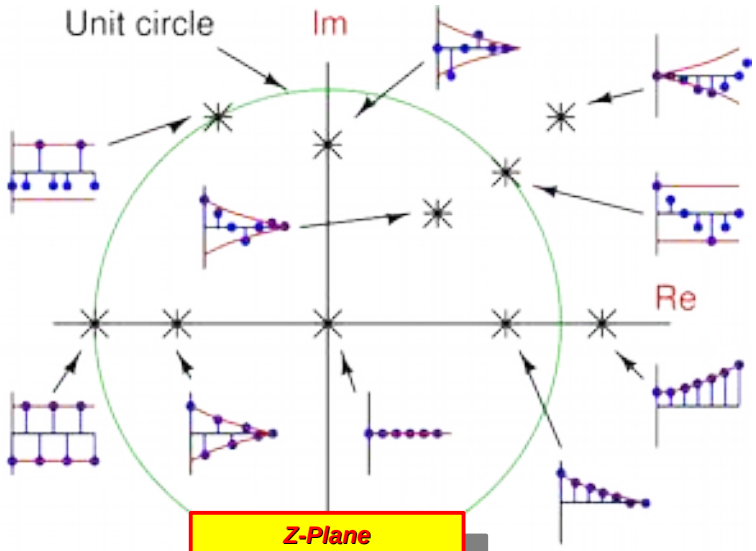
Feed-Back

Optimizing the loop behavior





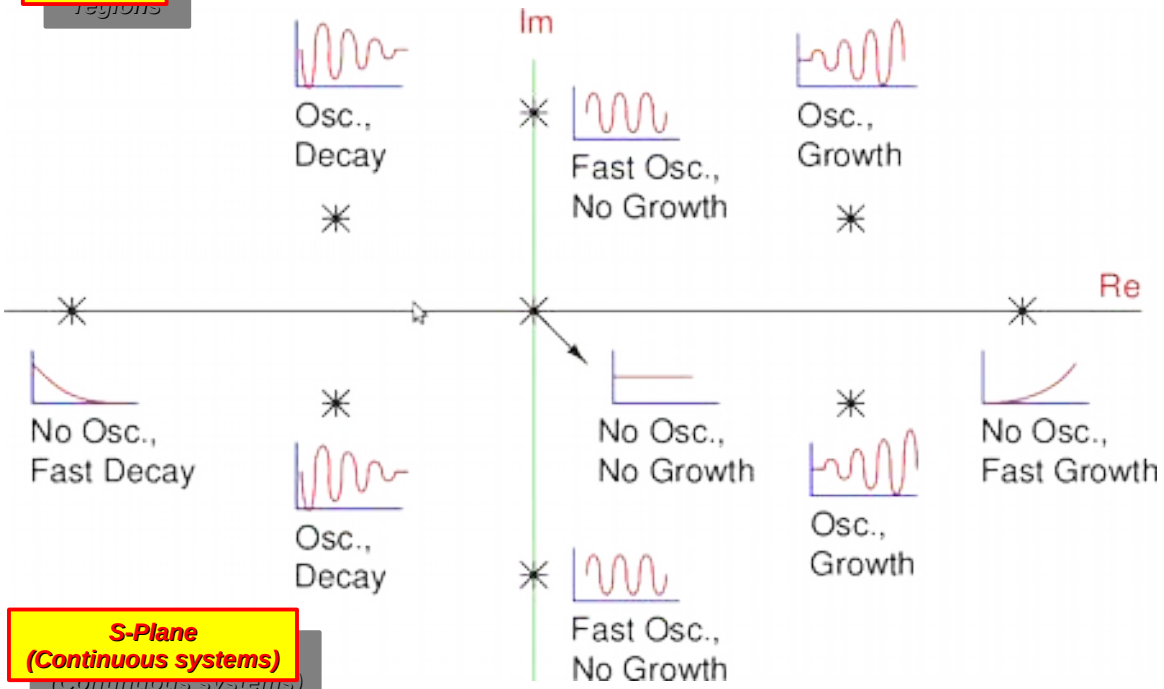
Stability regions



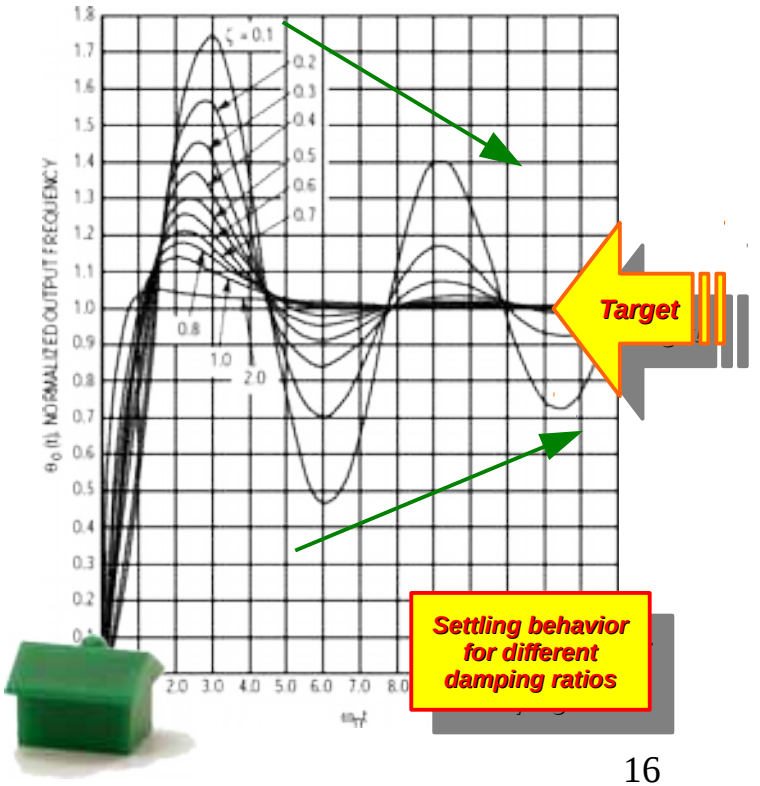
Z-Plane (Discrete systems)

Transfer function

$$T(s) = \frac{\omega_n^2(\tau s + 1)}{\frac{s^2}{N} + 2\xi s\frac{\omega_n}{N} + \frac{\omega_n^2}{N}}$$

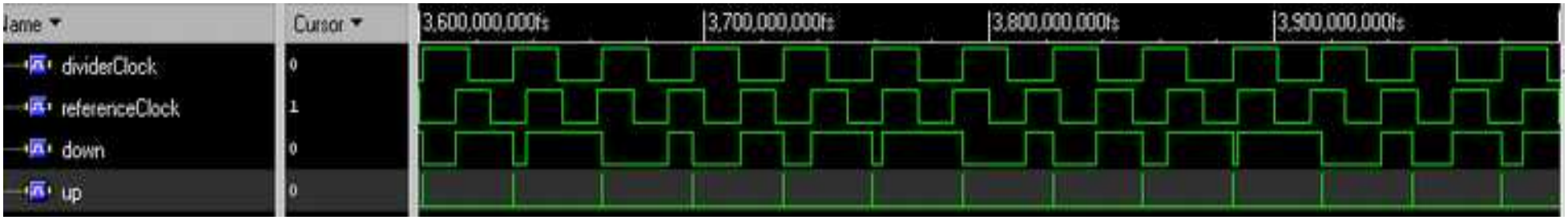


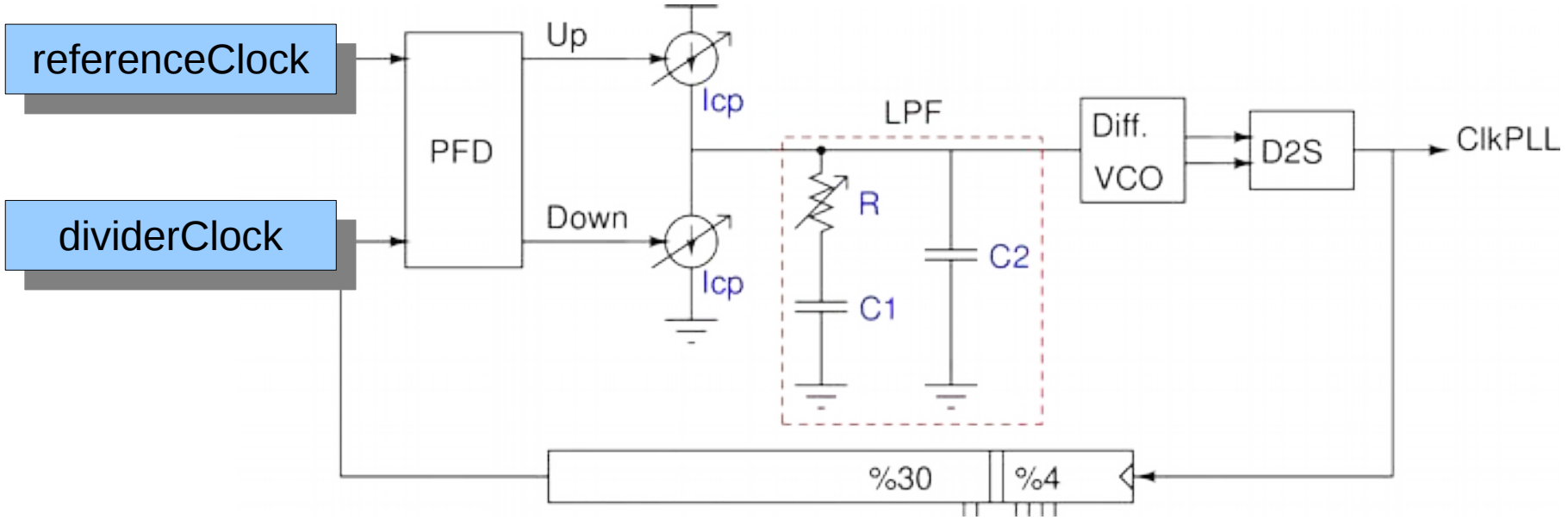
S-Plane (Continuous systems)



Simulation Movie Quiz

Remember the PLL



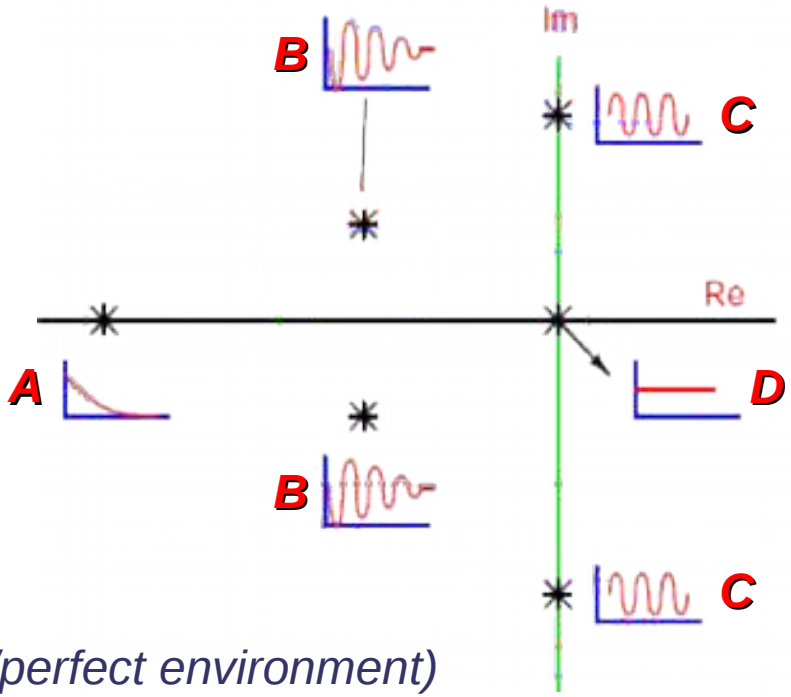


- ***Slow down*** the VCO, ***if*** it is ***too fast*** with respect to the reference
- ***Speed up*** the VCO, ***if*** it is ***too slow*** with respect to the reference

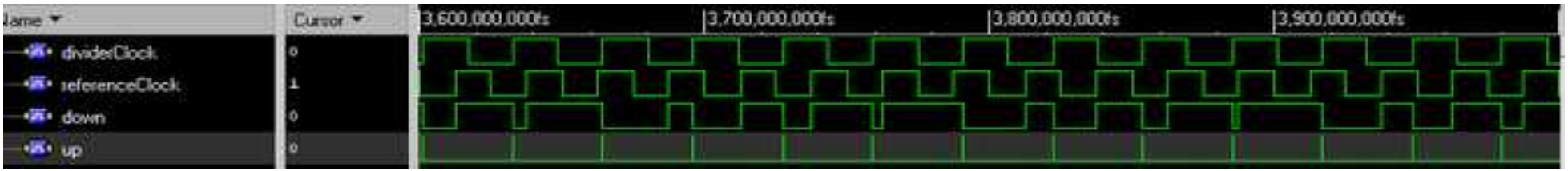
Simulation Movie Quiz

Different loop behaviors

- **See** the movies and **associate** the **behavior** to the **poles** on the **s-plane** (complex plane)
- Use your **intuition**



? - Slow-loop with **low damping** ratio (**noiseless**/perfect environment)



? - Fast-loop with **high damping** ratio (**noiseless** environment)

? - Slow-loop with **low damping** ratio (**noisy** environment)

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Different loop behaviors

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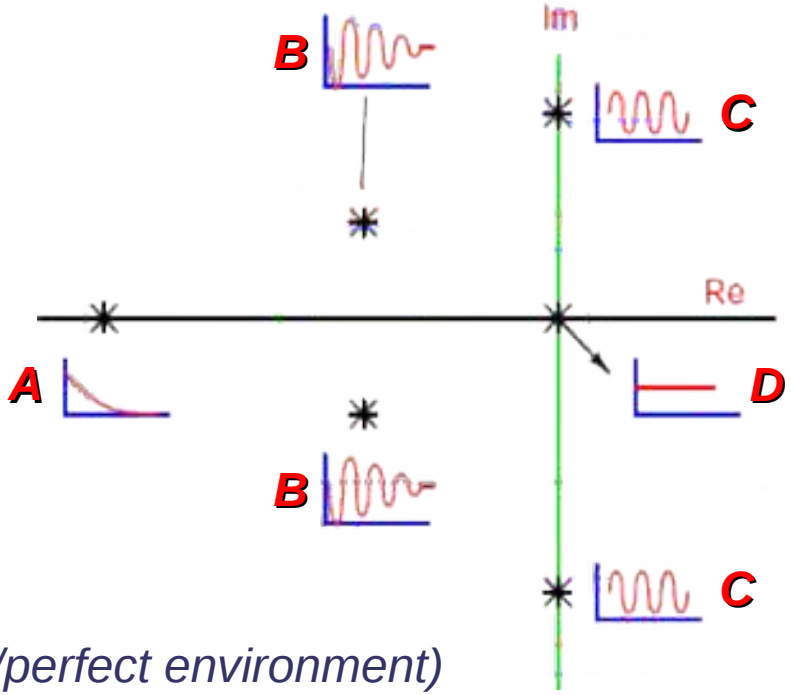


B - Slow-loop with **low damping** ratio (**noiseless**/perfect environment)

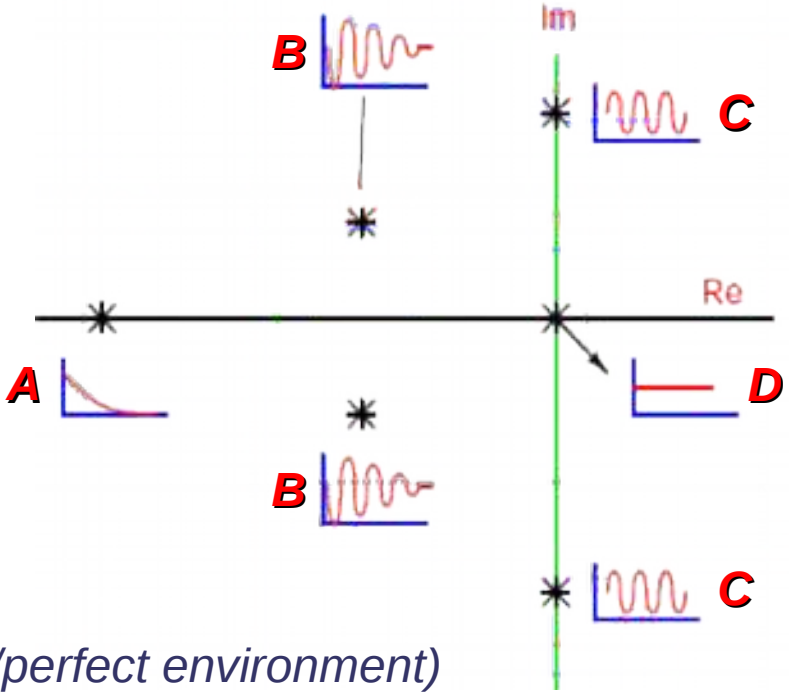
? - Fast-loop with **high damping** ratio (**noiseless** environment)

? - Slow-loop with **low damping** ratio (**noisy** environment)

Simulation Movie Quiz

Different loop behaviors

- **See** the movies and **associate** the **behavior** to the **poles** on the **s-plane** (complex plane)
- Use your **intuition**



B - Slow-loop with **low damping** ratio (**noiseless**/perfect environment)

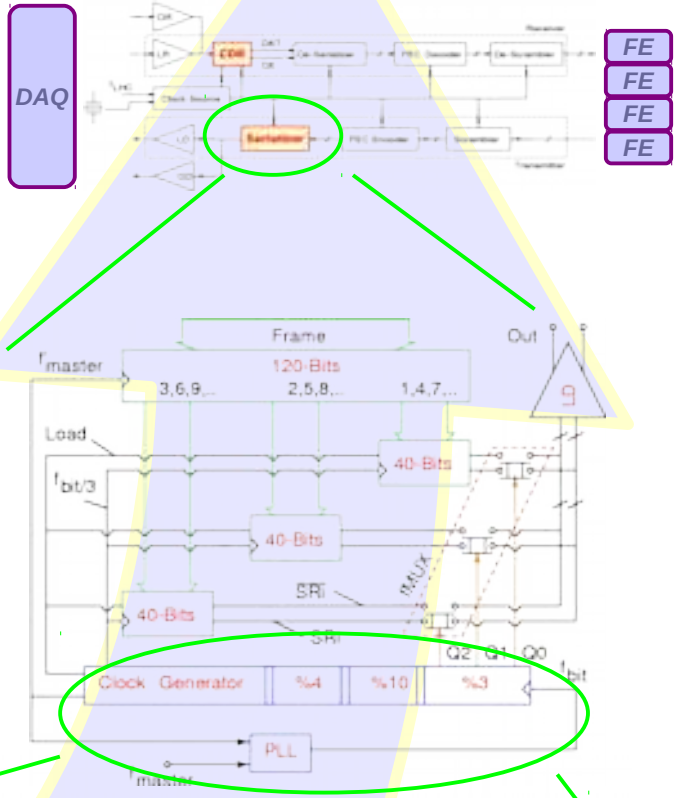
A - Fast-loop with **high damping** ratio (**noiseless** environment)

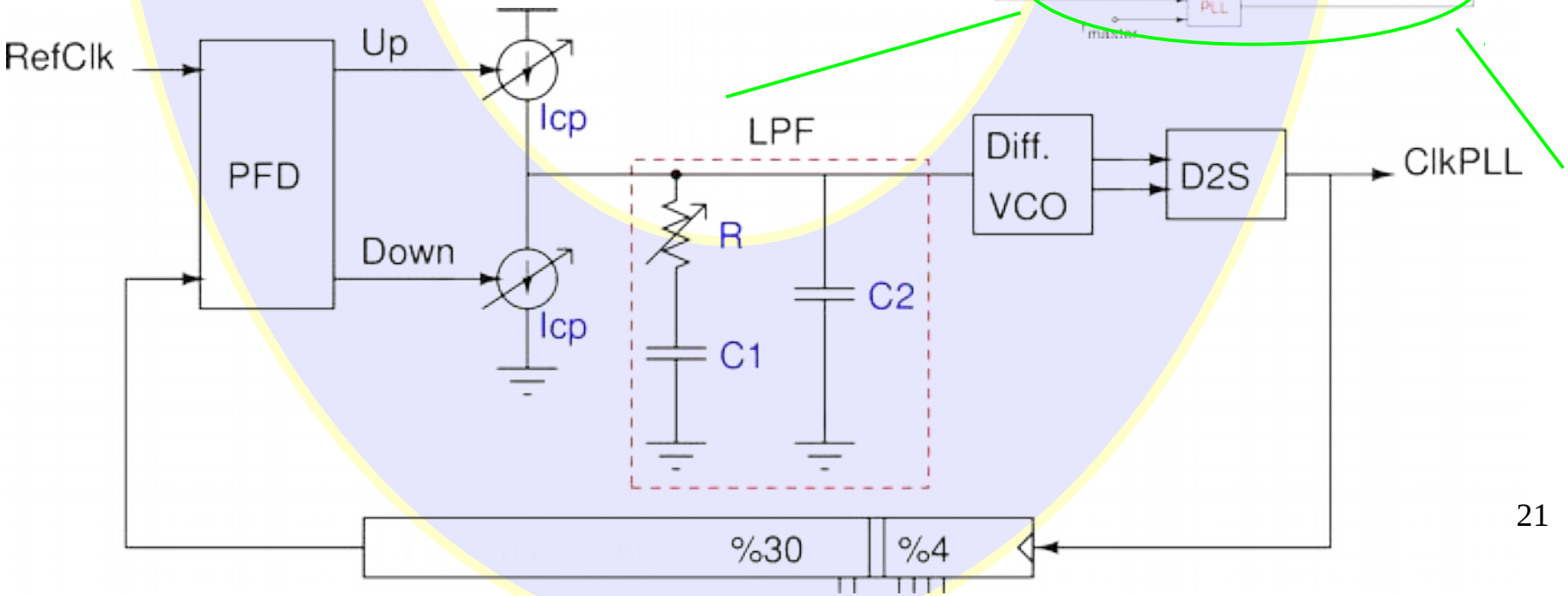
? - Slow-loop with **low damping** ratio (**noisy** environment)

Back to the big picture

If the PLL fails, then nothing works !..

- *In case the loop **parametrization** is wrong:*
  - *PLL can not deliver a proper **clock***
    - *No phase/frequency locked ClkPLL signal*
    - *Ignored LHC clock, no synchronization*
  - *SER fails*
    - *Some of the bits get **lost** or **duplicated***
    - *High **jitter** leading to closed **eye diagram***
  - *RO fails delivering the data from FE to DAQ*
  - *No DAQ → **Fatal error** !..*





Introduction to the Design of Full-Custom Front-End & Data Transmission ASICs*

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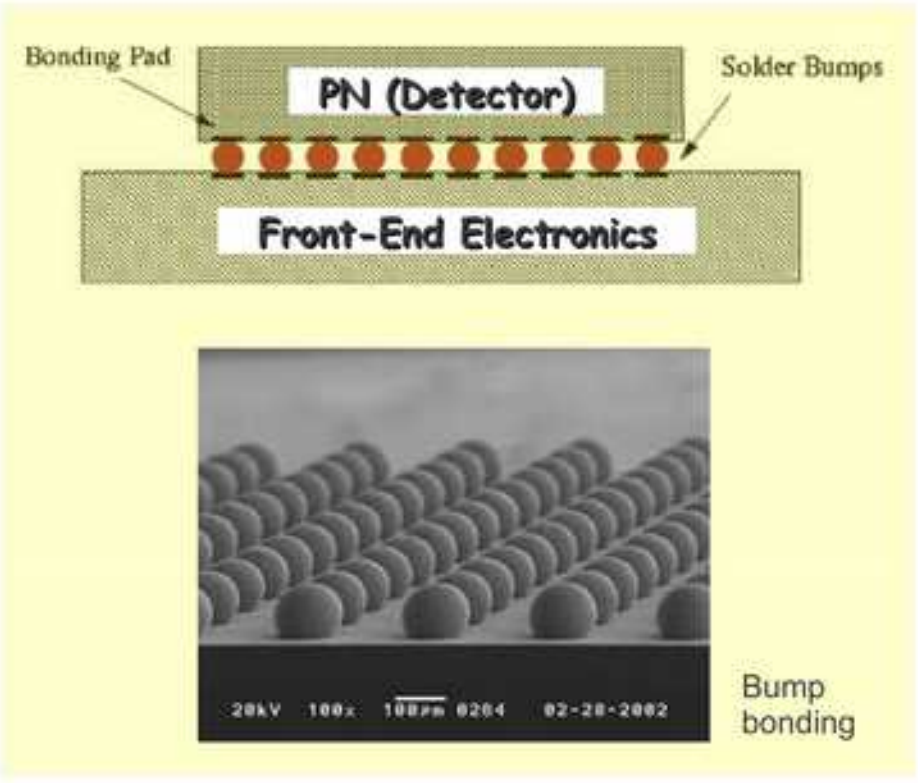
- **Radiation Tolerance Issues**
  - Definitions:
    - **Single event upset, analog single event transient, latch-up**
  - **Simulating** radiation effects on analog circuits

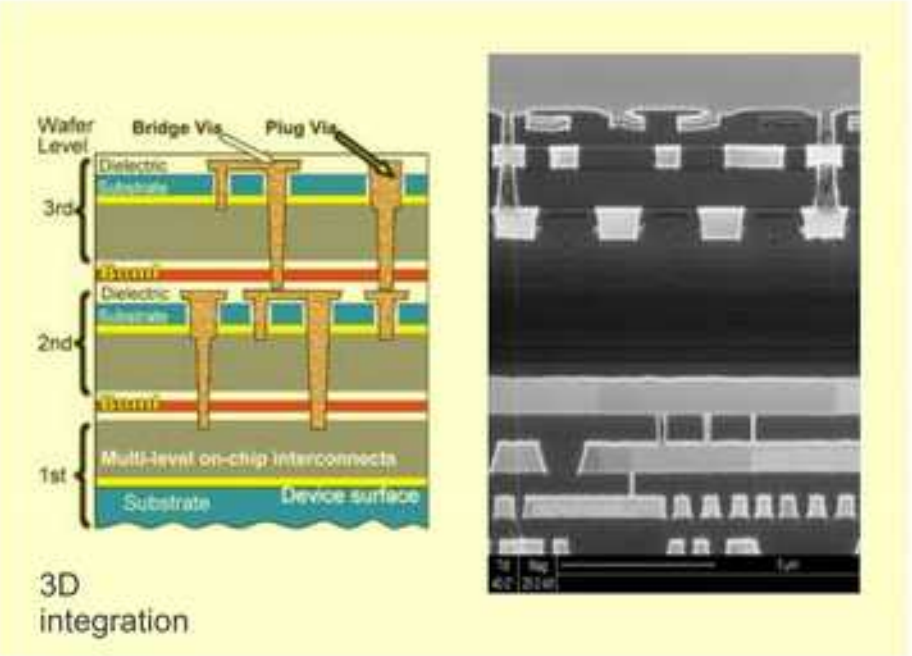
* *Application Specific Integrated Circuit*

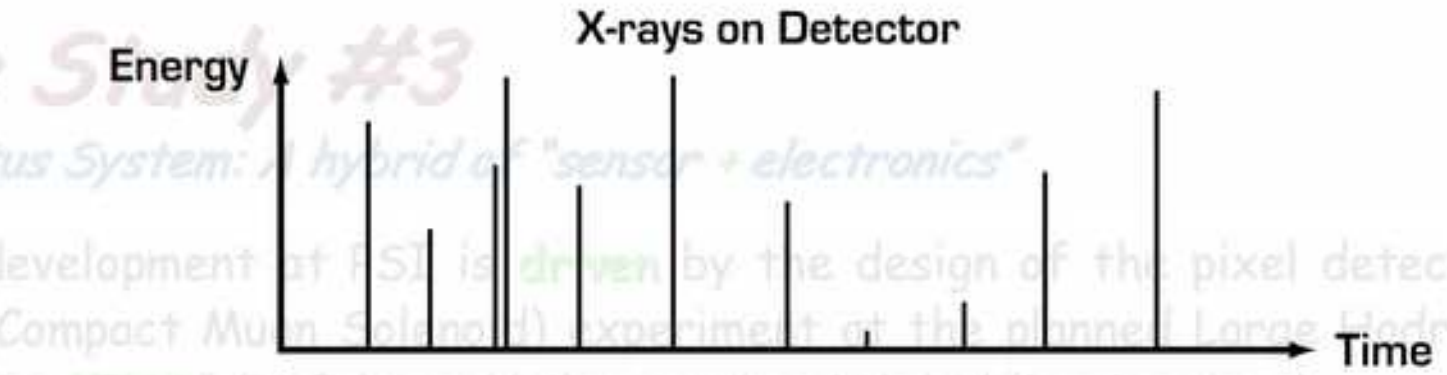
An Example

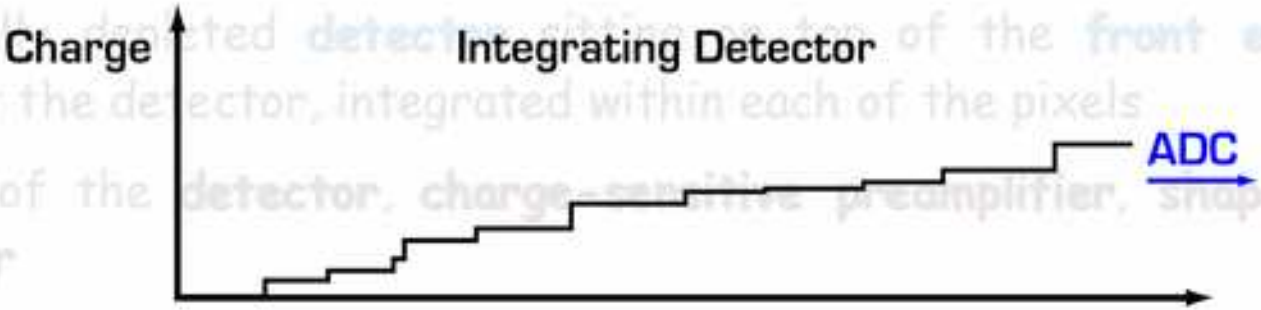
Pilatus System: A hybrid of "sensor + electronics"

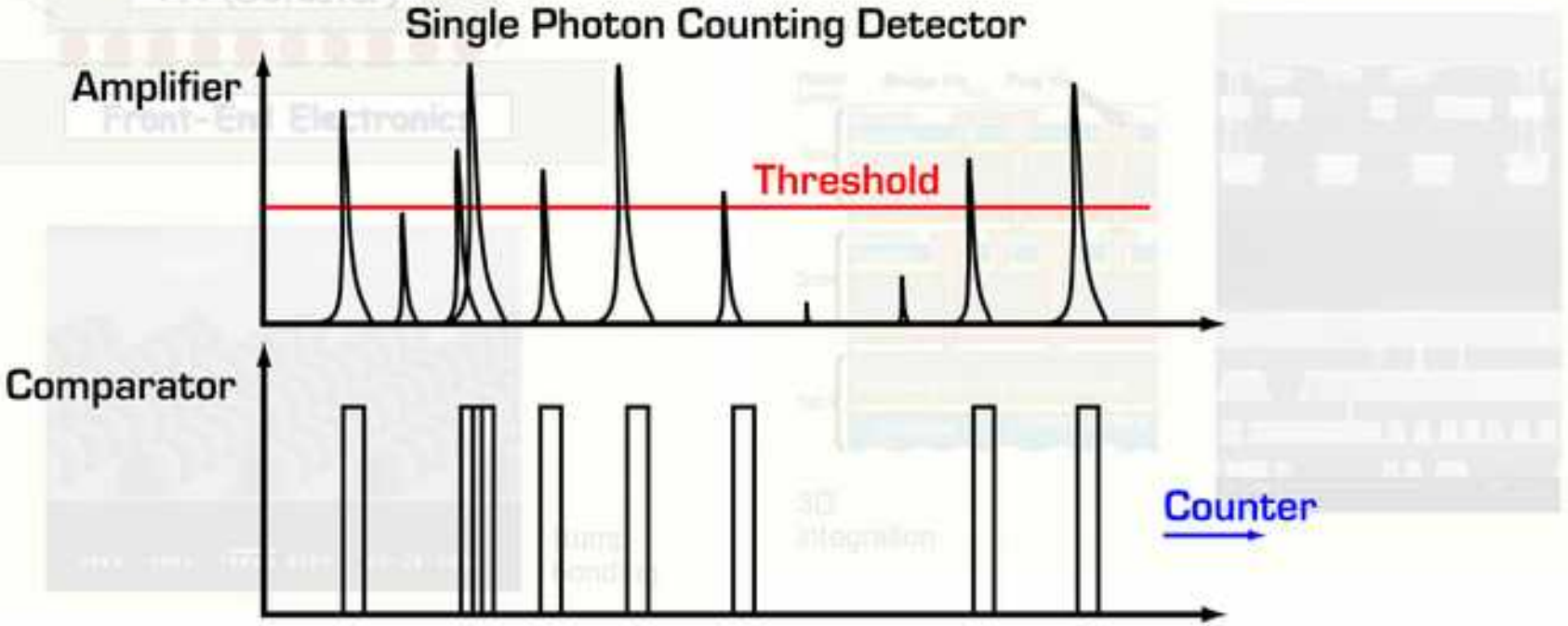
- "The development at PSI is **driven** by the design of the pixel detector for the **CMS** (Compact Muon Solenoid) experiment at the planned Large Hadron Collider (**LHC**) at **CERN**." (Ref: http://pilatus.web.psi.ch/publications.htm)
- **Hybrid**: fully depleted **detector** sitting on top of the **front end** electronics, reading out the detector, integrated within each of the pixels
- Composed of the **detector**, **charge-sensitive preamplifier**, **shaper**, **comparator** and **counter**

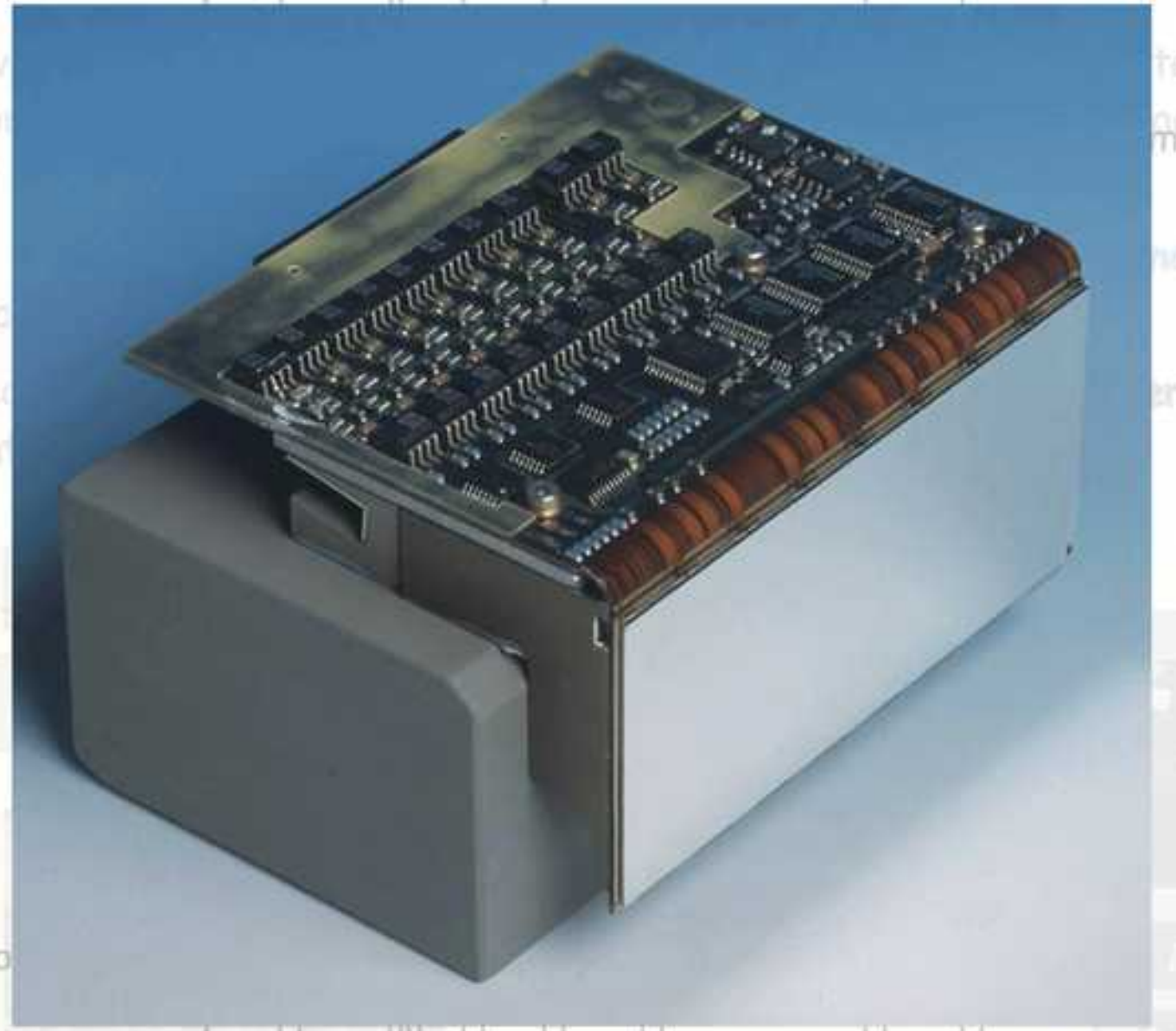


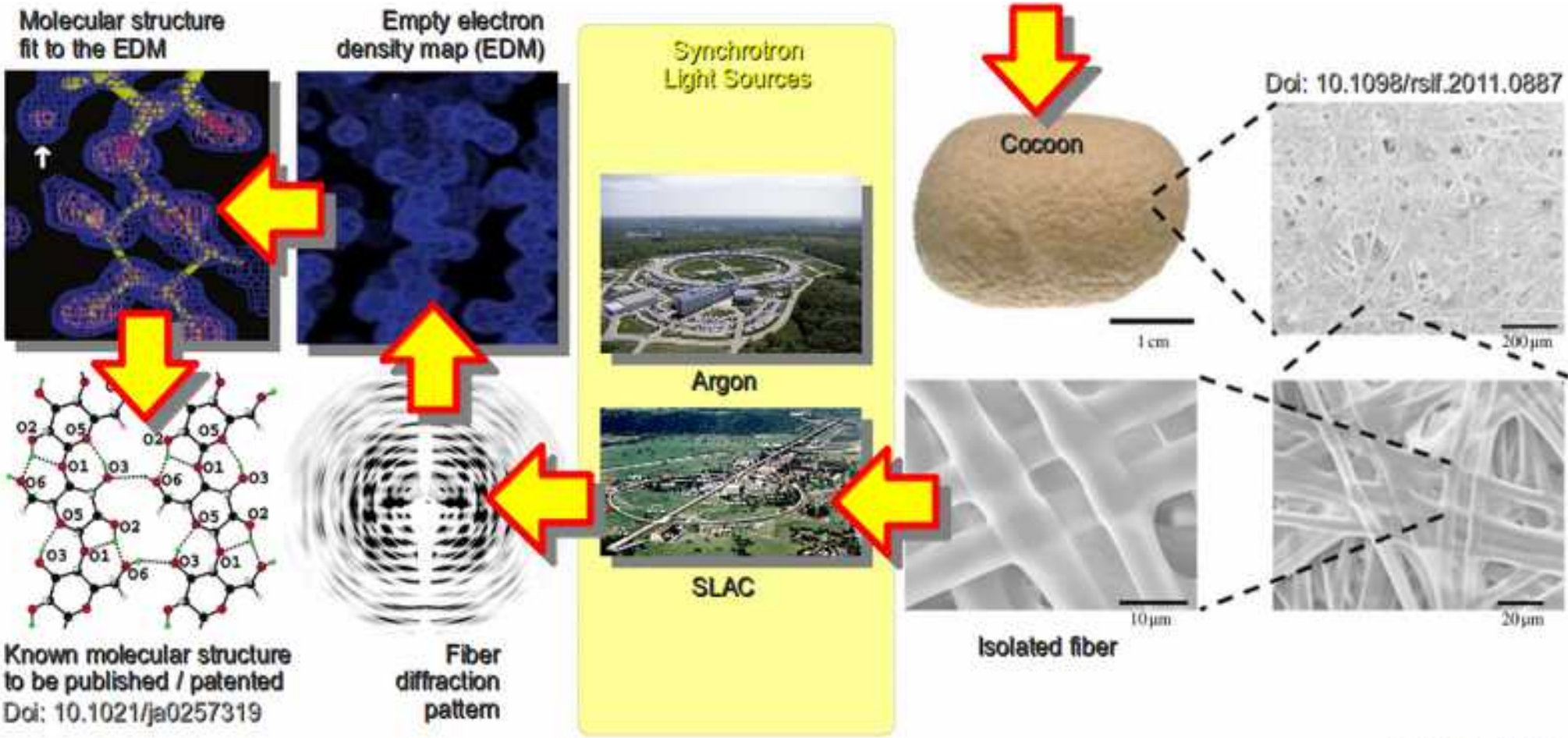


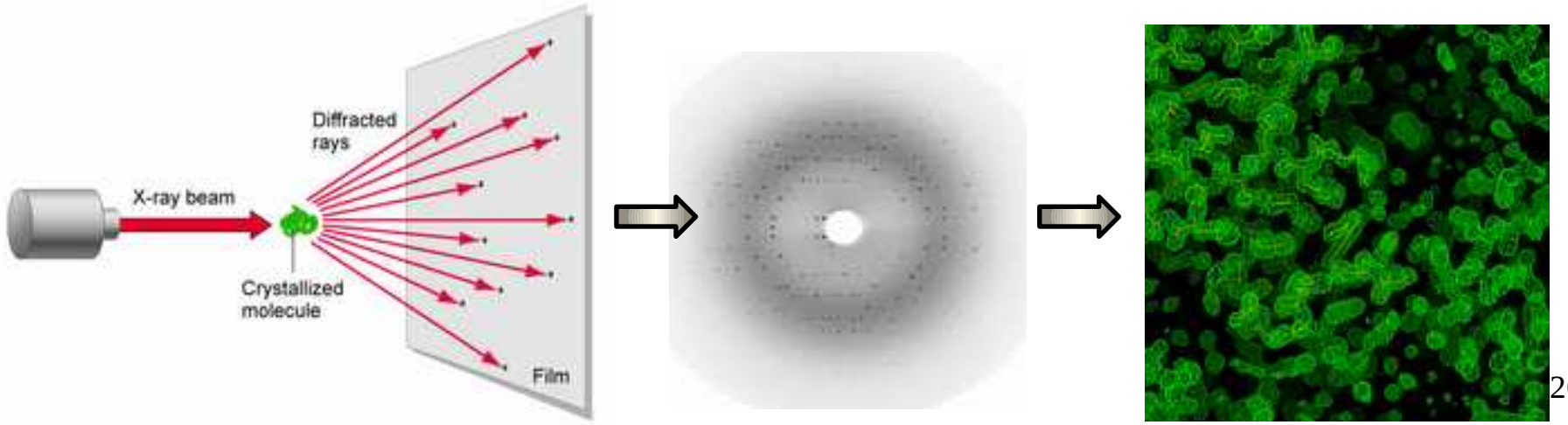

X-rays on Detector
Energy
Time


Charge
Integrating Detector
ADC


Single Photon Counting Detector
Amplifier
Threshold
Comparator
Counter







Difraction pattern

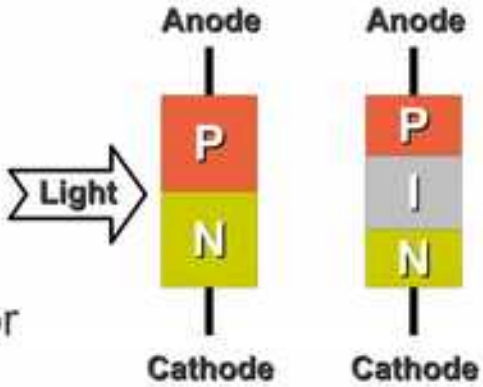
Electron density map

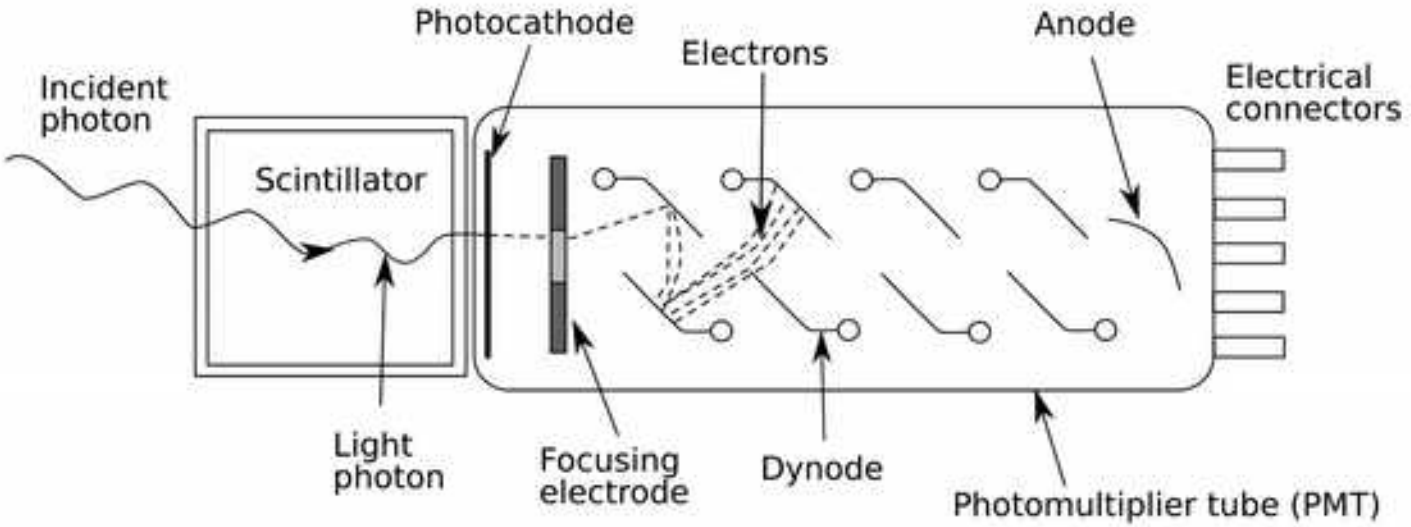
Crowd vs Counted Individuals

First interaction with the photons (and/or particles)

- Impossible to cover all
  - There are **many types** and even ***many more examples*** of particle detectors
- Therefore limited
  - Just a few types and examples ***should be enough***, given the limited **time**

- "Seeing" the photons → ***photodetector != photon counter***
  - ***Photo-detectors***: generate an ***analog level*** (i.e. ***I*** or ***V***) as a ***function*** of "light" ***intensity*** (e.g. ***PN*** and ***PIN*** structures)
  - ***Photon counters***: **count** individual bursts of ***photon bundles*** or ***single photons*** (e.g. ***PMT***s and ***avalanche diodes***)





Crowd ~~vs Counted Individuals~~

First interaction with the photons (and/or particles)

- **Photo-detectors**: generate an **analog level** (i.e. **I** or **V**) as a **function** of "light" **intensity** (e.g. **PN** and **PIN** structures)

- **Two modes** of operation:
  - Photo-**voltaic** mode
    - Depleted region is **exposed to light** and **voltage** is measured, with **no bias**
  - Photo-**conductive** mode
    - **Exposed light** generates a **current** flow, under **reverse-bias**

- Some important features:
  - Responsivity (I/P_{optic})
  - Active **area**
  - Max **photo current** (limited by saturation)
  - **Dark current** (in photoconductive mode)
  - **Bandwidth** (rise, fall times)
  - …
  - …

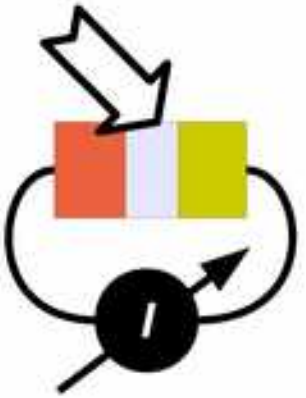


Photo-voltaic mode

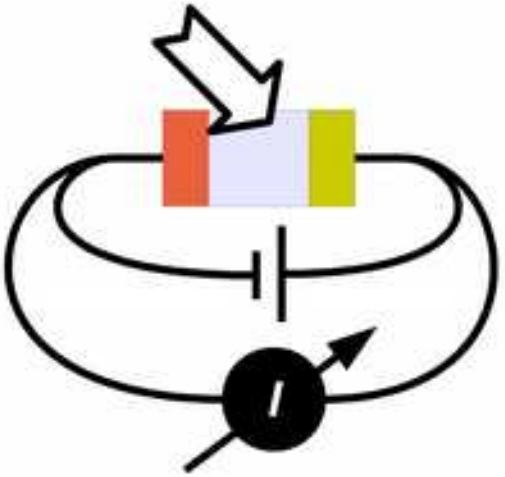
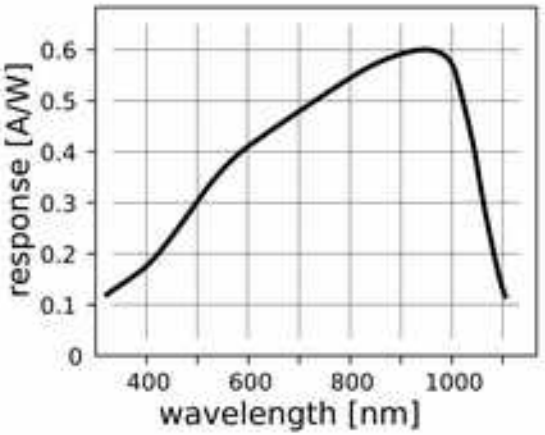


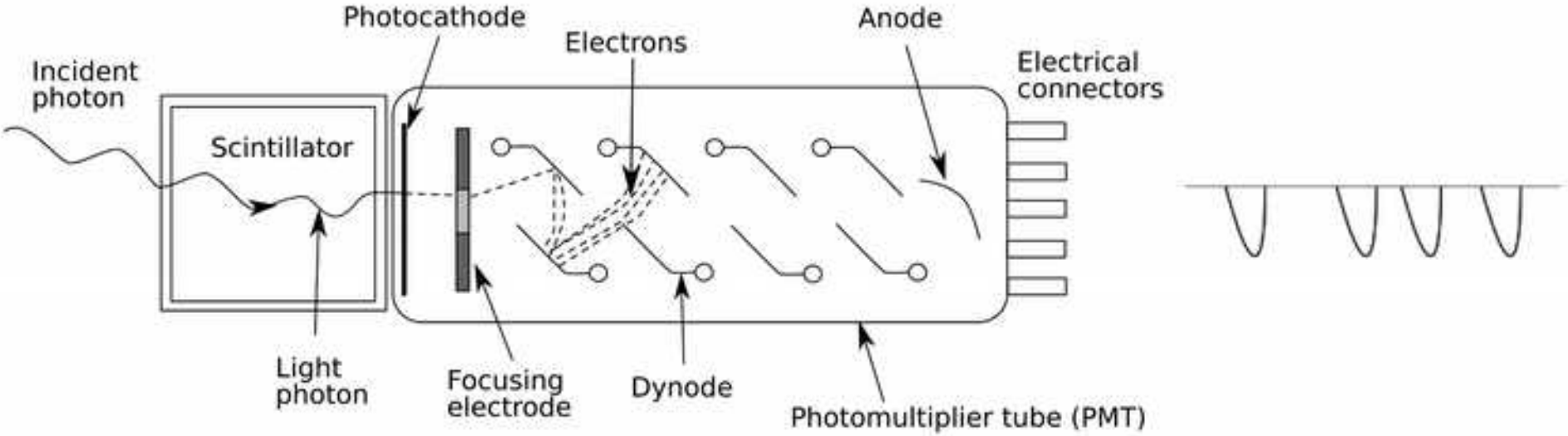
Photo-conductive mode



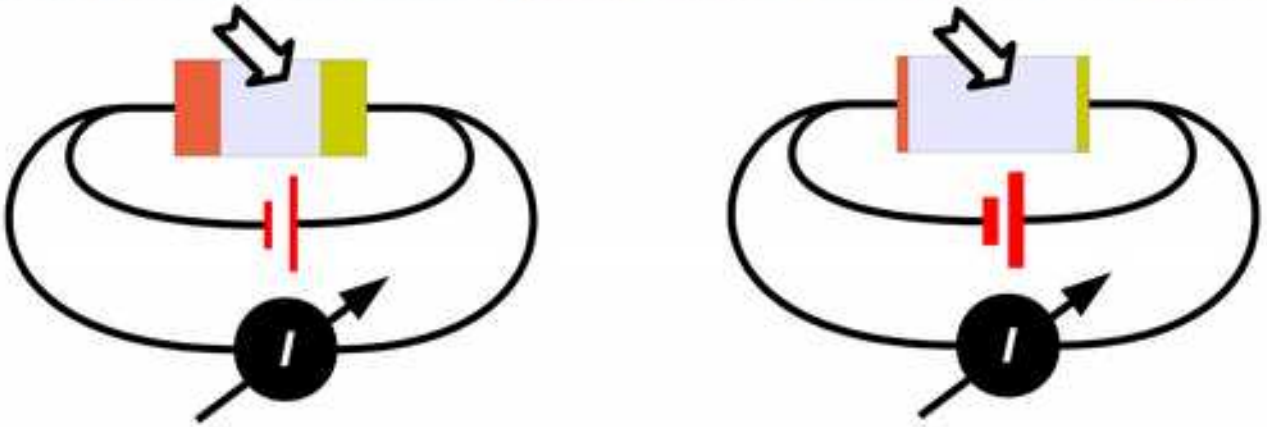
~~Crowd vs~~ Counted Individuals

First interaction with the photons (and/or particles)

- **Photon counters**: **count** individual bursts of ***photon bundles*** or ***single photons*** (e.g. ***PMTs*** and ***avalanche diodes or SPADs***)
  - ***Photomultipliers***: if photons arrive at the detector with ***low-enough frequency***



- ***Single Photon Avalanche Diodes (AD)***: PN junctions under strong reverse-bias



~~Crowd vs~~ Counted Individuals

First interaction with the photons (and/or particles)

- ***Photon counters***: **count** individual bursts of ***photon bundles*** or ***single photons*** (e.g. ***PMTs*** and ***avalanche diodes or SPADs***)
  - ***Avalanche Diodes (AD)*** are PN junctions ***reverse-biassed*** just ***below*** the break-down voltage such that single-photon induced electrons are accelerated within a few ***μm***s

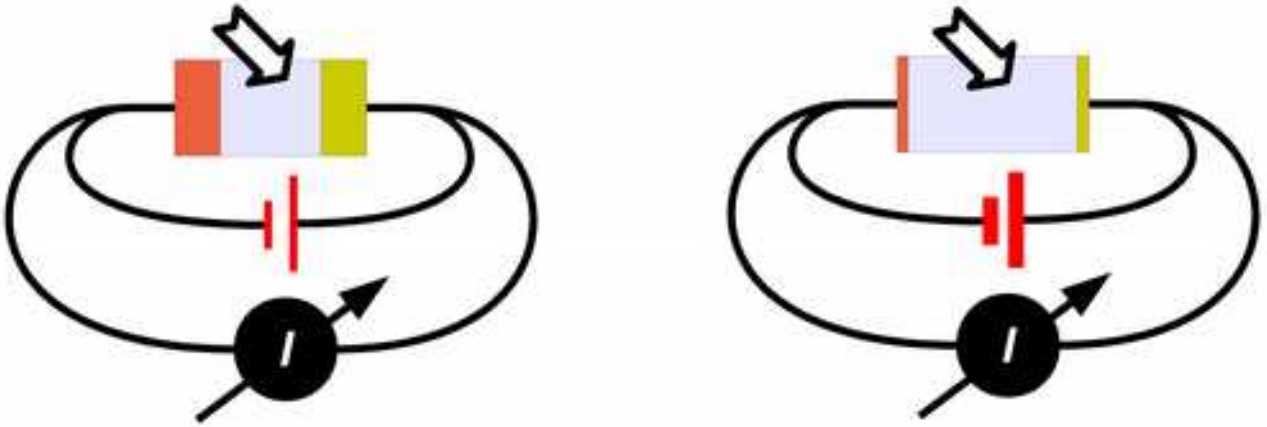


Photo-voltaic mode AD

  - ***Single-Photon Avalanche Diodes (SPAD)*** are PN junctions ***reverse-biassed*** just ***above*** the break-down voltage. When a photon strikes, bias voltage is droped down ***below the threshold*** (but not to break-down) for a short time (e.g. 100 ns) by carefully designed electronics to recover, such that the detector is ready for the next detection
  - ***SPADs*** can also be used for ***time-resolved*** techniques as they can provide information on photons ***time of arrival*** in addition

Position Sensitive Architecture

First interaction with the photons (and/or particles)

- Detect particles with the sensitivity of **where** they land; two main **paradigms**:
  - **Resistive charge division** on a single detection element:

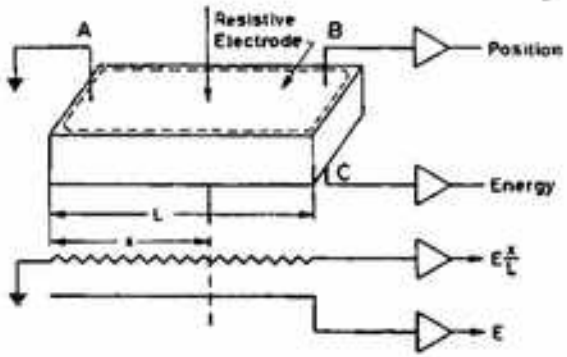


Fig. 10.14. Layout of a one-dimensional continuous position-sensitive detector using resistive charge division. A simplified equivalent circuit is shown below

* From Leo, p. 227

$$Position = \frac{B}{C}$$

A hybrid: Discrete array of resistive charge division

  - **Discrete array** of individual detection elements:

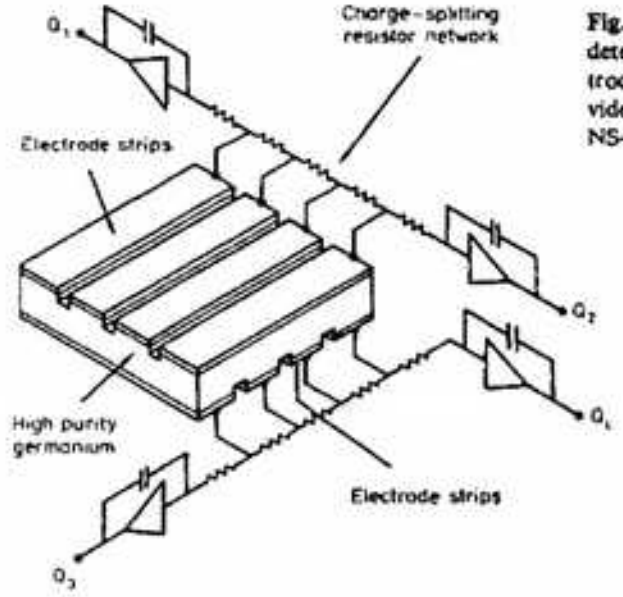
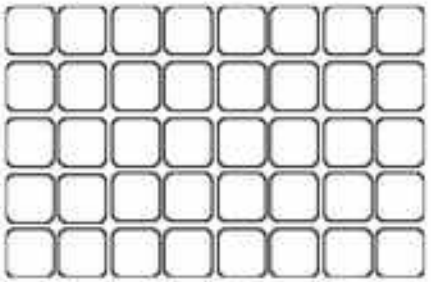


Fig. 10.15. Layout of a two-dimensional *matrix* detector. To reduce the readout electronics, the electrodes may be connected to an external resistive divider [from *Gerber* et al.: IEEE Trans. Nucl. Sci. NS-24, No. 1, 182 (1977)]

* From Leo, p. 229



Pixel detector

MEDIPIX

Position Sensitive Architecture

First interaction with the photons (and/or particles)

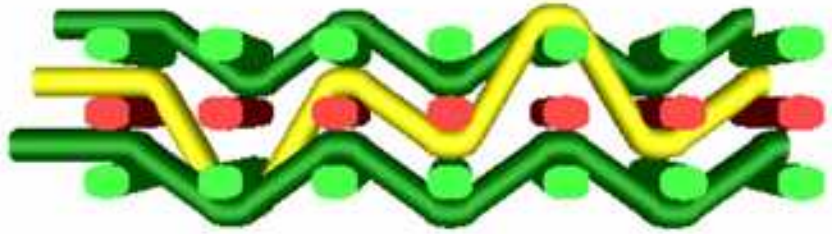


Fig. 1: Ideal repeating cell of general purpose two-electrode fabric construction: green yarns are conductive, yellow yarn is isolating binder, red yarns are isolators

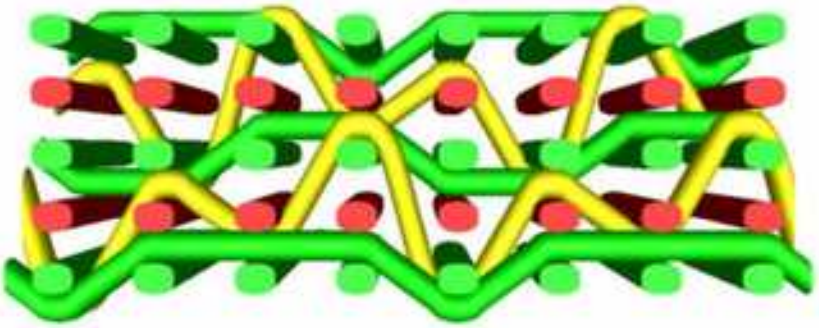
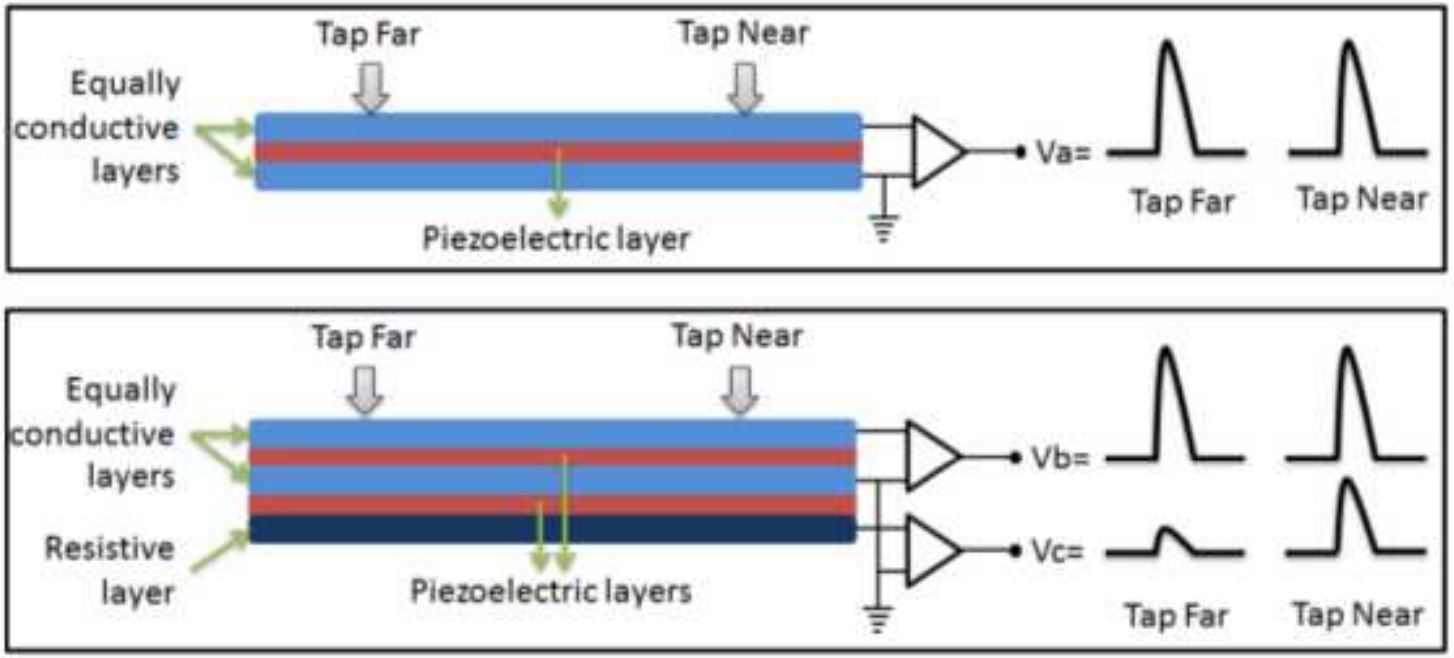
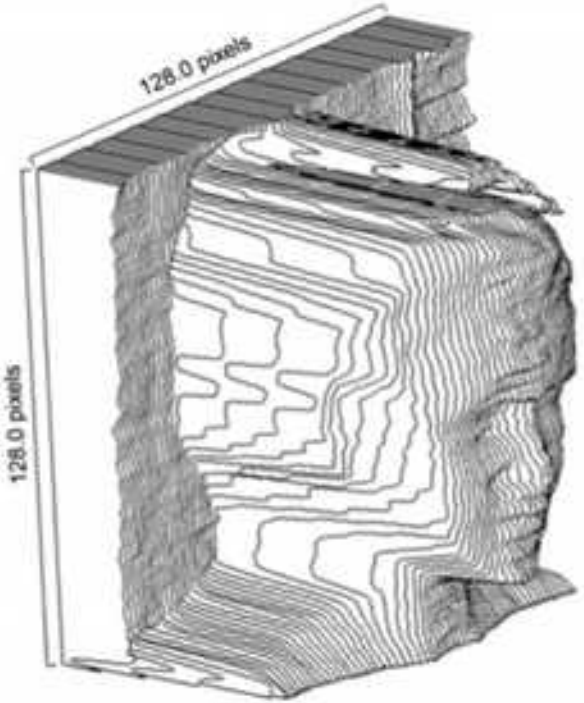


Fig. 2: Ideal repeating cell of general purpose three-electrode fabric construction: green yarns are conductive, yellow yarns are isolating binders, red yarns are isolators

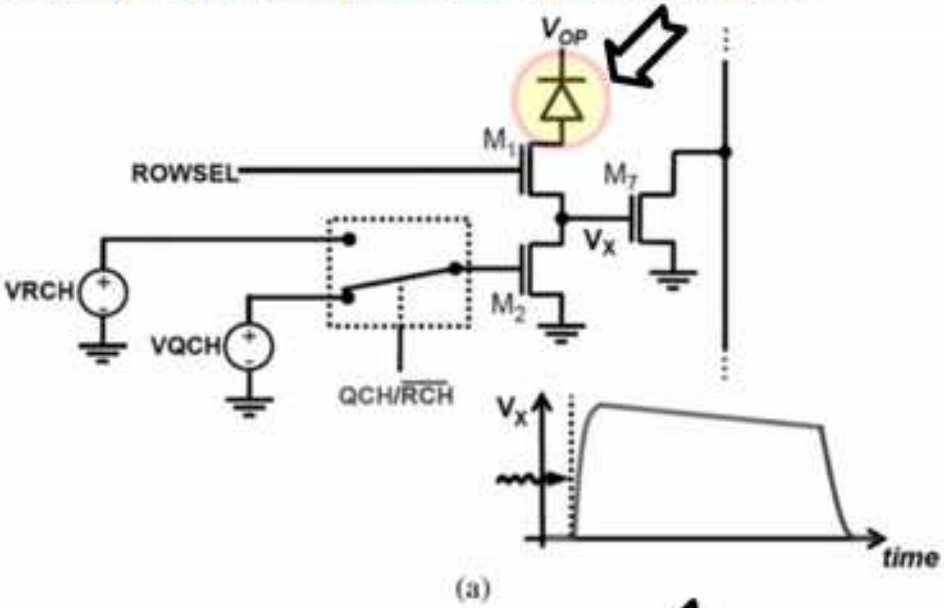


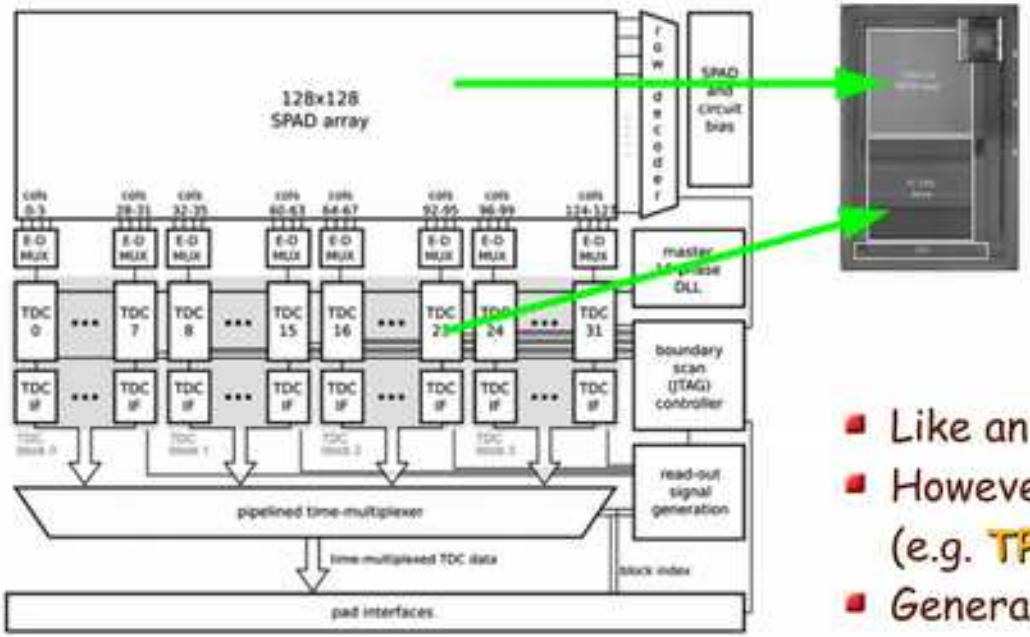
Time Resolved Architecture

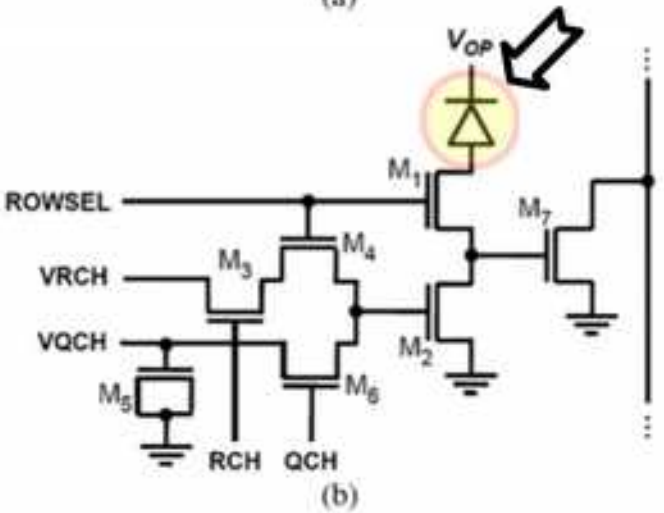
Flash the sample, start a timer, acquire single photons and their arrival times



A 128 128 Single-Photon Image Sensor, With Column-Level 10-Bit Time-to-Digital Converter Array, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 12, DECEMBER 2008





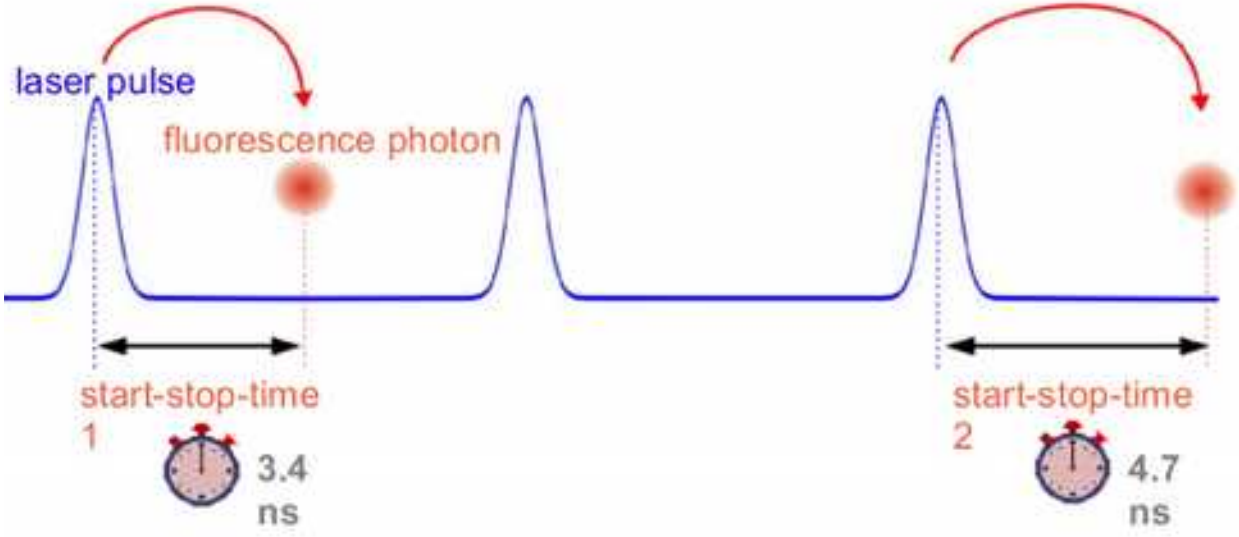


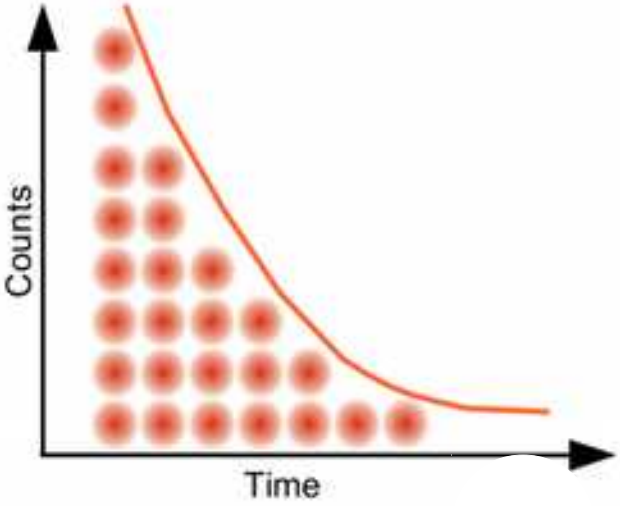
- Like an ordinary pixel detector (e.g. CCD)
- However measures "time" instead of "color" (e.g. TPC)
- Generates **3D** and **color-less** images

Time Correlated Architecture

First interaction with the photons (and/or particles)

- Measuring the profile of a **fast** (e.g. fluorescence, from ps to ns) and/or **weak** decay is tricky
- Recovering not only the **lifetimes** but also the **decay shape** requires the decay to be represented by at least 10s of samples
- The idea:
  - Meet the single photon counting **condition**(?)
    - Make your detector **fast**
    - Decrease the number of **photon creation** at the source
  - **Excite** the system to be probed (e.g. via a laser)
  - **Count** photons **per** reference excitation
  - Fill a **histogram** to visualize **decay profile**





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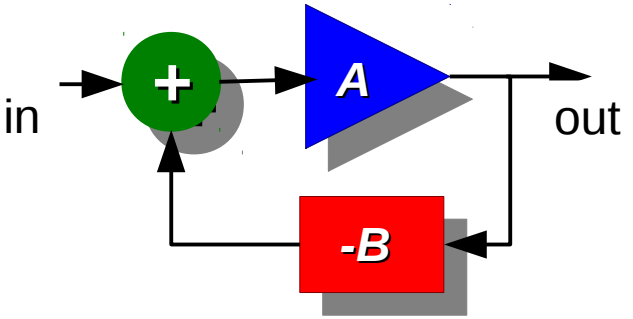
Pre-Amplifier

The first stage of the interpretation

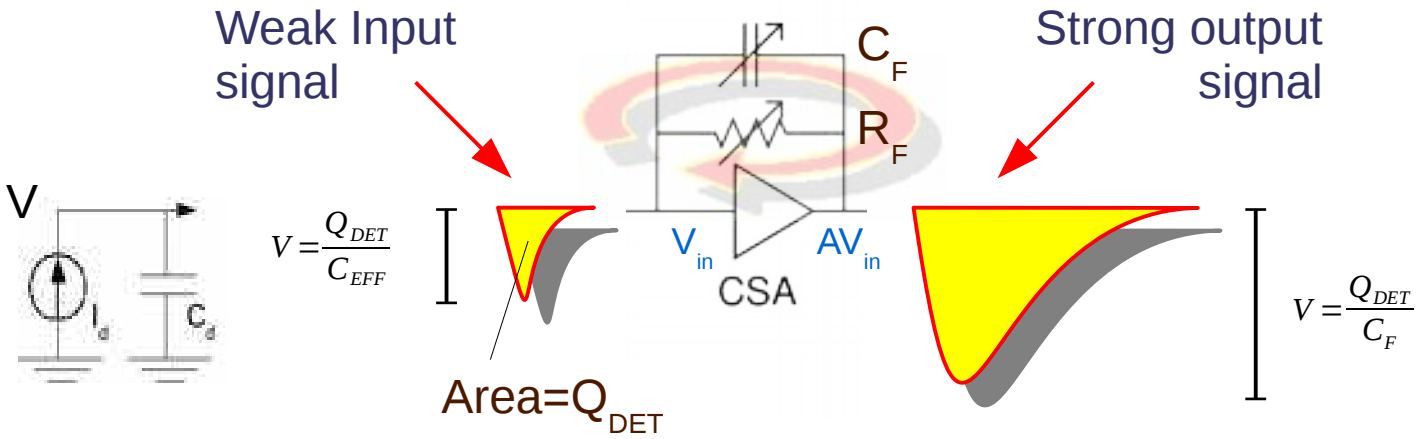


- ***Standardized*** experimental techniques ***over time***
- Our discussion on ***intuitive*** & ***descriptive*** level
- Three types of pre-amplifiers:

$$T = \frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + AB}$$

```
sage: T(A, B) = A/(1+A*B)
sage: T.limit(A=infinity)
(A, B) |--> 1/B
```

  - ***Voltage sensitive***: usually ***not preferred*** due to the fact that, for a given amount of charge generated by the detector (Q_{DET}), the ***output voltage*** of the detector (V) is a ***function*** of the ***effective capacitance*** (C_{EFF}) of the detector which is ***variable***
  - ***Current sensitive***: ***not preferred*** because they are ***suitable*** to be used with ***low impedance*** *devices,* ***however*** radiation ***detectors*** have usually ***high impedance***
  - ***Charge sensitive***: ***preferred*** type because its output is ***only*** a function of the charge (Q_{DET}) and a fixed C_F, provided that amplifier ***gain*** is sufficiently ***high***

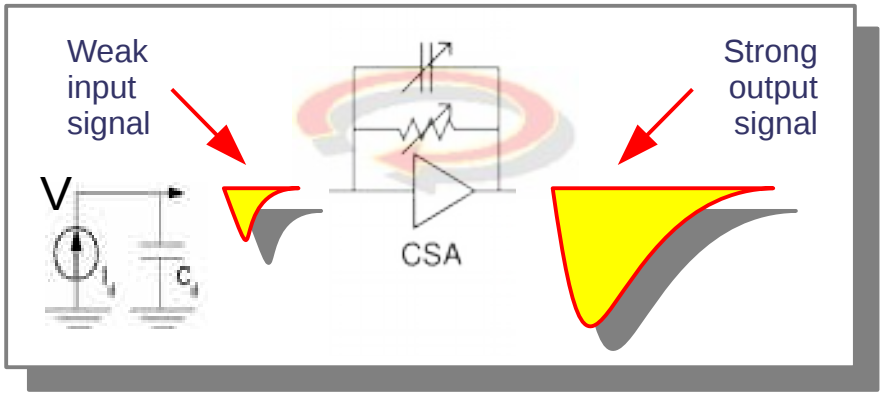


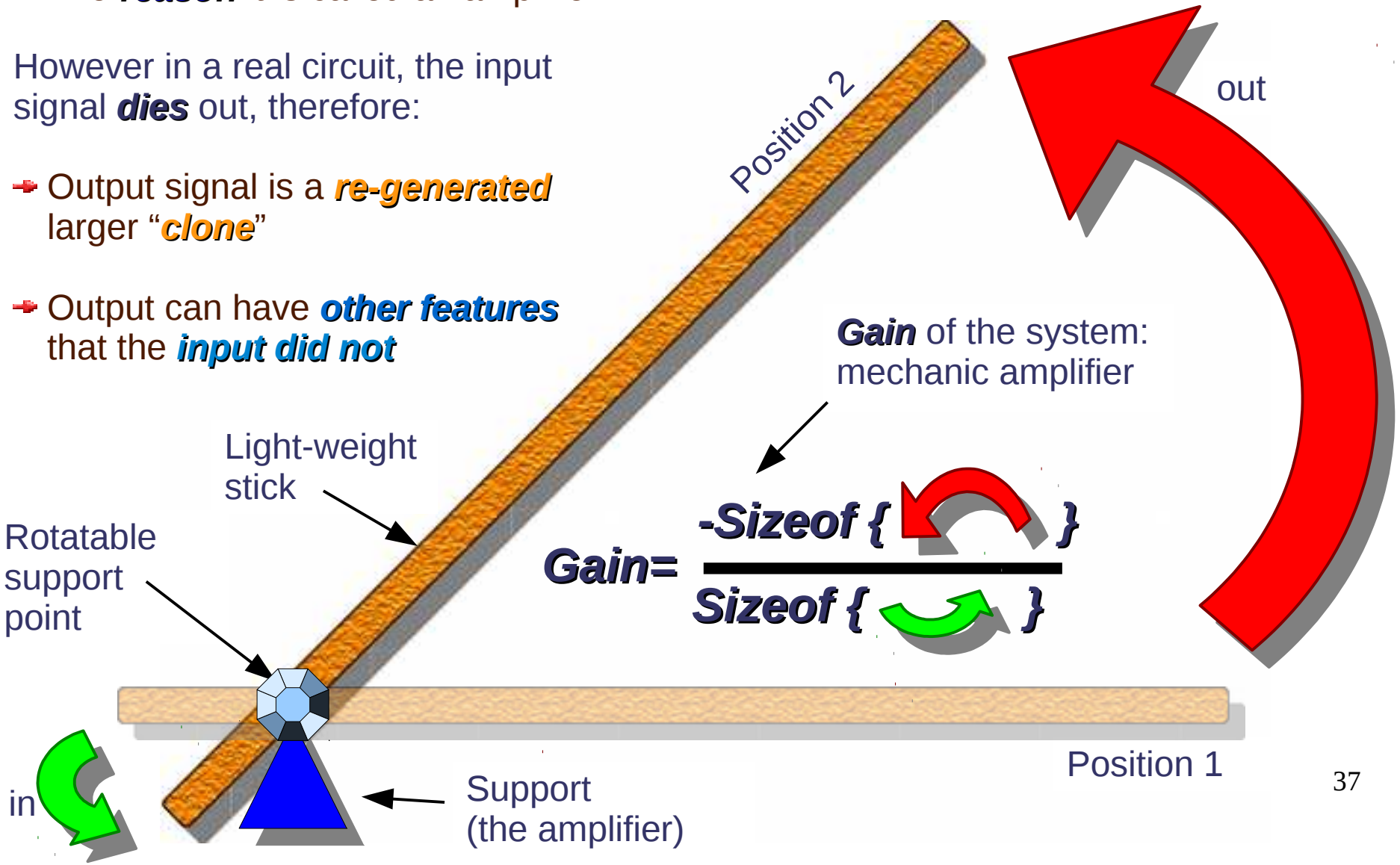
* Please refer to Techniques for Nuclear and Particle Physics Experiments: A How-to Approach by W. R. Leo

Amplifier Basic

How to amplify something

- We want a ***small change*** in the input to ***cause*** a ***big change*** at the output
  - The ***reason*** it is called an amplifier
- However in a real circuit, the input signal ***dies*** out, therefore:
  - Output signal is a ***re-generated*** larger "***clone***"
  - Output can have ***other features*** that the ***input did not***

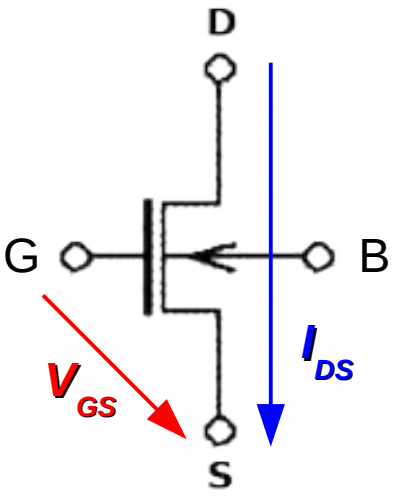




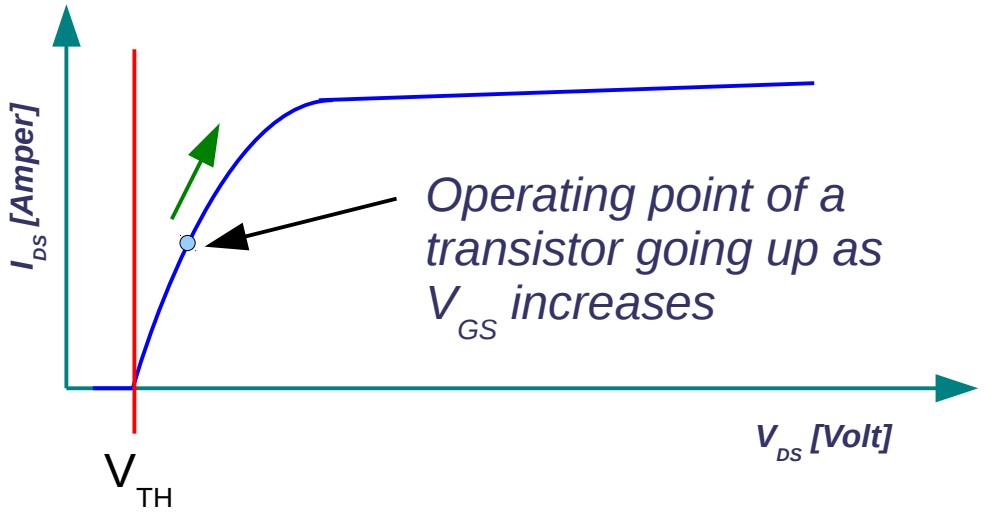
Transconductance - g_m

Figure-or-merit for a transistor

- Define a figure-of-merit (***FOM***) for a single nMOS
  - ***How well*** a transistor ***converts*** voltage into current
  - From input V_{GS} to output I_{DS}



$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{2I_D}{V_{GS} - V_{TH}}$$

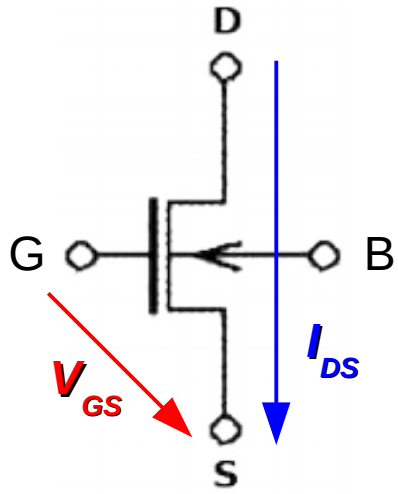


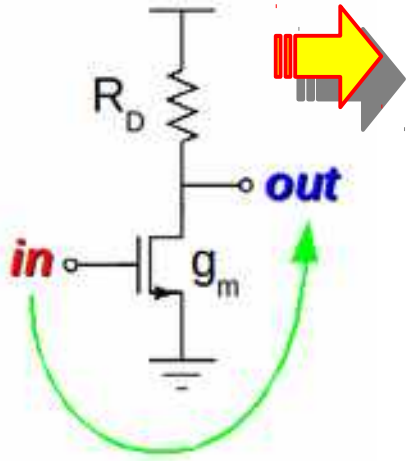
* Please refer to Design of Analog CMOS Integrated Circuits by B. Razavi

Basic CMOS Amplifier

Single-stage common-source amplifier and its evolution into a complete circuit

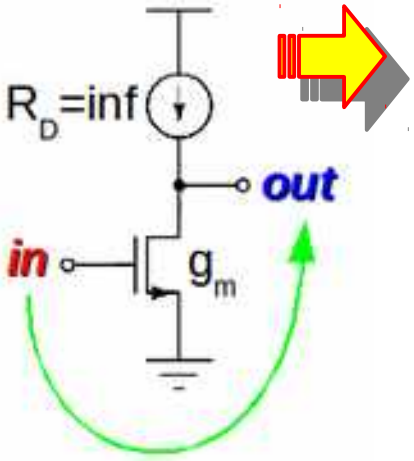
- Sink current through R_D
  - *As **in** increases, **out** decreases (faster)*
- $-g_m R_D$ suggests that we should increase the ***load impedance*** to have ***higher voltage gain***
  - An ***ideal*** current source has ***infinite impedance***
- A ***current mirror*** is a practical ***current source***
  - Simply a transistor biased as a current source
- Transconductance ***(g_m) increases*** with current
  - Supply ***additional current*** to the gain device to have higher gain





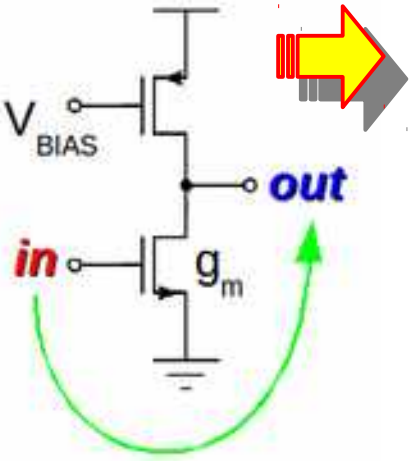
$A_V = -g_m R_D$

Common-source amplifier



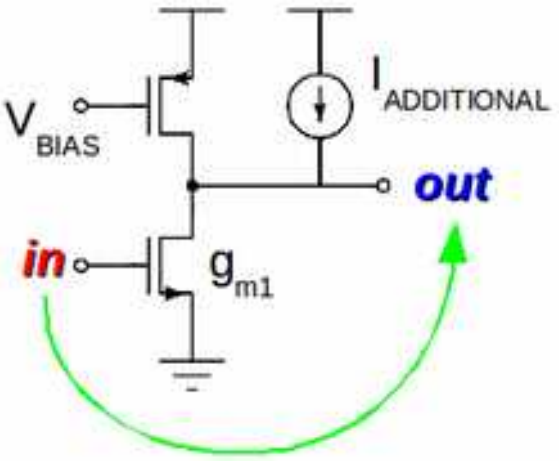
$A_V = -g_m r_o$

Common-source amplifier



$A_V = -g_m(r_{o1} \| r_{o2})$

Common-source amplifier



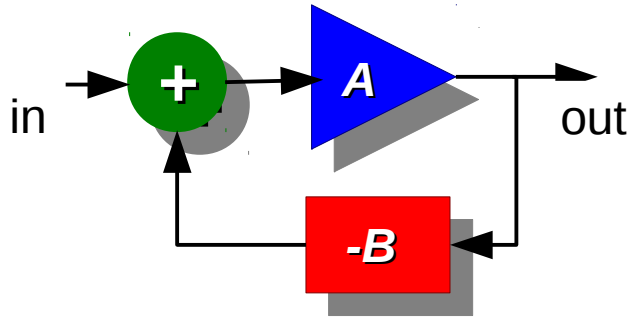
$A_V > -g_m(r_{o1} \| r_{o2})$

Common-source amplifier with current source load featuring higher gain due to increased current

Basic CMOS Amplifier

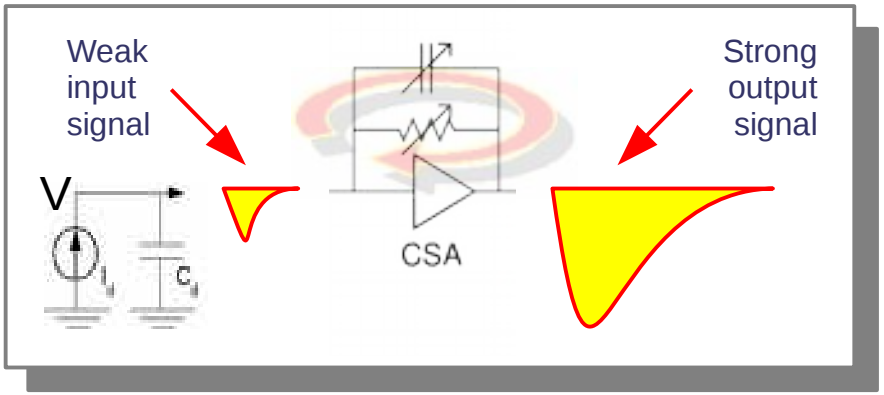
Single-stage common-source amplifier and its evolution into a complete circuit

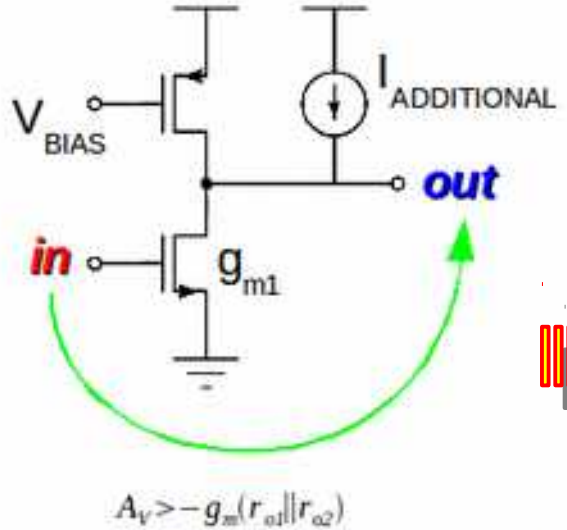
- Add the feedback network C_F & R_F forming the B such that
  - For high enough A_V, closed loop gain is $1/B$



$$T = \frac{V_{OUT}}{V_{IN}} = \frac{A}{1+AB}$$

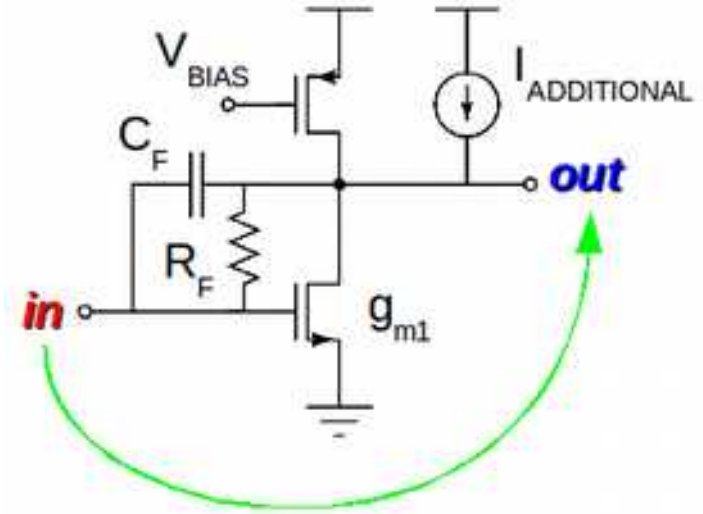
```
sage: T(A, B) = A/(1+A*B)
sage: T.limit(A=infinity)
(A, B) |--> 1/B
```





$$A_V > -g_m(r_{o1} \| r_{o2})$$

Common-source amplifier with current source load featuring higher gain due to increased current

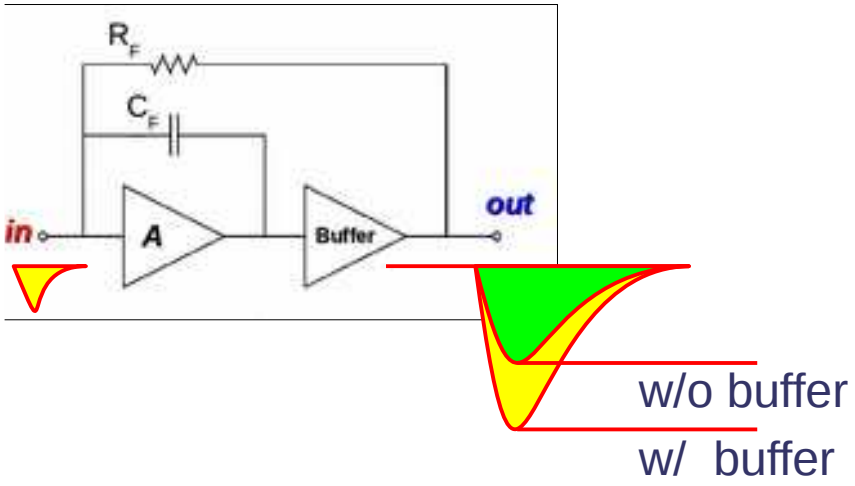


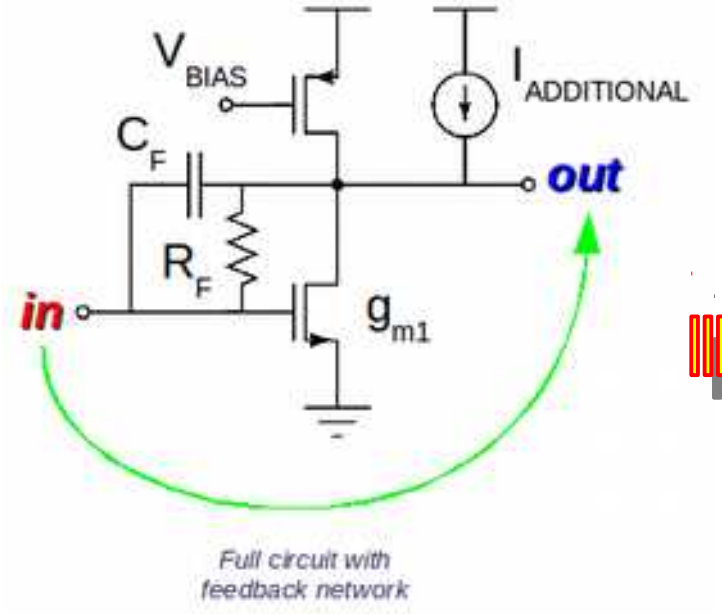
Full circuit with feedback network

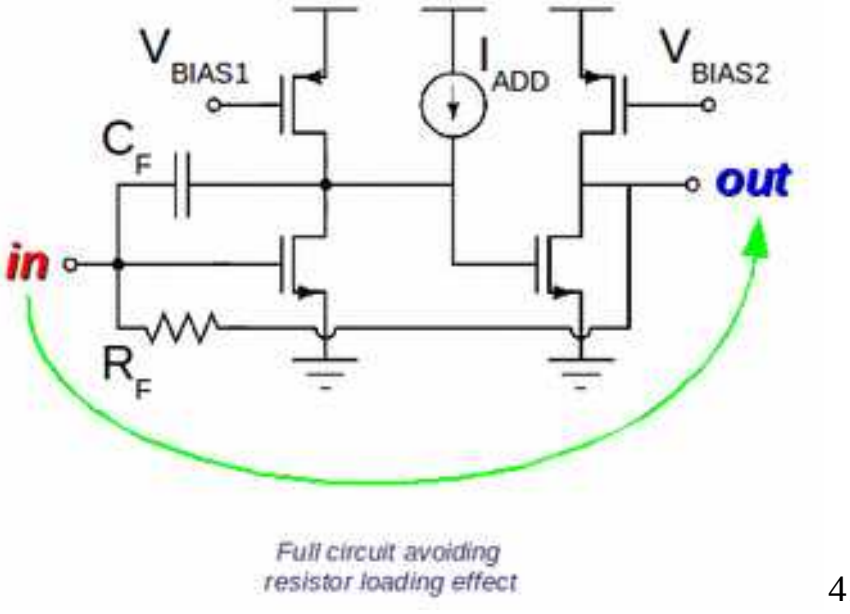
Basic CMOS Amplifier

Avoid loading effect of the resetting resistor

- Problem: while C_F is charged, R_F resets ***at the same time***
  - ***Lowering*** the voltage gain, therefore:
  - ***Loading effect*** of the feedback ***resistor*** should be ***avoided***
  - ***Integration*** and ***resetting*** should be ***de-coupled***
  - Employing a ***buffer*** is one of the possible solutions



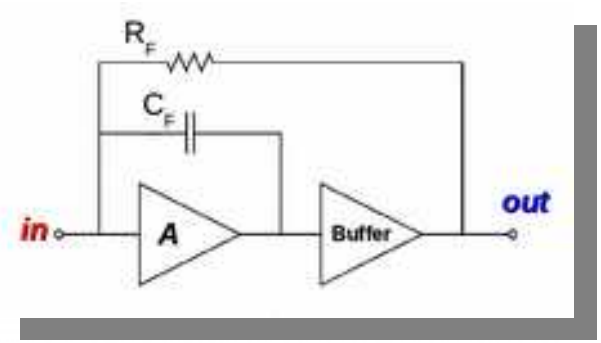


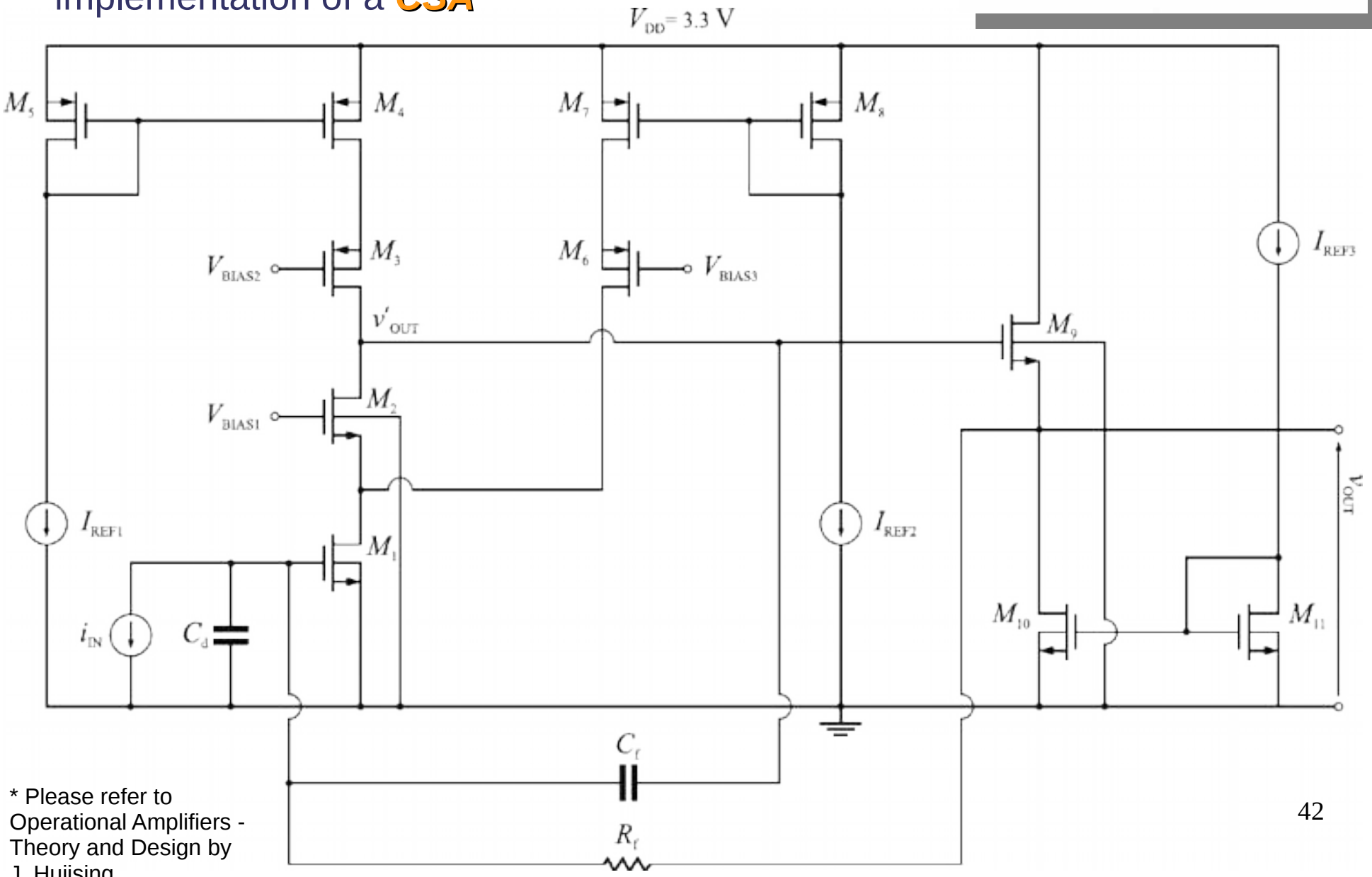


Pre-Amplifier

Full circuit (currently in use at a RICH detector)

- **Actual** CMOS device-level implementation of a **CSA**

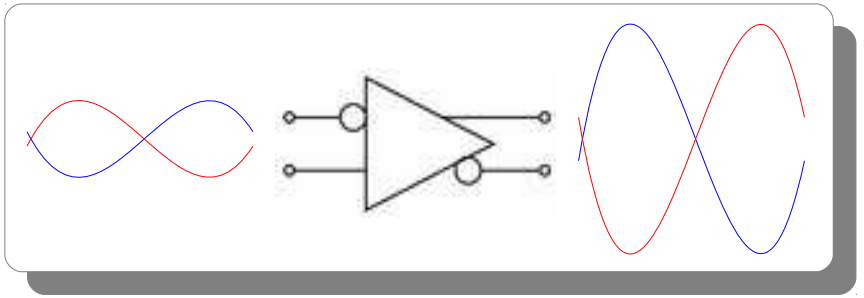


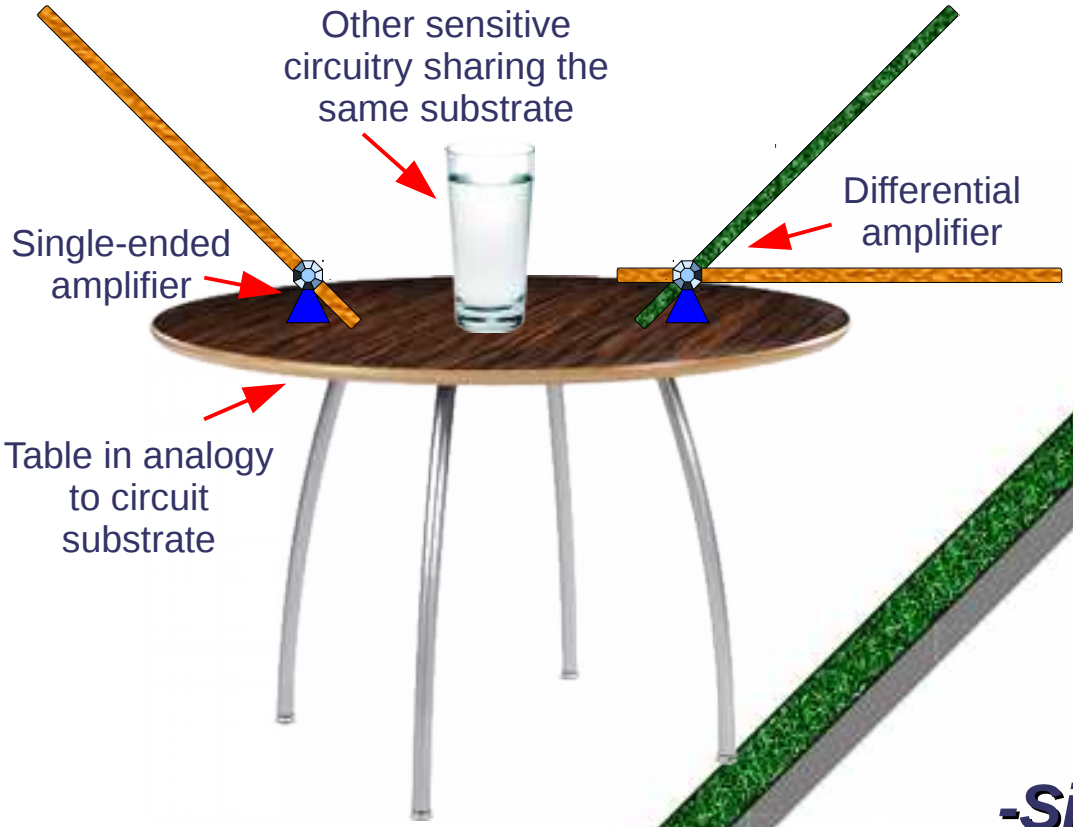


* Please refer to Operational Amplifiers - Theory and Design by J. Huijsing

Differential Amplifier

Generating less noise (also for others)
in the cost of more complex design





Stick 2

out

Gain of the system:
mechanic amplifier

$$Gain = \frac{-Sizeof\{\ \}}{Sizeof\{\ \}}$$

Rotational support
axis holding both
the sticks

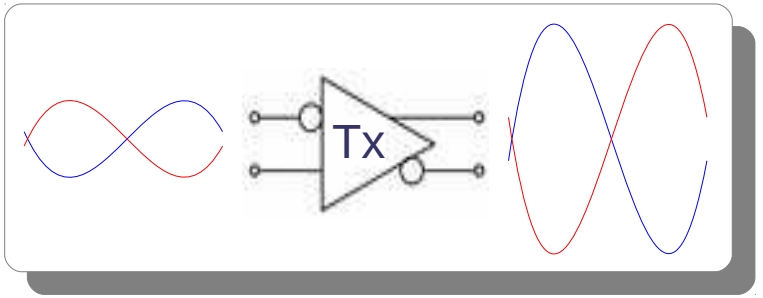
Stick 1

in

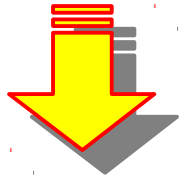
Support
(the amplifier)

Differential Signaling

Rejecting noise

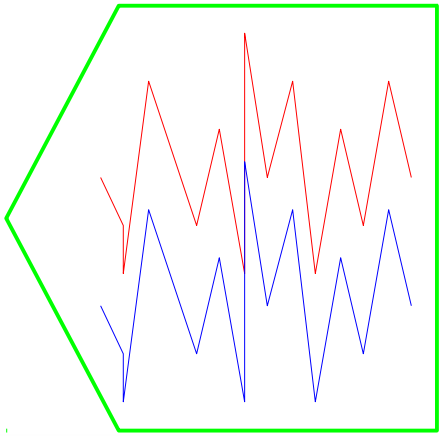


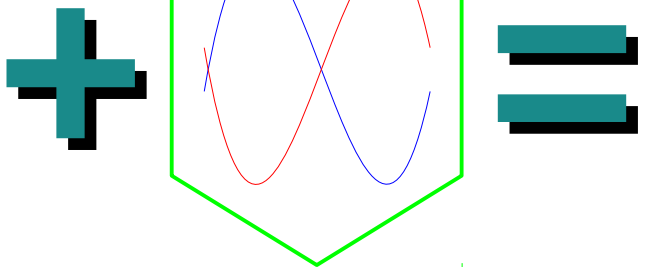
- The ***information*** Tx generates is in the ***difference***
  - Signal creates ***complementary current images*** on the substrate
  - Generating ***less noise*** for neighboring circuitry
- Rx ***compares*** the voltage levels of the pair
- Any noise source should affect both of the lines similarly
  - Generating almost ***identical transients*** on both of the wires
  - Pair wires are ***close*** to each other
- Practically high ***noise rejection*** is feasible



Metal wires

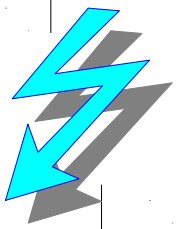
Injected noise
ΔV ~ 0

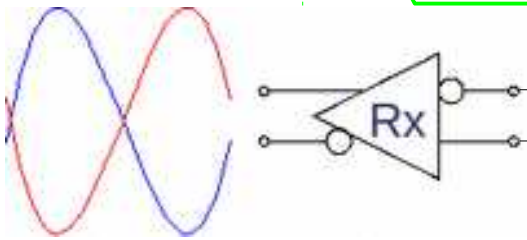




Differential signal

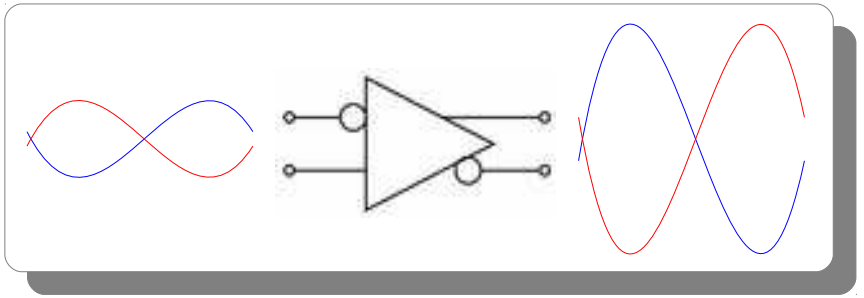
Noise source
(Ionizing particle passage, electronic noise injected by neighboring circuitry, etc.)



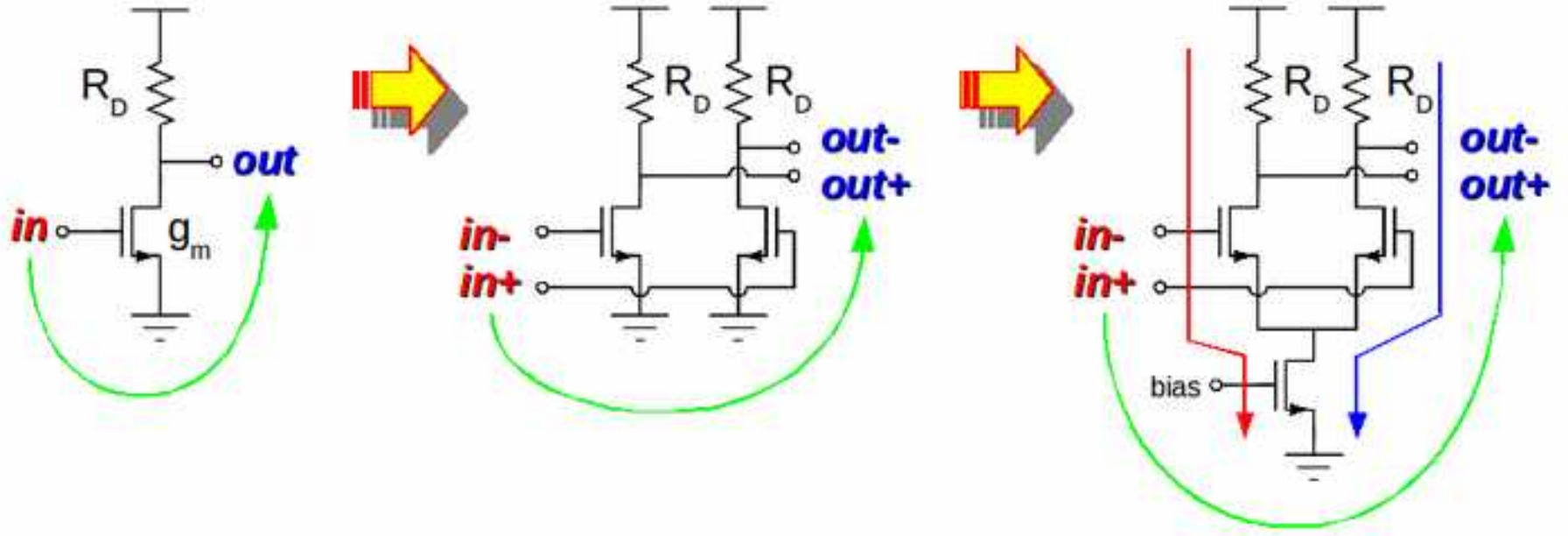


Differential Signaling

Differential gain stage



- Sink current through R_D
  - *As **in** increases, **out** decreases (faster)*
- Double the structure to act on both the signals
  - Drawback: signals can be identical (no differential information)
- Steer the current either through one inverter or the other
  - Transition at the input changes the path through which the current is steered
  - Unless metastable, the amplifier has always differential information at he output



* Please refer to Design of Analog CMOS Integrated Circuits by B. Razavi

Introduction to the Design of Full-Custom Front-End & Data Transmission ASICs*

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    - **Single event upset, analog single event transient, latch-up**
  - **Simulating** radiation effects on analog circuits

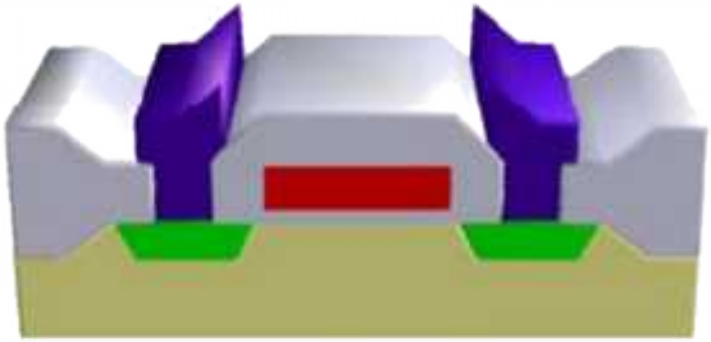
* *Application Specific Integrated Circuit*

Semiconductor Switch - Transistor

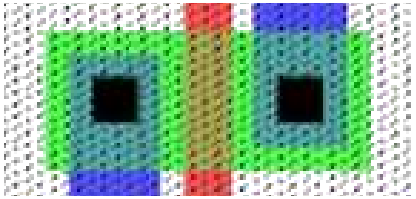
A masterpiece

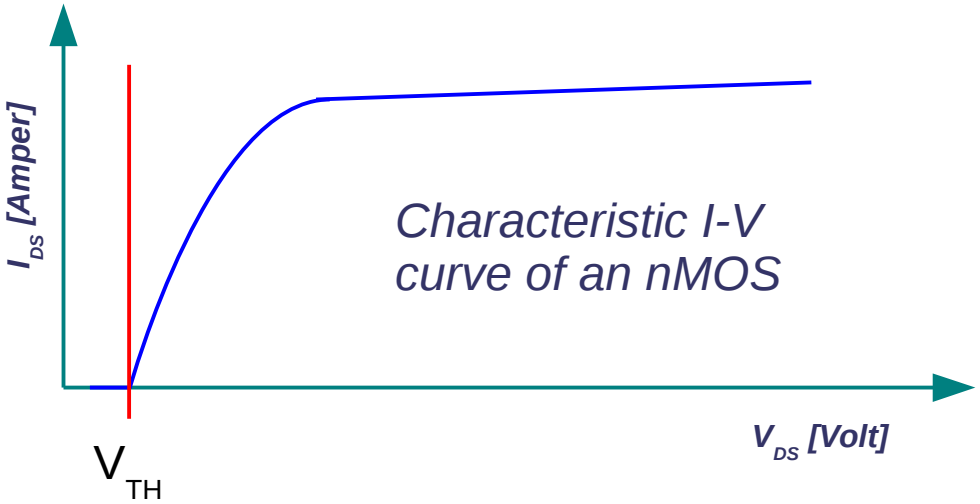
- Current conduction between **Drain-Source** as a function of **Gate-Source** voltage

3D view of a single MOS transistor

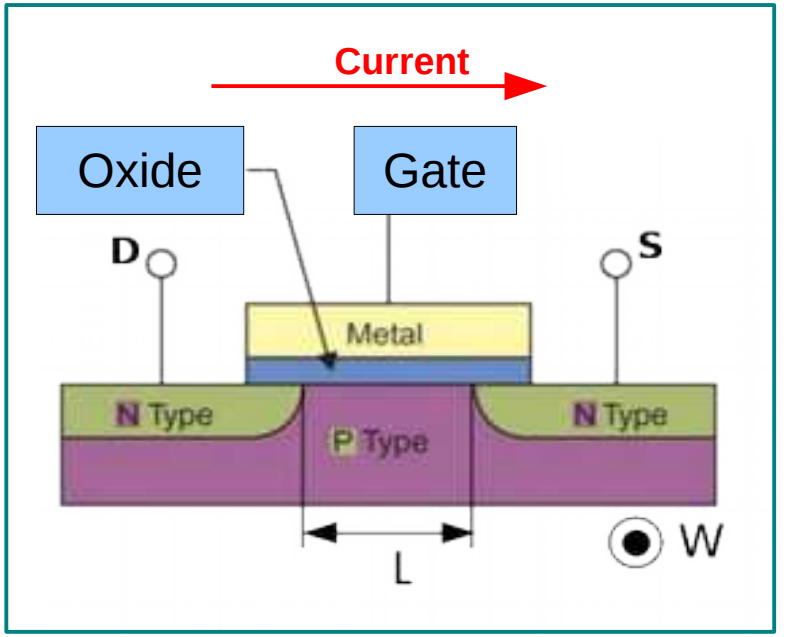


A single MOS transistor **as drawn by a designer**

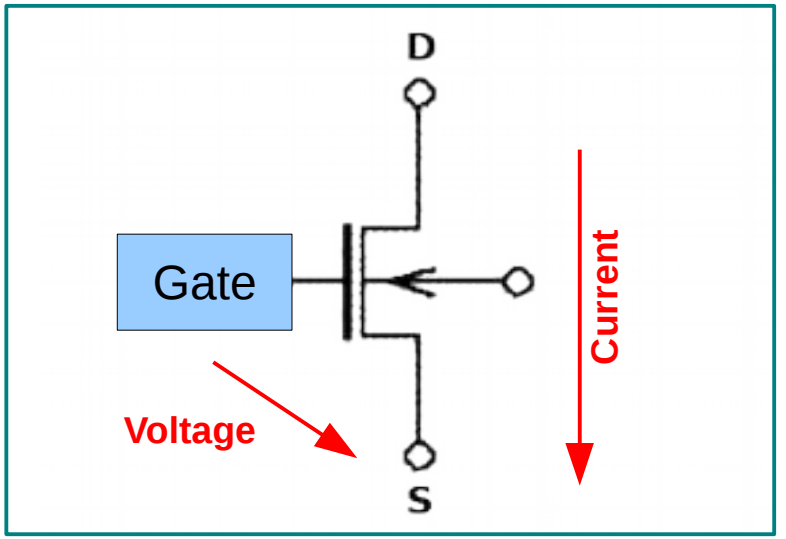




Layout



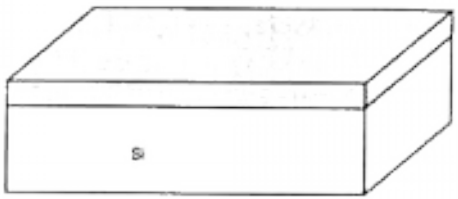
Symbol



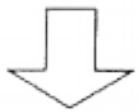
Lithography

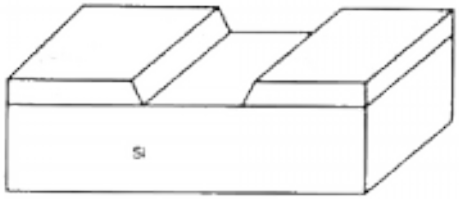
The art of light drawing

- A real microelectronic circuit is like a **city** composed of **many layers**
- A specific **lithographic mask** is needed **for each layer** to be created
- As an **example** we will create a "**line**" on an **oxide layer**



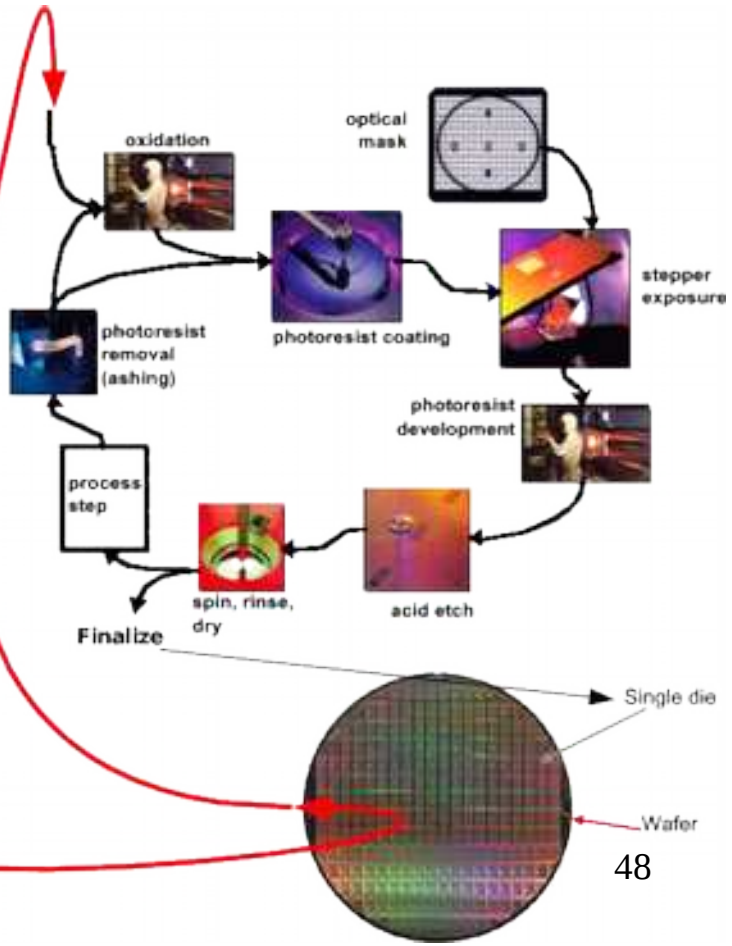
Initial state





Target

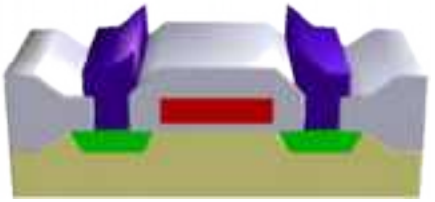
The ***ingot*** to be sliced into ***wafers***

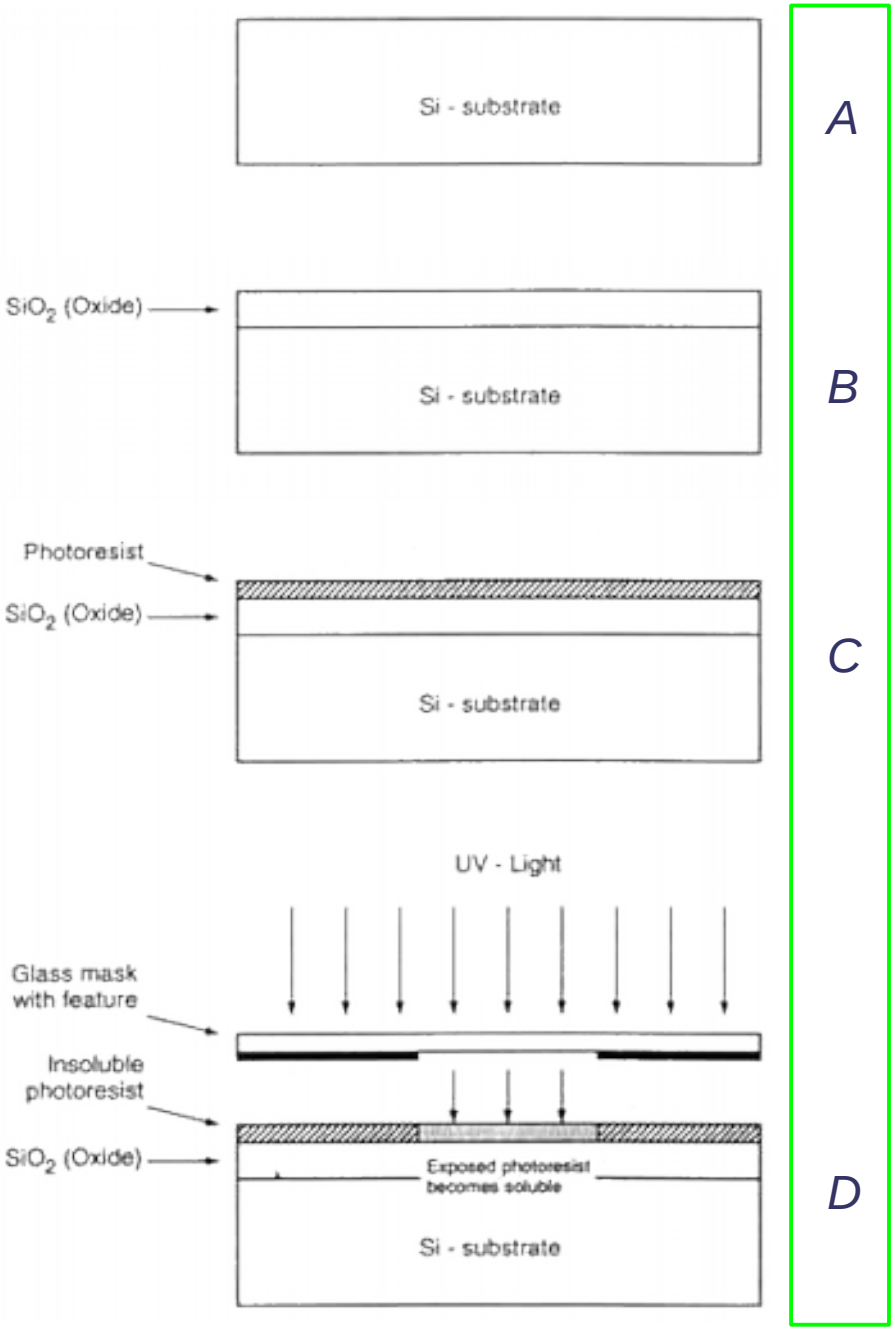


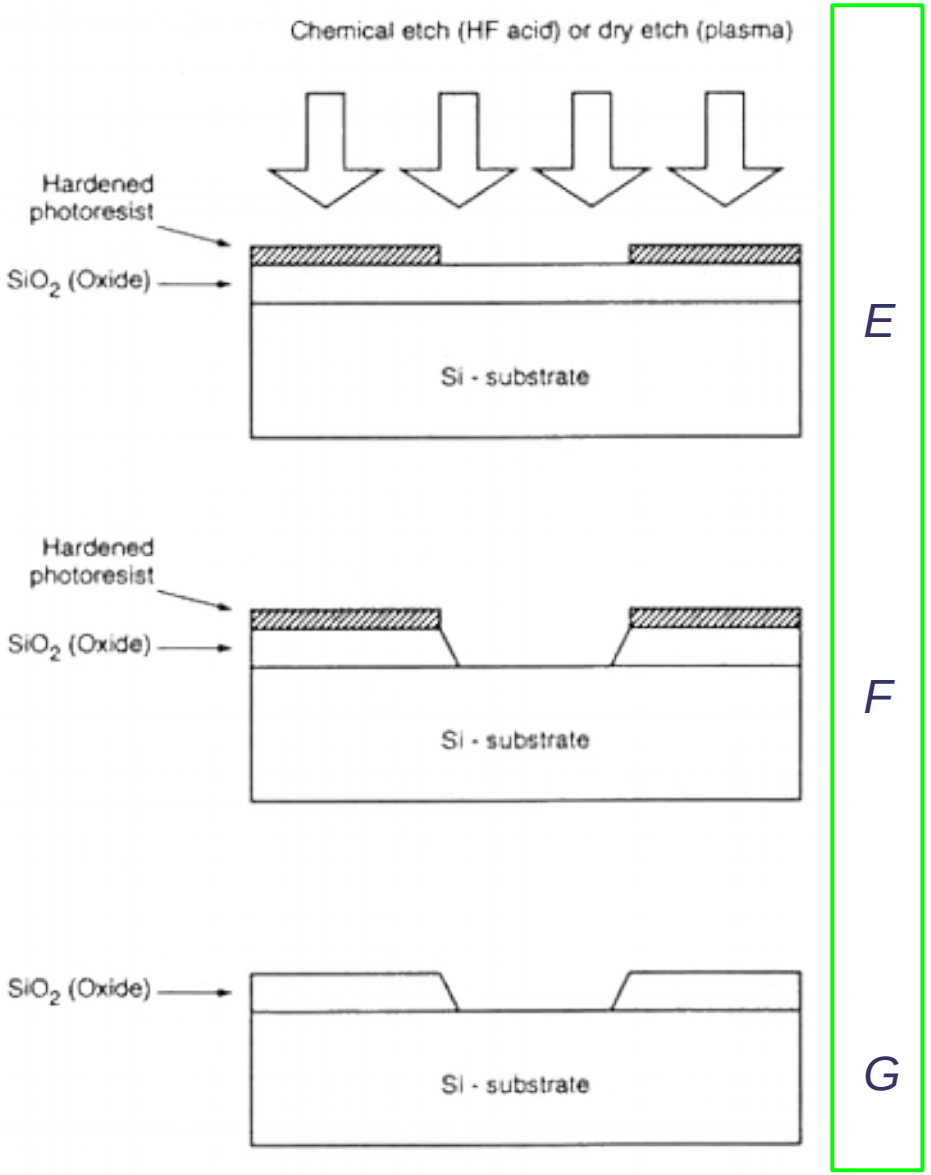
* Please refer to Semiconductor Devices: Physics and Technology by S. M. Sze

Just to draw a single line

Seven simplified steps

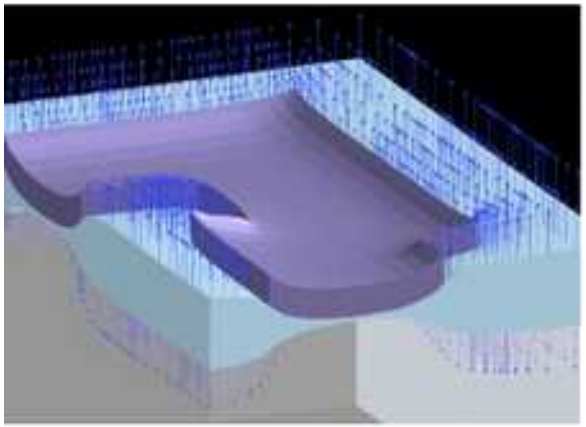






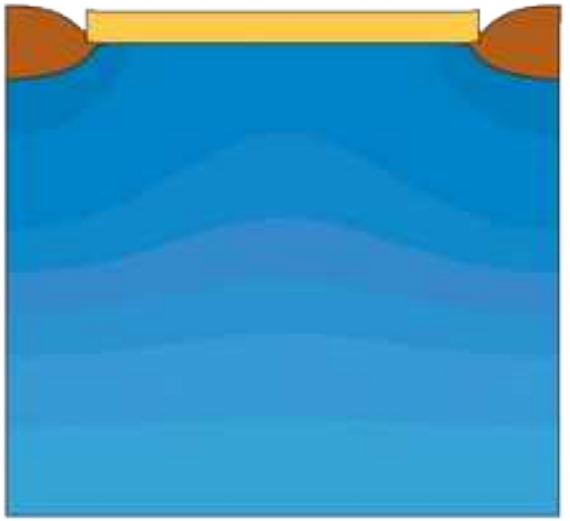
Fabrication of an nMOS

Simplified steps – Part I



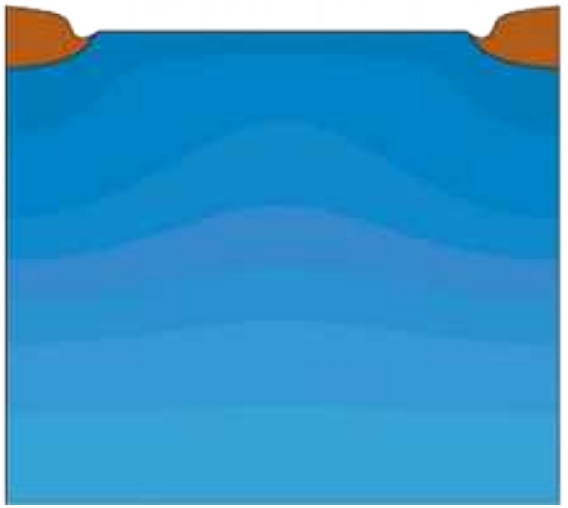
A. Definition of active area

B. Anneal and field oxide growth

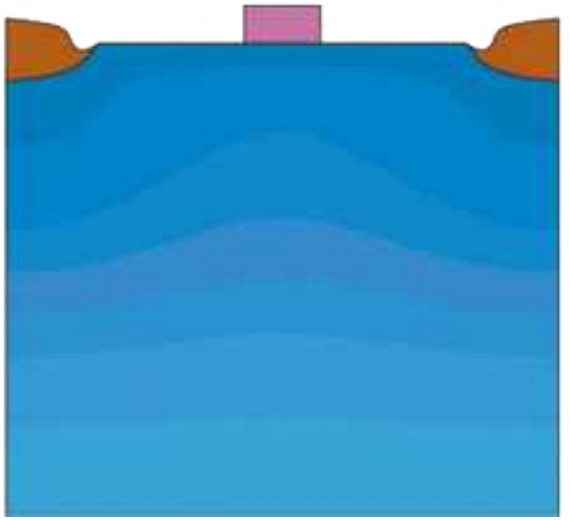


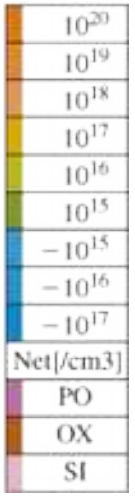
- ***Nitride*** *defines the active areas*
- ***FOX*** *is developed*
- *Nitride is removed by a solvent*
- *Polysilicon is deposited*

C. Channel implant



D. Gate formation (polysilicon deposition)





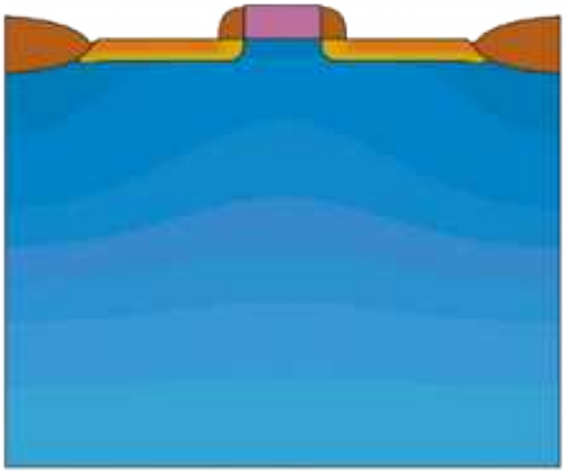
Images: CMOS Digital Integrated Circuits Analysis & Design by Sung-Mo (Steve) Kang and Yusuf Leblebici

Fabrication of an nMOS

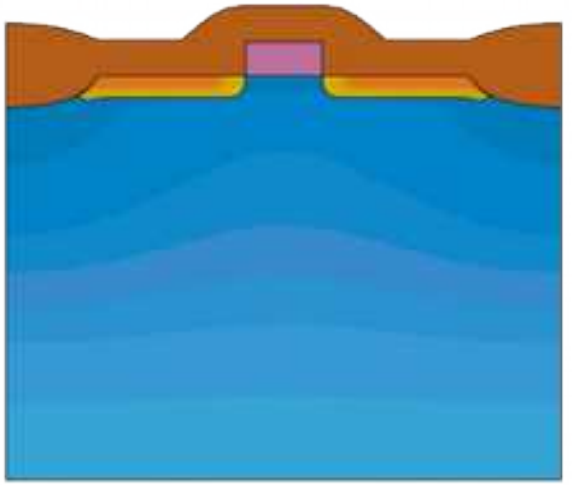
Simplified steps – Part II

- **Spacer & active** *field formation*
- *Dep. of* SiO_2
- ***Etch**ing contact holes*
- ***Metal** dep.*

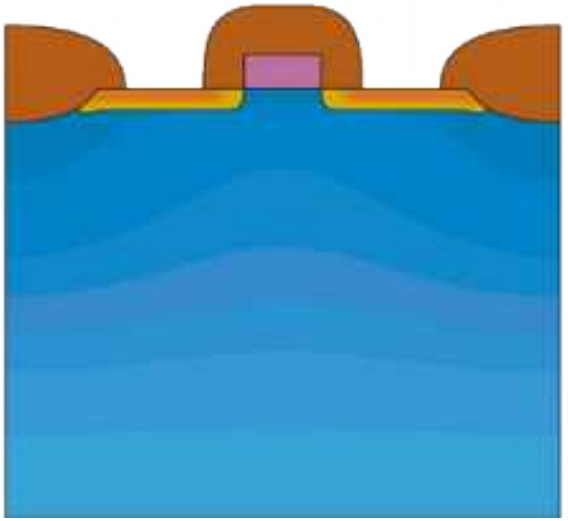
E. Spacer formation and S/D implant



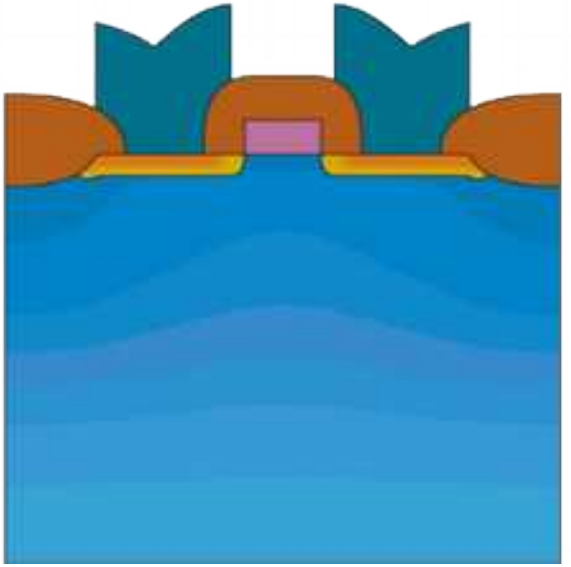
F. Oxide deposition



G. Contact hole etch

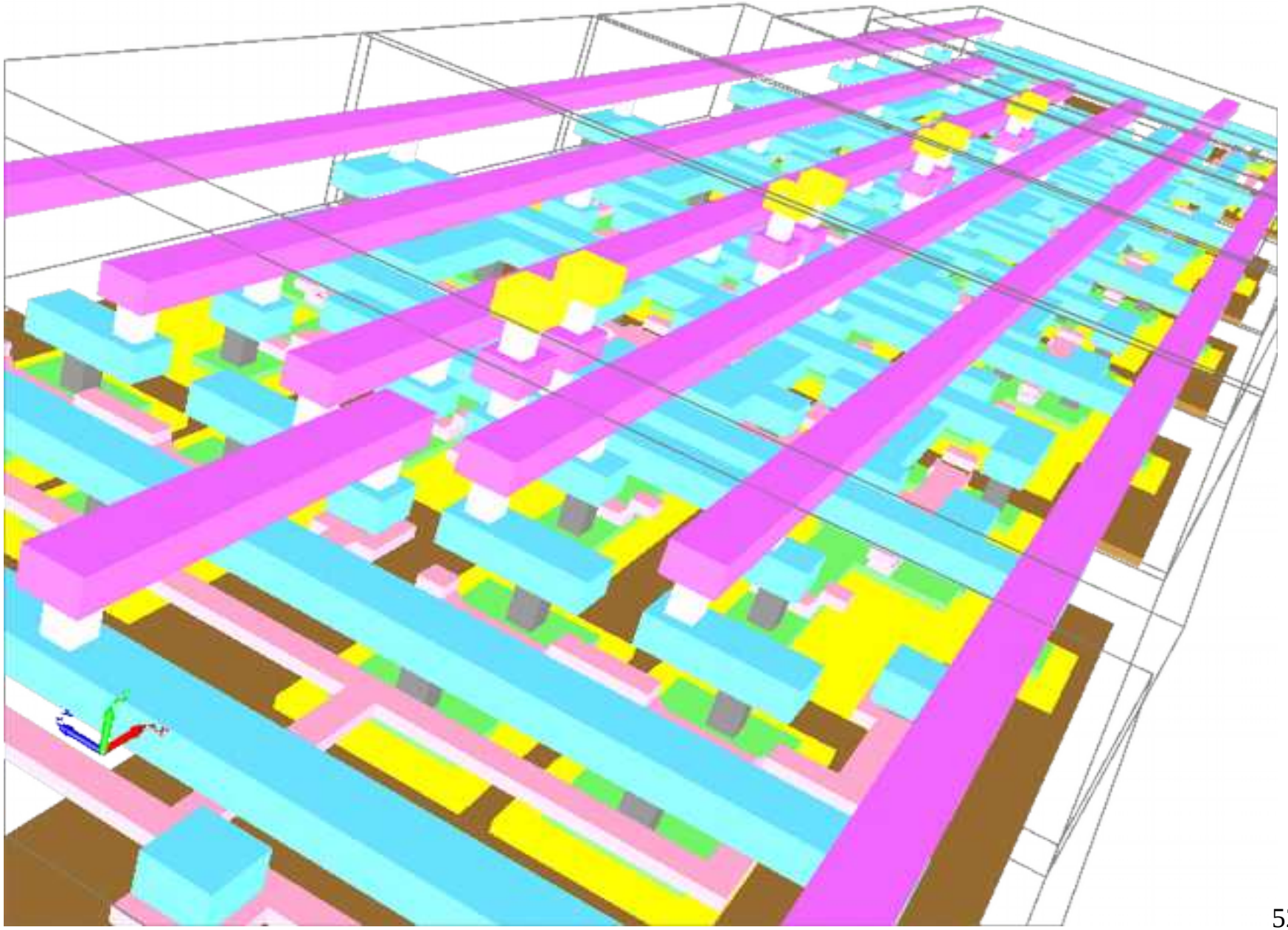


H. Metal deposition



How many layers do you see ?

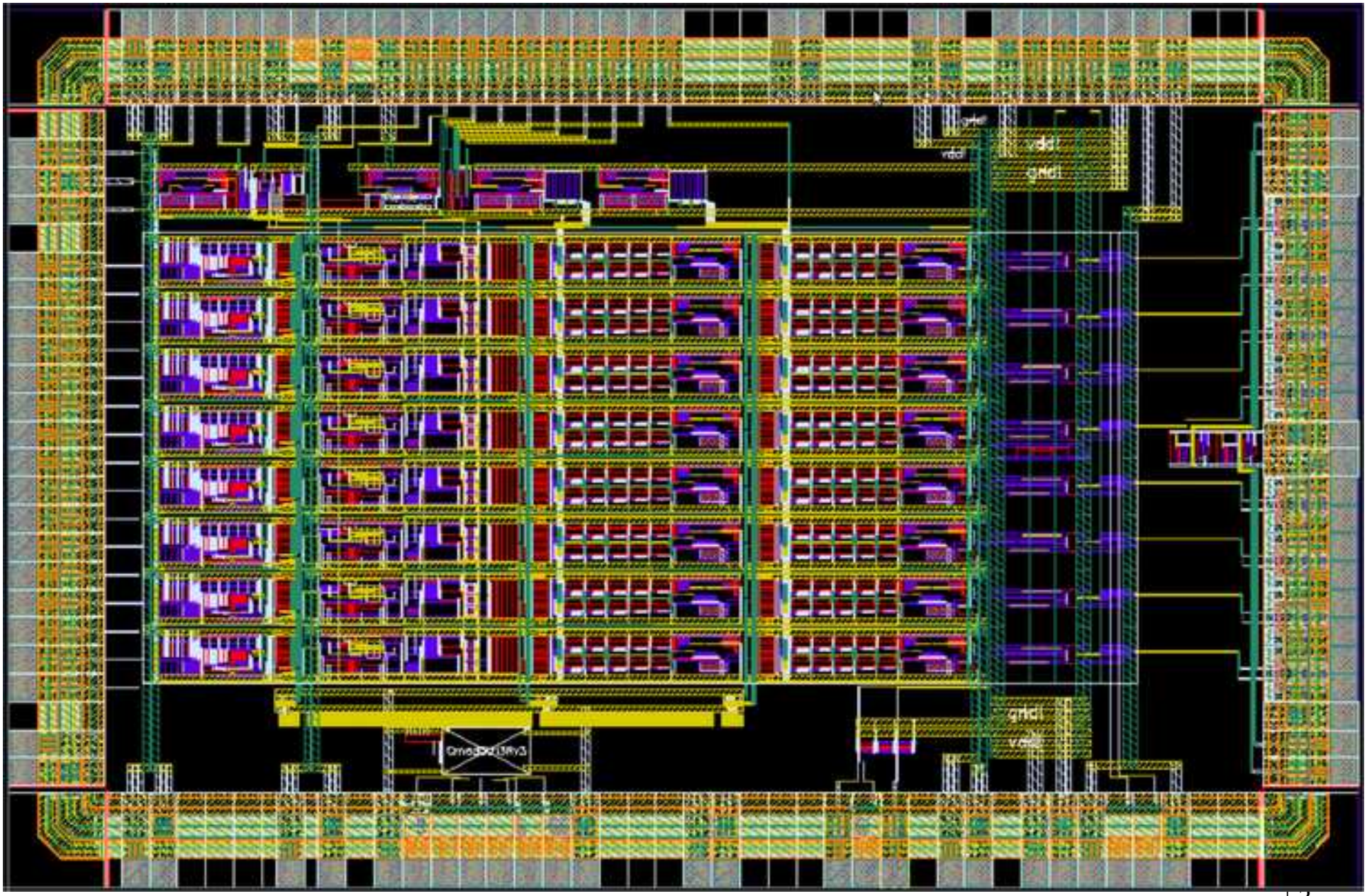
A process repeated a few hundred times



A ring-type oscillator

How many layers do you see ?

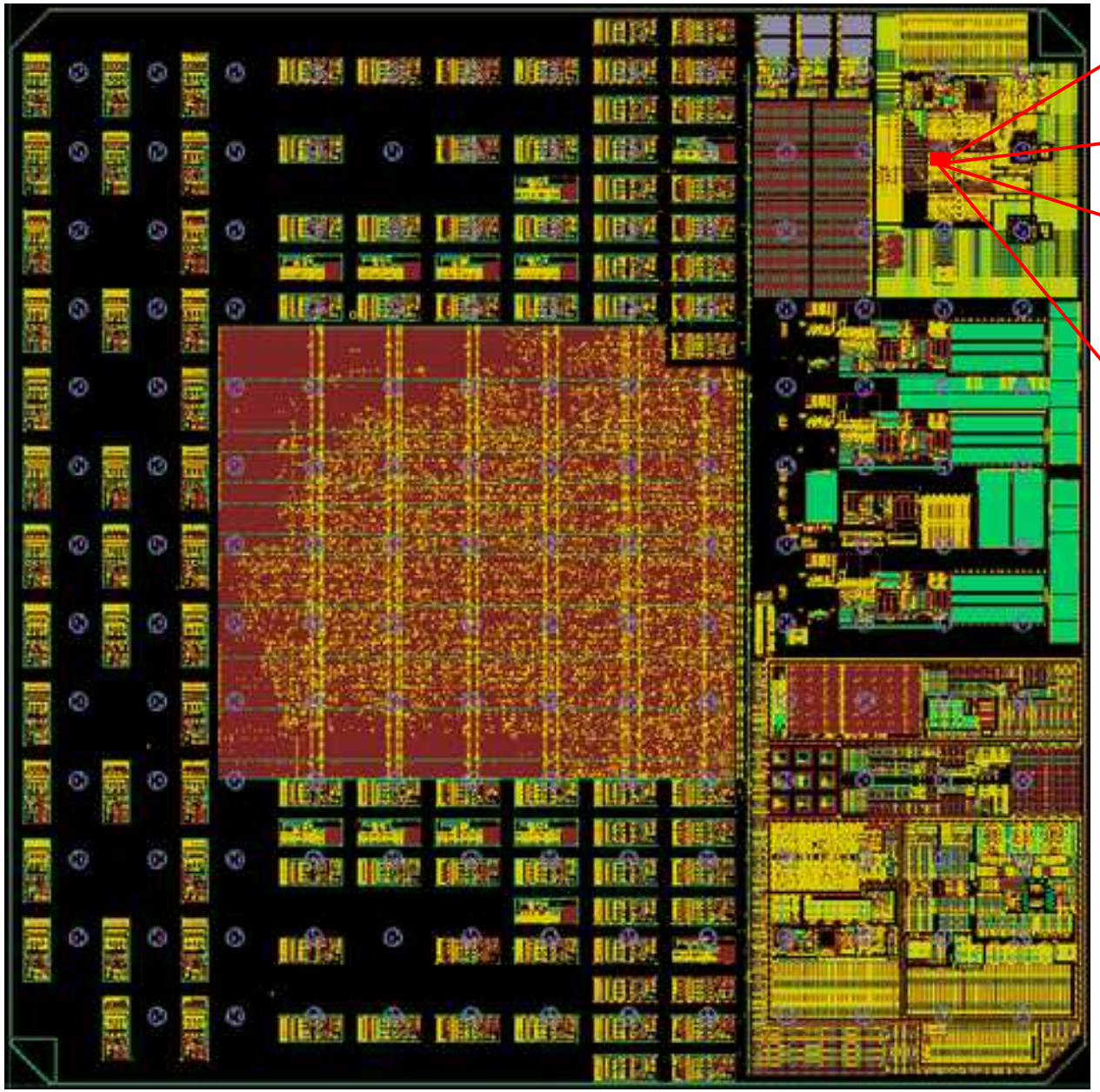
A process repeated a few hundred times

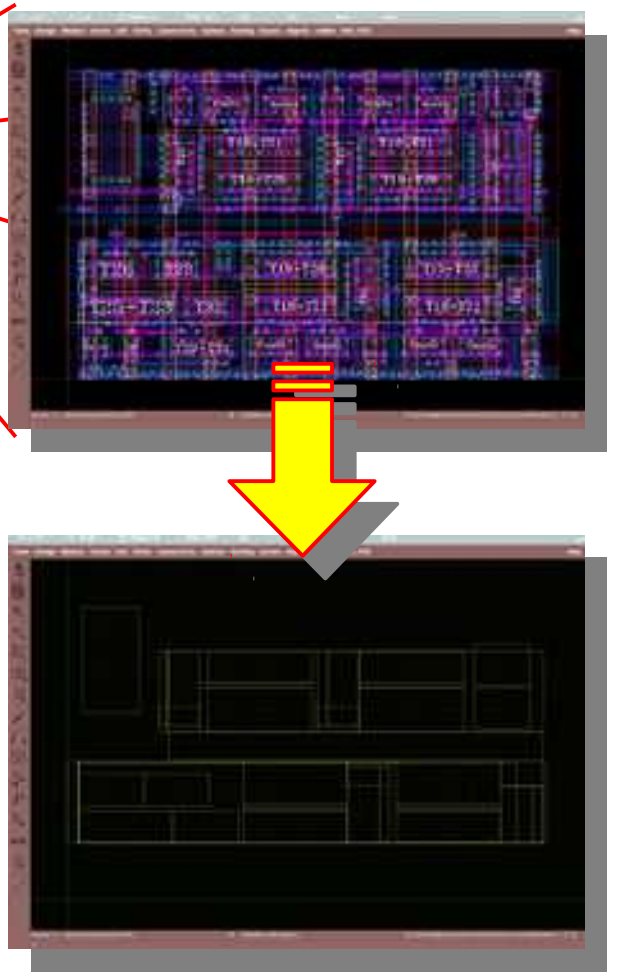


The CAMD front-end ASIC designed for RICH-I detector of COMPASS experiment at CERN. (350 nm CMOS).

How many layers do you see ?

A process repeated a few hundred times





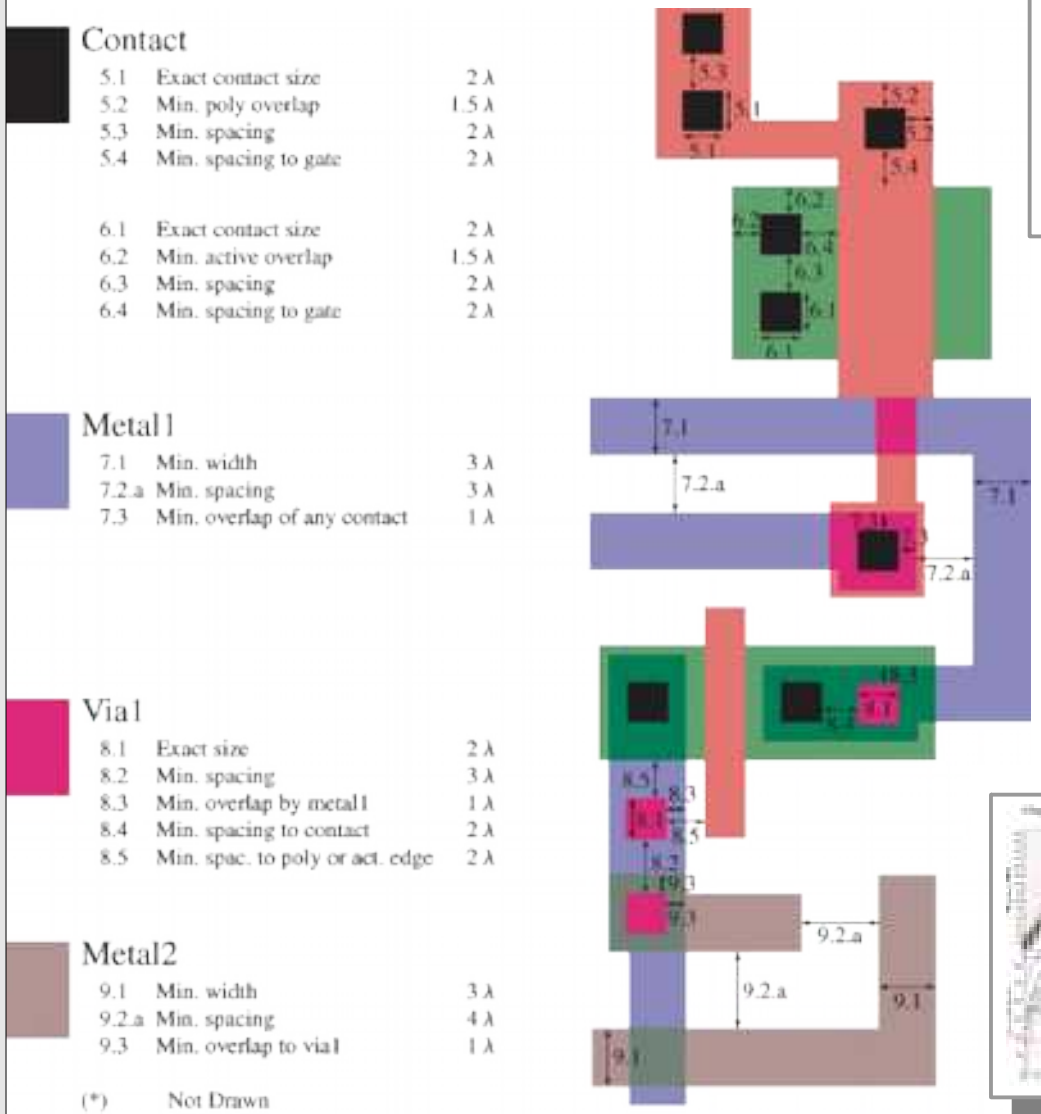
A sub-set of masks forming the above block
(Animated GIF image)

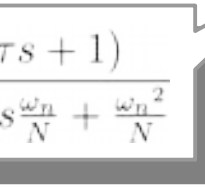
The first prototype of the SER-DES ASIC for the GBT13 chip-set under development for the Super-LHC at CERN. (130 nm CMOS)

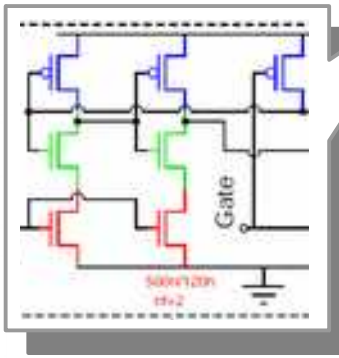
VLSI Design in Practice

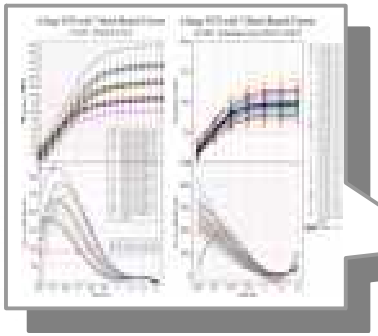
Daily life of an ASIC designer

- Interface between **process scientist** and **designer**
- Focus on **reliability** and increased **manufacturability**









Specifications

Schematic entry

Simulation

Layout

Design Rule Check

Parasitic Extraction

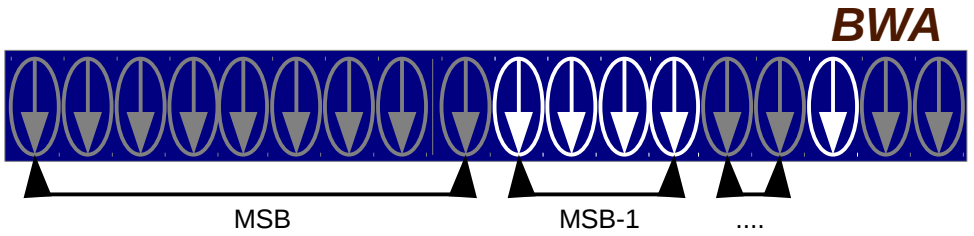
Layout Versus Schematic check

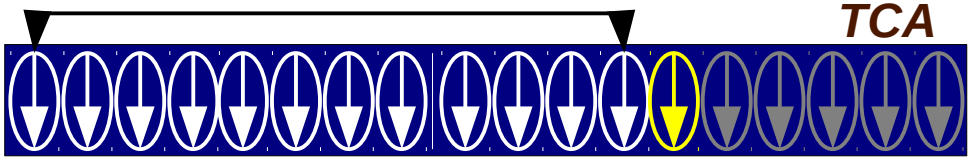
Post-Layout Simulation

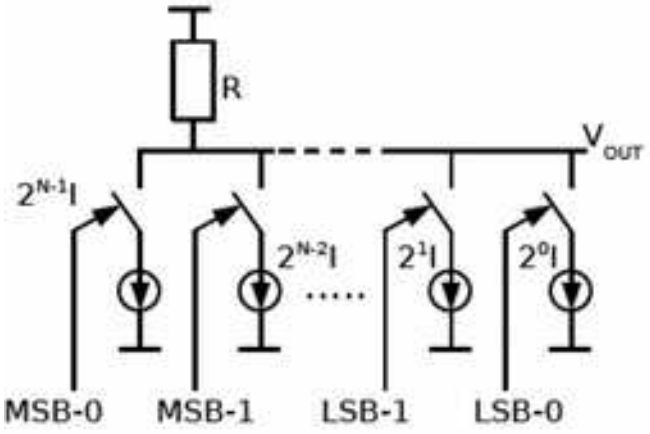
Architectural Choice

Quantitative comparison between different approaches

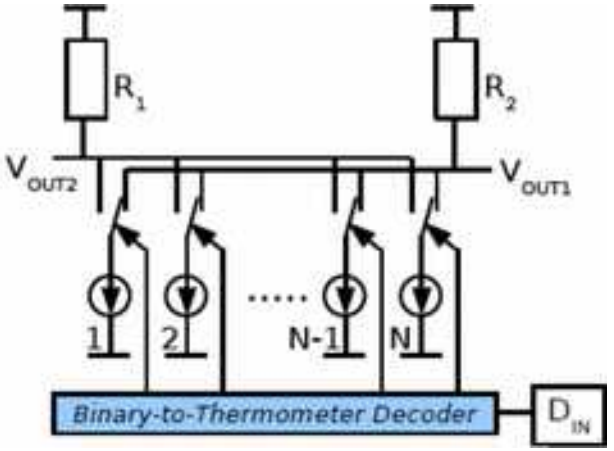
- A **10-Bit** current-mode D/A converter
- Two possible **architectures**; have to **choose one**
- Need for **qualitative comparison**: MC is a **must**



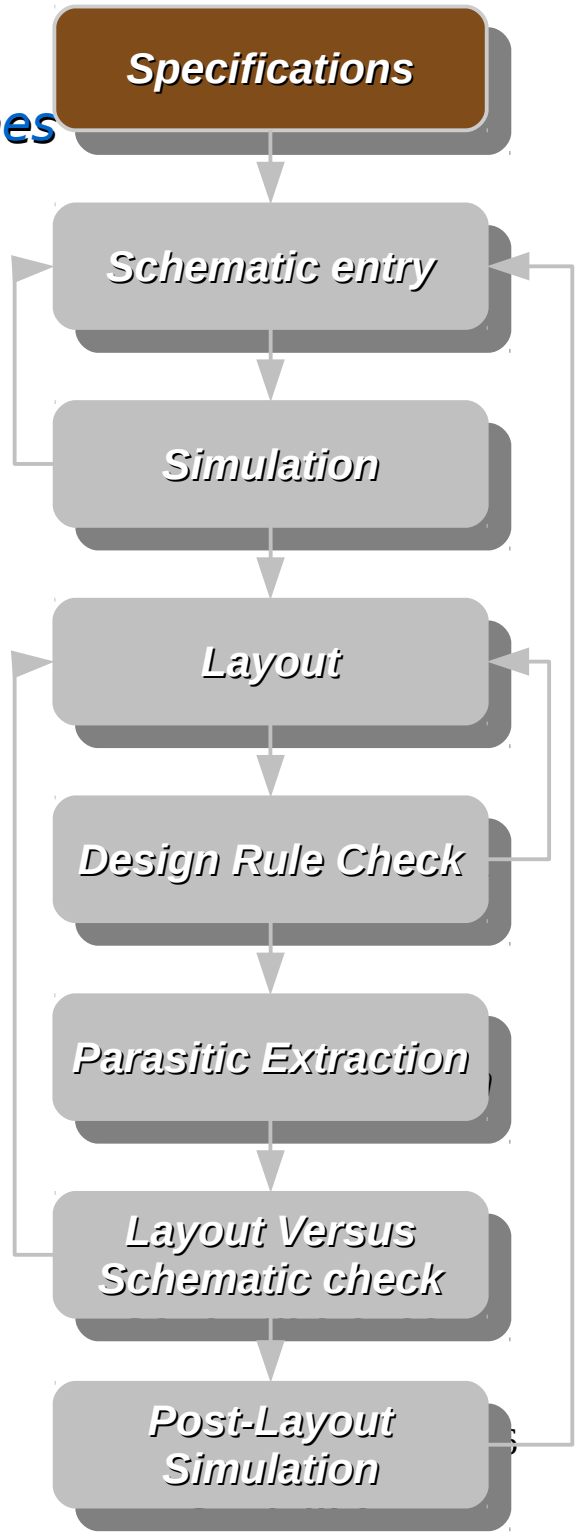




Binary weighted (BWA)



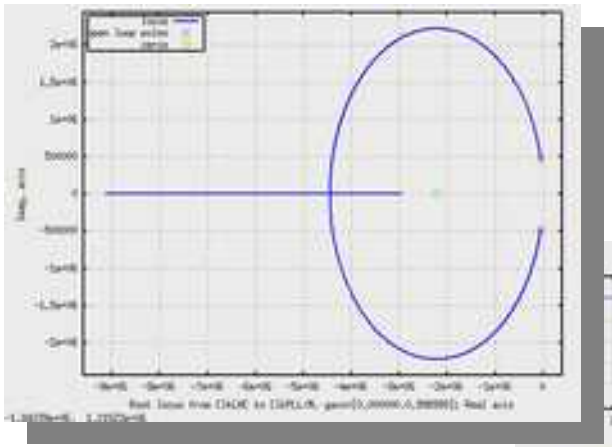
Thermometer coded (TCA)

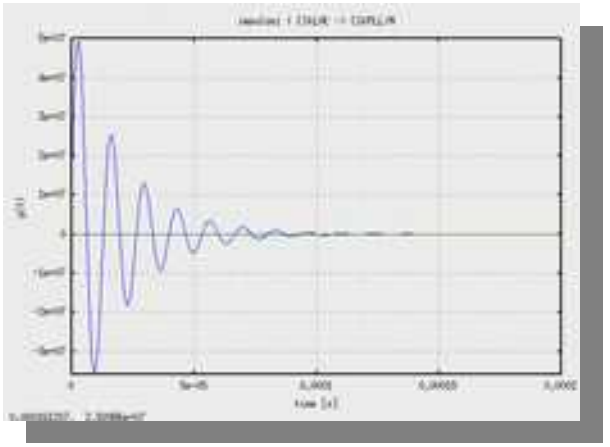


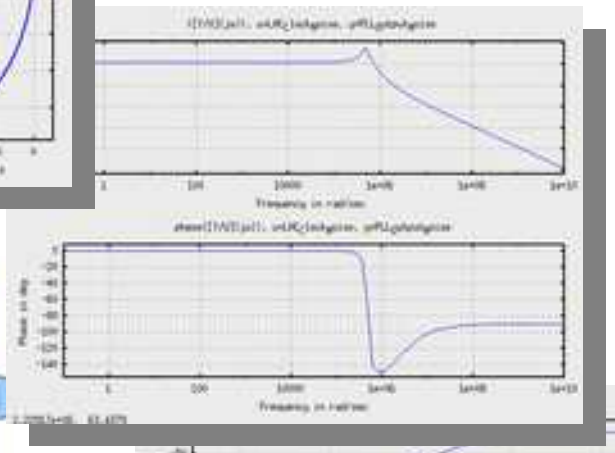
Parametrization

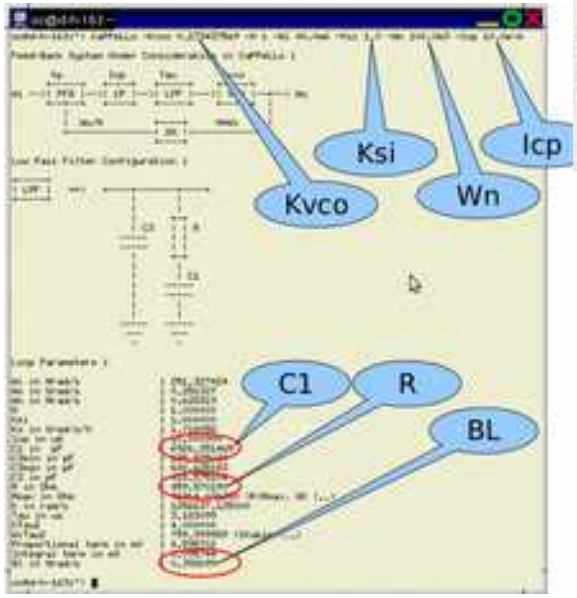
Optimizing the choice according to the application

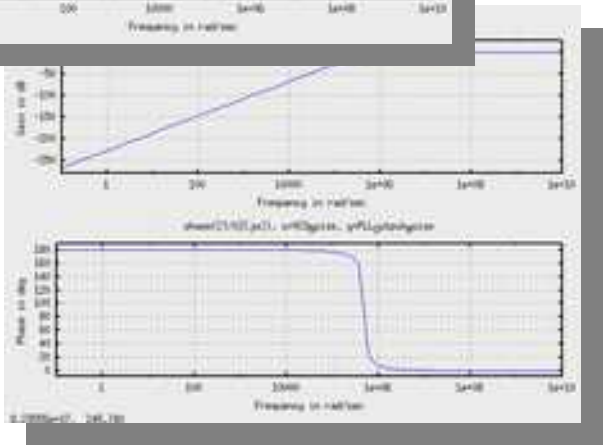
- Hand **calculations**
- Corresponding time & frequency domain **behavior**
- **Judgment**

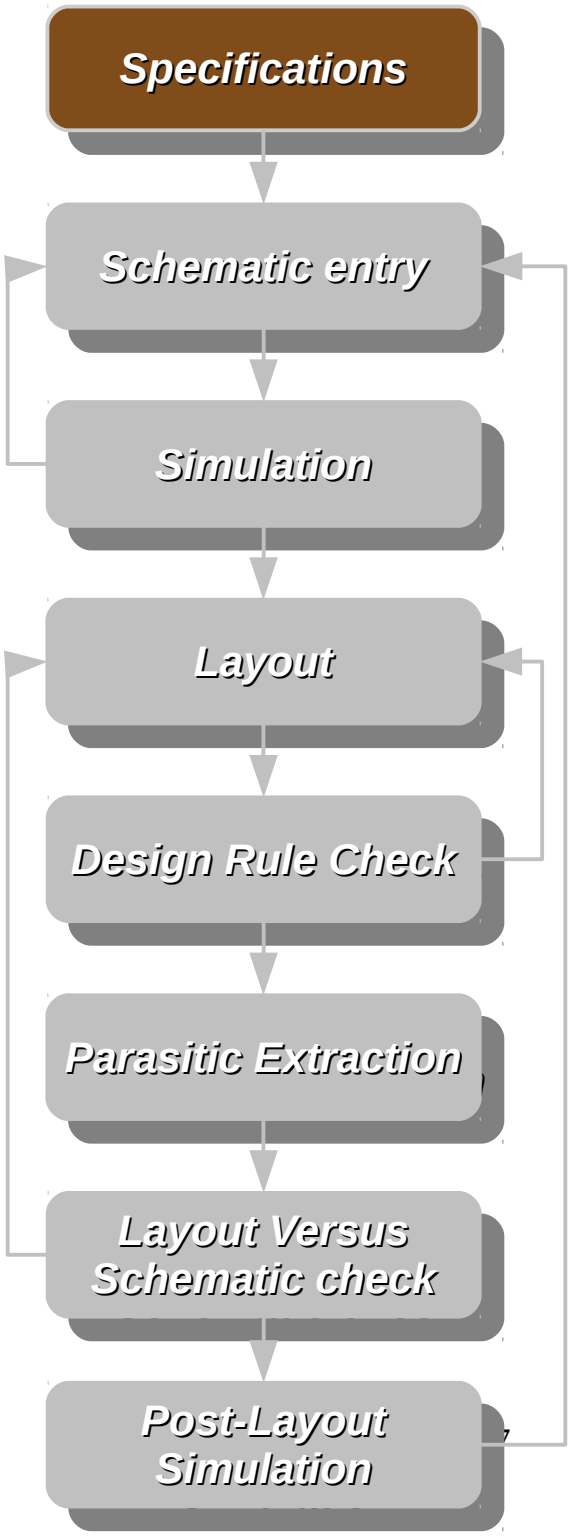


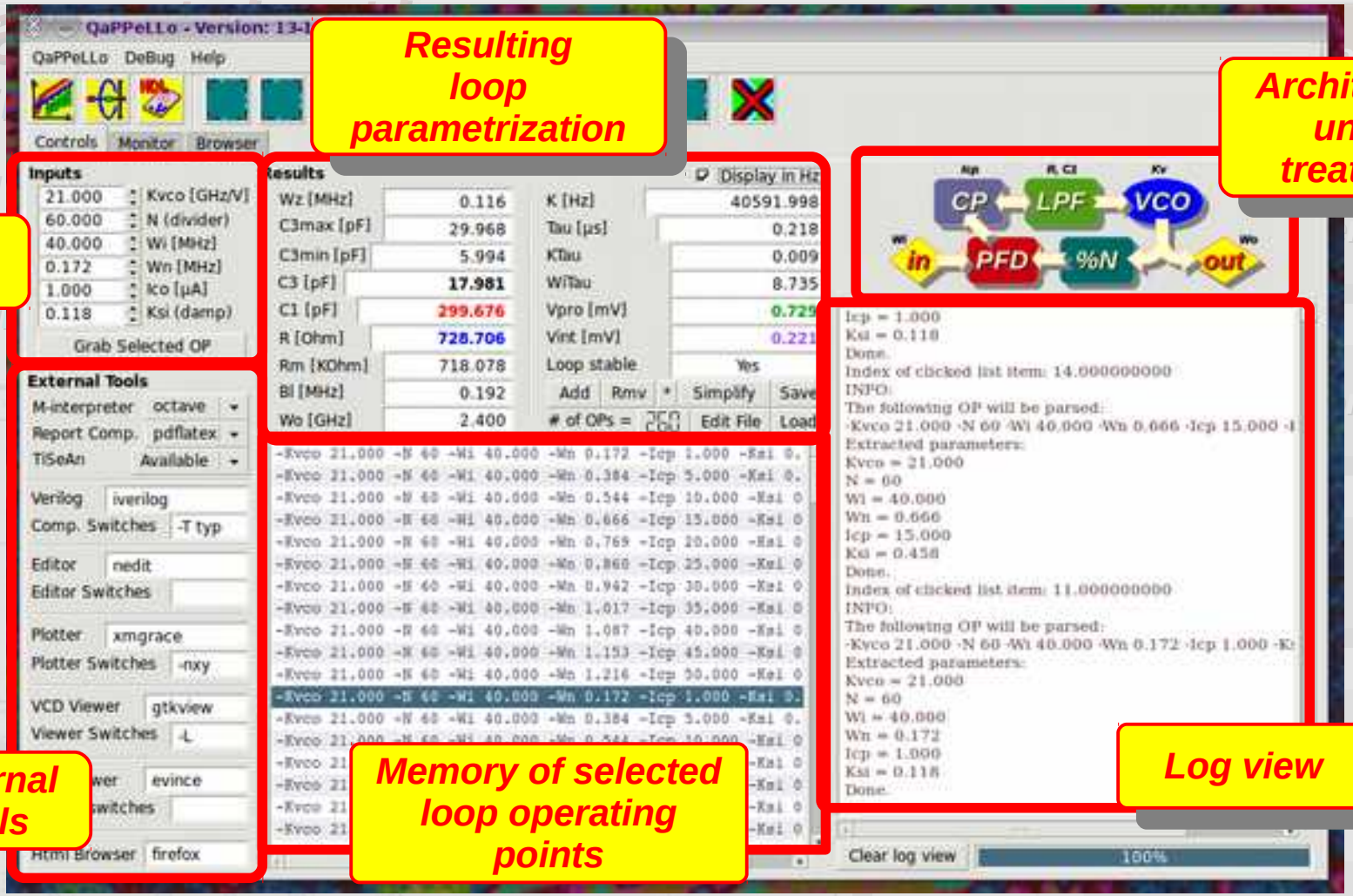








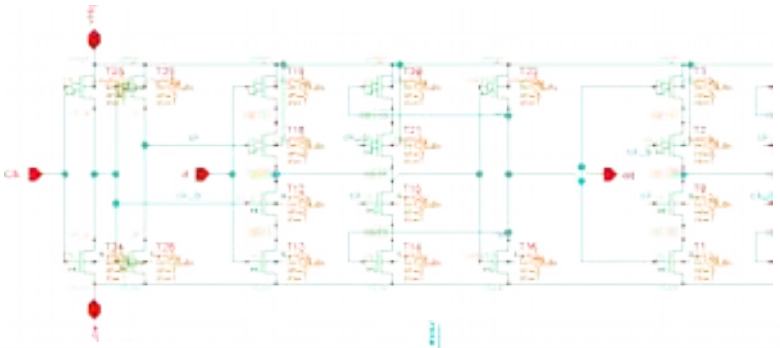


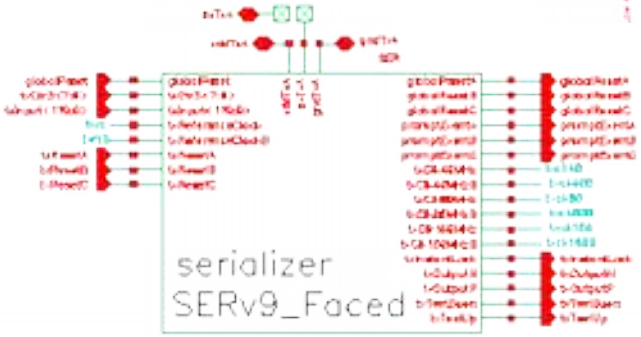


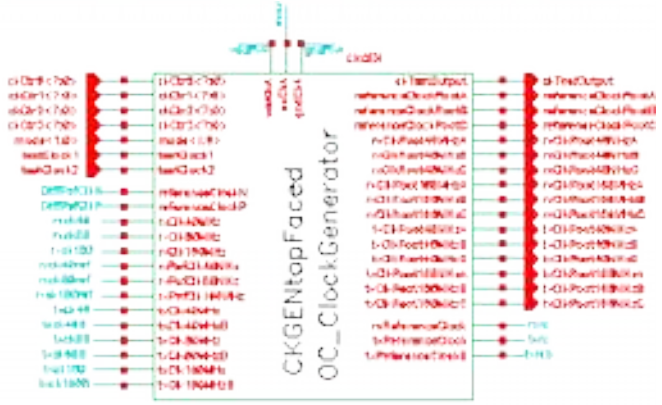
- **CaPPeLLo** gets just a few numbers and ***all automatically***:
  - Calculates loop parameters and generates the stability map for comparison
  - Calculates frequency domain loop response as
    - Bode and root locus plots, step & impulse responses, noise transfer functions, etc.
  - Generates the verilog model of the architecture with the selected parameters
    - Compiles and runs the verilog model, displays the wave forms
    - Analyzes the jitter data generated during the this simulation
  - Searches for chaos by means of time series analysis and creates attractors, etc.
  - Generates a report summarizing all above actions

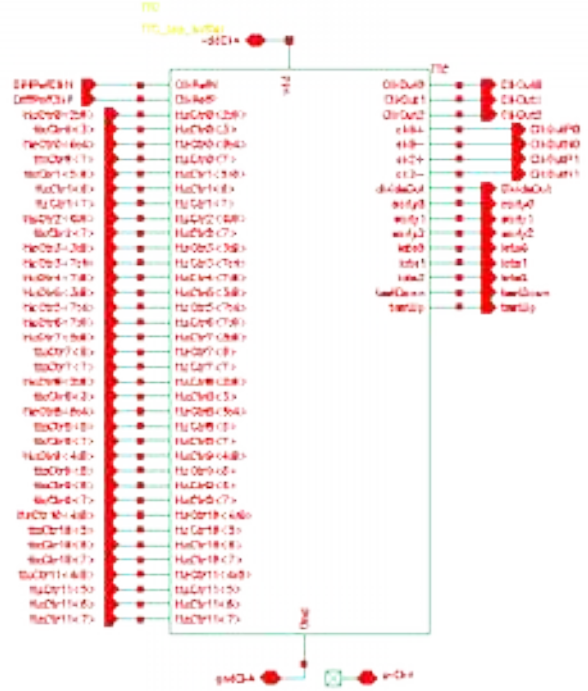
Schematic-Level Design

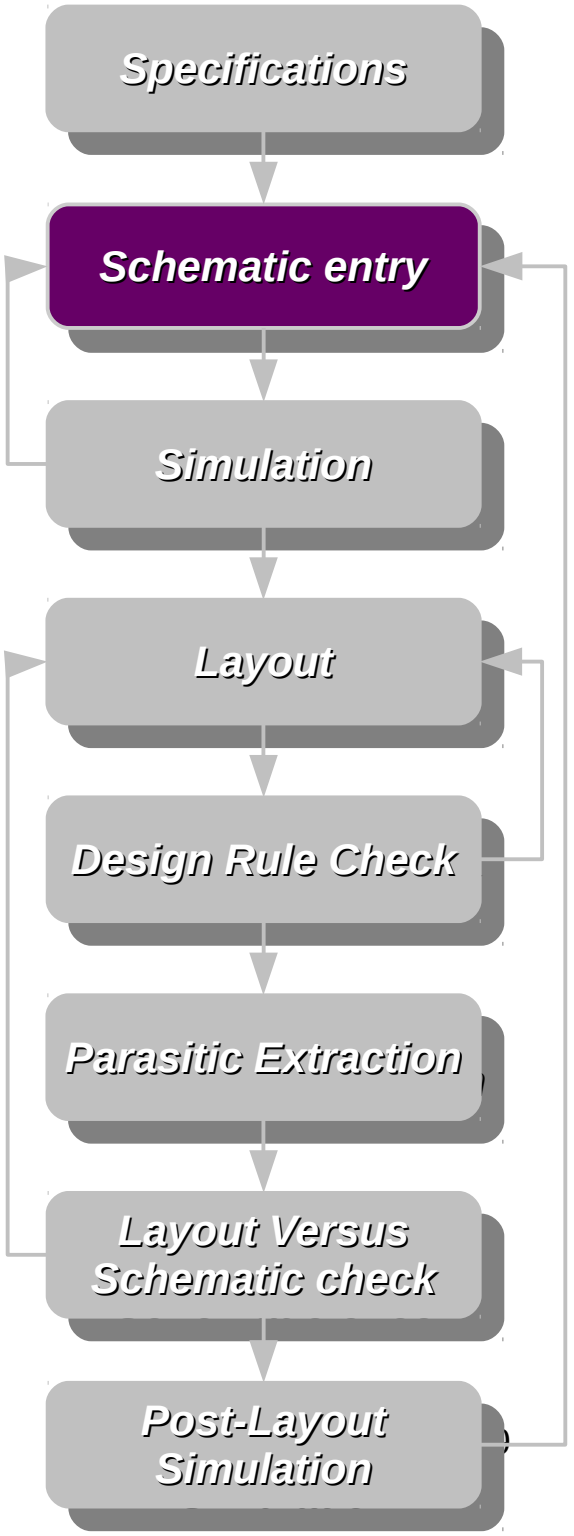
- Place **devices**
- Connect **ports**
- Build a **hierarchy**





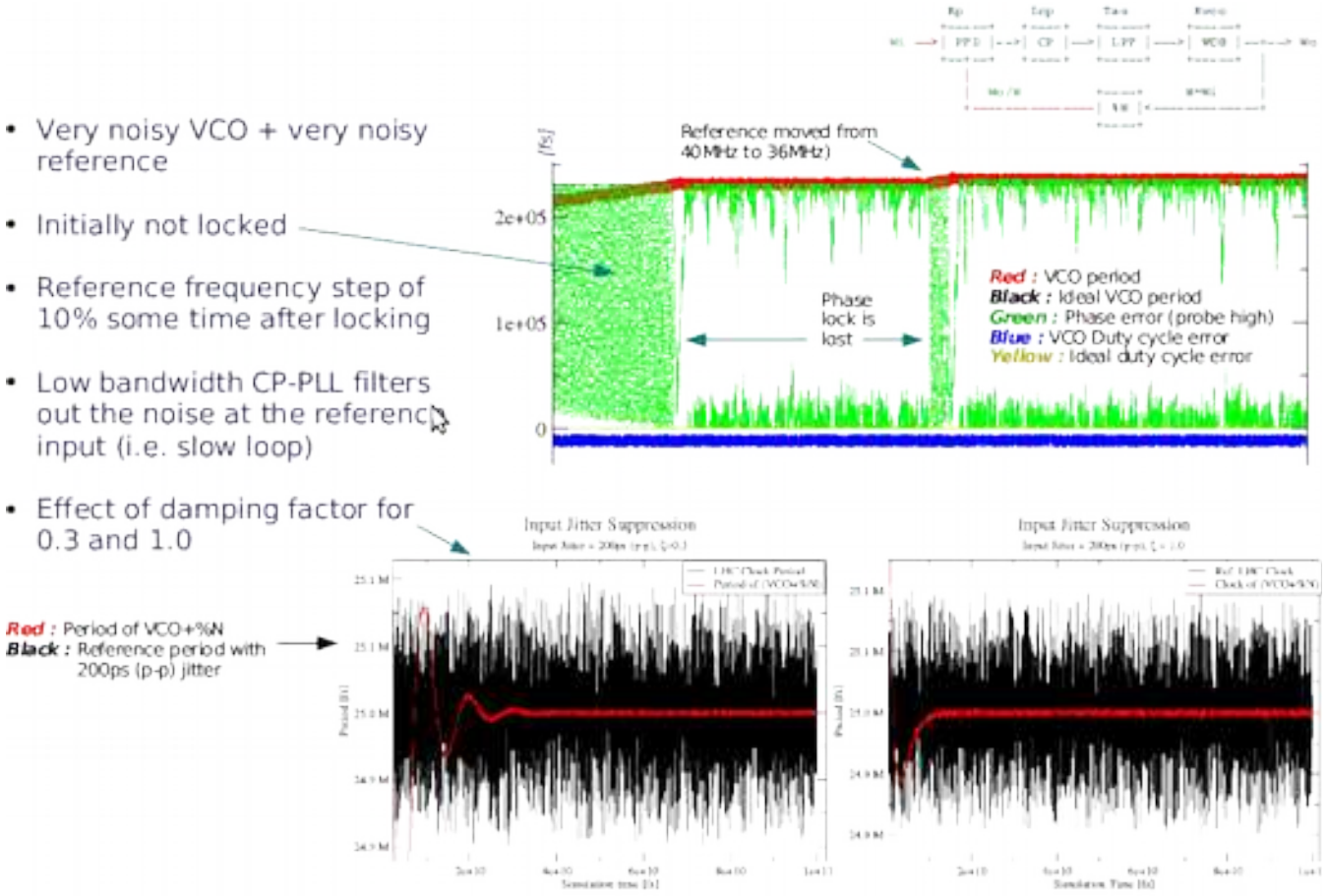


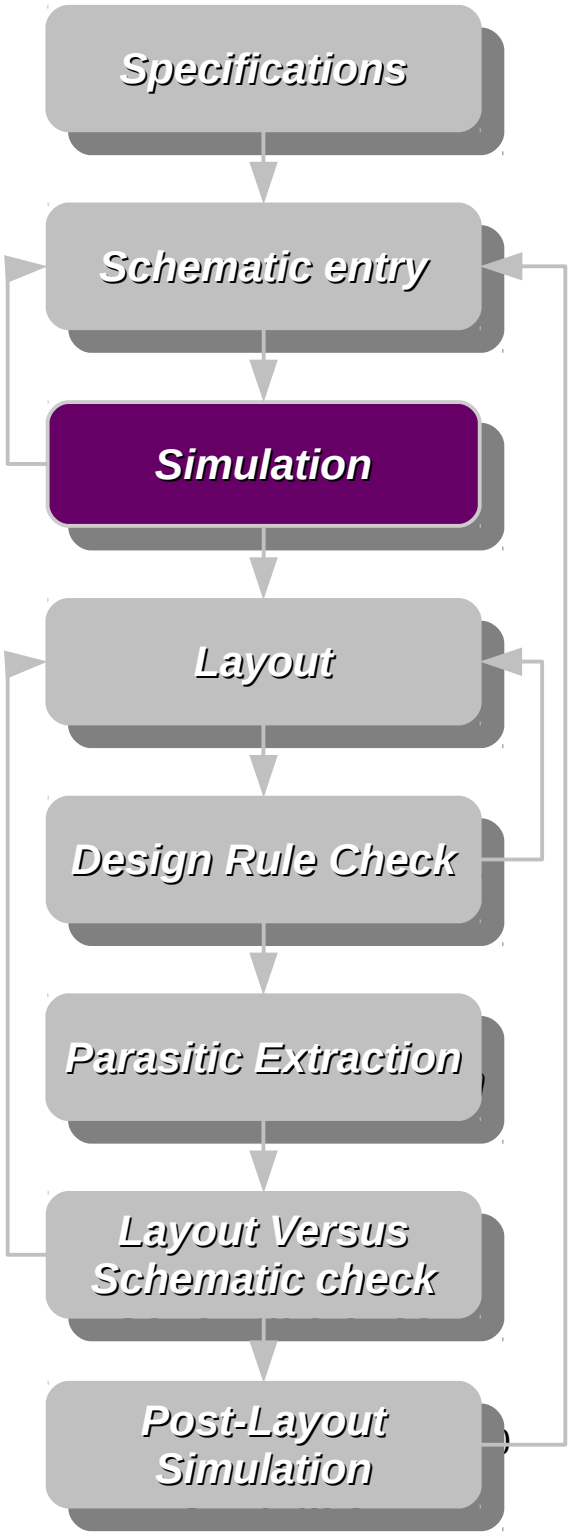




Simulation

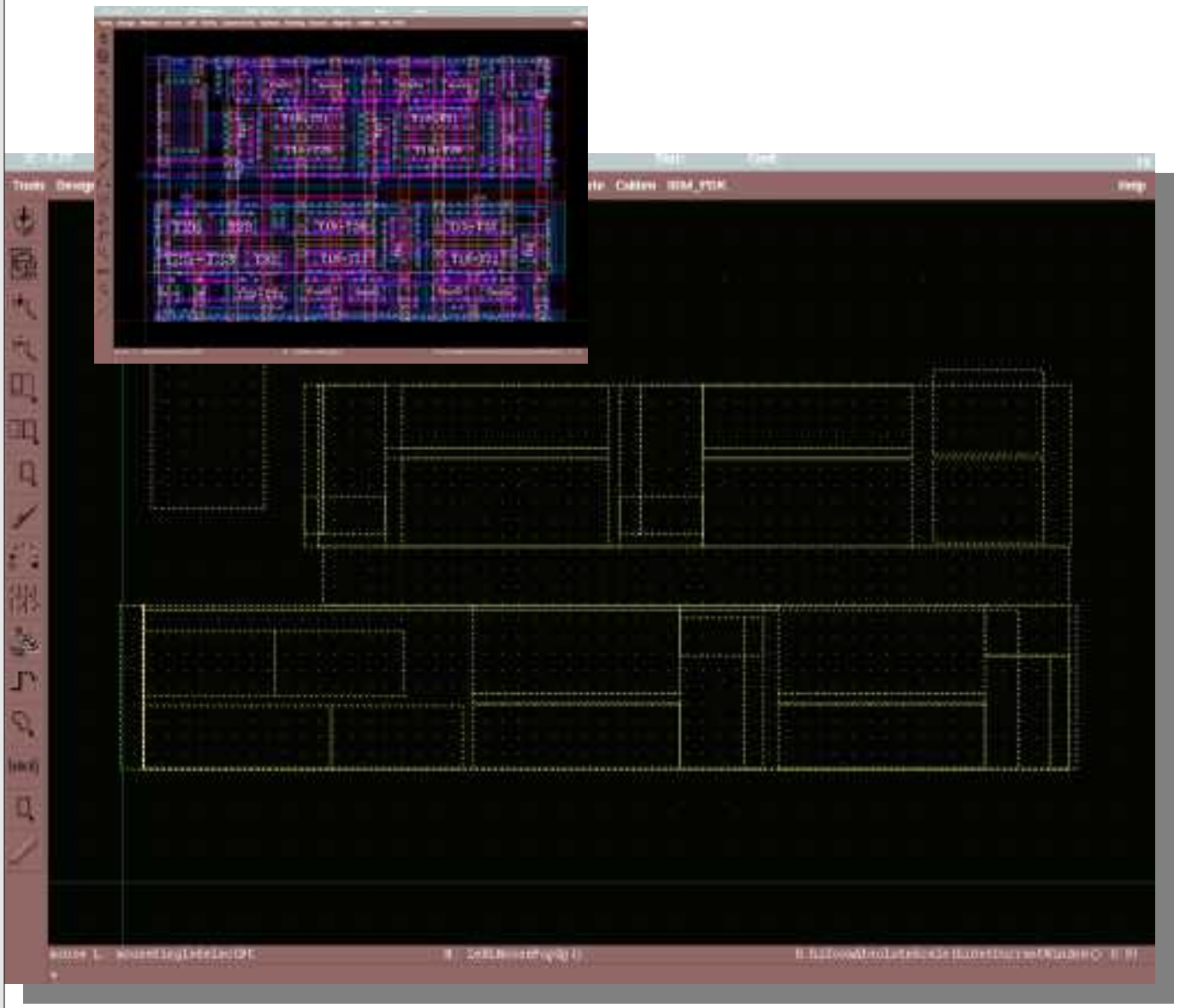
- **Model-based** time-step simulations (HDLs, MatLab, Octave, Cadence, etc.)
- **Transistor-level** SPICE simulations (Spectre, UltraSim, etc.)
- **Radiation** simulations (Process simulators, Spectre, etc.)

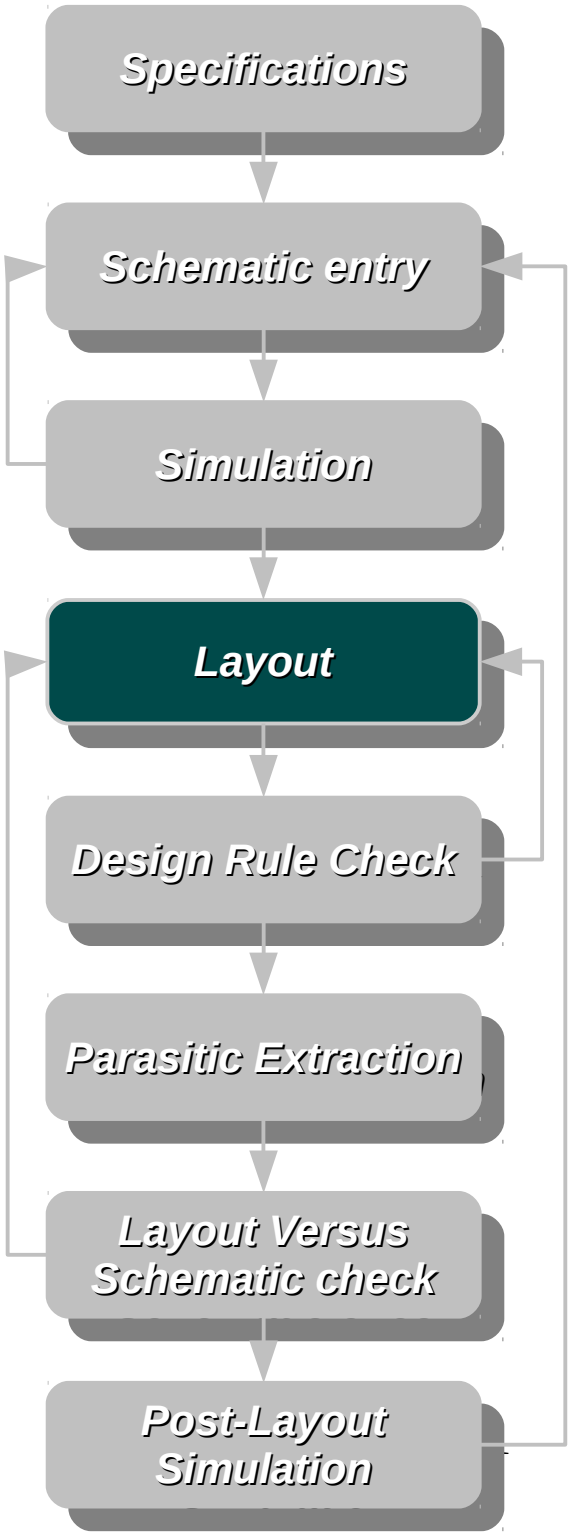




Layout

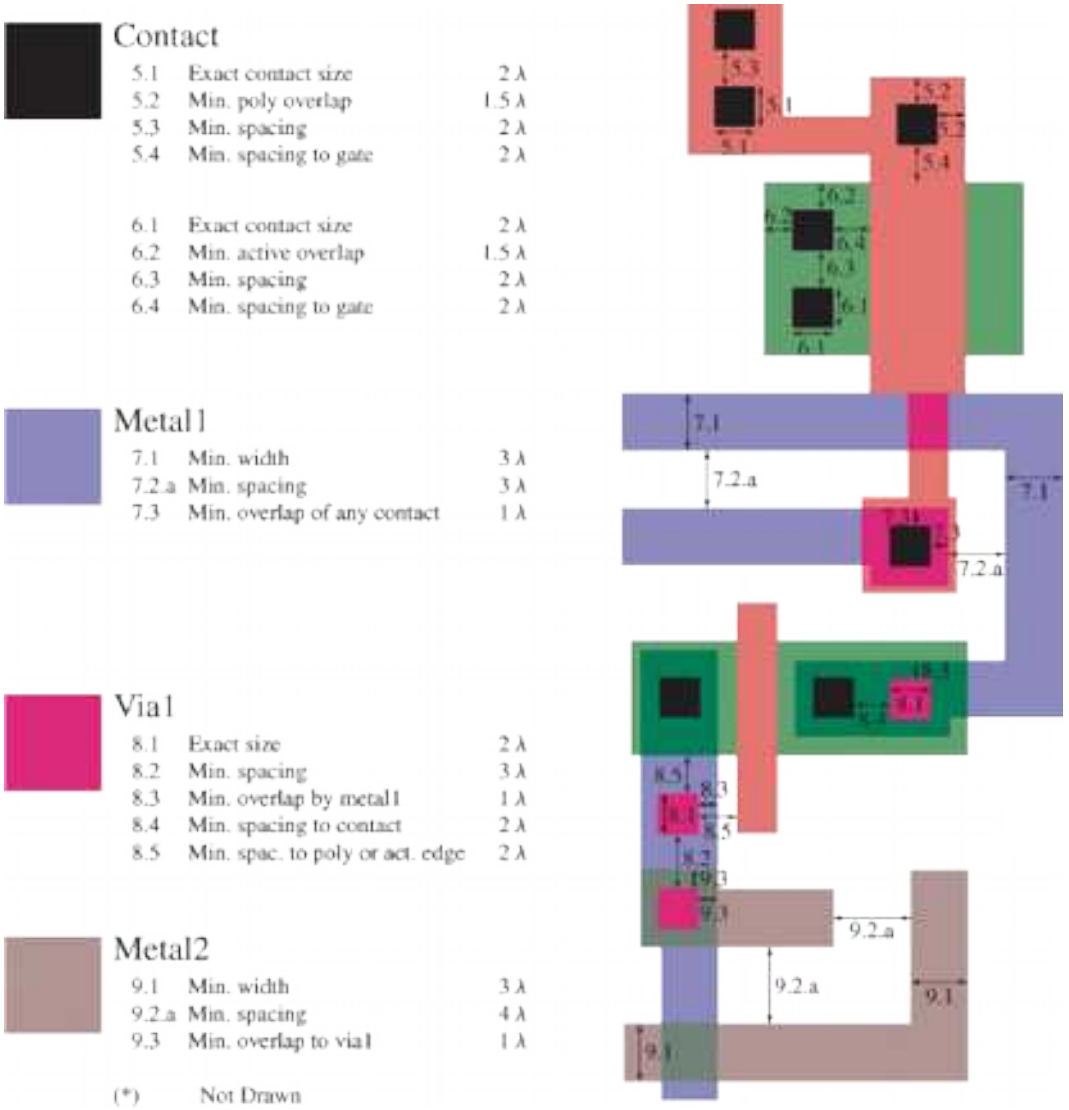
- Lithographic **masks** are designed
- Actual representation of a circuit on the **die**





DRC

- **Infinite** *different paths of matching what the schematic represent (art)*



Contact

5.1	Exact contact size	2 λ
5.2	Min. poly overlap	1.5 λ
5.3	Min. spacing	2 λ
5.4	Min. spacing to gate	2 λ
6.1	Exact contact size	2 λ
6.2	Min. active overlap	1.5 λ
6.3	Min. spacing	2 λ
6.4	Min. spacing to gate	2 λ

Metal1

7.1	Min. width	3 λ
7.2.a	Min. spacing	3 λ
7.3	Min. overlap of any contact	1 λ

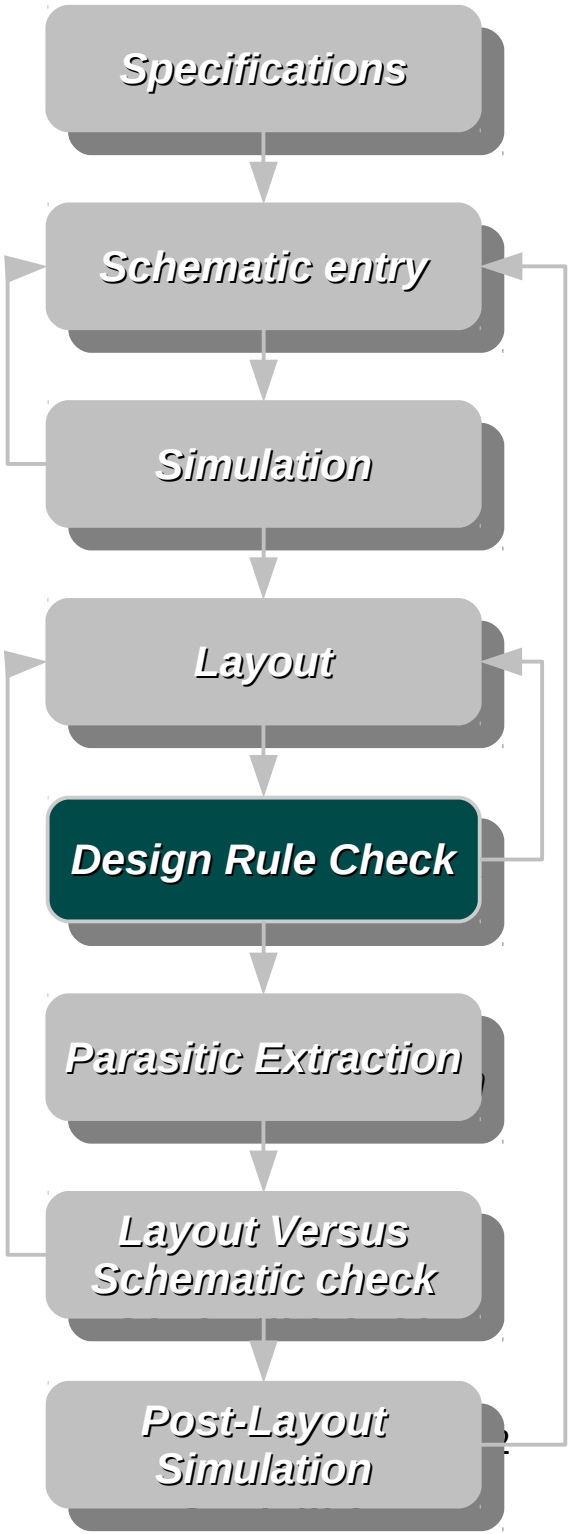
Via1

8.1	Exact size	2 λ
8.2	Min. spacing	3 λ
8.3	Min. overlap by metal1	1 λ
8.4	Min. spacing to contact	2 λ
8.5	Min. spac. to poly or act. edge	2 λ

Metal2

9.1	Min. width	3 λ
9.2.a	Min. spacing	4 λ
9.3	Min. overlap to via1	1 λ

(*) Not Drawn



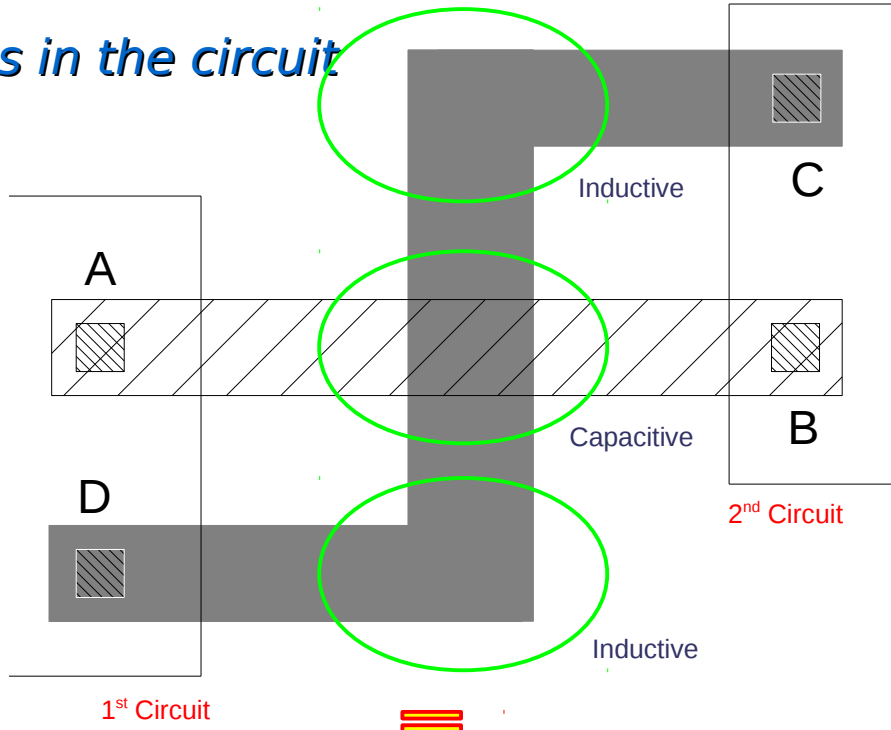
Parasitic Extraction

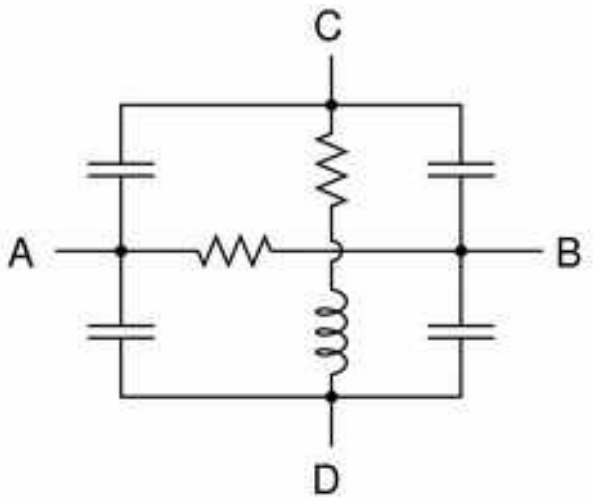
For a better physical representation of what is in the circuit

- *Perform two **simple connections**:*
  - *Connect the pin **A** to pin **B** with **metal-1***
  - *Connect the pin **C** to pin **D** with **metal-2***

- *Designer **did not draw** any device but the **effective circuit** has at least the followings:*
  - *4 capacitors*
  - *2 resistors*
  - *1 inductor*

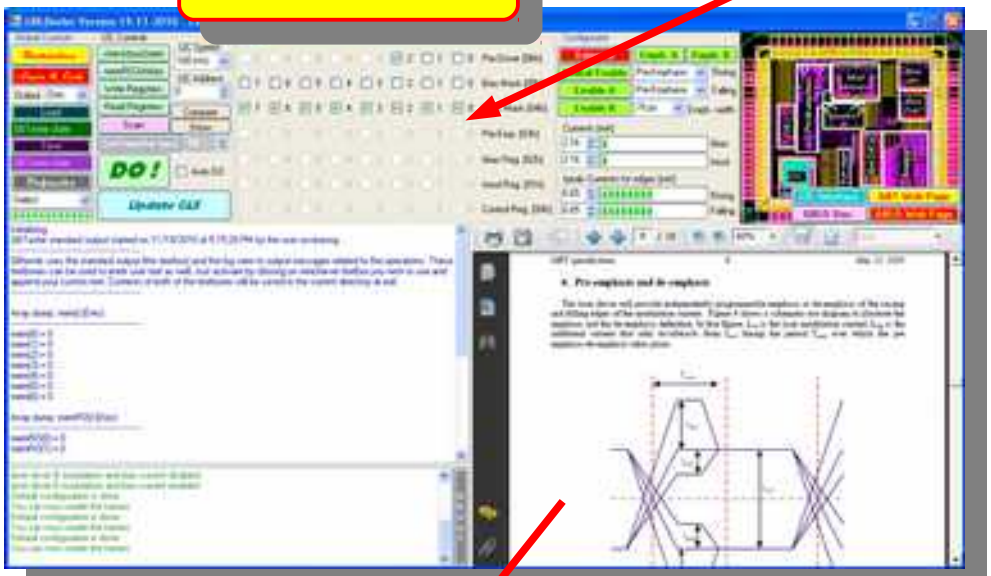
- *Things which are not taken into account in schematic are the parasitic devices that **can not be avoided** but minimized/maximized*
  - *e.g. minimize input capacitance of a FE or wire capacitances between building blocks*
  - *e.g. maximize narrow-band PLL filter capacitance or de-coupling capacitors of any ASIC*

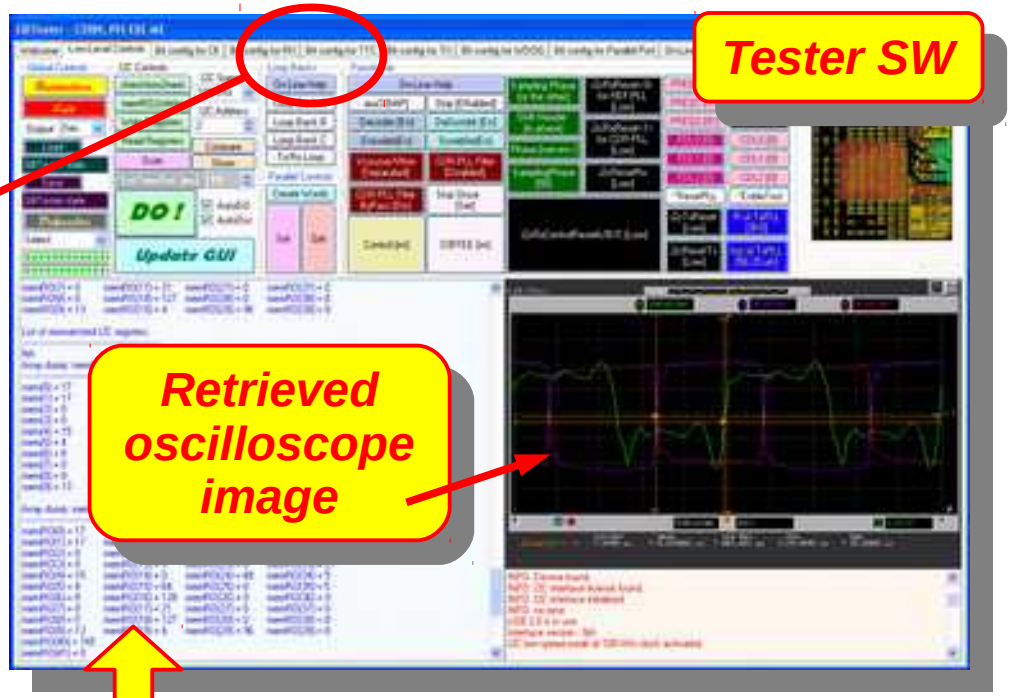


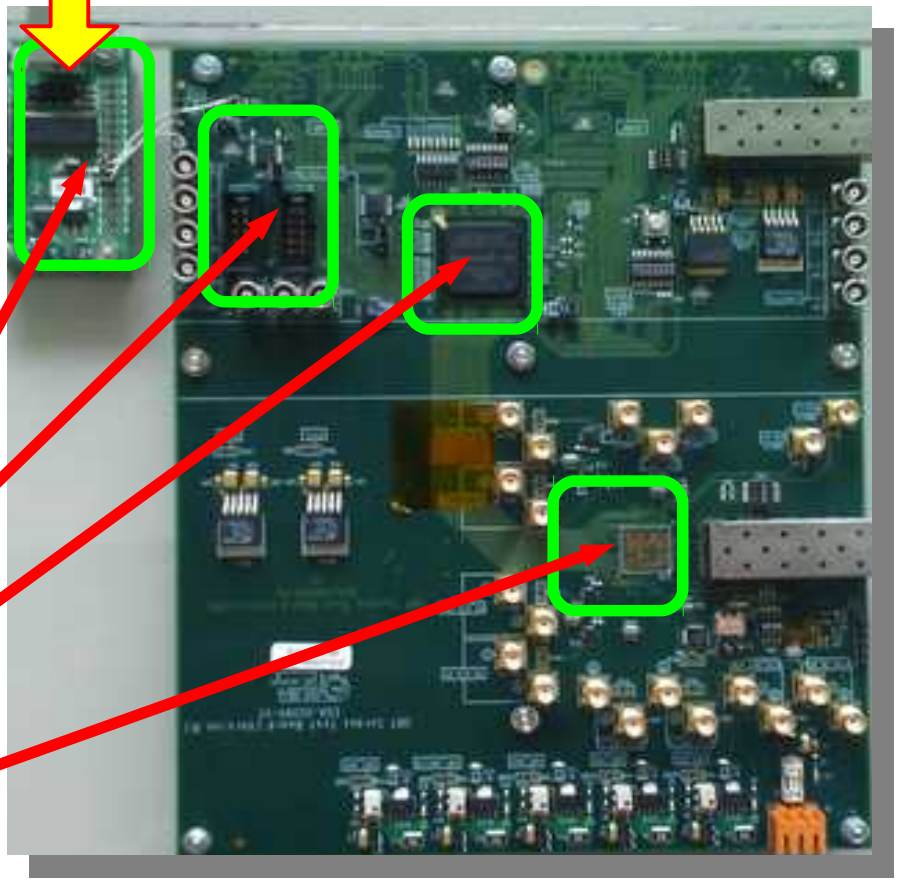


Test Boards

and tester/configurator application







Introduction to the Design of Full-Custom Front-End & Data Transmission ASICs*

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- ***The Big (but Brief) Picture***
  - Briefly **front-end** - FE
  - Briefly **read-out** - RO
  - Briefly **serializer** - SER
  - Briefly **phase-lock loop** - PLL
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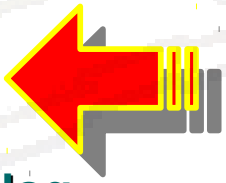
  - A **qualitative** introduction
  - **Natural frequency** concept - ω_n
  - Real-world examples:
    - **Binary** read-out
    - **Time-over threshold**
  - Adjusting/optimizing loop behavior
    - Damping ratio
- ***Reminder on Detectors***
  - Photodetectors ***vs*** photon counters
  - ***Position-sensitive*** detectors
    - Resistive charge division
    - Discrete array of elements
  - ***Time-resolved*** detection
- **Detector Front-End ASICs**
  - **Pre-Amp**: basic idea – V_{OUT} / V_{IN}
  - **Transconductance** of a transistor - g_m
  - Evolving a **single-stage amplifier** into a real-world application
- **Processing Technology**
  - **Transistor** switch – A masterpiece
    - **Lithography**
    - Formation of an **nMOS** transistor
  - VLSI design flow
    - Parasitic **extraction**
  - Real-world ASIC examples
- **Radiation Tolerance Issues**
  - Definitions:
    - **Single event upset, analog single event transient, latch-up**
  - **Simulating** radiation effects on analog circuits



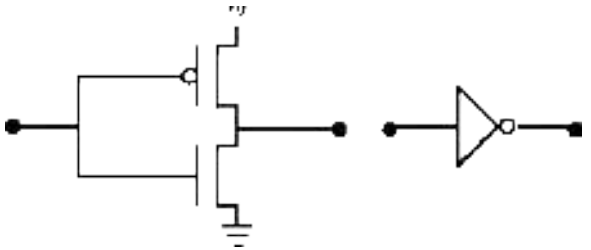
* *Application Specific Integrated Circuit*

Radiation Issues

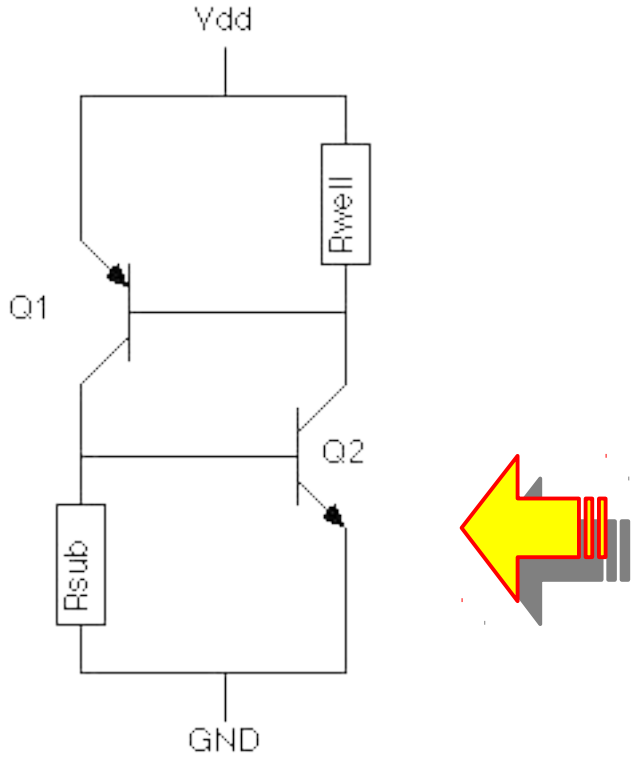
Definitions and failure mechanism

- Single Event Transient (***SET***)
  - A transient perturbation on an analog signal due to charge released by an ionizing radiation.
- Single Event Upset (***SEU***)
  - State change of a digital circuit due to charge released by an ionizing radiation.

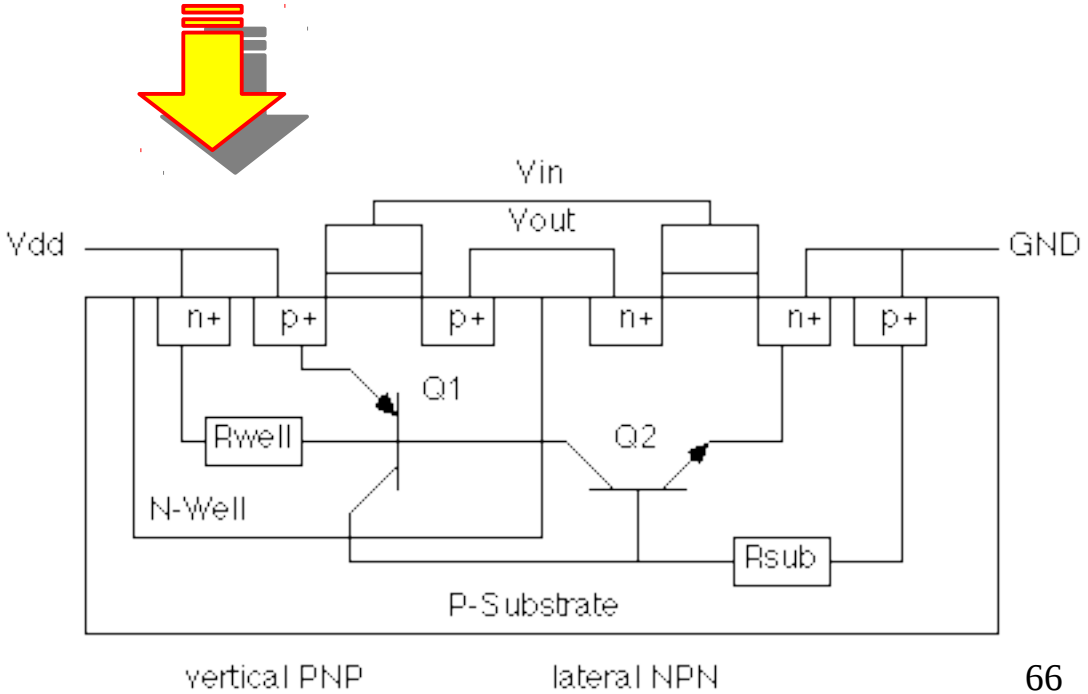
- ***Latch-Up***
  - Creation of a low-resistance path between Vdd and Gnd due to a positive feedback loop formed by parasitic devices.



CMOS inverter and its symbol



Equivalent parasitic BiPolar circuit



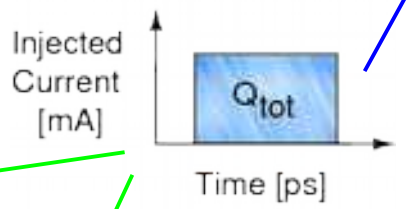
Wafer cross-section of the inverter

Modeling Radiation Effects

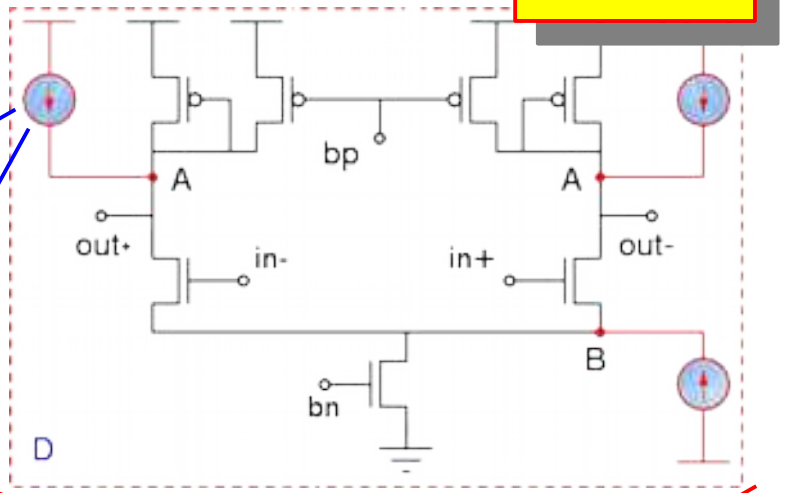
Taking radiation into account in simulations

- Radiation = current pulse
  - E.g.: 0.3 ***pC*** in 130 nm CMOS
- Plot: Effect vs Q
  - Define/check specifications
  - Repeat the cycle

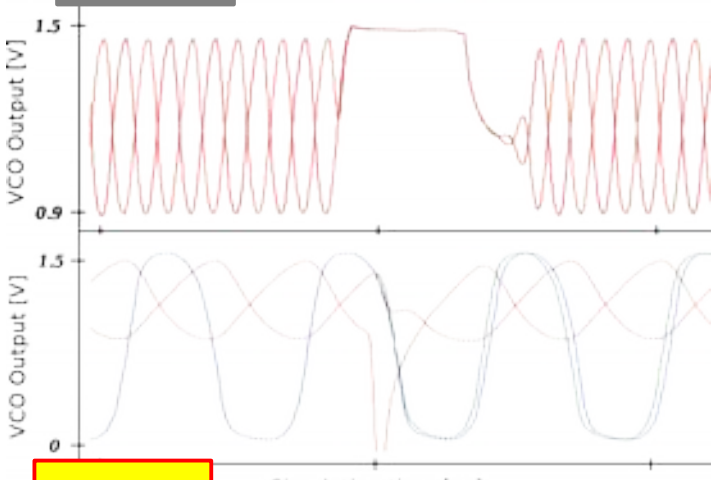
Q



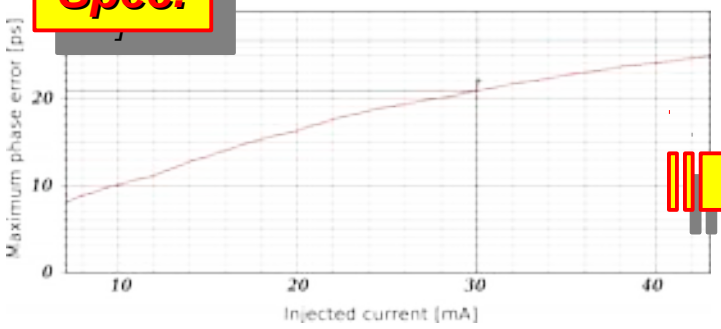
Circuit



SETs

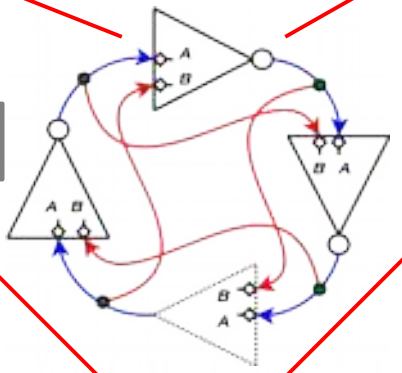


Spec.

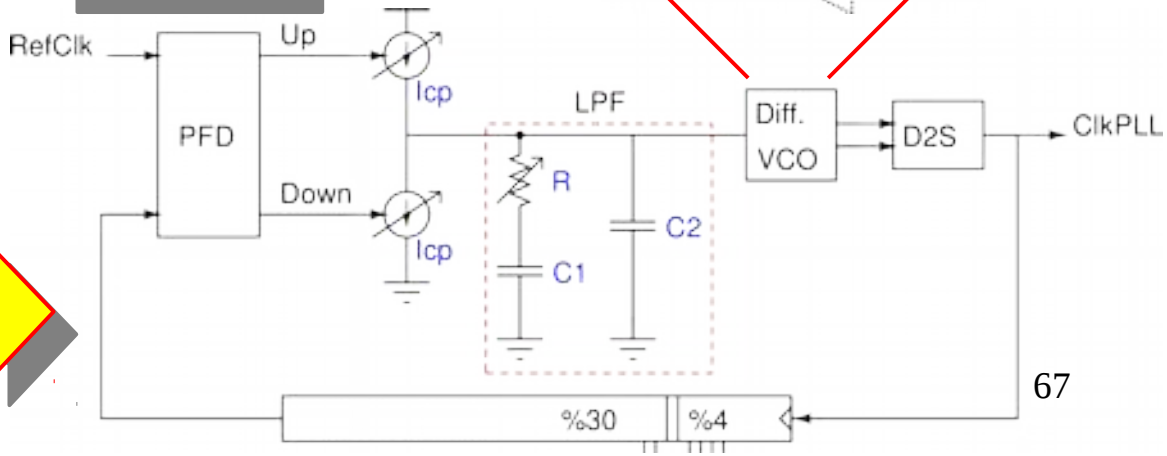


You start here !!

VCO

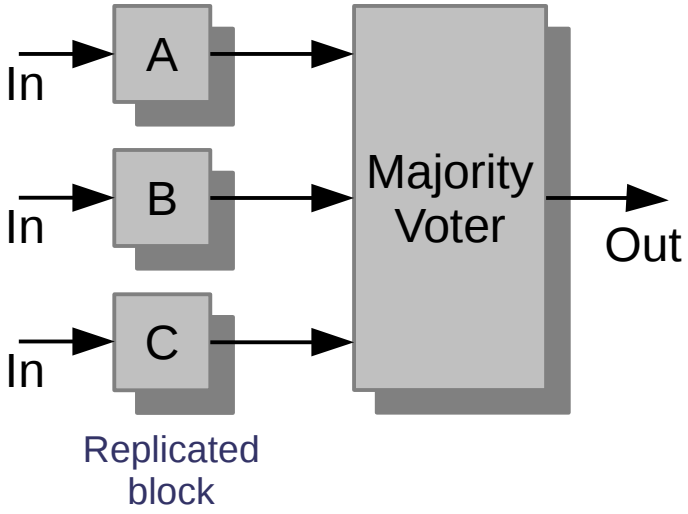


System

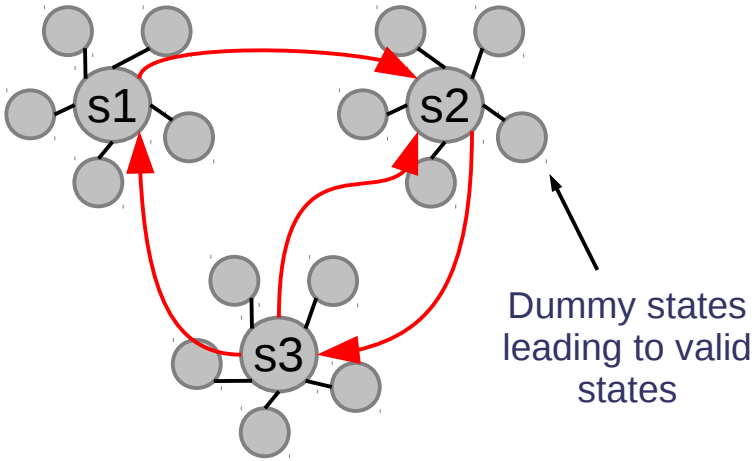


Rad-Hard Design Tricks

Adding robustness to circuits



- Use ***higher current levels*** and/or larger devices
  - The current/voltage excursions ionizing particles generate stay insignificant
  - Prise to pay: increased circuit footprint and power dissipation, slower operation, etc.
- Use ***triple-well*** and/or ***guard-ring*** structures frequently
  - To ground any noise before it reaches to sensitive circuitry
- Use ***Modular Redundancy*** (nMR)
  - Replicate circuitry and vote at the output, Triple Modular Redundancy (TMR) is commonly used
  - The probability for an ionizing particle to affect all the three blocks at the same time is very low, therefore this technique is commonly used to harden designs against SEU



- Use ***dummy states*** to protect Finite State Machines (***FSM***) against SEUs
  - If a state change occurs due to an ionizing particle passage, the FSM can return to a valid state without impairing
  - Prise to pay: more complex FSM design, increased power dissipation and circuit footprint
- Place the ASICs within magnet ***shadows*** (where applicable)
  - To decrease radiation tolerance requirements

Introduction to the Design of Full-Custom Front-End & Data Transmission ASICs*

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* *Application Specific Integrated Circuit*