Front End Readout for the sPHENIX Time Projection Chamber

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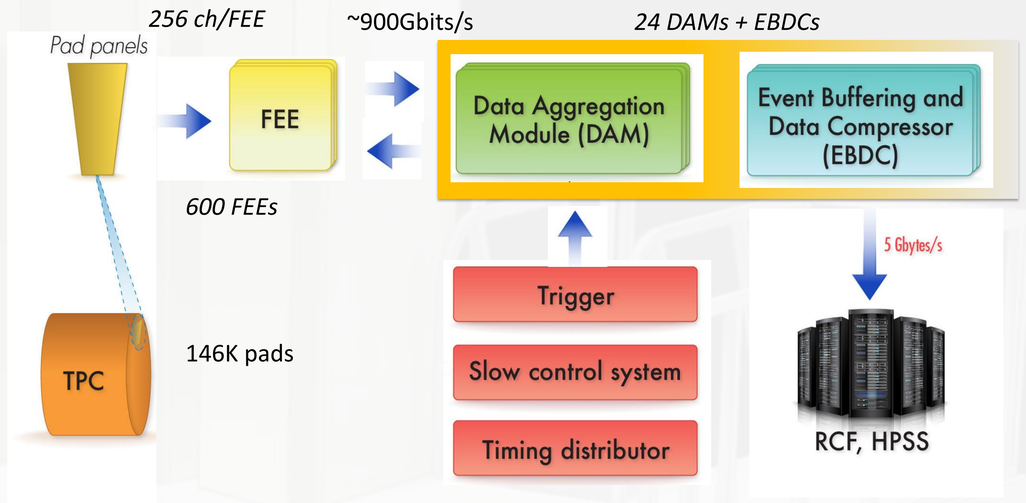
Abstract

The sPHENIX is the upgrade project of the PHENIX detector whose operation has just ended. This upgrade project mainly focuses on the detailed measurement of the jets and Upsilons. We have proposed to build a time projection chamber (TPC) as the main tracker for the sPHENIX, which has a radial coverage of 20 cm to 78cm with rapidity coverage of $|\eta|<1.1$ and full azimuth. The number of readout channels will be ~150K, and the raw data volume is expected to reach as much as ~1Tbps. In order to fully exploit the data within the limitation of the bandwidth of the end tape device, we introduce a new continuous readout scheme followed by a fast data processing system. We show the initial design of the front end readout scheme for the sPHENIX TPC.

Whole readout scheme



sPHENIX TPC and specification

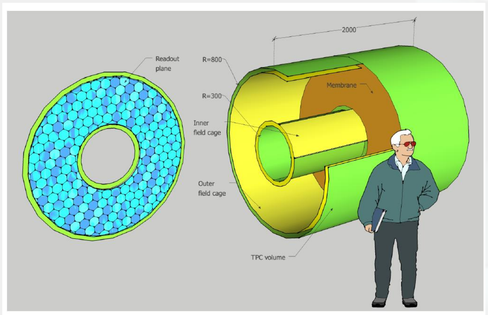
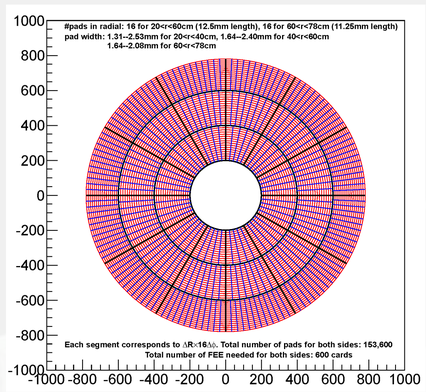


Figure 4.26: Schematic layout of TPC main elements.

5 FEEs for 20<r<40cm, 8 for 40<r<60cm, 12 for 60<r<78cm, for each 1/12 of full azimuth

Each cell = 16pads in ϕ

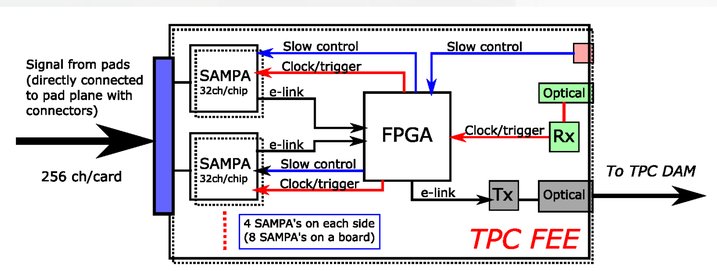


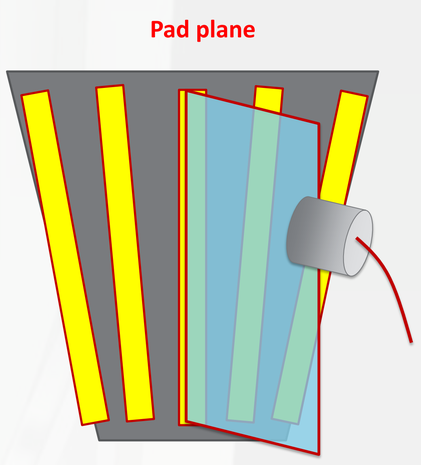
- Detector geometry
  - 20<r<78cm (20-30cm will be instrumented, but not to be readout in A+A collisions)
- Use of Ne-CF4-iC4H10: 95% - 3% - 2% gas
- GEM readout module, continuous readout.
- Pad configuration
  - 3 segments in ***r*** direction, each divided into 16
  - 12 segments in ϕ direction, each divided into multiple of 16
  - Variable pad size as a function of radial position
- 146K readout channels from both ends
  - 40 measurements (clusters) in ***r*** direction
- 15KHz is the baseline trigger rate
  - We assume that beam interaction may be as much as 100KHz for $|z|<1m$
- $dN_{ch}/dy = 180$ (minbias Au+Au 200GeV)
  - → 400 tracks in $|\eta|<1.1$
  - Background and fakes effectively doubles the number of tracks.
  - We assume 800 tracks in TPC in a MB event

Also see posters by K Dehmelt, P Garg, V.C. Roman and S. Tarafdar

FEE

- Each FEE takes care of 256 inputs. We fabricate 600 FEEs
  - Use of SAMPA chips (SAMPA is “shaper + ADC + DSP”)
  - SAMPA accepts 32 inputs; we place eight SAMPAs on one board (four SAMPAs on each side)
  - Sampling rate in z-direction: 10MHz (= 100nsec)
- Peaking time is 160nsec, ~350nsec for whole pulse shape.
  - More than 4 samples in timing (z) direction. We will take 5 samples including pre-signal
- One FPGA for traffic control
  - Receiving/distributing slow control and timing/clock
  - Collecting digitized data from SAMPAs and format them for sending out (Optical connection)
- Output data Rate (no header included)
  - 1.42Gbps/FEE for 30<r<40cm, 1.45Gbps/FEE for 40<r<60cm, 0.77Gbps/FEE for 60<r<80cm
  - ➔28Gbps/(1/12 full azimuth)
- Direct plug-in to the backside of the pad plane





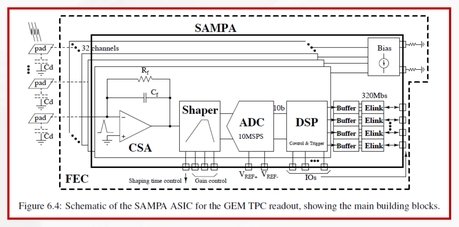
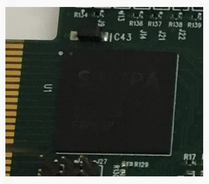


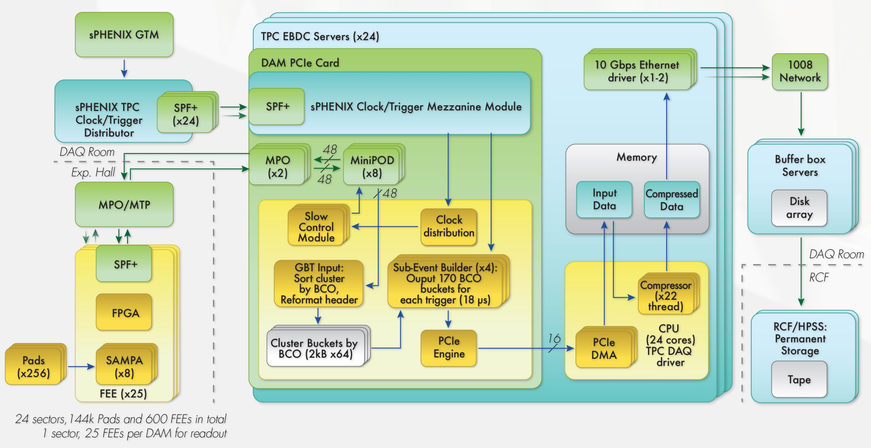
Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

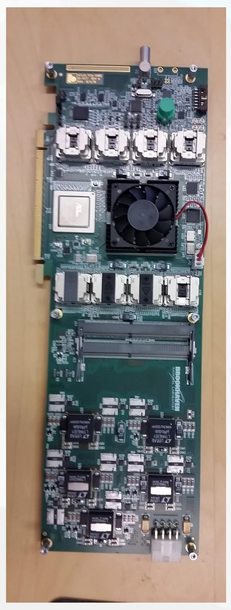
Chip size: 1.5cmx1.5cm



DAM + EBDC

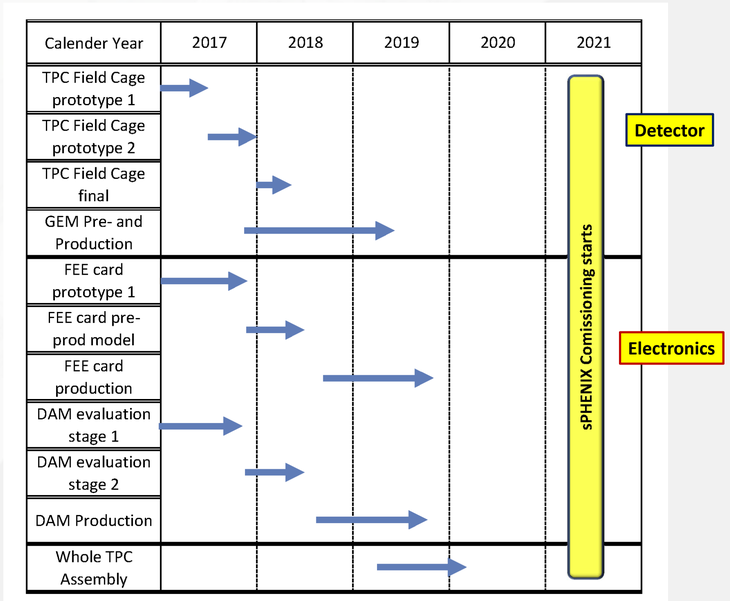
- DAM will be a PCIe Gen3 x16 card plugged into a PC (EBDC server).
- We base on FELIX card developed for the ATLAS experiment
  - Similar scheme and function as ALICE CRU
- One DAM + EBDC will take care of 25 FEEs
  - corresponding to 1/12 of full azimuth ≡ one sector. 24 DAMs + EBDCs in total for both ends.
- Bidirectional optical connection
  - Average continuous rate: 28Gbps/sector (1.45Gbps/fiber is the maximum)
  - Downlink fiber send clock and slow control to FEEs
- FPGA will buffer the data input and align with Beam Clock
  - FGPA will also take trigger and pick corresponding portion of the data
  - Once minimum data reduction is performed, the data will be sent to EBDC server by DMA.
  - Demonstrated rate limit for FELIX (PCIe x16) = 100 Gbps
  - Enough band width for maximum average continuous rate (28 Gbps)
- Planning to perform multithread compression for further reduction of data
  - Algorithm: LZO on multi-event chunks
  - Demonstrated compression ratio = 60%





Schedule and Summary

- sPHENIX will start its commissioning in Apr 2021, and have physics runs from 2022.
- Readout development is ~3-year project
- We are now developing the prototype of FEE and DAM+EBDC
- We welcome people for this interesting project!



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