The new Inner Tracking System of the ALICE experiment

Paolo Martinengo – CERN

on behalf of the ALICE Collaboration

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The new ALICE Inner Tracking System

OUTLINE

• Motivations and Experimental Strategy
• Design Objectives and Layout
• Selected topics from the R&D
• Construction and Integration Schedule
• Conclusions
ALICE Upgrade – From observation to precision measurement

In March 2013 a new physics programme for ALICE was approved

Physics Goal ➔ high-precision measurements of QGP properties

- Open HF (charm & beauty, mesons & baryons), Quarkonia down to zero $p_T$
  - thermalisation, hadronization, recombination, temperature evolution of the QGP
- Vector mesons and low-mass di-leptons
  - chiral symmetry restoration, virtual thermal photons
- High-precision measurement of light (anti-)nuclei and hyper-nuclei
  - nucleosynthesis, exotics
- and more
Main requirements for the new Inner Tracking System:

- High tracking efficiency and resolution at low $p_T \ (60\% \ @ \ 100 \ MeV/c)$
  
  Increase granularity, reduce material thickness

- Excellent secondary vertex resolution ($\Lambda_c \ c\tau \sim 60 \ \mu m$)
  
  Move closer to Interaction Point (IP), new beam pipe, smaller diameter

- High-statistics, un-triggered data sample ( $\geq 10 \ nb^{-1} \ Pb-Pb$)
  
  Increase readout rate, reduce data size (online data reduction)
New ITS Design Objectives

1. Improve impact parameter resolution by a factor of 3 (5) in $r\varphi$ ($z$) @ $p_T = 500$ MeV/c
   • Get closer to IP (position of first layer): 39 mm ➔ 23 mm
   • Reduce $x/X_0$ /layer: $\sim 1.14\%$ ➔ $\sim 0.3\%$ (for the 3 innermost layers)
   • Spatial resolution: currently 12 µm x 100 µm (SPD) ➔ 5 µm x 5 µm

2. Improve tracking efficiency and $p_T$ resolution at low $p_T$
   • Increase granularity:
     • 6 layers ➔ 7 layers
     • silicon pixel, drift and strip ➔ all-pixels

3. Exploit LHC luminosity increase ➔ fast readout
   • readout Pb-Pb interactions up to 100 kHz, i.e. 2 x expected peak luminosity after LS2 (currently limited at 1kHz)

4. Withstand radiation load (10 years operation):
   • TID: $\sim 270$ krad, NIEL: $\sim 1.7\times10^{12}$ 1MeV $n_{eq}$ / cm²

5. Reliability ➔ fast insertion/removal for yearly maintenance
   • possibility to access faulty components during yearly shutdown
     ➔ Services (power, cooling, R/O) connected only on one side
Layout of the new ITS

7-layer barrel geometry, fully equipped (~24000 chips) with dedicated **MAPS:**

**ALice Piixel DEtector (ALPIDE)**

r-coverage: 23 – 400 mm

η coverage: |η| ≤ 1.3

**Monolithic Active Pixel Sensors**

Material /layer: 0.3% $X_0$ (IB), 1% $X_0$ (OB)

12.5 G-pixel camera (~10 m² active Si)
Binary read-out
Performance of new ITS (MC simulations)

Cellular automaton, i.e. online tracking & vertexing mandatory in Run3, 1.1 TB/s of data (ITS 40 GB/s)

poster by Maximiliano Puccio

Impact parameter resolution

40 μm at $p_T = 500$ MeV/c

Tracking efficiency (ITS standalone)

~60% at $p_T = 100$ MeV/c
B± not accessible with the present ITS

Measure energy loss for b, quantitative verification of $\Delta E_c > \Delta E_b$ vs. $p_T$
Physics performance with the new ITS (MonteCarlo)

\( \Lambda_c \) not accessible (in Pb-Pb) with the present ITS
\( \nu_2 \) measurement possible with the new one

Large improvement also for \( D^0 \) & \( D_s \) signals, possibility to discriminate between thermal and coalescence hadronization models
Huge R&D effort started 6 years ago

- Simulation
- Pixel sensor, connectivity
- Cooling, power distribution
- Read-out chain
- Assembly tools & procedure
- Construction database
- Mechanical support (carbon fiber)
- Integration in ALICE
- and more

First prototype usually does not meet all requirements
ALPIDE – Technology and Pixel Layout

Pixel Sensor using TowerJazz 0.18 μm CMOS Imaging Process

Deep PWELL shields NWELL of PMOS transistors (full CMOS circuitry within pixel active area)

In-pixel:
- Amplification
- Discrimination
- 3-hit storage register (MEB)
- In-matrix sparsification

Reverse bias voltage (-6 V < V_{BB} < 0 V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode

Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (~fF)

High-resistivity (> 1 kΩ cm) p-type epitaxial layer (25 μm) on p-type substrate

MFT based on the same chip

Poster by A. Uras
**ALPIDE – Final Version**

**Production started Dec 2016, to be completed by Dec 2017**

Key features:

- Dimensions: 30 mm x 15 mm
- Pixel pitch: 29 µm x 27 µm
- Ultra-low power (entire chip): ~40 mW/cm², (requirement < 100 mW/cm²) 140 mW full chip
- Triggered acquisition (200 kHz Pb-Pb, 1 MHz pp) or continuous (progr. integration time: 1µs - ∞)

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8/02/2017

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ALPIDE – Detection Efficiency and Fake-Hit Rate

- Big operational margin with only 10 masked pixels (0.002%), **fake-hit rate < $$10^{-10}$$ pixel/event** (requirement < $$10^{-6}$$)
- Chip-to-chip fluctuations negligible
- Non-irradiated and NIEL/TID chips show similar performance
- Sufficient operational margin after 10x lifetime NIEL dose

**Availability and excellent support from test beam facilities all around the world**
- BTF Frascati, CERN, DESY, Pohang/Korea, SLRI/Thailand
- has been a key factor for the success of the development of the chip
• Chip-to-chip fluctuations negligible
• Non-irradiated and TID/NIEL chips show similar performance
• Resolution of about 5µm at a threshold of 200 electrons
• Sufficient operational margin even after 10x lifetime NIEL dose
Detector Barrel Staves

1500 mm length
80 gr weight
cooling integrated in C fiber support
Stave Layout

**Inner Barrel**
- Flexible PCB
- 9 sensors
- Cold Plate
- Space Frame

**Outer Barrel**
- Power Bus
- 2x7 sensors
- Cold Plate
- Space Frame
- Half-stave

**FPC side**
- 2x7 chips
- Length 245 mm
- x-cables for connection to power bus

**Sensor side**
- 9 chips, stave length ~450 mm
- Sensors thinned to 50µm
Prototype series of Inner Barrel and Outer Barrel HICs Staves with pALPIDE-3

- Characterization with different modes of operation, readout rates and environmental conditions (power supply and temperature)
- Sensor performance comparable to standalone chip
- Pre-series production with ALPIDE chips starting now

X-ray ($^{55}$Fe) image of IB HIC (radiography of 3 sensors)

Outer Barrel HIC – threshold measurements
Chip series test and Hybrid Integrated Circuit (HIC) assembly

Machines installed at production sites, training started

ALICIA (IBS)
6 machines (+1 MFT)
(Chip probe testing & HIC assembly)

ALICIA = ALice Integrated Circuit Inspection and Assembly

Korea-YS01 (C-On)
1 machine
(mass chip probe testing)
24000 chips needed
+ MFT & spares
• Communication between detector (ALPIDE) and off-detector electronics via SAMTEC firefly cables
• Distribution of CLK and slow-control at 40MHz
• Data readout at 1.2Gb/s (IB) & 0.4Gb/s (OB)

ALPIDE will be the only electronics component around the Interaction Point, the off-detector electronics will sit 5 m away

Eye diagram of signal propagated over 5m-long cable
Measured BER (no errors over 14 h) < 1.6 \times 10^{-14}
Overall ITS Planning (Simplified Global View)

Sensor: Production started
HIC: EDR ok, PRR in March
Mechanics: PRR passed
R/O: EDR ok, PRR end ’17
Cooling: PRR passed

EDR = Engineering Design Review
PRR = Production Readiness Review
Conclusions

• The new ALICE Inner Tracking System project has successfully completed the R&D phase

• All requirements have been met or even exceeded

• With the start of the production of the ALPIDE sensor a major milestone was achieved

• Production sites are equipped with custom machines for test & assembly

• Detector production will enter full swing during 2017

• The project is well on track for installation starting middle 2020
Posters related to the upgrade

#348, “Performance evaluation of Si PAD detector for the ALICE FoCal development” by Tomoko Sakamoto
#454 “Prospects for ALICE physics with the Muon Spectrometer Upgrade and the new MFT” by Antonio Uras
#247, “Detector Control System of the new Muon Forward Tracker at ALICE” by Kenta Shigaki
#543 “A Cellular Automaton tracking algorithm for the Upgrade of the ITS of ALICE” by Maximiliano Puccio
#437, “The new Fast Interaction Trigger detector for the ALICE Upgrade” by Wladyslaw Henryk Trzaska
#442, “Forward high granularity electromagnetic calorimeter for direct photon measurements at LHC” by Hongkai Wang

Posters related to the present detectors

#171, “Performance of ALICE EMCal and DCal in Electron Identification” by Erin Frances Gauger
#324, “Space-charge distortions in the ALICE TPC in LHC RUN 2” by Ernst Hellbar
#474, “Calibration and Performance of EMCal and DCAL Detectors at ALICE” by Justin Thomas Blair
SPARES
ALICE ITS Upgrade – entirely new, all-pixel detector, after LS2

Central Barrel Tracking
- Silicon: 39 – 430 mm
- Gas (TPC, TRD): 88 – 368 cm

Readout rate is currently limited by TPC and ITS (SDD)
~ 1kHz for Pb-Pb
All chips show the same correlation
Neither irradiation nor settings influence the correlation
At low cluster size, the loss of detection efficiency leads to a deterioration
Cluster size can be used to infer position resolution
ALPIDE – Technology and Pixel Layout

- **Full-scale prototype:** 1024 x 512
- 4 sectors with pixels variants
- Pixel pitch: 28µm x 28µm
- 1 register/pixel, no final interface

- 4 sectors with pixels variants
- Optimization of in-pixel and peripheral circuits
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)

- **8 sectors with pixel variants, 3 registers / pixel**
- All final features, including 1.2 Gbit/s data serial output

Main changes wrt pALPIDE-3
- Full matrix with same pixel type
- Time skew of global signals
- Improved protection against SEUs
- Improvement of PLL \( \Rightarrow \) High-speed Serial Output
R&D on Pixel Chip to FPC Interconnection – Selective Laser Soldering

**Laser soldering**: connection of Pixel chip to flexible printed circuit

R&D addressed:
- Geometry of the interconnection
- soldering ball, interface pad and VIA
- laser beam profile and power time profile

All process main issues were solved
More time needed to bring the process to a steady single interconnection yield of ~99.99%
Remains a very promising interconnection technology for future applications
FPC to Chip interconnection – Wire Bonding

Flexible Printed Circuit (FPC) cross section

- solder mask
- aluminum (IB) / copper (OB)
- polyimide
- aluminum (IB) / copper (OB)
- solder mask

Flexible Printed Circuit (FPC) to Chip interconnection – Wire Bonding

- solder mask
- aluminum (IB) / copper (OB)
- polyimide
- aluminum (IB) / copper (OB)
- solder mask

Droplets of glue (epoxy resin) dispensed on the FPC

chip pads aligned to FPC VIAs

FPC to Chip interconnection (Al wire bonding)
Hybrid Integrated Circuits (HIC) and Stave Prototypes

Stave temperature measurements while powering on stave in two steps
1) Power on (with CLK): ~ 80 mW digital + 20 mW analogue / chip
2) Activation of high-speed serial output (DTU): ~ 160 mW digital + 20 mW analogue / chip
Inner Barrel Stave Mechanics & Cooling

Coolant: H₂O, leak-less
Sensor temperature < 30°C
Temperature non-uniformity < 5°C

W = 100 mW / cm² (> x2 nominal), H₂O flow rate = 3 Lh⁻¹

Tin=15.8°C
Tout=16.6 °C

Max T periph=18.5°
Outer Barrel Stave Mechanics & Cooling

- Power bus
- FPC
- 2x7 sensors
- Cold Plate

~1500mm length
~80gram weight

- Single-phase H₂O leak-less
- Temperature < 30°C
- Non-uniformity < 5°C
- Dissipation < 100mW/cm²

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Inner Detector Barrel

3 half-layers are connected together to form half-barrel
An outer Cylindrical Structural Shell (CYSS) connects the opposite end-wheels of and avoids external loads are transferred to Staves

The end-wheels, ensure precise positioning of staves in a layer

Each barrel is divided into two halves, which are mounted separately around the beam pipe
Outer Detector Barrel

Service Barrel

Conical Structural Shell

3310mm

Stave

Outer Detector Half Barrel

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Readout Electronics - Architecture

Detector Readout ➔ 192 READOUT UNIT

Inner layer (0,1,2)
- 0.6 (1.2) Gb/s high speed data,
- 80 Mb/s clock and control

Outer layers (3,4,5,6)
- 400 Mb/s high speed data,
- 80 Mb/s clock and control

Central Trigger Processor
- One way, passive optical splitting, no busy back

GBT optical
- Trigger

Each Readout Unit is connected to one stave both for Inner and Outer Barrels

Common Readout Unit & O2

Identical Readout Units (RU) cover the full ITS

GBT optical
- Control
- Data (9.6 Gb/s max)

Control
- Clock
- Data (320 Mb/s max)

Data (960 Mb/s max)
Prototype Readout Unit – 2015

- Based on SRAM FPGA (Xilinx Kintex7) + GBTx FMC (daughter board)
- Extensive use of radiation mitigation techniques
  - Communication with Trigger and DAQ via GBT link validated
  - Communication with sensors via high-speed copper serial links validated

Radiation induced fault rates
- Intensive SEU test campaigns:
  - MTBF/device: ~2400 hours ($10^9$ h/cm$^2$)
  - MTBF/entire system: ~12 beam hours
  - System downtime $\sim 10^{-5}$
## Pixel Chip Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Inner Barrel</th>
<th>Outer Barrel</th>
<th>ALPIDE*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon thickness</td>
<td>50μm</td>
<td>100μm</td>
<td></td>
</tr>
<tr>
<td>Spatial resolution</td>
<td>5μm</td>
<td>10μm</td>
<td>~5μm</td>
</tr>
<tr>
<td>Chip dimension</td>
<td>15mm x 30mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power density</td>
<td>&lt; 300mW/cm²</td>
<td>&lt; 100mW/cm²</td>
<td>&lt; 40mW/cm²</td>
</tr>
<tr>
<td>Event time resolution</td>
<td>&lt; 30μs</td>
<td></td>
<td>&lt;10μs</td>
</tr>
<tr>
<td>Detection efficiency</td>
<td>&gt; 99%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fake hit rate **</td>
<td>&lt; 10⁻⁶/event/pixel</td>
<td></td>
<td>&lt;&lt;&lt; 10⁻⁶/event/pixel</td>
</tr>
<tr>
<td>NIEL radiation tolerance ***</td>
<td>1.7x10¹³ 1MeV n_eq/cm²</td>
<td>10¹² 1MeV n_eq/cm²</td>
<td></td>
</tr>
<tr>
<td>TID radiation tolerance ***</td>
<td>2.7Mrad</td>
<td>100krad</td>
<td></td>
</tr>
</tbody>
</table>

* extrapolation of the ALPIDE performance based on prototype results

** revised numbers w.r.t. TDR

*** including a safety factor of 10, revised numbers w.r.t. TDR