

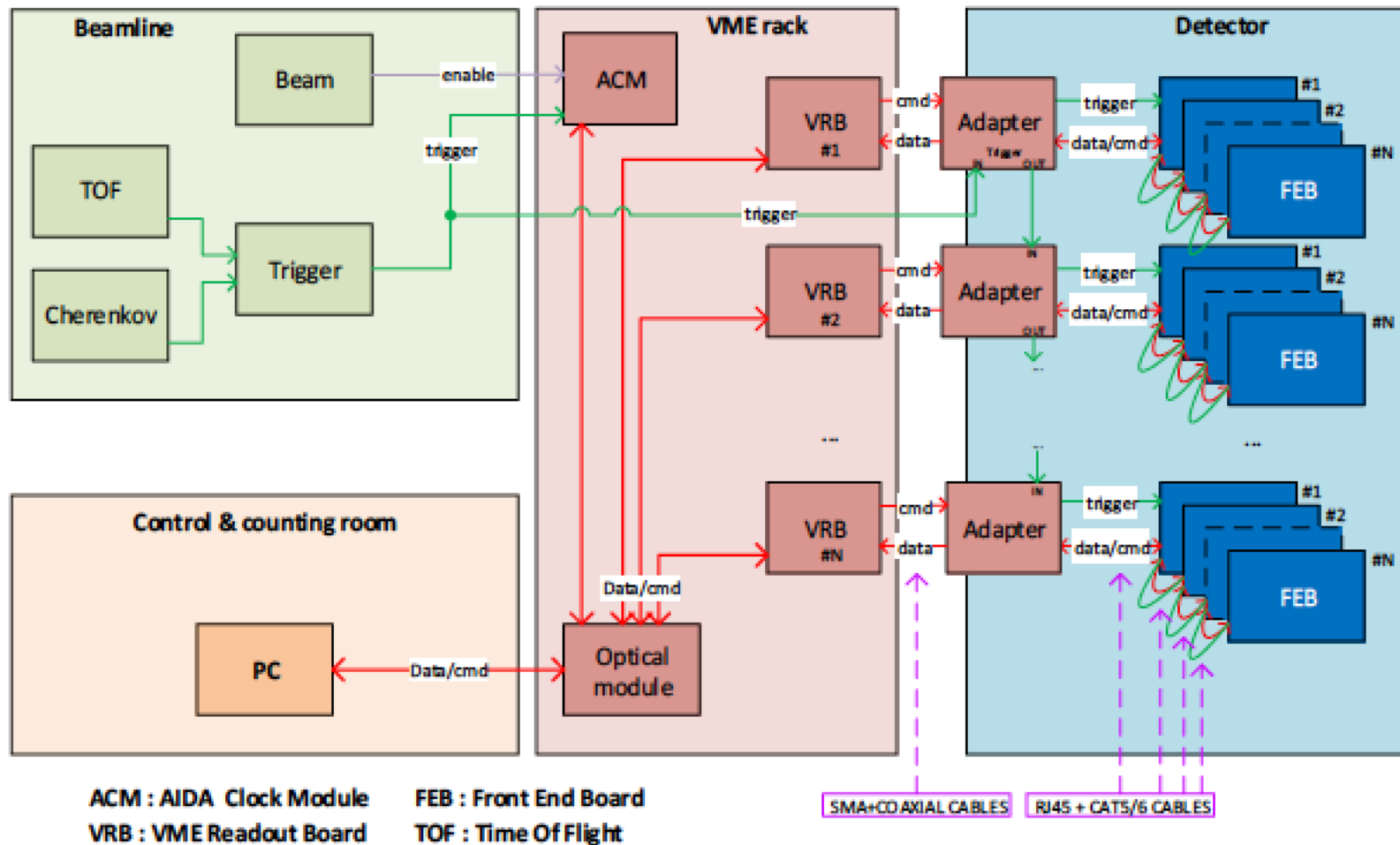


Electronics update

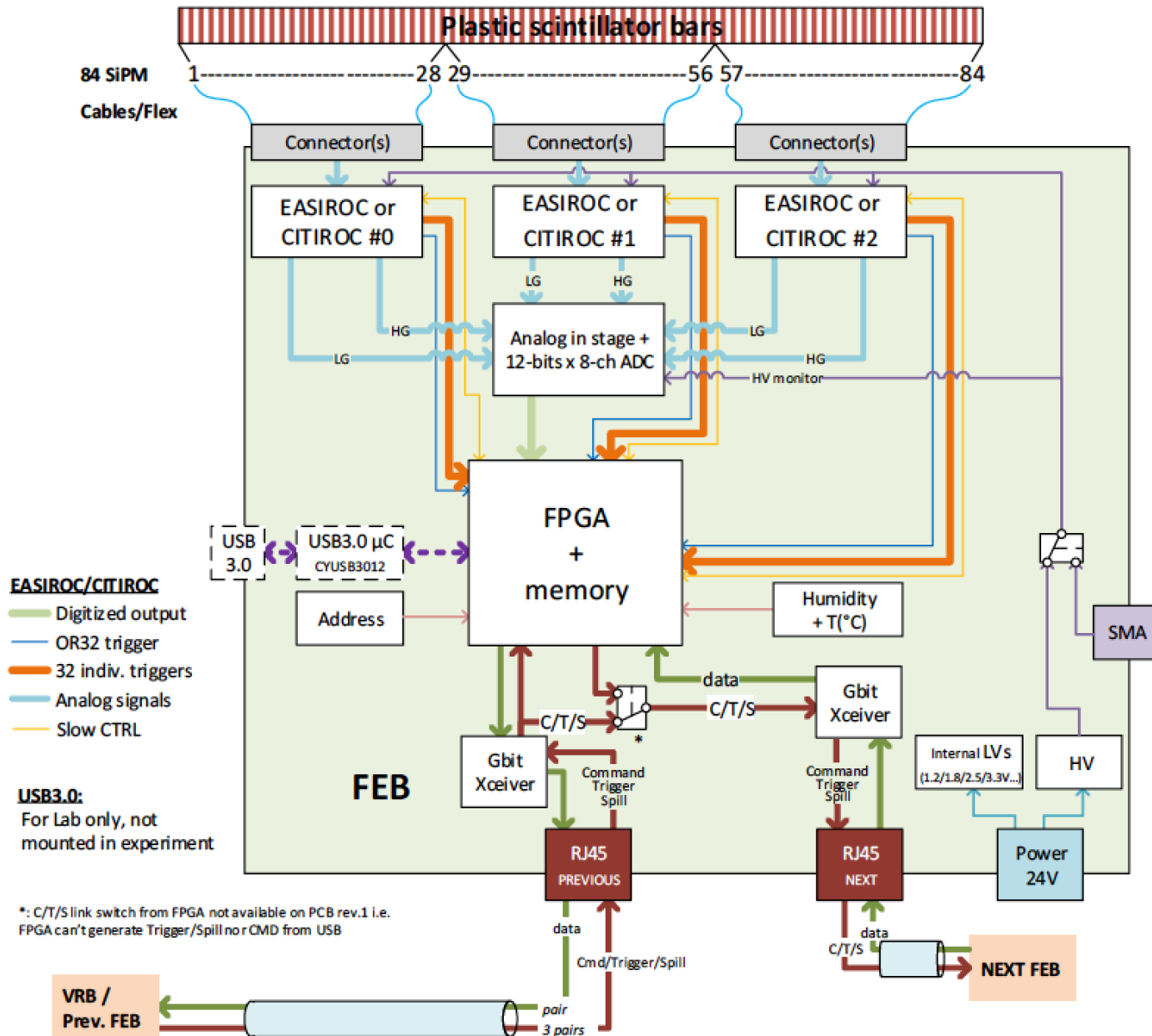
E. Noah, A. Blondel, Y. Favre, R.
Tsenov

29 July 2015

Baby MIND electronics chain



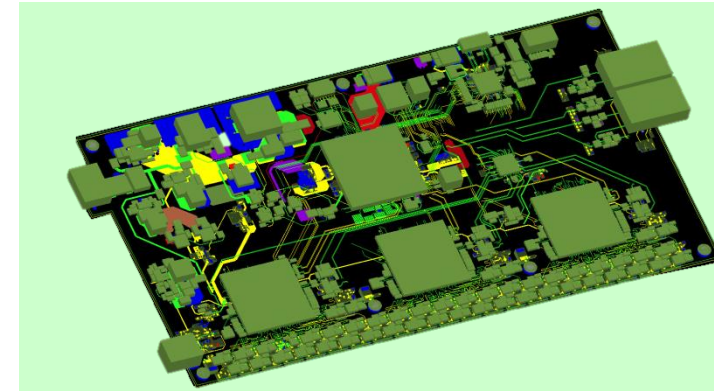
Baby MIND FEB sketch



Baby MIND FEB

■ FEB characteristics :

- 96 SiPM channels (mini coax. connectors), 84 used for Baby MIND
- 3 CITIROC ASICs (32 ch charge ampl., trigs, ext. common HV + independent 0/4V)
- 12-bits 8-ch ADC 40Ms/s/ch
- 2 x 6Gb/s transceiver (800Mb/s for Baby MIND)
- USB3.0 (5Gb/s) μ C for lab, calib. & maintenance
- LV & HV power supplies
- Altera ARIA 5 FPGA (mid-range), firmware :
 - 84 ch. Timing meas (2/2.5ns resolution)
 - Charge meas. (from 12-bits ADC)
 - Baseline computation (filtering)
 - USB3.0 gateway
 - Gigabit protocol for readout (exp.)



- PCB:
 - 8 layers
 - 120 μ m space/width lines
 - Impedance & length control (TDC)
- Schedule:
 - First **prototype FEB 11 March 2015**
 - **Firmware** development ongoing
 - **~ 30 Baby MIND FEBs Dec. 2015**

Baby MIND FEB (Photo by Y. Favre 12 March 2015)



- Detailed and well documented architecture
- **Large fraction** of firmware is **written**
 - **USB3** connectivity tested to **2.5 Gbit/s**
 - **CITIROC ASIC** configuration **untested**
- **Firmware versions:**
 - First version of firmware allows for **charge readout** – *end Aug. 2015*
 - Second version of firmward allows for **charge and timestamp** – *end Sept. 2015*

Tests with CITIROC Evaluation Board

Photosensors

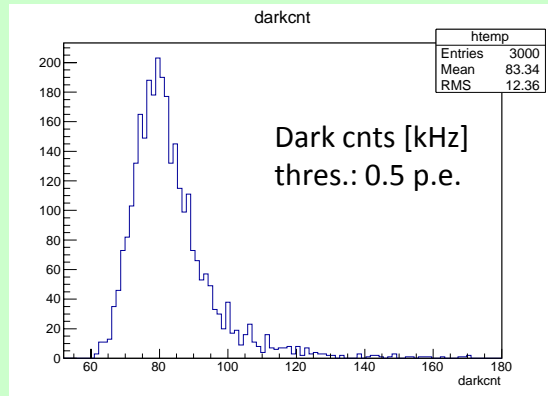
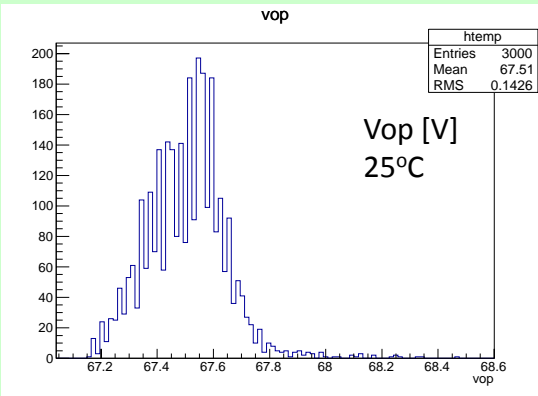
Options tested:

- MPPC/ASD40/KETEK/SensL
- Several MPPC variants

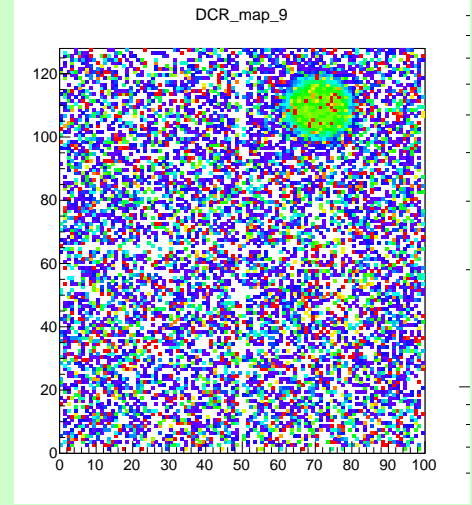
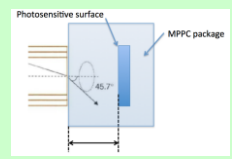
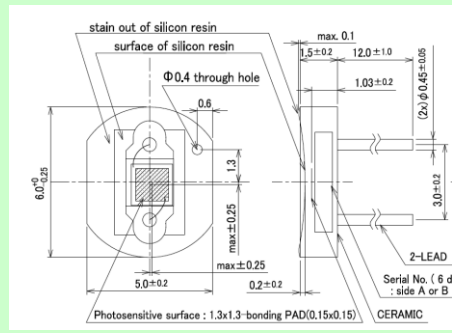
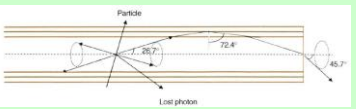
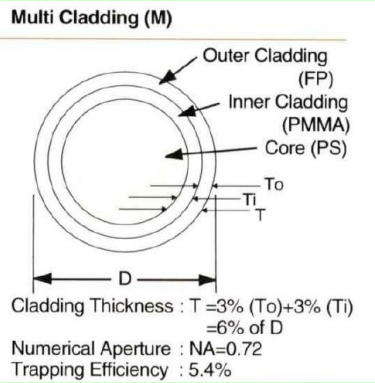
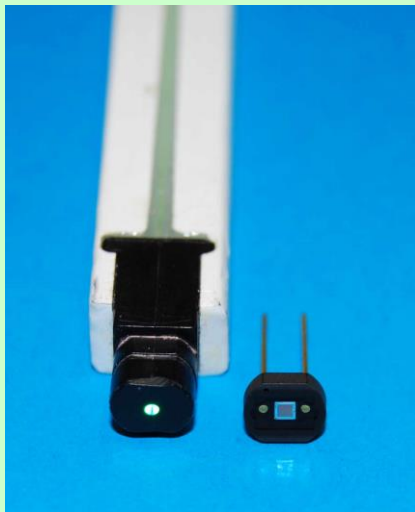
Selection:

- Hamamatsu MPPC S12571-025C
- $1 \times 1 \text{ mm}^2$
- $25 \mu\text{m}$ cell size
- **3000** delivered by **6 Mar. 2015**

MPPC test data by Hamamatsu

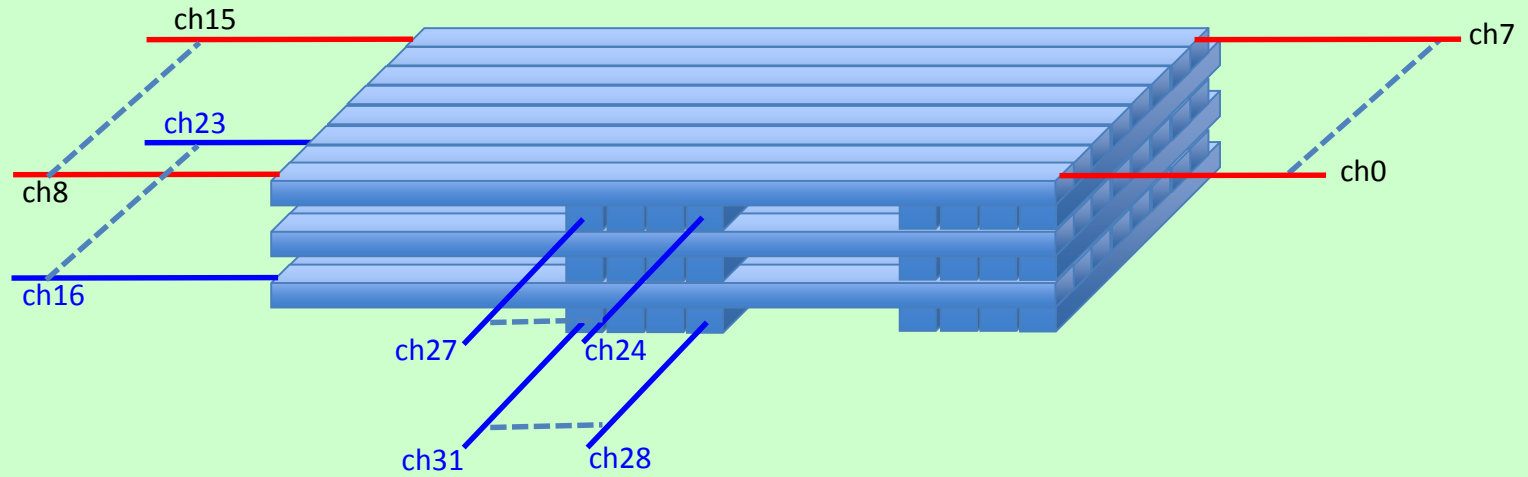


WLS fiber and MPPC alignment

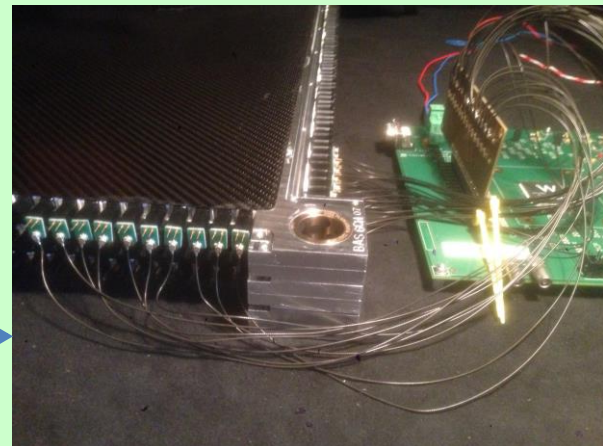


Bar light yield test: post module assembly

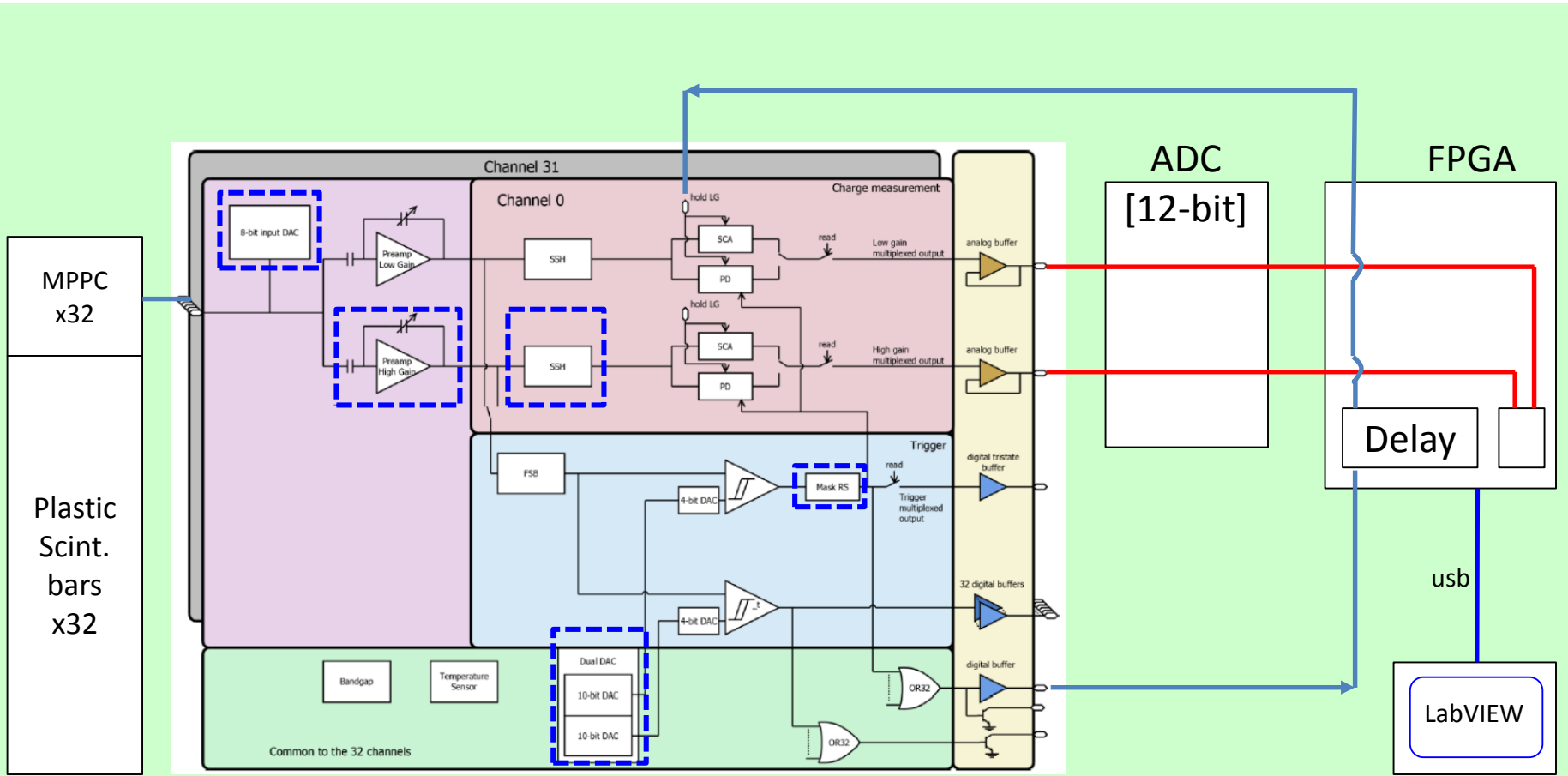
Channel configuration: channels under test ch0-15



Setup in dark room



Module characterisation with CITIROC evaluation board



CITIROC shaper time constant

12.5 ns

25 ns

37.5 ns

50 ns

62.5 ns

75 ns

87.5 ns

10 ns

20 ns

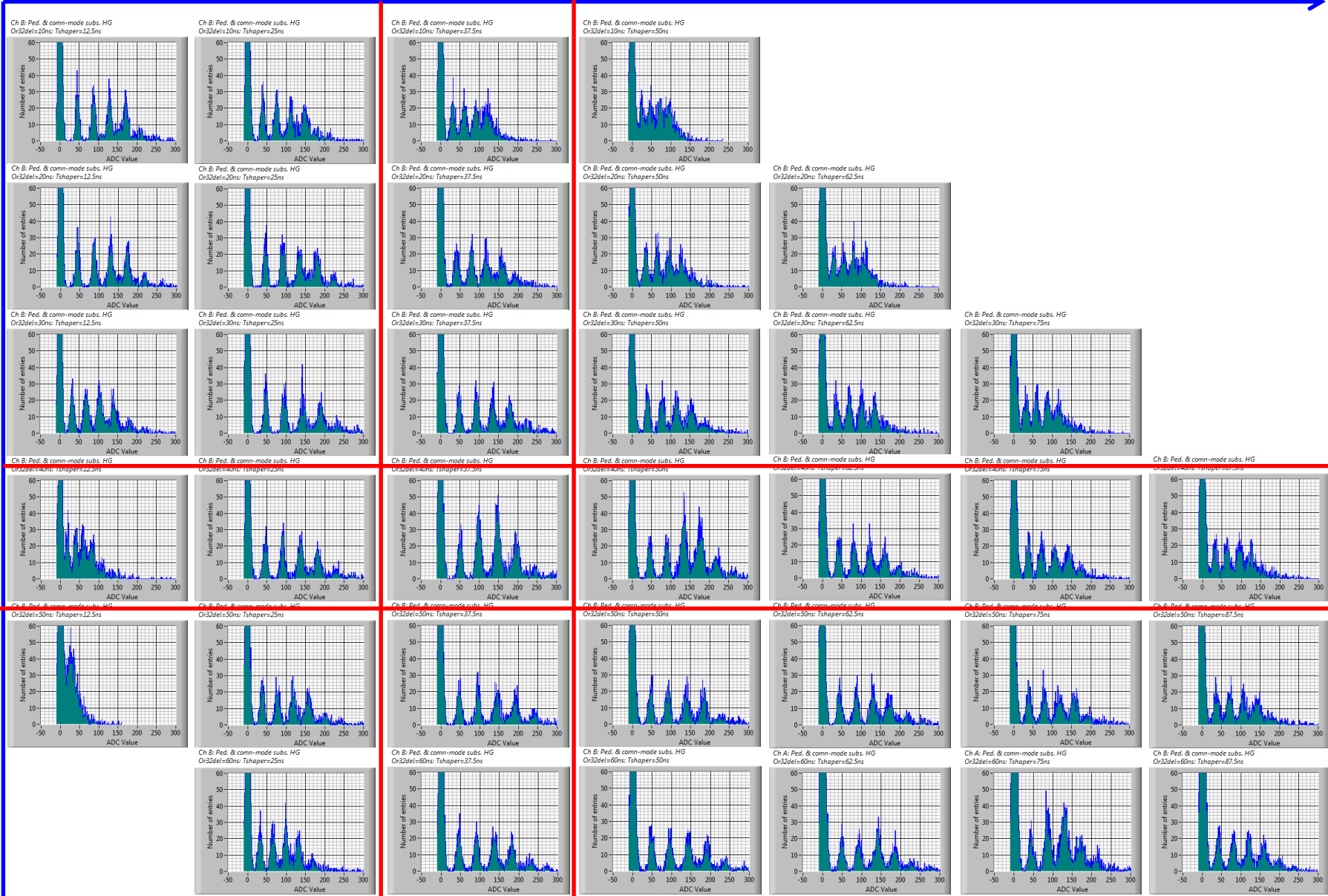
30 ns

40 ns

50 ns

60 ns

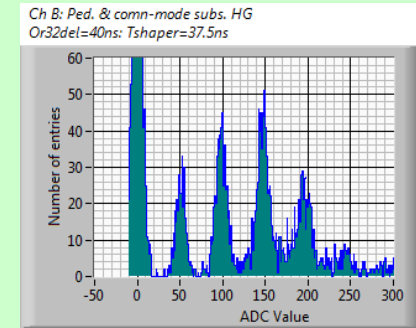
OR32/hold delay



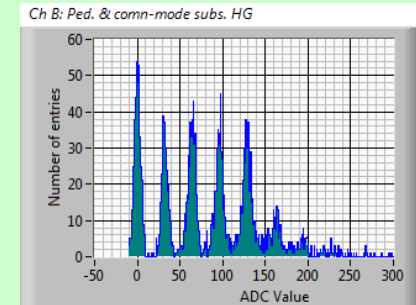
Varying Pre-amp Feedback capacitance

- Regime:
 - high enough gain to resolve individual p.e. peaks
whilst avoiding saturation
- Dynamic range (HG):
 - 12-bit ADC
 - Baseline ~ 950
 - 19.3 ADC/p.e.
 - 160 p.e.
- > 1600 p.e. with LG.

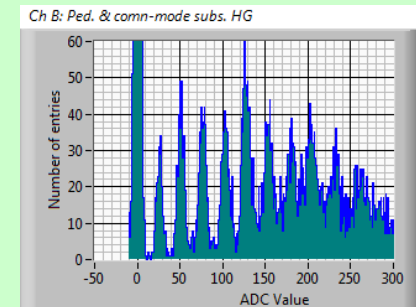
Feedback capa.
= 1 [arb.]
48.2 ADC/p.e.



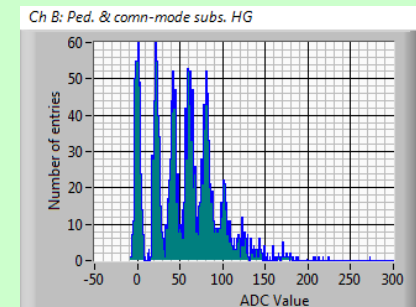
Feedback capa.
= 4 [arb.]
32.2 ADC/p.e.



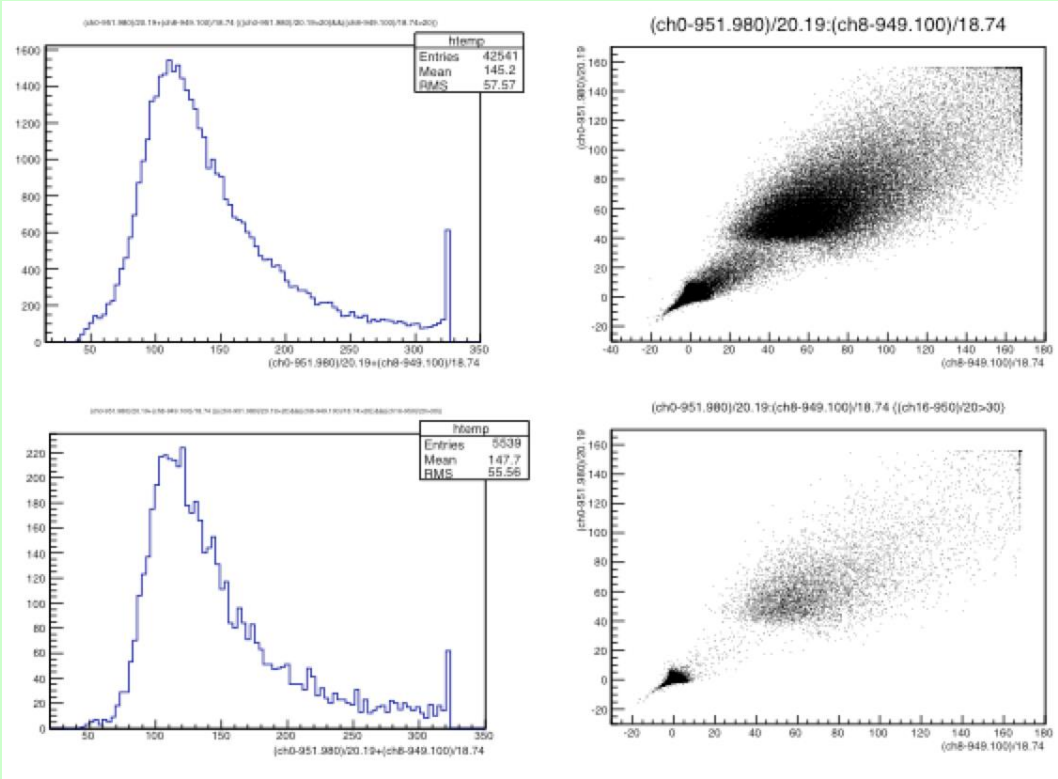
Feedback capa.
= 6 [arb.]
25.6 ADC/p.e.



Feedback capa.
= 8 [arb.]
19.3 ADC/p.e.

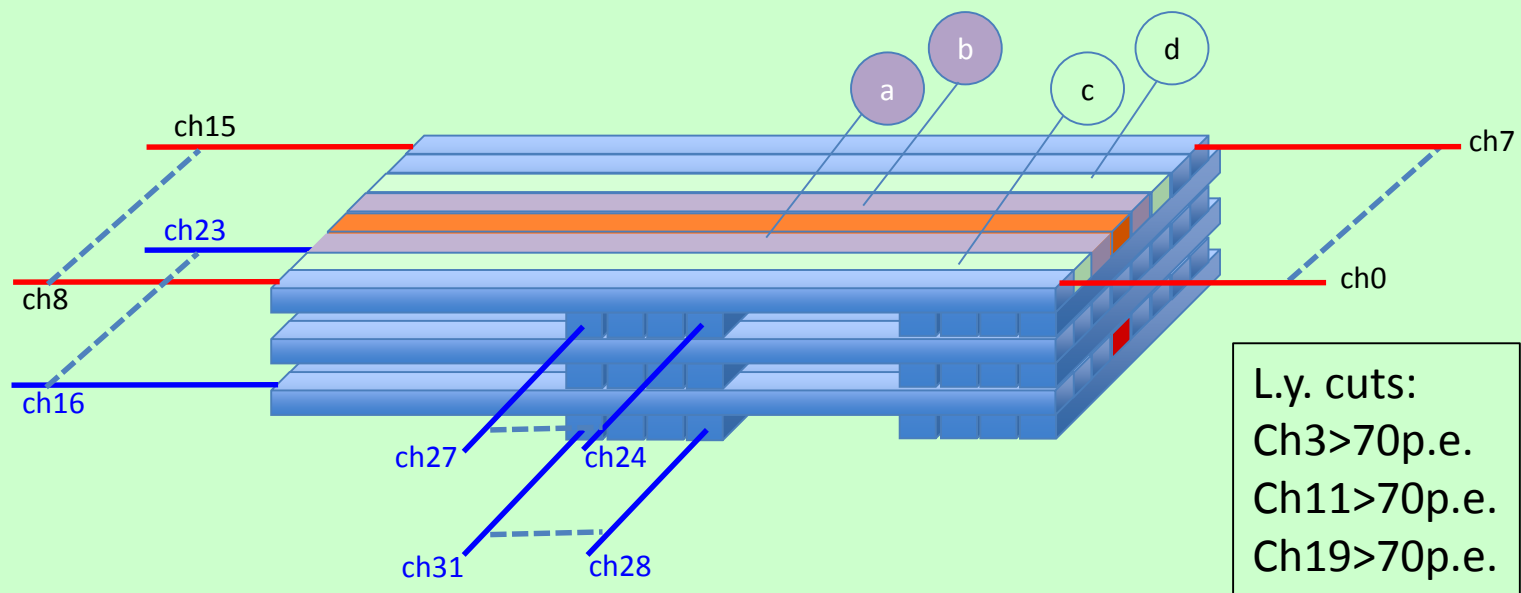


Light yield: sum of both ends of bar

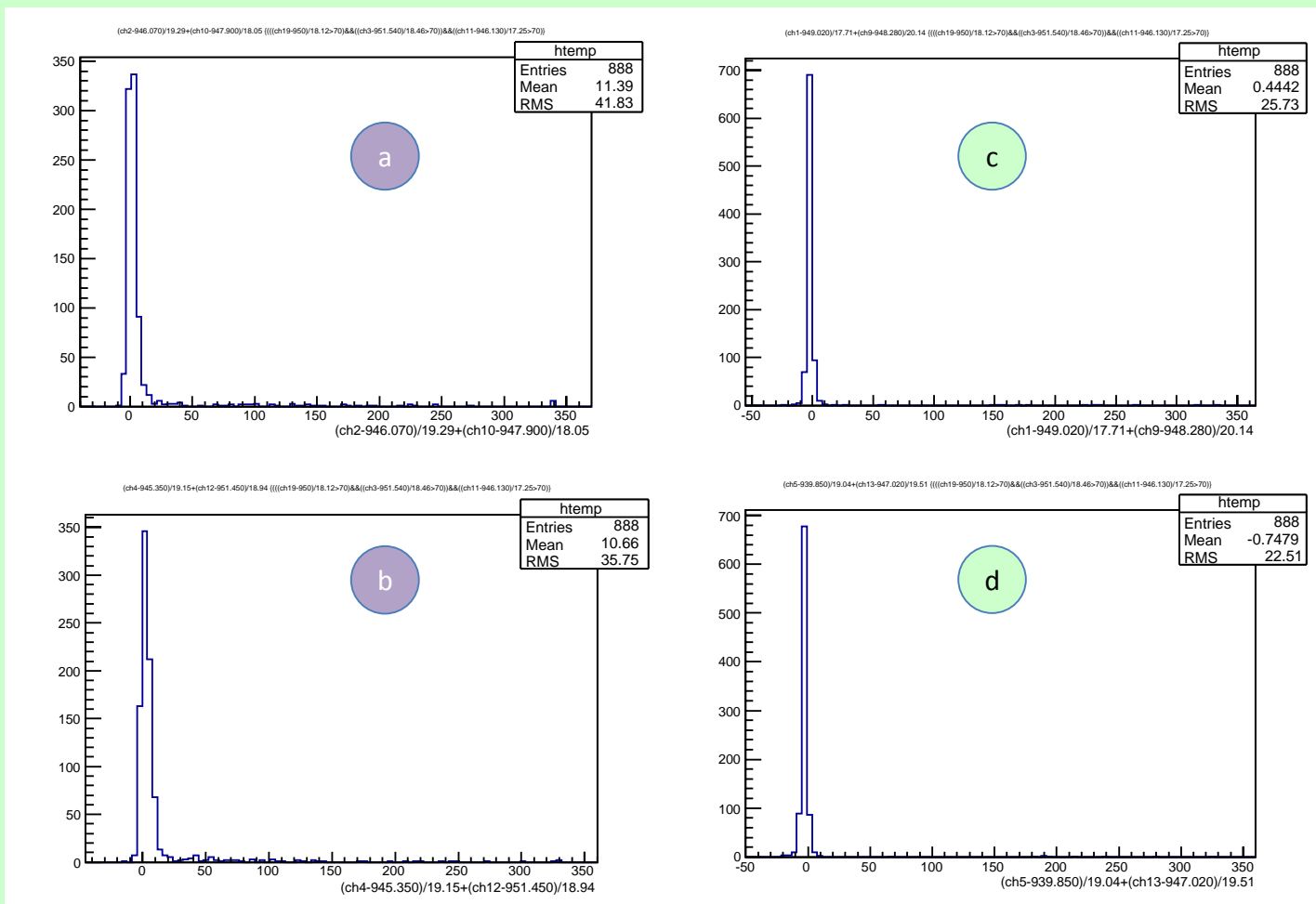


Bar pos. [#]	Bar ID [#]	Bar INR [p.e.]	Module [p.e.]
1	6421	124.4	145.2
2	6411	125.4	155.4
3	6422	119.0	138.7
4	6410	134.6	153.6
5	6414	112.9	142.5
6	6409	118.6	136.6
7	6412	129.4	146.2
8	6413	119.0	183

“Optical” crosstalk: light yield in adjacent bars



“Optical” crosstalk: l.y. sum of both ends collected in adjacent bars



- Electronics-related work proceeding with two cards:
 - The **Baby MIND FEB**: firmware writing, first version end of August will do charge only
 - The **CITIROC evaluation board**: exploration of range of configuration parameters for the CITIROC