Design & test of SciFi FEB

- Overview SciFi Read Out Box
- PCBs in a ROB
- TFC/ECS distribution
- Data path
- PCB design
- Master Board tests

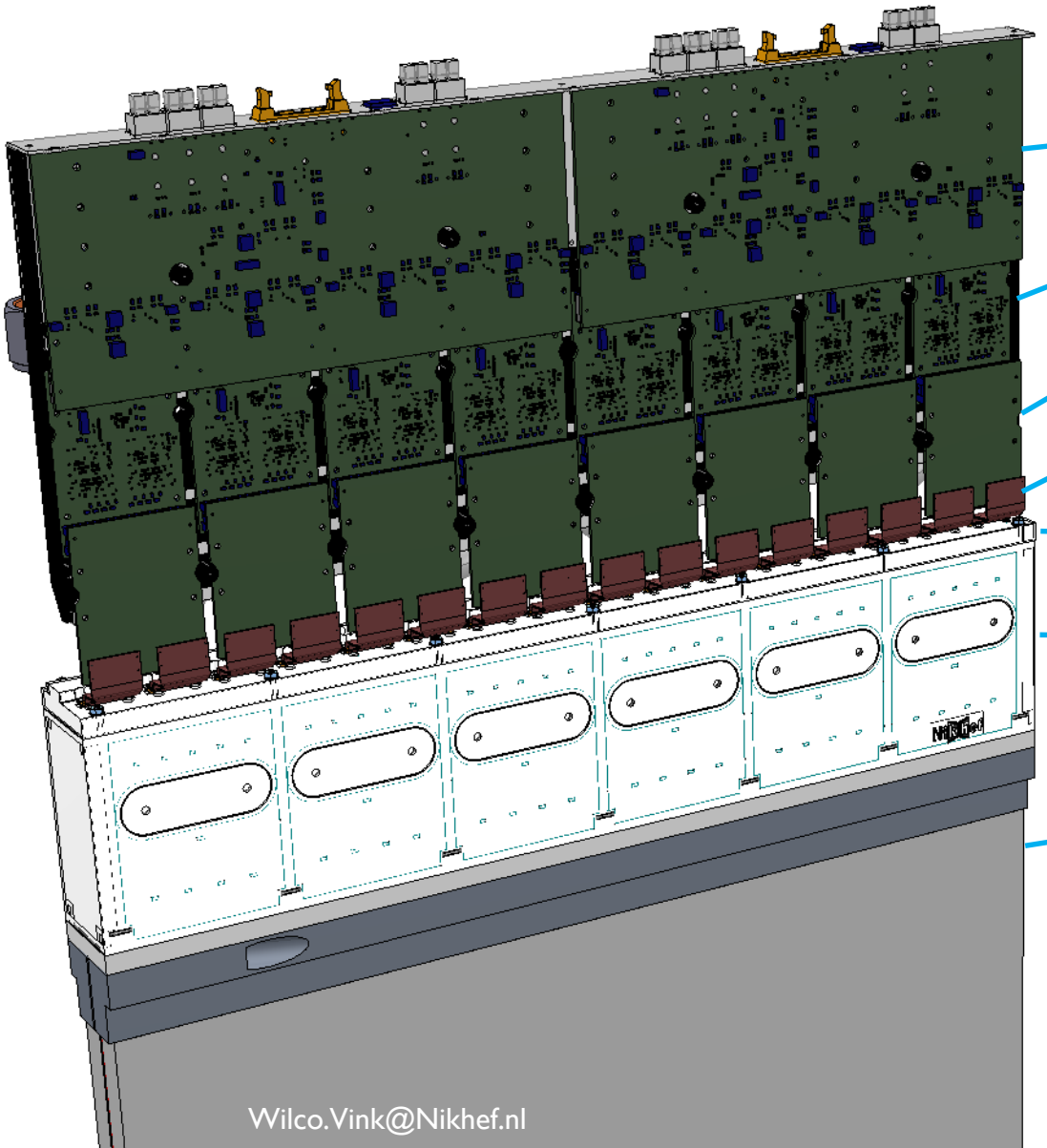
LHCb Upgrade electronics meeting

3 September 2015

Ad Berkien, Cairo Caplan(CBPF), Mauricio Feo(CBPF)

Charles Ietswaard, Antonio Pellegrino, Hans Verkooijen, Wilco Vink, Rob Walet,

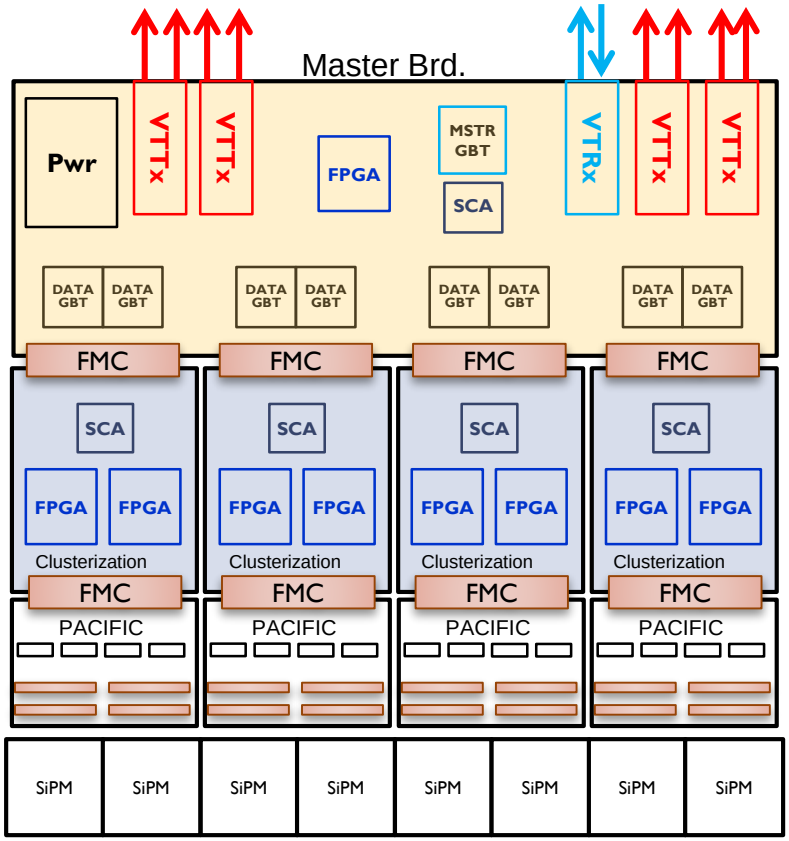
SciFi Read Out Box (ROB)



- Electronics
  - Master Brd.
  - Clusterization Brd.
  - PACIFIC Brd.
- SiPM modules
- Cold box top cover
- Cold box
- Scintillating Fibers

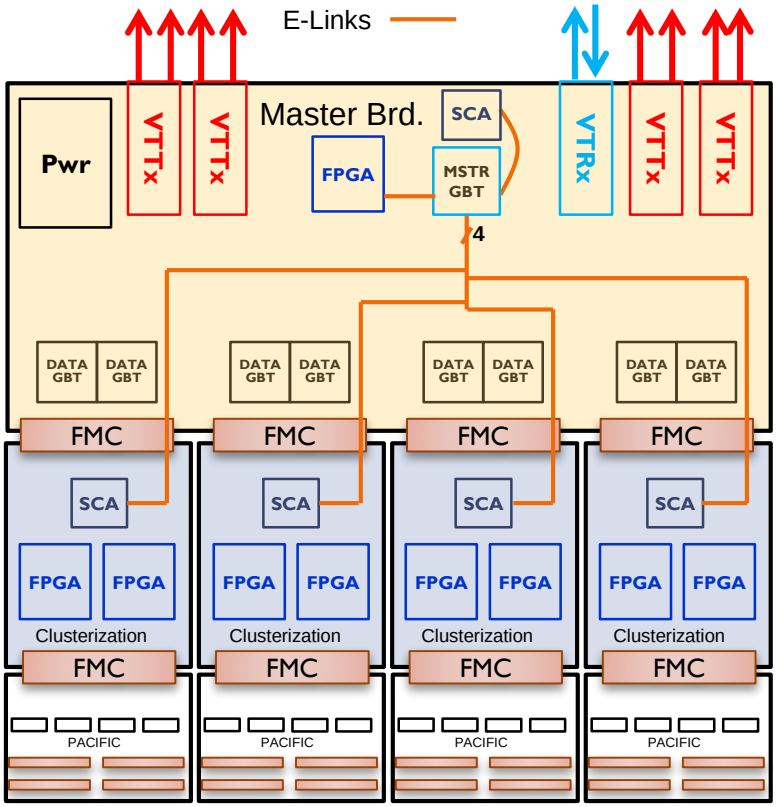
PCBs in a ½ ROB

- Master Board
  - Master GBT → TFC/ ECS distribution
  - Data GBTs → Data serialisation
  - Power supplies
  - Versatile link optical components
- Clusterization board
  - Clustering FPGAs
  - SCA for slow controls → Clusterization FPGAs and PACIFIC ASICs
- PACIFIC Board
  - Amplifier, shaper and ADCs, 2b/channel output based on three threshold values
- SiPM: Silicon Photo Multiplier modules
  - 2 arrays of 64 channel avalanche photodiodes



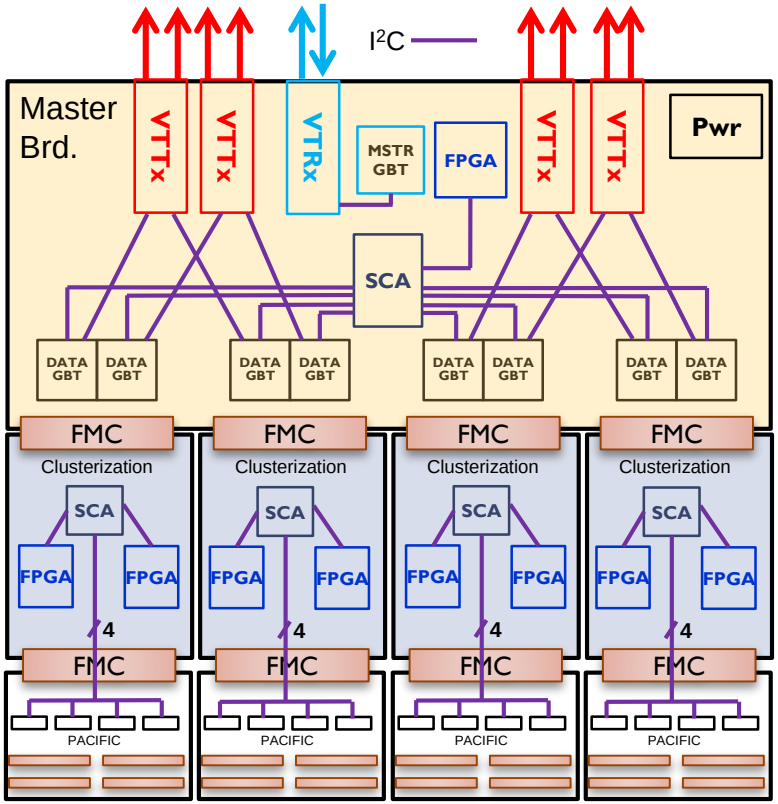
ECS E-links

- Slow controls done by the SCA, which is controlled via the Master GBT e-link ports
- GBT dedicated E-Link port used for Master Board SCA
- Four E-links for each of the Clusterization boards
- One spare/debug E-link to FPGA



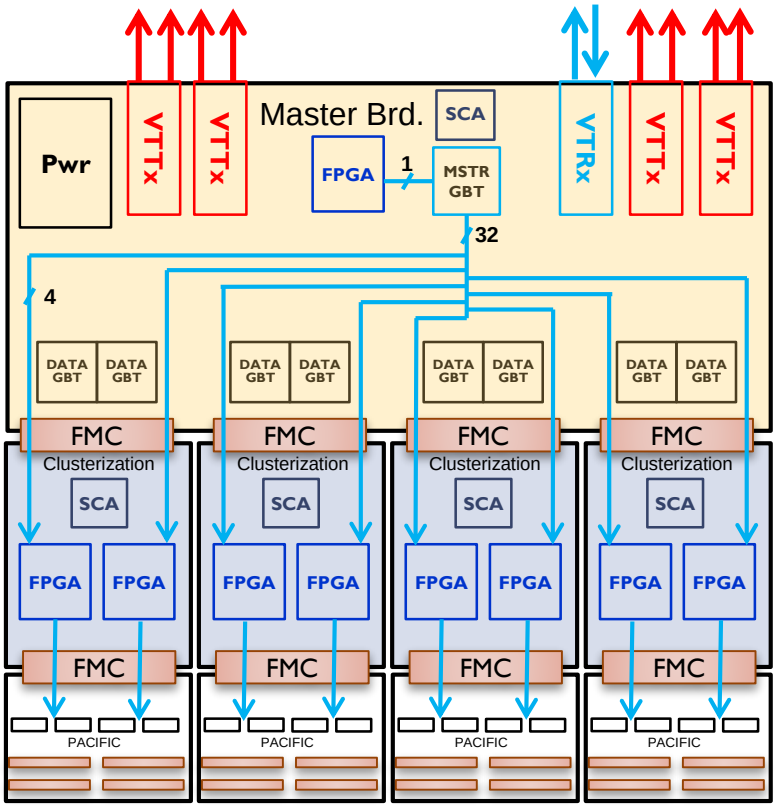
ECS / Slow control paths

- Master Board SCA
  - Eight VTTx GBLD I^2C register settings through Data GBT
  - Eight I^2C ports for Data GBT configuration
  - ADCs for board temperature monitoring
  - SPI or JTAG for re-programming FPGA
  - VTRx GBLD control through Master GBT
- Clusterization Board SCA
  - Two Clusterization FPGAs: I^2C register settings
  - Four PACIFIC ASICs settings via I^2C on PACIFC Boards
  - Four ADC inputs for PACIFIC and SiPM temperature monitoring
  - Four ADC inputs for SiPM Bias voltage monitoring
  - JTAG or SPI for FPGA re-programming



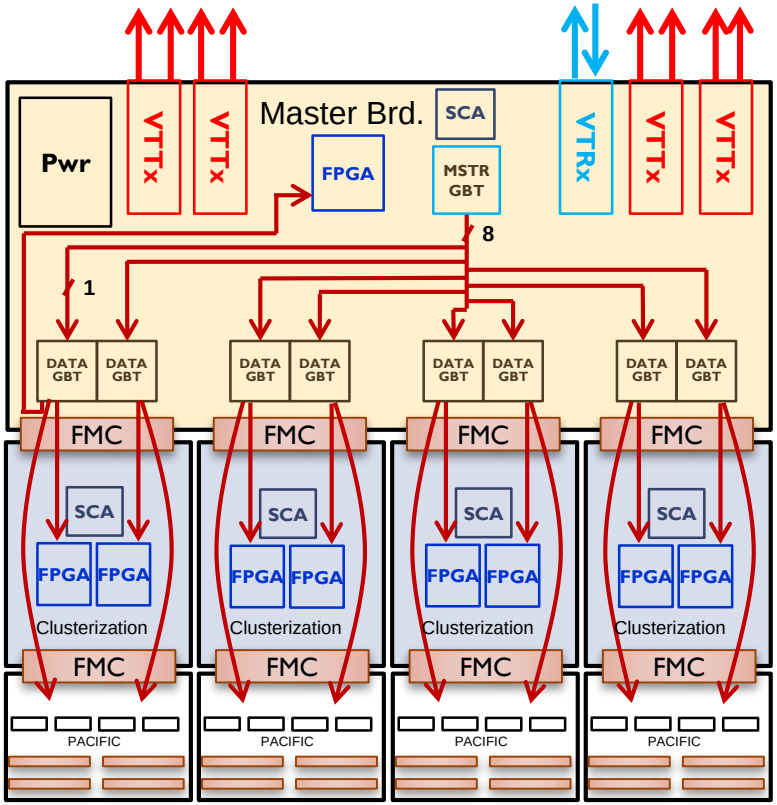
TFC: commands distribution

- Eight identical sets of TFC signals routed from Master GBT via FMC connector to Clusterization Boards
  - Each set contains 4 signal lines with 2 multiplexed TFC commands (80Mb/s)
- TFC commands in a set:
  - Bxid Reset
  - Fe Reset
  - Header only or-ed with BxVeto
  - Two calibration mode bits (1:0)
  - Synch Command
  - NZS Mode
  - Snapshot
- TFC commands synchronous clock connected to FPGAs
  - Eight Master GBT E-link clocks used for TFC synchronous clocks (Dclk)
- One calibration bit(2) and a Dclk synchronisation pulse via FPGA to PACIFIC

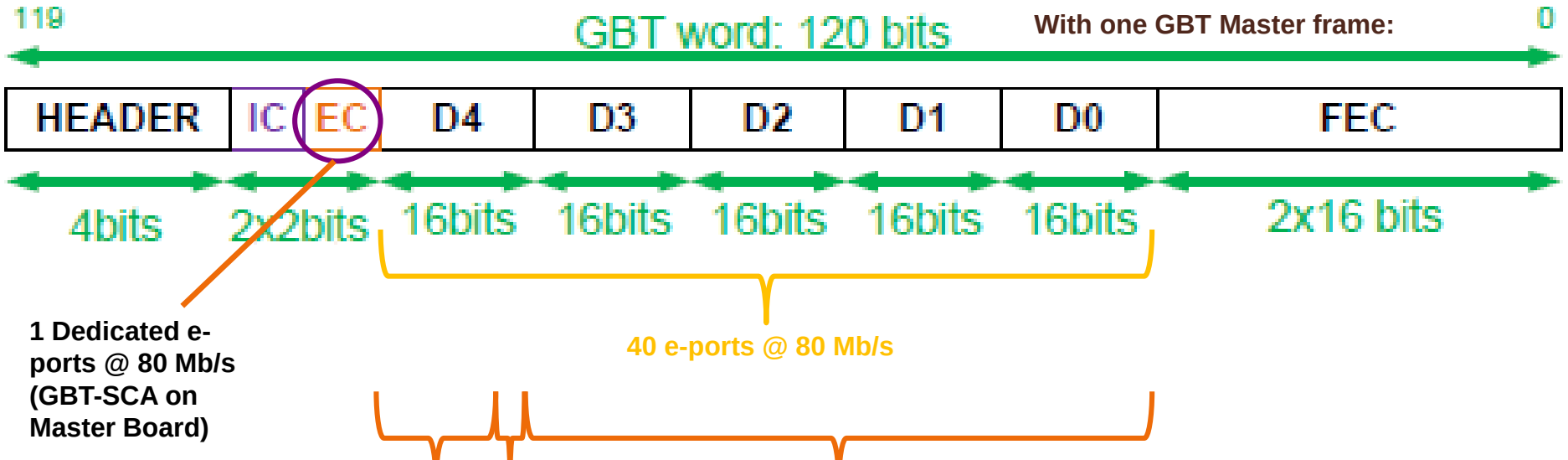


TFC: clock distribution

- GBTs used as clock fan-out tree:
  - Master GBT uses on package x-tal as reference clock
  - Master GBT clock fan-out to eight data GBTs
    - ClockDesP/N (0-7), eight deskewable clock outputs
      - Reference clock for Data GBTs
  - Data-GBT is clock fan-out to Clusterization and PACIFIC boards
    - Two clocks to each clusterization FPGA
    - Four 160 MHz clocks to PACIFIC chip
    - One clock from first data GBT to light injection system



Master GBT signal mapping



7 e-ports @ 80 Mb/s

- 4 GBT-SCAs one on each Clusterization Board
- 1 spare connected with Master Board housekeeping FPGA
- (2 reserved for an optional Concentrator Board)

1 e-ports @ 80 Mb/s:

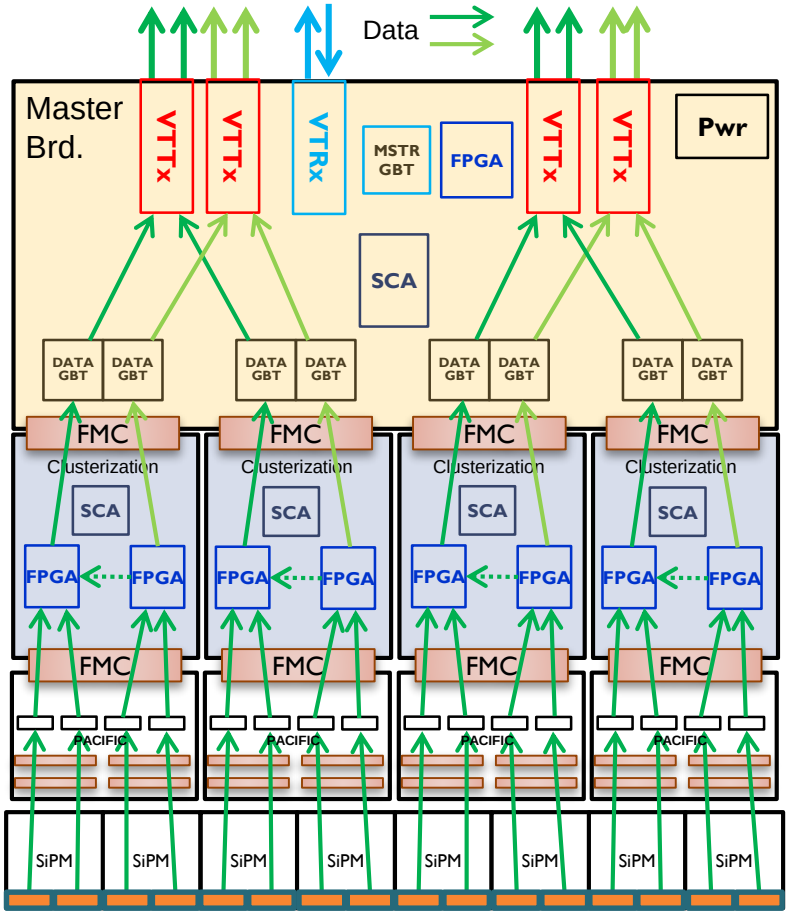
- TFC command Calibration for light injection system

32 e-ports @ 80 Mb/s:

- 8 sets of 4 bits, one set per cluster FPGA GBTX data out bits only
- 8 e-link clocks used for TFC synchronous clock

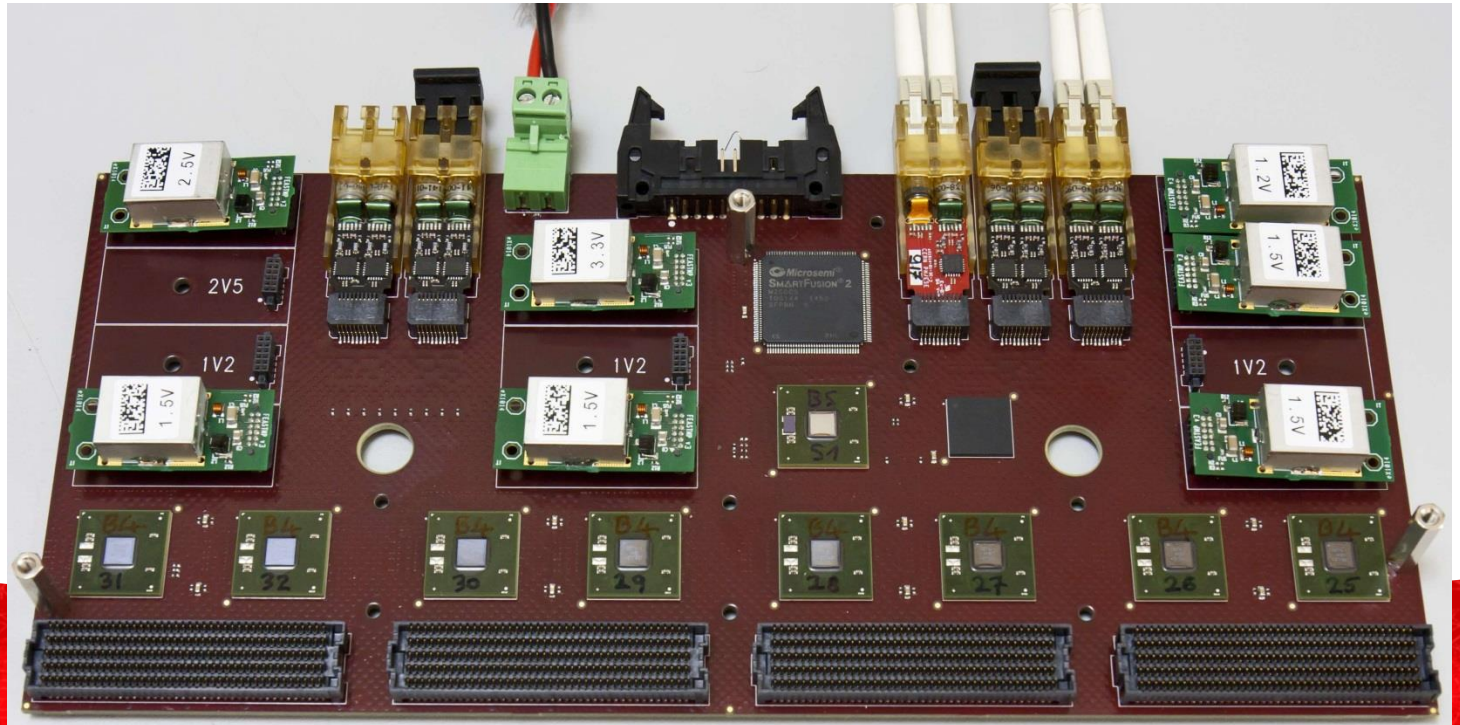
Data path on the front end

- Data path on a Master Board:
  - 16 x 64 channel SiPM arrays
    - Two arrays on a single SiPM module
  - Data digitized by PACIFIC ASIC
  - Clusterization of neighbouring active channels in the Clusterization FPGAs (Microsemi IGLOO2)
  - Serialised data by eight data GBTs in wide bus mode
  - Optical transmission by four versatile link VTTx devices



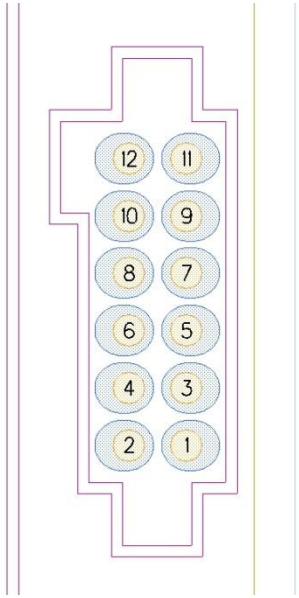
PCB Design

- Master Board and Clusterization Board have the same PCB specs
  - Dielectric material: Halogen free Isola DE1568
  - Eight power and eight signal layers
  - 76um traces and clearances
  - IPC class 3 assembled
- Due to the large number of boards, PCBs are reviewed for manufacturability and testability
  - 576 Master Boards, 2304 Clusterization boards



PCB Design : DFM

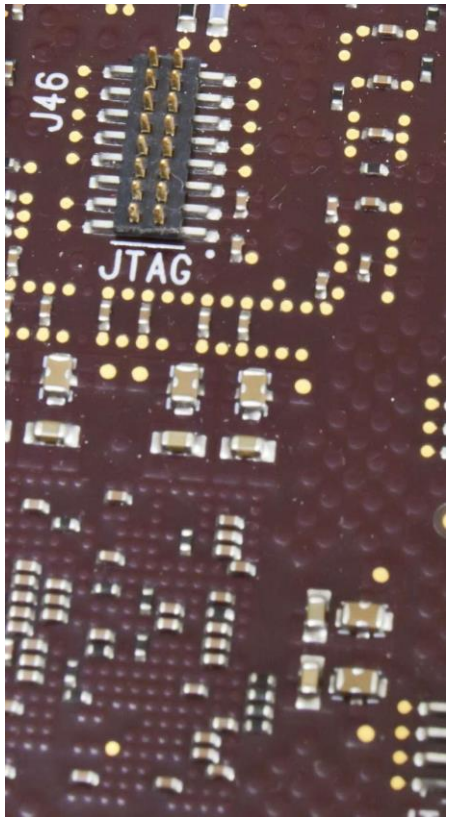
- Design For Manufacturability (DFM)
  - Complex design, ten 0,8mm pitch BGAs and four 400 pins high pin count connectors
  - High density of 0402 parts under BGAs
- Board design: component placement and footprints optimized for assembly process
  - Minimize the risk of errors during assembly
  - Minimize assembly stages → minimize the cost
    - E.g. Use Pin In Paste(PIP) for through hole components → no wave soldering needed



PCB Design : DFT

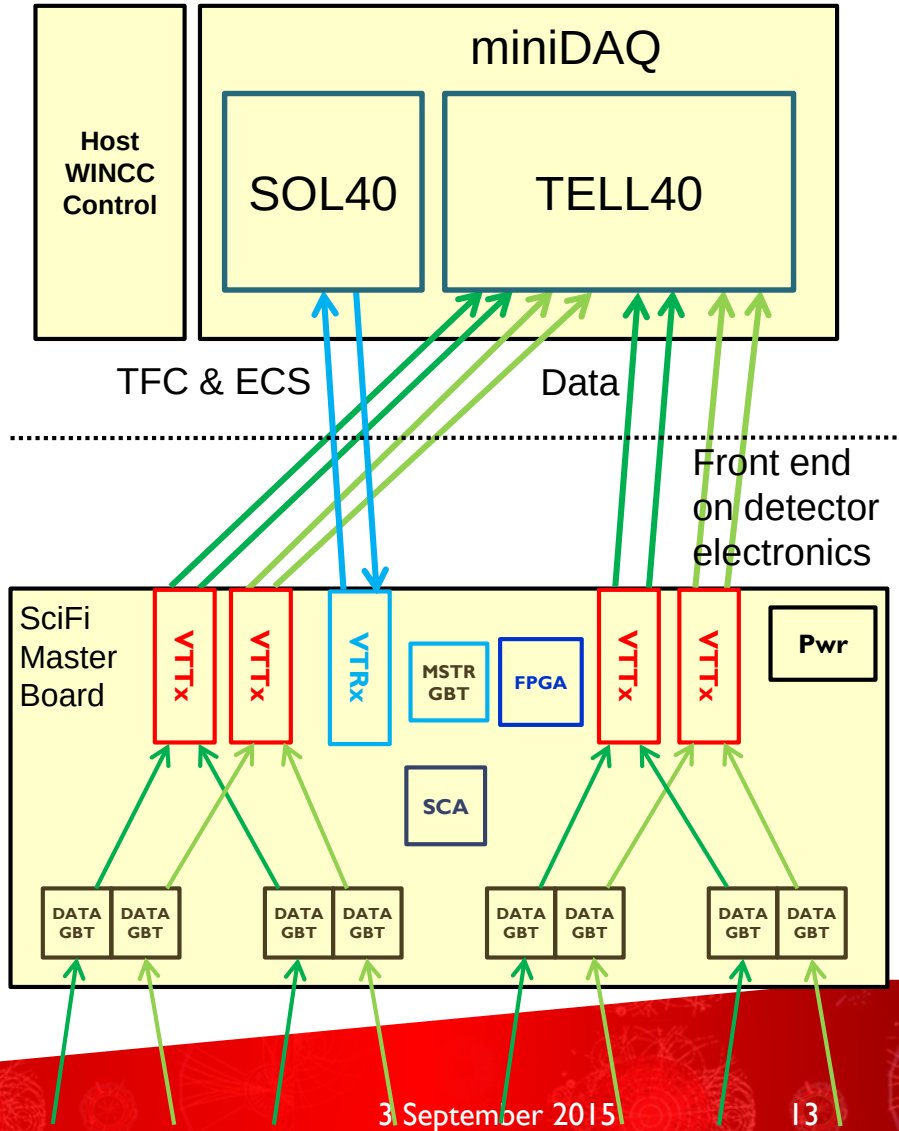
- Design For Test (DFT)
  - Design optimized for test during & after assembly → High yield
  - Optimize for test connectivity between Boundary scan capable devices
  - Place test points for flying probe access, when not possible component pads can be used

- DFT stages:
  - 3DAOI : 3D Automated Optical Inspection
    - Every time after applying paste, component placement and reflow soldering process
  - Flying probe test
    - Test electrical connections and component values
  - EBST : Extended Boundary Scan Test (series production only)
    - Test electrical connections between components. Active loopback board(s) are used for routing to connectors.



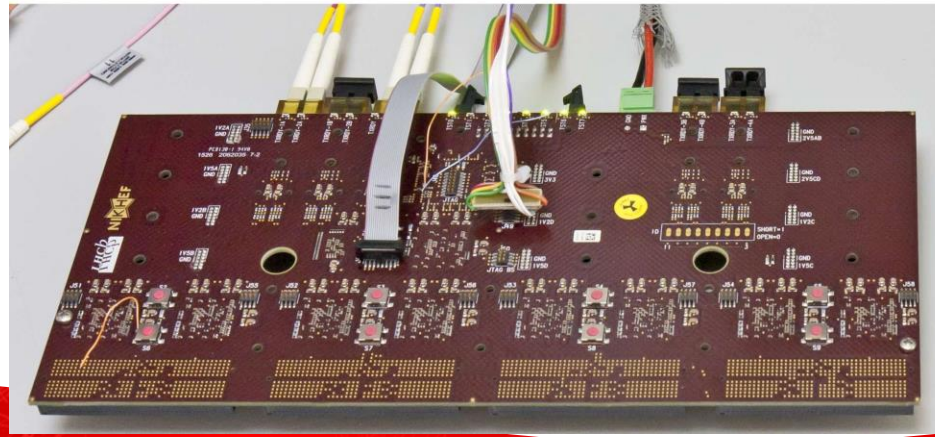
SciFi FE boards tests

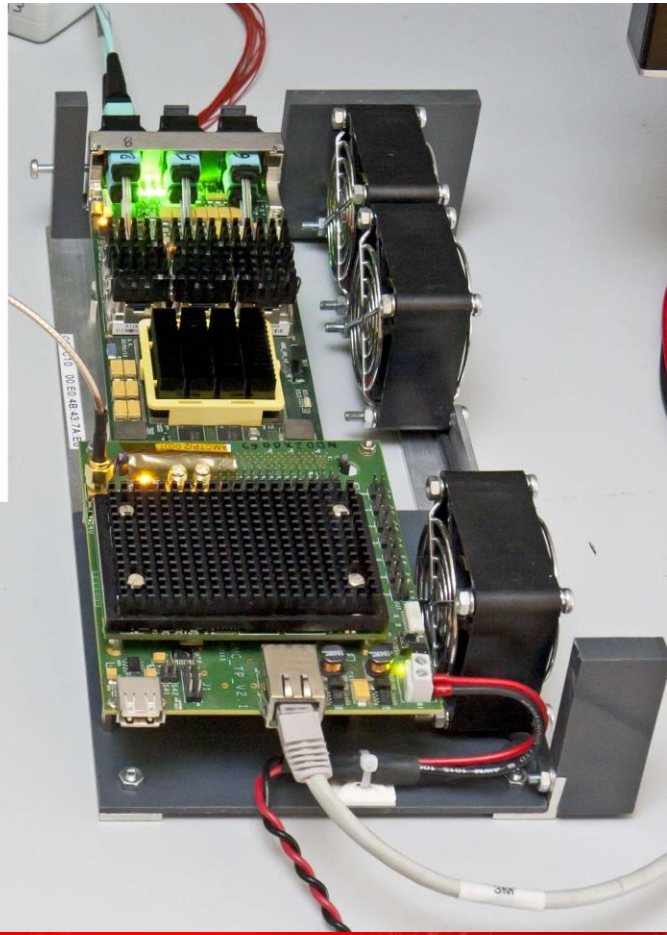
- In the Master Board tests the Mini-DAQ is being used for:
  - Configuration of the FE (ECS)
  - Fast control and clocks (TFC)
  - Monitoring of the FE (ECS)
  - Data path from FE to BE (DAQ)



SciFi FE boards tests

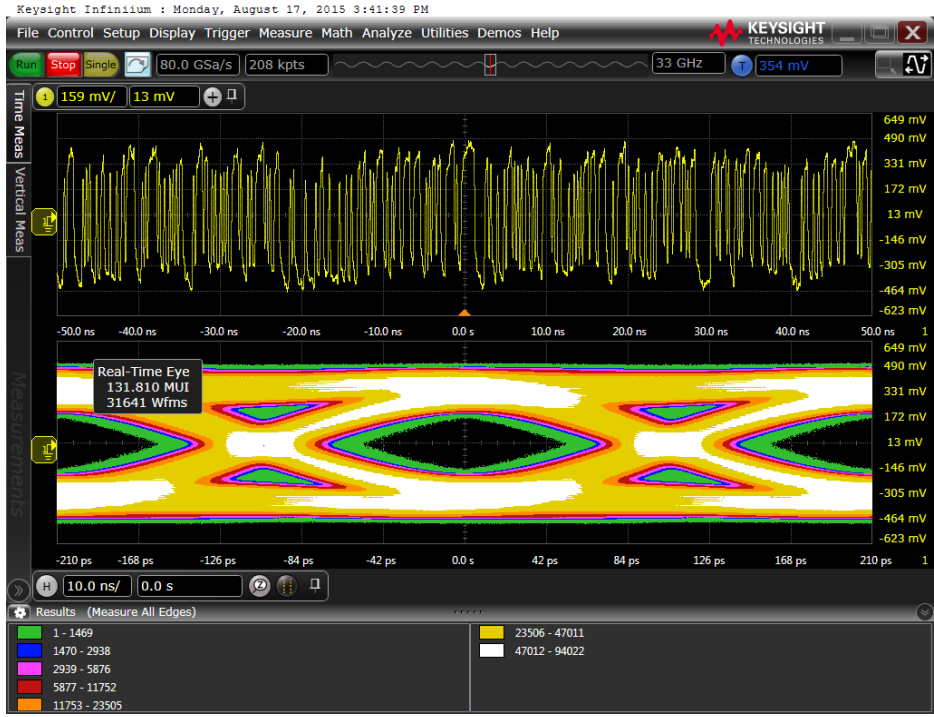
- Configuration of the Master GBT
  - Device is not fused (yet), Random values in registers after power on. All register needs to be programmed via external I^2C port after power cycle.
  - After configuration the Master GBT can be programmed via the GBT frame IC bits.
  - Configure the first stage of the clock tree to reference clocks of Data GBTs
- All data GBTs are configured via the Master GBT and the Slow Control Adapter.
  - Configuration stored in file and written by WINCC via the MiniDAQ to the Master Board
- Configuration of the HouseKeeping FPGA
  - Identical to FPGAs on the Clusterization Boards
  - Hardware read/write tested OK, read back via MiniDAQ/WinCC needs debugging.





Data link tests

- SciFi uses GBT wide bus protocol, testing data links requires a MiniDAQ with SOL40 and TELL40 functionalities.
  - SOL40 part needed for board configuration
- Data link stable on a StratixIV based receiver
  - Send data from GBT in test mode
- Eye pattern measurement at the input of the Versatile link VTTx
  - Eye opening of 354 mV
  - Long path from clock generator → StratixIV → MiniDAQ → Master GBT → Data GBT introduces jitter.
    - Path can be optimized
  - Layout improvements possible



ROB electronics cooling

- Temperature test in preparation
- Electronics will be cooled with 20˚C water