



Status report for TFC and ECS*

F. Alessio, CERN

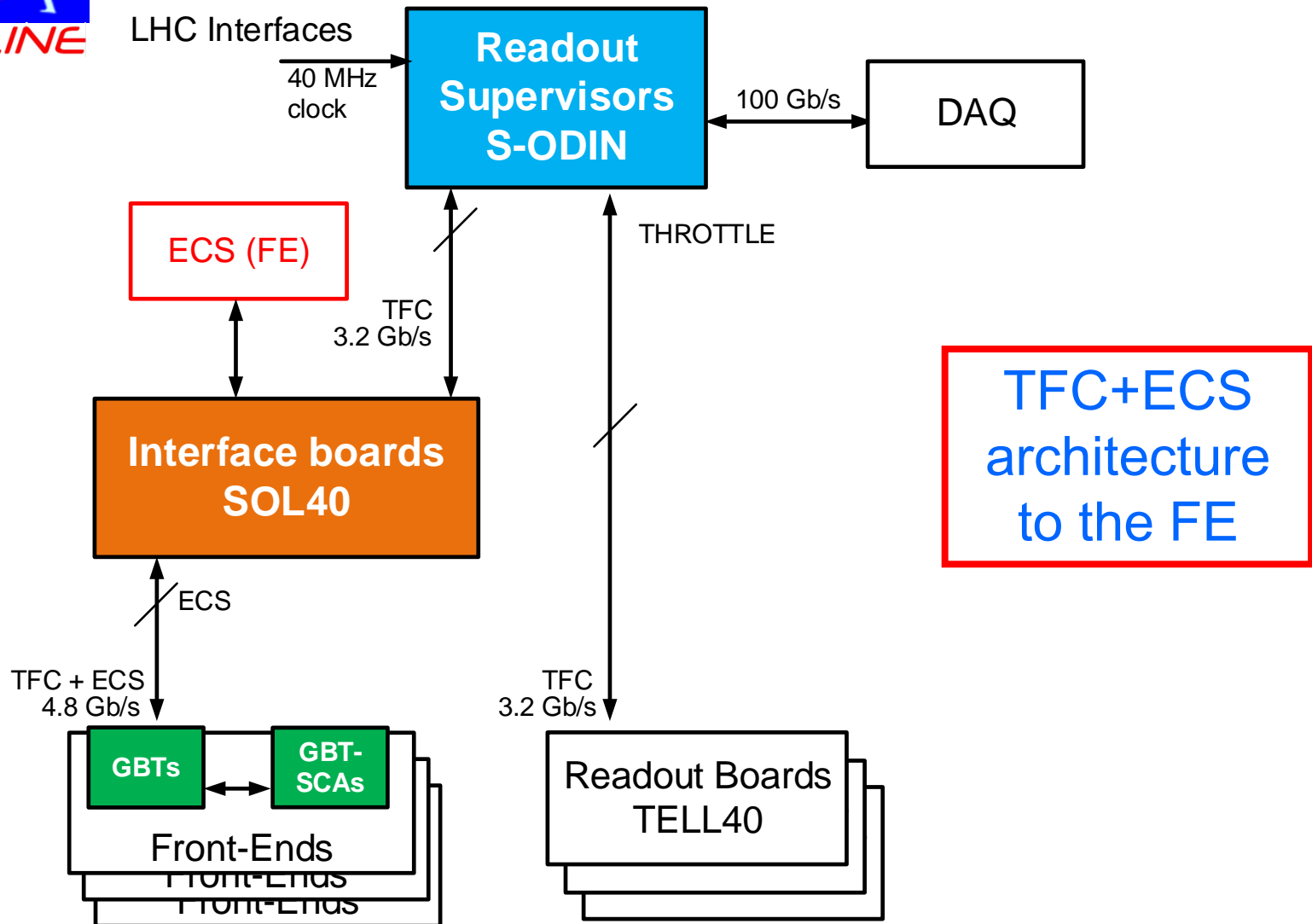
with acknowledgements to Cairo (Caplan), Mauricio (Rivello),
Luis (Granado), Joao (Barbosa), Clara (Gaspar), Ken & PH-ESE group

LHCb Upgrade Electronics meeting

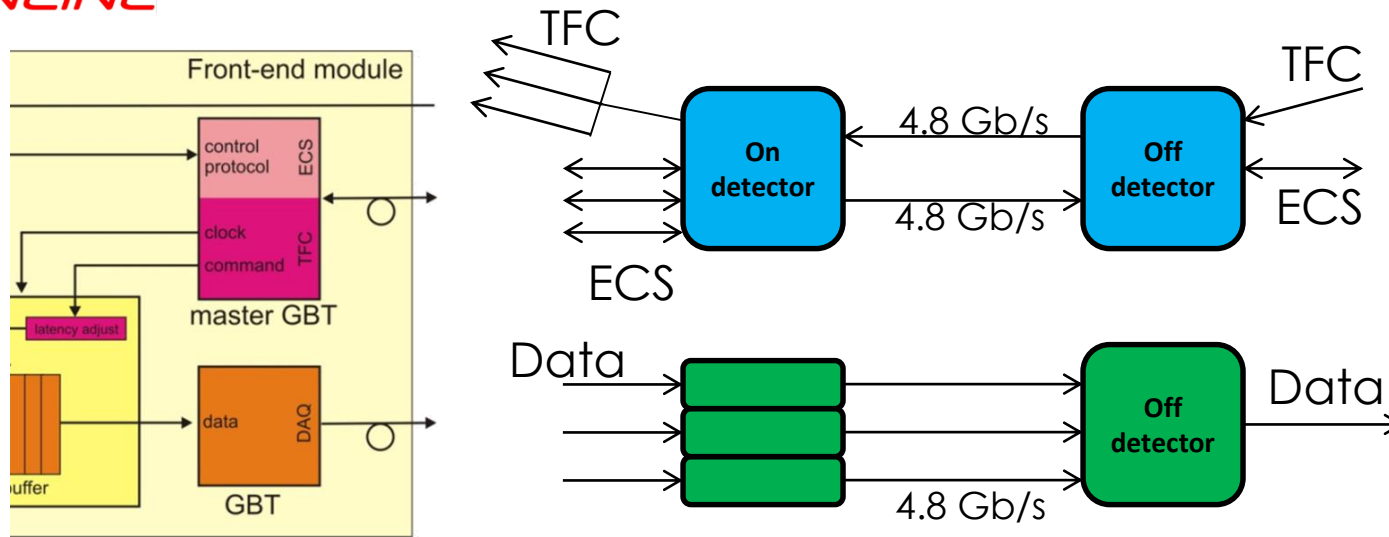
03-09-2015

* here only covered firmware developments

Reminder: generic architecture



Reminder: Fast & Slow control to FE



Separate links between controls and data

- A lot of data to collect
- Controls can be fanned-out (especially fast control)

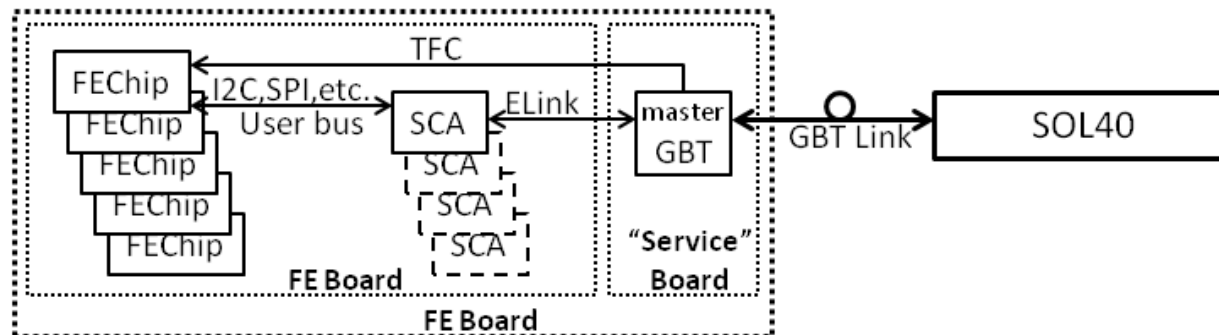
Compact links merging Timing, Fast and Clock (TFC) and Slow Control (ECS).

- Extensive use of GBT as Master GBT to drive Data GBT (especially for clock)
- Extensive use of GBT-SCA for FE configuration and monitoring

Reminder: main features

One SODIN as Readout Supervisor + one or more SOL40 are used to control a slice of your FE:

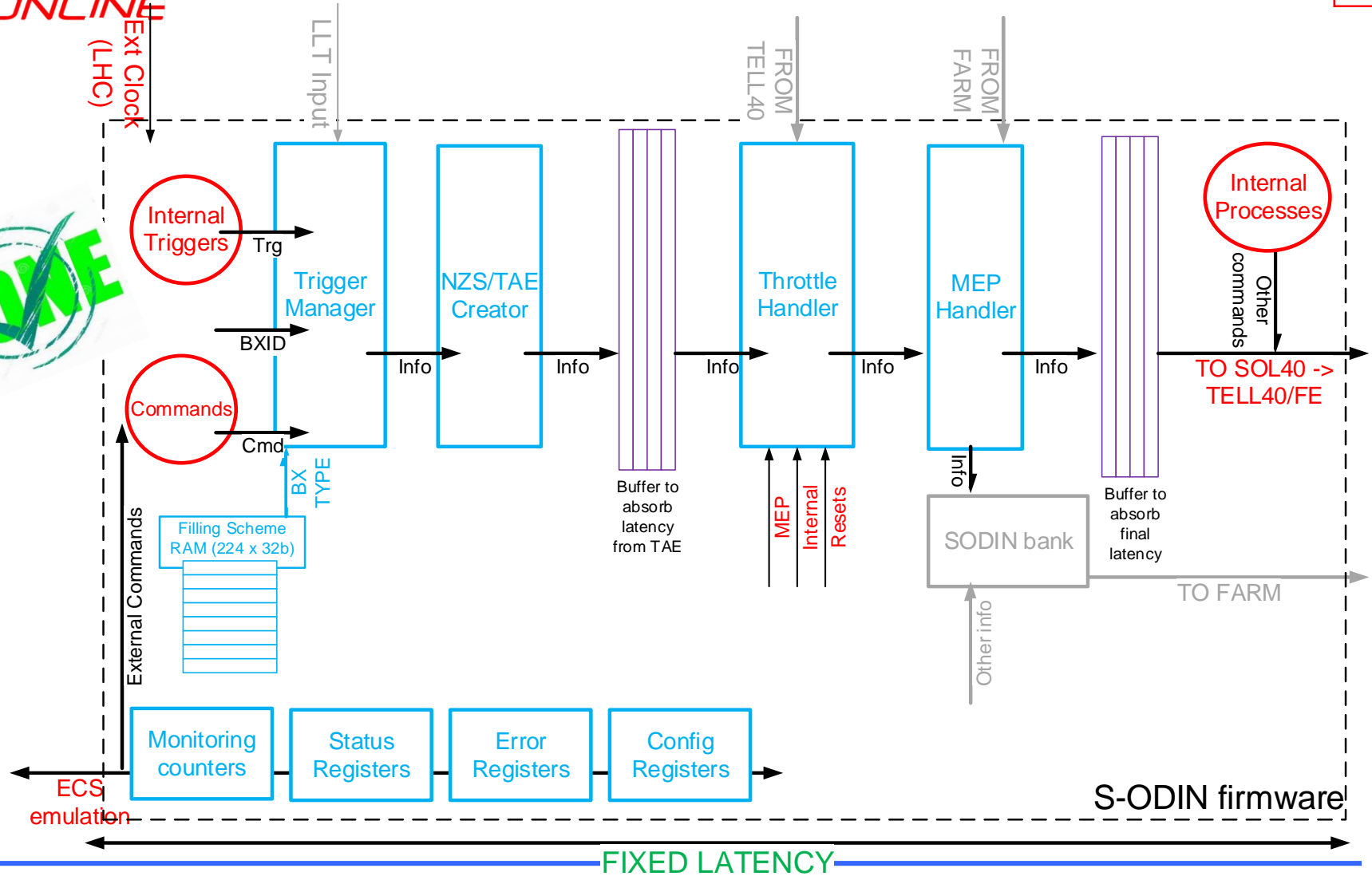
- Propagate TFC information to the FE
 - TFC triggers and commands, see [LHCb-PUB-2012-017](#) and [LHCb-PUB-2012-001](#)
- Propagate ECS information to the FE
 - Configure/control Master GBTX
 - Configure/control Slave GBTXs
 - Configure/control GBT-SCAs
 - Configure/control FE chips
- Receive back ECS information from the FE
 - From all devices at the FE, return path
- Control all of this from WinCC, as usual
 - Within global LHCb ECS



Current developments: SODIN firmware

FA

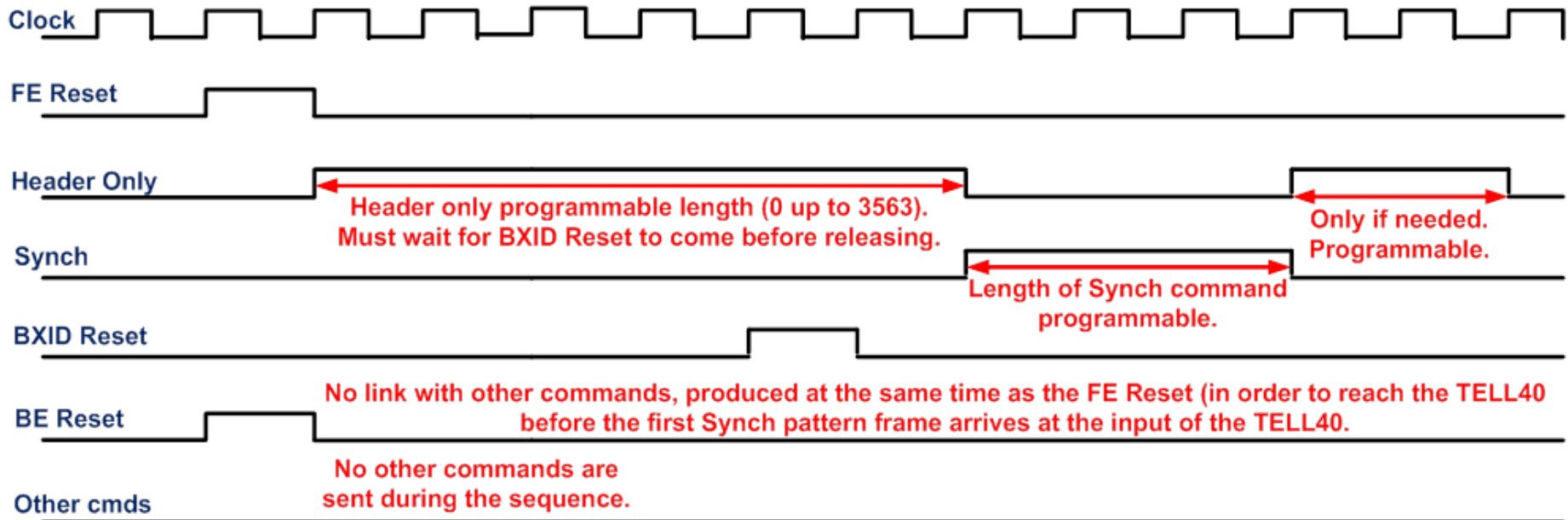
DONE



Features:

start-up synchronization mechanism

“Start-of-run” timing diagram



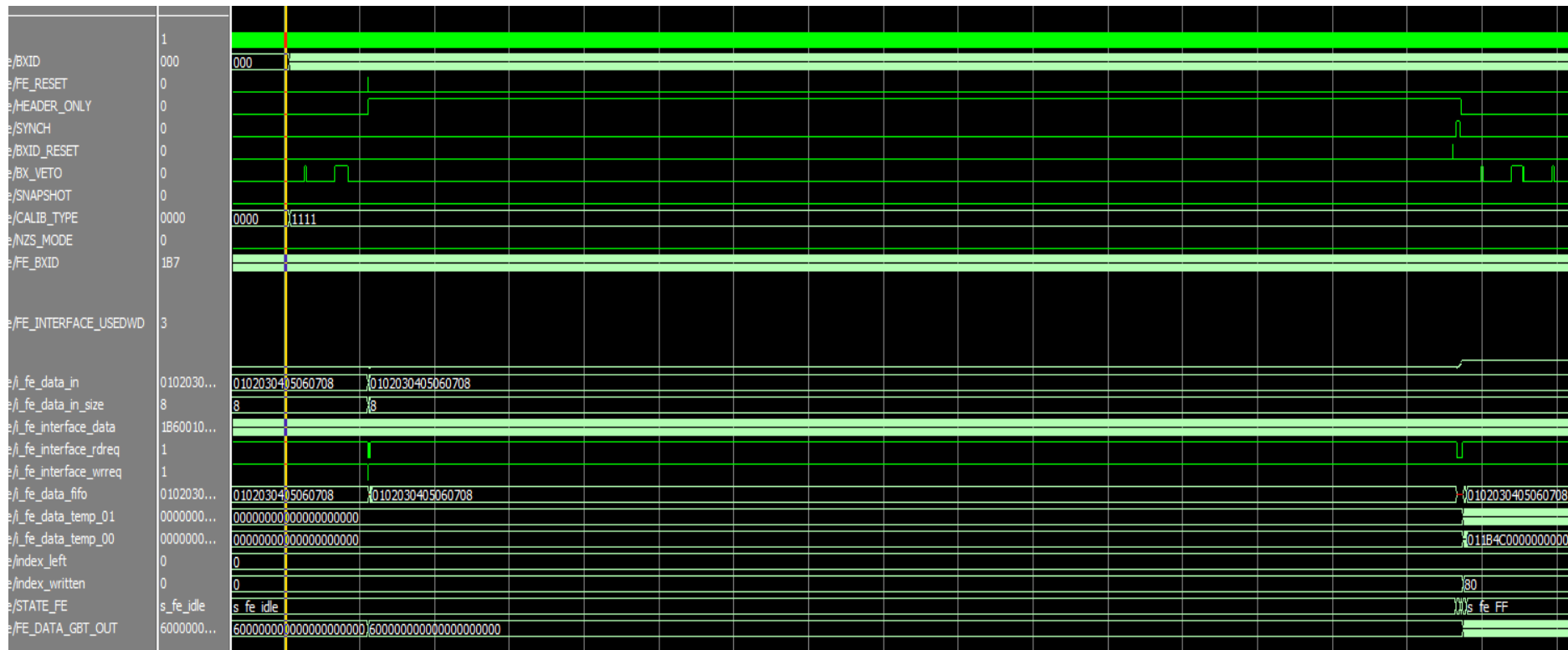
Important mechanism to allow TELL40 to synchronize to the correct event fragment

- See <https://indico.cern.ch/event/291719/> for details
- Please comply! And then test it with the firmware on the git repository.



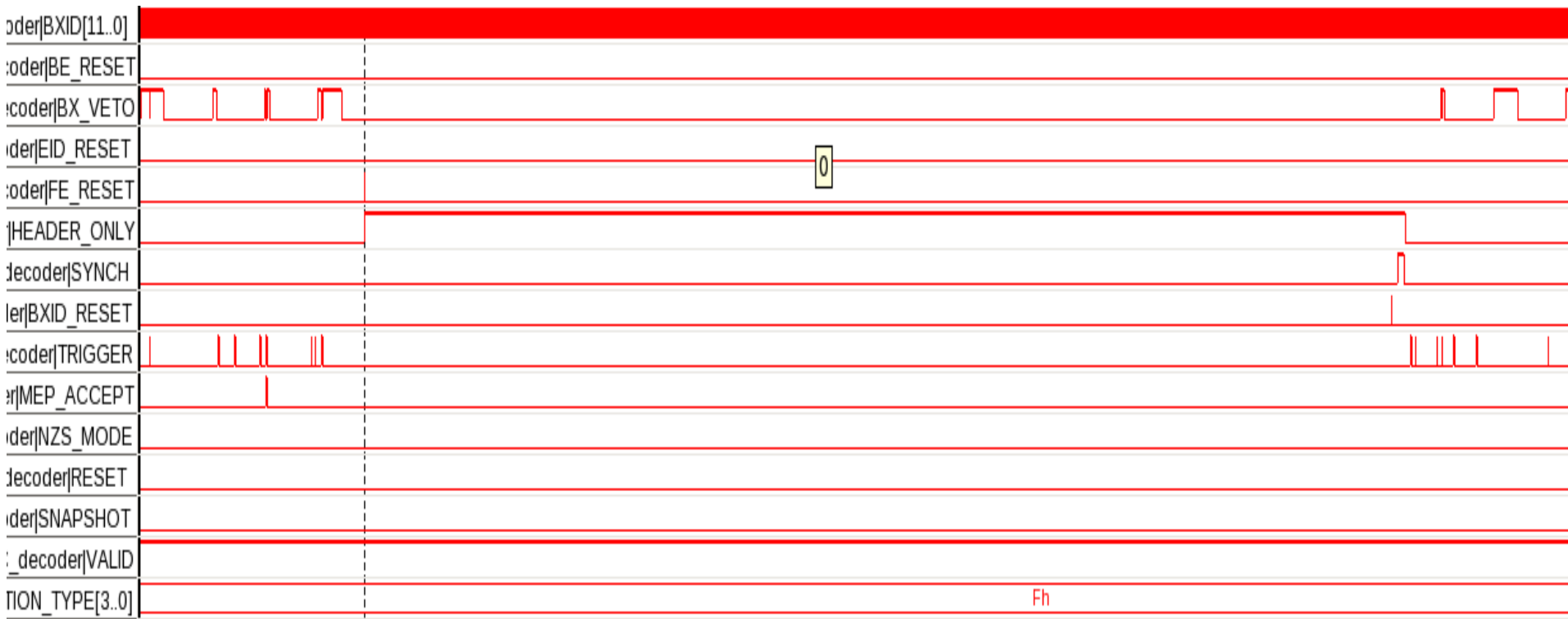
Features:

start-up synchronization mechanism (simulation)



Features:

start-up synchronization mechanism (firmware)

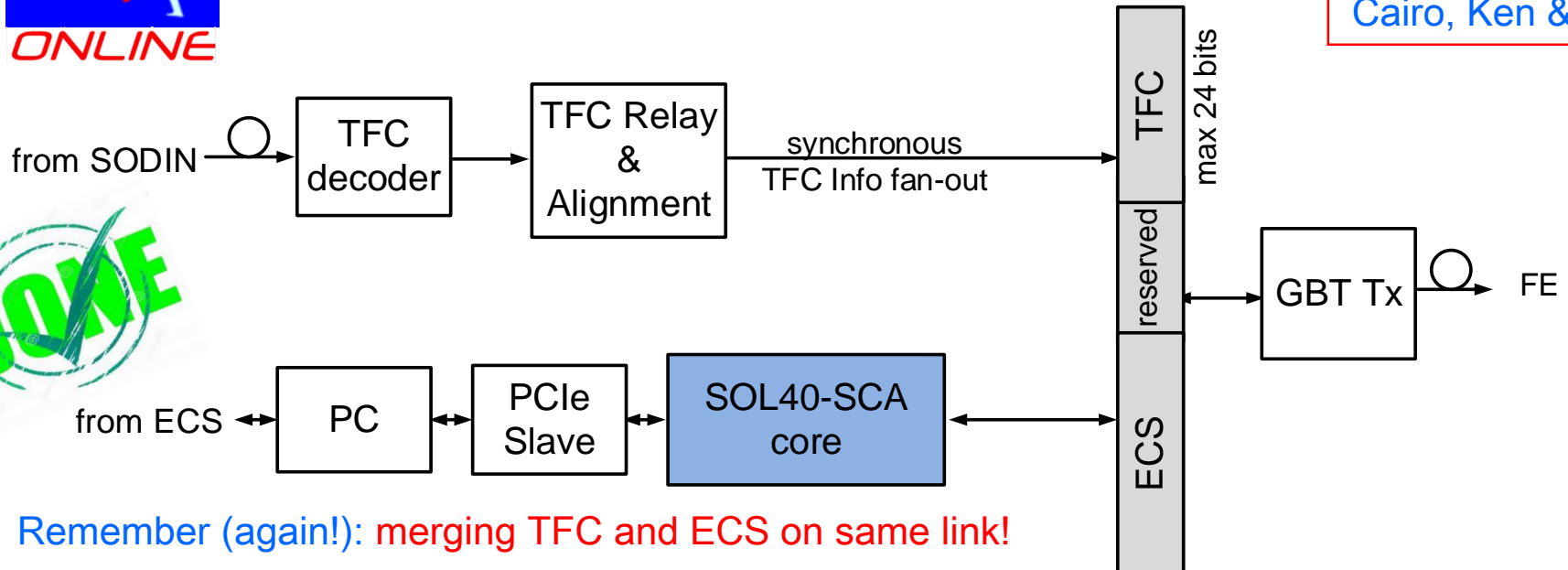


Outlook: SODIN firmware

- First complete and tested version is ready on git: SODIN_v1r06
 - All triggers and commands implemented
 - Including the various synchronization mechanisms for FE-TELL40
 - Including trigger/command decoding block in SOL40
 - Sub-detectors should come with their favorite bit/command ordering for their Front-End and I will include it in the .vhd
 - Based on the mapping at the GBT side
- To-do:
 - Still missing the ODIN bank towards the FARM (for later)
 - Throttle handling between SODIN-TELL40
 - Tests with FE chips/developers
- Next step: architectural developments
 - What technology for TTC backbone? Technologies evaluation with ESE group.
 - Clock and phase tests with PCIe40. To do with Marseille's group.
 - ... test test test ... with you!

Current developments: SOL40 firmware

Cairo, Ken & FA



Remember (again!): merging TFC and ECS on same link!

→ SOL40 firmware will take care of doing all the complicated bit manipulations needed to control GBTs, its SCAs and your FE chipsets

- Single firmware for everybody with all necessary features and requirements
 - minimize unconformities, highly programmable and customizable
 - Modular (can get a core and put it somewhere else in an eval board?)
- Centrally provided

→ In addition it will distribute the TFC commands from SODIN to FE with fixed latency.

Features: SOL40-SCA core

Cairo, Ken & FA

It's a **firmware core** inside the SOL40 firmware which is responsible to:

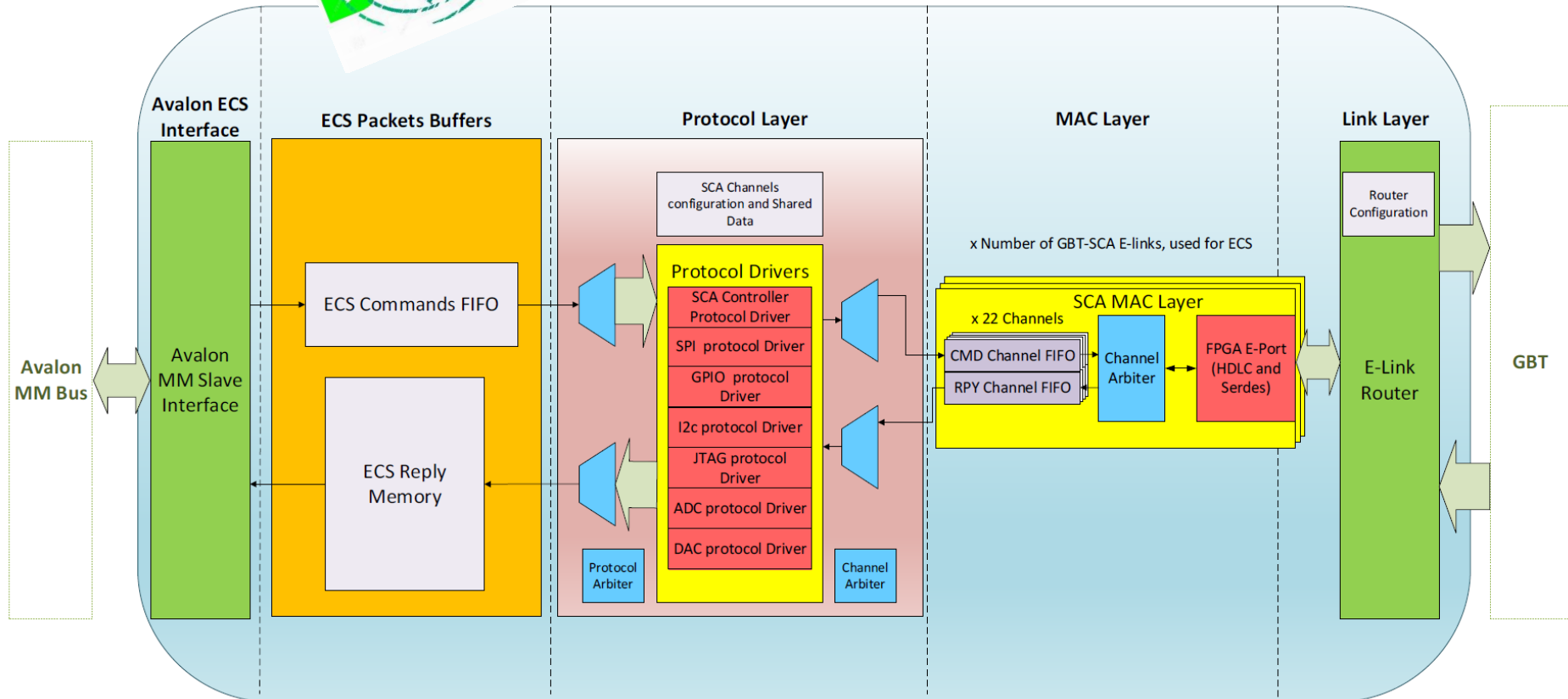
- **control the Master GBT**
 - 1 Master GBT per optical link
- **control all GBT-SCAs associated to that Master GBT**
 - Up to 16(+1) GBT-SCAs per GBT link
 - Serialize/Deserialize with proper encoders (HDLC)
 - Targeting 36 GBTs to start with (programmable at compilation)
 - One SOL40 could cover up to ~600 SCAs and ~9000 I2C devices...
- **control all the FE chips associated to those GBT-SCAs**
 - Including the **Slave GBTs** connected to the SCAs (I2C dedicated bus)
 - Support for all GBT-SCAs buses in a programmable way
 - Generic in the sense that it is transparent to your FE chip architecture

For more details, see Cairo's presentation at Electronics Meeting in October 2014

<https://indico.cern.ch/event/291724/contribution/2/material/slides/0.pdf>

The core follows the GBT specs and GBT-SCA specs

- (see [GBT project public webpage](#) for details)



1 core per GBT, scalable support for SCAs, all SCA buses, *vendor/FPGA independent*, modular control, error detection capabilities

Outlook: SOL40 firmware

- Ready and deployed on git: SOL40_v1r12
 - It also includes the part to control the Master GBTx
 - And SOL40-SCA core with I2C chain fully implemented and validated/qualified, now testing the other protocols
 - We need your FE chip (and you possibly!)
 - We have setup a test-bench in the ESE lab to welcome you with comfort. a ready-to-go setup and a close-by cafeteria ☺
 - Basically bug tracking/fixing from now on
- To do:
 - generic matrix to assign GBT-SCA to pair of bits
 - retransmission of packets in case something went wrong
 - checks of transmitted packets, error reporting, semaphores with ECS
 - *Programming of FPGAs via JTAG? SPI?*
- Next steps:
 - Work has started in ECS team (Joao, Clara, Luis) to develop the necessary software to control the firmware core in an efficient way
 - Ccserve for Mini-DAQ, server for PCIe40
 - WinCC components (+scripts, panels etc)
 - More news from them at LHCb Week!

Resources utilization

Analysis & Synthesis Resource Utilization by Entity				
	Compilation Hierarchy Node	LC Combinationals	LC Registers	Block Memory Bits
1	▲ [Q_Top_Level_comp]	64935 (74)	50241 (33)	13870380
1	▷ Clocks_Generator:Clocks	44 (12)	38 (6)	0
2	▷ Q_SODIN_Top_Level:SODIN	7053 (0)	6610 (0)	195584
3	▲ Q_SOL40_Top_Level:SOL40	18677 (0)	10377 (0)	8989072
1	▲ Q_SOL40:SOL40_link1	18677 (920)	10377 (427)	8989072
1	▷ ODIN_counters:SOL40_CNT_01	363 (0)	704 (0)	0
2	▷ SC_IC:SC_IC_SOL40	5899 (6)	2519 (6)	8388608
3	▷ STFC_decoder:TFC_decoder	197 (136)	93 (40)	110592
4	▷ fifo_pipeline_2bits:OUT_FE_VALID_PIPE_FIFO	61 (0)	53 (0)	4096
5	▷ fifo_pipeline_84bits:OUT_FE_PIPE_FIFO	61 (0)	53 (0)	344064
6	▷ fifo_pipeline_84bits:OUT_SODIN_PIPE_FIFO	61 (0)	53 (0)	4096
7	▷ fifo_pipeline_84bits:OUT_TELL40_PIPE_FIFO	61 (0)	53 (0)	57344
8	▷ sol40_sca:SOL40_SCA_CORE	11054 (0)	6422 (0)	80272
4	▷ mep_top:mep_top_0	1315 (0)	1167 (0)	1310720
5	▷ sld_hub:auto_hub	93 (1)	77 (0)	0
6	▷ top_level_TELL40:TELL40	13525 (1513)	12514 (945)	2246144
7	▷ top_lll_6chs:LLI	24154 (92)	19425 (36)	1128860

- Mini-DAQ firmware compilation report (24k ALMs / 234 k) Stratix V

- 1 SODIN
- 1 SOL40 with 1 core to drive 1 GBT
- 1 SOL40_SCA core for one GBT and 16(+1) SCAs

→ For a Mini_DAQ to control 6 GBTs and 16(+1) SCAs+FEs each that would mean ~100k ALMs / 230k

→ OK for an Arria X (# of GBTs and SCAs are programmable, so we can optimize)

X But we can't fill up a full SOL40 with 48 bidir links and fully loaded FE chips



Software tools to get you started

Cairo, Mauricio,
Luis & FA

- Developed first software tools to help you get started and use the firmware efficiently on possible test-benches/lab tests
 - WinCC panels to control SODIN

Statistics and status

DeviceName: SODIN_GBTtest.Core0
Version: 1.06
Date: 20131204.03
State: **RUNNING**

Orbits	Periodic Trig. A	Periodic Trig. B	Calib. Trig. A	Calib. Trig. B	Calib. Trig. C	Calib. Trig. D	Random Trig. A	Random Trig. B0	Random Trig. B1	Random Trig. B2	Random Trig. B3	Random Trig. C	Random Trig. D	EID Accept
231741192	115321728	115321727	115321725	0	0	0	3330164876	3498862891	1703414102	1703404487	2752005312	622496274	59563392	1430273966
	5.92 kHz	5.92 kHz	5.92 kHz	0.00 kHz	0.00 kHz	0.00 kHz	1054.85 kHz	179.87 kHz	87.23 kHz	87.28 kHz	7862.65 kHz	31.97 kHz	3.06 kHz	73.56 kHz

Triggers

	Raw	Raw Rates (kHz)	Gated	Gated Rates (kHz)
Orbit	231741192	11.846		
Bunch ID	0x00000000			
Random A	3330164876	1054.852	1316511453	1050.552
Random BB	2752005312	7862.051	0	0
Random B1	1703414102	87.231	0	0
Random B2	1703404487	87.275	0	0
Random EE	3498862891	179.872	0	0
Random C	622496274	31.972	432626733	31.957
Random D	59563392	3.063	41355685	3.058
Periodic 1	115321728	5.923	80177287	5.923
Periodic 2	115321727	5.923	80177288	5.923
Calibration A	115321725	5.923	80177288	5.923
Calibration B	0	0	0	0
Calibration C	0	0	0	0
Calibration D	0	0	0	0
Physics	0	0	0	0
Auxiliary	0	0	0	0
All Triggers	4274240477	1103.338	4274240313	1655.007

Commands

	Raw	Raw Rates (kHz)	Gated	Gated Rates (kHz)
FE Reset	3		4	
BE Reset	0		2	
BXID Reset	231741202	11.846	231741202	17.769
EID Reset	1018812366		1018812370	
TFC Reset	2			
Synch	10		12	
Snapshot	16181	0	16181	0
BX Veto	3461820091	7015.929	3461819086	10523.895
NZS Mode	0	0	2	0
EID Accept	1430273966	73.556	1430273965	73.556
Throttle	5997			
TELL40 Throttle	0			

Calibration Triggers

	Raw	Raw Rates (kHz)	Gated	Gated Rates (kHz)
Calib A BXID	3087		3087	
Calib A periodicity	2	2		
Calib B BXID	1199		1199	
Calib B periodicity	2	2		
Calib C BXID	2527		2527	
Calib C periodicity	2	2		
Calib D BXID	527		527	
Calib D periodicity	2	2		

Trigger Types

	Raw	Raw Rates (kHz)	Gated	Gated Rates (kHz)
Periodics	9		9	
Calibrations	10		10	
Randoms	4		4	
NZS	7		7	
Luminosity	2		2	
Physics	0		0	
Beamgas	1		1	
Auxiliary	14		14	
Others	15		15	

Offsets

	Raw	Raw Rates (kHz)	EventID Low32	EventID High32
Physics Trigger	3459		0	
Auxiliary Trigger	512			
NZS/TAE latency	13			
OUT latency	4			

Orbit clock

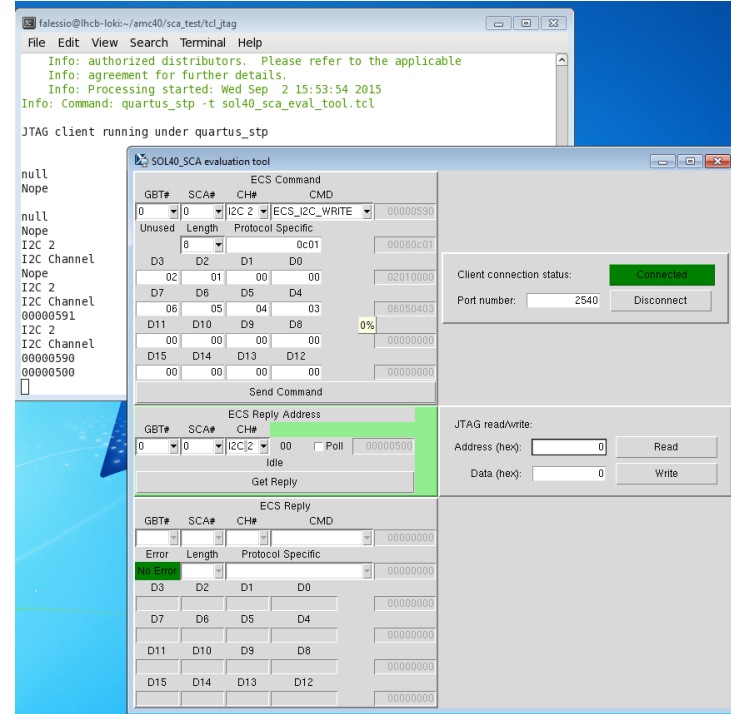
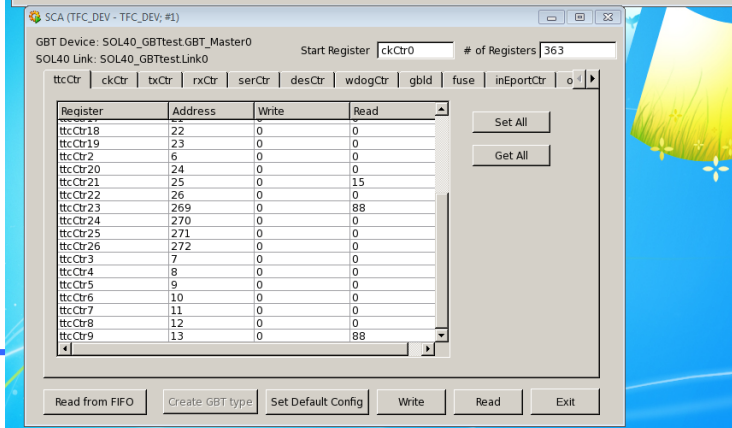
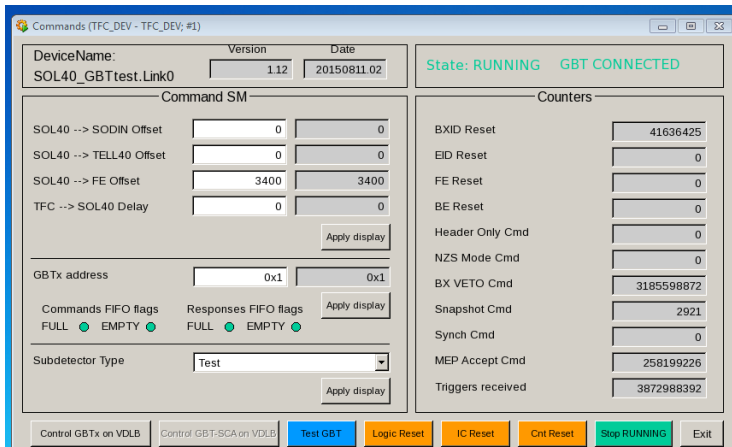
	Raw	Raw Rates (kHz)	EventID Low32	EventID High32
BXTYPE 00	2409624250	7202.572	0	
BXTYPE 01	4070459700	1753.257		
BXTYPE 10	4070459988	1753.258		
BXTYPE 11	3626227054	31511.267		



Software tools to get you started

Cairo, Mauricio,
Luis & FA

- Developed first software tools to help you get started and use the firmware as efficiently as possible in test-benches/lab tests
 - WinCC panels to control SODIN + SOL40 + GBT + SCAs
 - **Altera Quartus tcl/tk scripts/GUIs to control the SCAs and external chips in a generic way**



Note of caution: these are not the final software, but only evaluation tools to help you manage the TFC+ECS part of the firmware in lab



Ok, now what?

- SODIN and SOL40 ready!
 - o Now you can get your preferred GBT or SCA configured with the Mini-DAQ and with some handy tools
 - Just on time for the VDLBs to come out on the market ...
 - o Everything is on git, only documentation is missing (sorry, it will come soon ^_^)
- Next step(s)
 - o **Sub-detectors experts are very much encouraged to come to me (and/or Ken) to test whichever system you have in your hands**
 - We like challenges so we want it as difficult as it can be
 - o ECS friends to develop software to control the firmware, so tune up for the LHCb Week online parallel session if you want to hear more.
- ✓ It is vital to test your FE chips as early as possible to discover non-conformities, problems or even if we need to change anything in our architecture/framework.
 - **The sooner, the better***

*I'm going on holidays until the 14th of September, so your request will be taken care of from then on... ©



Backup

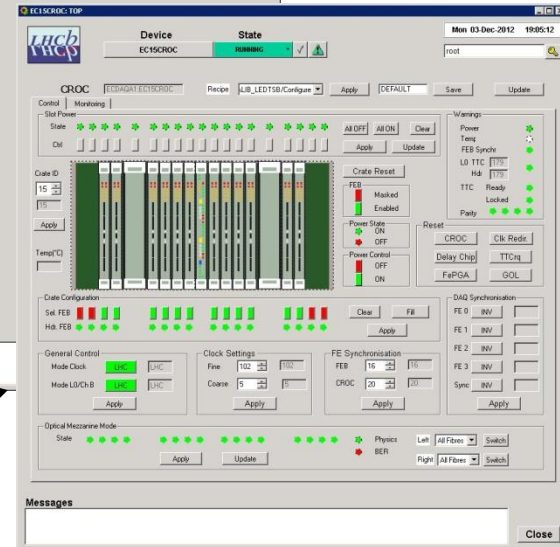
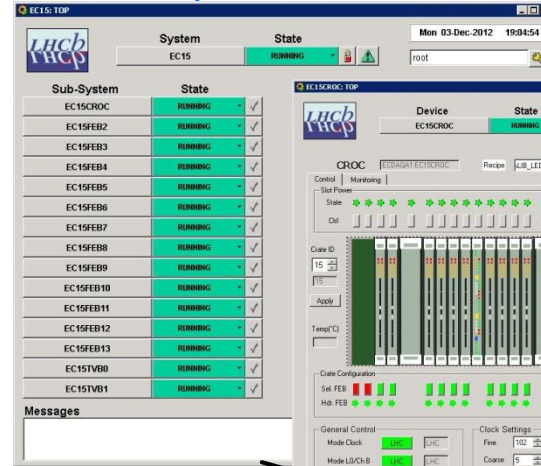
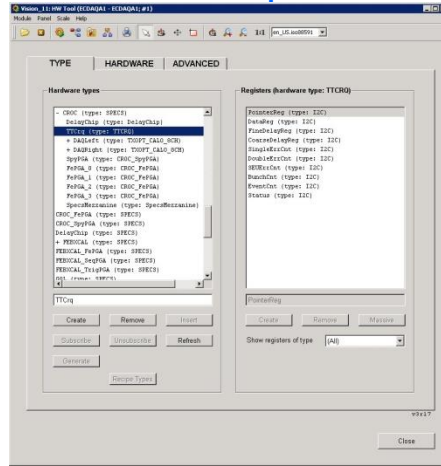
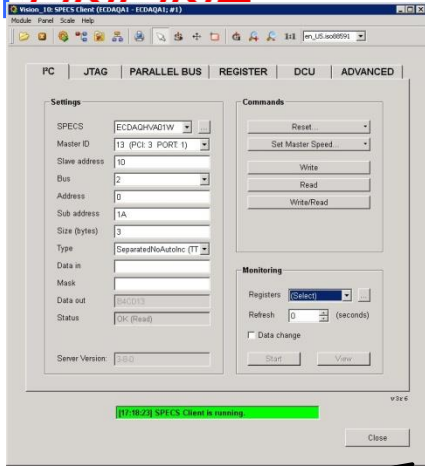


Current developments: software

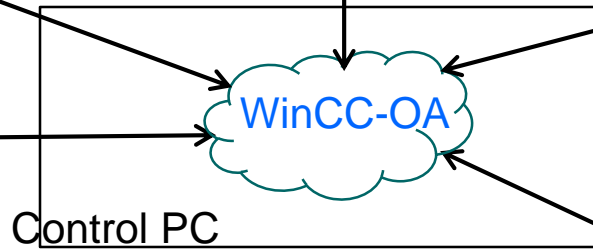
Clara, Luis, Pierre-Yves

HW Description UI

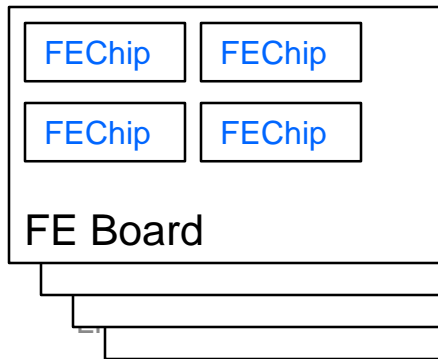
Operation UI



Test UI

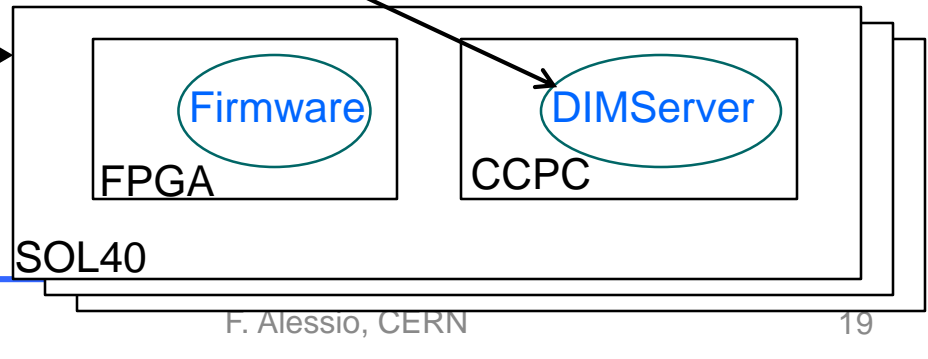


Control PC

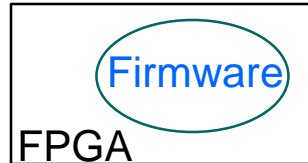


FE Board

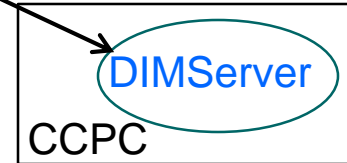
GBT Link



SOL40



FPGA



CCPC



Current developments: software

- Will be centrally provided
 - Low-level libraries and command-line tools for the PC of the SOL40
 - Will allow accessing the different FE chips
 - A DIM server running on the SOL40 PC
 - Will implement higher-level commands to configure and monitor the FE
 - A WinCC-OA component(s)
 - Providing the high-level description and access of all electronics components