

# Status report for TFC and ECS\*

F. Alessio, CERN with acknowledgements to Cairo (Caplan), Mauricio (Rivello), Luis (Granado), Joao (Barbosa), Clara (Gaspar), Ken & PH-ESE group

> LHCb Upgrade Electronics meeting 03-09-2015

> > \* here only covered firmware developments





### Reminder: Fast & Slow control to FE



Separate links between controls and data

- A lot of data to collect
- Controls can be fanned-out (especially fast control)

Compact links merging Timing, Fast and Clock (TFC) and Slow Control (ECS).

- Extensive use of GBT as Master GBT to drive Data GBT (especially for clock)
- Extensive use of GBT-SCA for FE configuration and monitoring



### Reminder: main features

One SODIN as Readout Supervisor + one or more SOL40 are used to control a slice of your FE:

- Propagate TFC information to the FE
  - TFC triggers and commands, see <u>LHCb-PUB-2012-017</u> and <u>LHCb-PUB-2012-001</u>
- Propagate ECS information to the FE
  - Configure/control Master GBTX
  - Configure/control Slave GBTXs
  - Configure/control GBT-SCAs
  - Configure/control FE chips
- Receive back ECS information from the FE
  - From all devices at the FE, return path
- Control all of this from WinCC, as usual
  - Within global LHCb ECS





LHCb Upgrade Electronics Meeting, 03/09/15

F. Alessio, CERN



#### Features:

#### start-up synchronization mechanism

#### "Start-of-run" timing diagram



Important mechanism to allow TELL40 to synchronize to the correct event fragment

- See https://indico.cern.ch/event/291719/ for details
- Please comply! And then test it with the firmware on the git repository.



## Features: start-up synchronization mechanism (simulation)





#### Features: start-up synchronization mechanism (firmware)

oder BXID[110]	
oder BE_RESET	
coder BX_VETO	
der EID_RESET	
oder FE_RESET	 U
HEADER_ONLY	
:lecoder SYNCH	
ler BXID_RESET	
coder TRIGGER	
r/MEP_ACCEPT	
der NZS_MODE	
Jecoder RESET	
der SNAPSHOT	
_decoder VALID	
TION_TYPE[30]	 Fh



### Outlook: SODIN firmware

- First complete and tested version is ready on git: SODIN\_v1r06
  - All triggers and commands implemented
  - Including the various synchronization mechanisms for FE-TELL40
  - Including trigger/command decoding block in SOL40
    - Sub-detectors should come with their favorite bit/command ordering for their Front-End and I will include it in the .vhd
    - Based on the mapping at the GBT side
- To-do:
  - Still missing the ODIN bank towards the FARM (for later)
  - Throttle handling between SODIN-TELL40
  - Tests with FE chips/developers
- Next step: architectural developments
  - What technology for TTC backbone? Technologies evaluation with ESE group.
  - Clock and phase tests with PCIe40. To do with Marseille's group.
  - ... test test test ... with you!



- → SOL40 firmware will take care of doing all the complicated bit manipulations needed to control GBTs, its SCAs and your FE chipsets
  - Single firmware for everybody with all necessary features and requirements
    - $\rightarrow$  minimize unconformities, highly programmable and customizable
    - $\rightarrow$  Modular (can get a core and put it somewhere else in an eval board?)
  - Centrally provided
- $\rightarrow$  In addition it will distribute the TFC commands from SODIN to FE with fixed latency.



#### Features: SOL40-SCA core

Cairo, Ken & FA

It's a firmware core inside the SOL40 firmware which is responsible to:

- control the Master GBT
  - 1 Master GBT per optical link
- control all GBT-SCAs associated to that Master GBT
  - Up to 16(+1) GBT-SCAs per GBT link
  - Serialize/Deserialize with proper encoders (HDLC)
  - Targeting 36 GBTs to start with (programmable at compilation)
    → One SOL40 could cover up to ~600 SCAs and ~9000 I2C devices...
- control all the FE chips associated to those GBT-SCAs
  - Including the Slave GBTs connected to the SCAs (I2C dedicated bus)
  - Support for all GBT-SCAs buses in a programmable way
  - Generic in the sense that it is transparent to your FE chip architecture

For more details, see Cairo's presentation at Electronics Meeting in October 2014 https://indico.cern.ch/event/291724/contribution/2/material/slides/0.pdf The core follows the GBT specs and GBT-SCA specs

• (see <u>GBT project public webpage</u> for details)



1 core per GBT, scalable support for SCAs, all SCA buses, *vendor/FPGA independent*, modular control, error detection capabilities



### Outlook: SOL40 firmware

- Ready and deployed on git: SOL40\_v1r12
  - It also includes the part to control the Master GBTx
  - And SOL40-SCA core with I2C chain fully implemented and validated/qualified, now testing the other protocols
    - We need your FE chip (and you possibly)!
      - → We have setup a test-bench in the ESE lab to welcome you with confort. a ready-to-go setup and a close-by cafeteria ☺
    - Basically bug tracking/fixing from now on
- To do:
  - generic matrix to assign GBT-SCA to pair of bits
  - o retransmission of packets in case something went wrong
  - o checks of transmitted packets, error reporting, semaphores with ECS
  - Programming of FPGAs via JTAG? SPI?
- Next steps:
  - Work ha started in ECS team (Joao, Clara, Luis) to develop the necessary software to control the firmware core in an efficient way
    - Ccserv for Mini-DAQ, server for PCIe40
    - WinCC components (+scripts, panels etc)
    - More news from them at LHCb Week!



#### **Resources utilization**

Analysis & Synthesis Resource Utilization by Entity					
	Compilation Hierarchy Node	LC Combinationals	LC Registers	Block Memory Bits	
1	▲ O Top Level comp	64935 (74)	50241 (33)	13870380	
1	Clocks_Generator:Clocks	44 (12)	38 (6)	0	
2	Q_SODIN_Top_Level:SODIN	7053 (0)	6610 (0)	195584	
3	A [Q_SOL40_Top_Level:SOL40]	18677 (0)	10377 (0)	8989072	
1	4 [Q_SOL40:SOL40_link1]	18677 (920)	10377 (427)	8989072	
1	ODIN_counters:SOL40_CNT_01	363 (0)	704 (0)	0	
2	SC_IC:SC_IC_SOL40	5899 (6)	2519 (6)	8388608	
3	ISTFC_decoder:TFC_decoder	197 (136)	93 (40)	110592	
4	Ififo_pipeline_2bits:OUT_FE_VALID_PIPE_FIFO	61 (0)	53 (0)	4096	
5	Ififo_pipeline_84bits:OUT_FE_PIPE_FIFO	61 (0)	53 (0)	344064	
6	Ififo_pipeline_84bits:OUT_SODIN_PIPE_FIFO	61 (0)	53 (0)	4096	
7	Ififo pipeline 84bits:OUT TELL40 PIPE FIFOI	61 (0)	53 (0)	57344	
8	Isol40_sca:SOL40_SCA_CORE	11054 (0)	6422 (0)	80272	
4	<pre>&gt; [mep_top:mep_top_0]</pre>	1315 (0)	1167 (0)	1310720	
5	▷ [sld_hub:auto_hub]	93 (1)	77 (0)	0	
6	Itop_level_TELL40:TELL40	13525 (1513)	12514 (945)	2246144	
7	▷ [top_lli_6chs:LLI]	24154 (92)	19425 (36)	1128860	

Mini-DAQ firmware compilation report (24k ALMs / 234 k) Stratix V

- o 1 SODIN
- o 1 SOL40 with 1 core to drive 1 GBT
- 1 SOL40\_SCA core for one GBT and 16(+1) SCAs
- → For a Mini\_DAQ to control 6 GBTs and 16(+1) SCAs+FEs each that would mean ~100k ALMs / 230k
- $\rightarrow$  OK for an Arria X (# of GBTs and SCAs are programmable, so we can optimize)
  - X But we can't fill up a full SOL40 with 48 bidir links and fully loaded FE chips



Ηŀ

#### Software tools to get you started

Cairo, Mauricio, Luis & FA

- Developed first software tools to help you get started and use the firmware efficiently on possible test-benches/lab tests
  - WinCC panels to control SODIN

	🍪 Commands (TFC_DE	V - TFC_DEV; #1)								• 💌
			. Triggers				— Commands			
		Raw	Raw Rates (kHz)	Gated	Gated Rates (kHz)		Raw	Raw Rates (kHz)	Gated Ga	ted Rates (kHz)
	Orbit	231741192	11.846			FE Reset	3		4	
😵 Vision_2: TFC Local Run Control (TFC_DEV - TFC_DEV; #1)	Bunch ID	0x0000000				BE Reset	0	]	2	
Module Panel Scale Help	Random A	3330164876	1054.852	1316511453	1050.552	BXID Reset	231741202	11.846	231741202	17.769
📄 🖄 📽 📽 🖁 🕹 🔽 🤹 🕂 🗖 🧔 🖓 11 en_US.iso88591 🔽	Random BB	2752005312	7862.651	0	0	EID Reset	1018812366		1018812370	
DeviceName: Version Date State: PLINNING	Random B1	1703414102	87.231	0	0	TFC Reset	2	]		
SODIN_GBTtest.Core0 1.06 20131204.03	Random B2	1703404487	87.275	0	0	Synch	10	1	12	
Statistics and status — TFC Functions — TFC Functions —	Random EE	3498862891	179.872	0	0	Snapshot	16181	0	16181	0
Orbits 231741192 Periodic Trig. A 115321728 5.92 kHz	Random C	622496274	31.972	432626733	31.957	BX Veto	3461820091	7015.929	3461819086	10523.895
Bunch IDs 0x000 Periodic Trig. B 115321727 5.92 kHz 🔽 Calibration Trg A O	Random D	59563392	3.063	41355685	3.058	NZS Mode	0	0	2	0
Event ID 994249443 Calib. Trig. A 115321725 5.92 kHz Calibration Trg B C	Periodic 1	115321728	5.923	80177287	5.923	EID Accept	1430273966	73.556	1430273965	73.556
Total Triggers 4274240477 Calib. Trig. B 0 0.00 kHz Calibration Trg D 0	Periodic 2	115321727	5.923	80177288	5.923	Throttle	5997	1		
Gated Triggers 4274240313 Calib. Trig. C 0 0.00 kHz	Calibration A	115321725	5.923	80177288	5.923	TELL40 Throttle	0	1		
Trigger Rate 1103.34 kHz Calib Trig. D 0 0.00 kHz F Random Trg B	Calibration B	0	0	0	0		Others			
Inst Trg Loss 0.077 % Random Trig. A 3330164876 1054.85 kHz	Calibration C	0	0	0	0		Raw	Raw Rates (kHz)		
Synch Cmd 10 Random Trig. B0 3498862891 179.87 kHz TAE	Calibration D	0	0	0	0	BXTYPE 00	2409624250	7202.572	EventID Low32	0
Snapshot Cmd      16181      Random Trig. B1      1703414102      87.23 kHz      F NZS Mode      O	Dhusion	0	0	0		BXTYPE 01	4070459700	1753.257	EventID High32	994249443
BX VETO Cmd 3461820091 Random Trig. B2 1703404487 87.28 kHz 7 Snapshot	Auxillion	0	0	0		BXTYPE 10	4070459988	1753.258		
Header Only Cmd 5997 Random Trig. B3 2752005312 7862.65 kHz	Auximary		, 	·		BXTYPE 11	3626227054	31511.267		
NZS Mode Cmd 0 Random Trig. C 622496274 31.97 kHz F Header Only	All Triggers	4274240477	1103.338	4274240313	1655.007					Exit
FE Reset 3 Random Trig. D 59563392 3.06 kHz Lumi Trg O	Lumi B	1-e rate (kHz)	2000.0000	2000.0000	NZS/TAE inhibit length	16	16	1		
BE Reset 0 EID Accept 1430273966 73.56 kHz F MEP Destination	Lumi B	2-e rate (kHz)	2000.0000	2000.0000	TAE half window or # of NZS triggers	2	2		- Offsets	
TFC Reset 2 Basics (TFC_DEV 🗇 🛛 🖾	Lumi e	-e rate (kHz)	1000.0000	1000.0000	# of events in a MEP	15	15	Physics Trigger	3459	3459
SODIN Single Shots	Rando	m C prescaler	256	256	or or or one in a mes	1 10	Apply display	Auxiliary Trigger	512	512
	Rando	m D prescaler	256	256			Apply display	NZS/TAE latency	13	13
Stop RUNNING Cour SystemReset Shoot Single shots Exit			200			Frigger Types	]	OUT latency	4	4
TEC Reset				Apply uisplay	Periodics	9	9			Apply display
SUL40		Calibrati	on Triggers		Calibrations	10	10		Orbit clock	
FE Reset Shoot	Calib A	BXID	3087	3087	Randoms	4	4	External/Internal Ort	oit 🔽 Ext 😐	
BE Reset Shoot	Calib A	periodicity	2	2	NZS	7	7	Orbit length	3564	3564
Cat Baset	Calib E	3 BXID	1199	1199	Luminosity	2	2	NZS/TAE latency	100	100
	Calib E	speriodicity	2	2	Physics	0	0	External orbit missin	ig 🔴	
EID Reset Shoot	Calib C	BXID	2527	2527	Beamgas	1	1	Orbit desynchroniza Orbit presence	ation O	
Synch Shoot	Calib C	2 periodicity	2	2	Auxiliary	14	14			Apply display
	Calib E	DBXID	527	527	Others	15	15			
	Calib D	D periodicity	2	2			Apply display			Exit
				Apply display						



### Software tools to get you started

Cairo, Mauricio, Luis & FA

- Developed first software tools to help you get started and use the firmware as efficiently as possible in test-benches/lab tests
  - WinCC panels to control SODIN + SOL40 + GBT + SCAs
  - Altera Quartus tcl/tk scripts/GUIs to control the SCAs and external chips in a generic way

S Commands (TFC_DEV - TFC_DEV; #1)	S falessio@lhcb-loki:~/amc40/sca_test/tcl_itag
DeviceName <sup>-</sup> Version Date	File Edit View Search Terminal Help
SOL40_GBTtest.Link0 1.12 20150811.02 State: RUNNING GBT CONNECTED	Info: adutorized distributors. Please refer to the applicable
Command SM Counters	Info: Processing started: Wed Sep 2 15:53:54 2015 Info: Command: quartus sto + t sol40 sca eval tool.tcl
SOL40> SODIN Offset 0 0 BXID Reset 41636425	JTAG client running under quartus_stp
SOL40> TELL40 Offset 0 0 EID Reset 0	D2 SOL40 SCA evaluation tool
SOL40> FE Offset 3400 3400 FE Reset 0	null ECS Command
TFC> SOL40 Delay      0      0      BE Reset      0	
Apply display Header Only Cmd 0	Nope Unused Length Protocol Specific
NZS Mode Cmd 0	12C 2   8   0.01 0008001 12C Channel D3 D2 D1 D0
GBTx address 0x1 0x1 BX VETO Cmd 3185598872	Nope 02 01 00 00 02010000 Client connection status: Connected
Commands FIFO flags Responses FIFO flags Apply display Snapshot Cmd 2921	12C Channel 06 05 04 03 06050402 Port number: 2540 Disconnect
FULL © EMPTY © FULL © EMPTY © Synch Cmd	12C 2 D11 D10 D9 D8 0%
Subdetector Type	122 Channel 00 00 00 00 00 0000000 00000590 D15 D14 D13 D12
	00000500 00 00 00 00 0000000
	Send Command
Control GBTx on VDLB Control GBT:SCA on VDLB Test GBT Logic Reset IC Reset Cnt Reset Stop RUNNING Exit	GBT# SCA# CH# JTAG readwrite:
	0 9 0 9 12C(2 9 00 POII 0000000 Address (hex): 0 Read
🕸 SCA (TFC_DEV - TFC_DEV; #1)	Get Reply Data (hex): 0 Write
GBT Device: SOL40_GBTtest GBT_Master0 SOL40 Link: SOL40 GBTtest Link0 Start Register ckCtr0 # of Registers 363	ECS Reply
ttcCtr ckCtr txCtr rxCtr serCtr desCtr wdogCtr gbld fuse inEportCtr o	GBT# SCA# CH# CMD
Register Address Write Read	Error Length Protocol Specific
ttcCtr18 22 0 0 0 Set All	
ttcCtr19 23 0 0 ttcCtr2 6 0 0 Get All	
ttcCtr20 24 0 0 0 ttcCtr21 25 0 15	
ttcCtr22 26 0 0 1 ttcCtr23 269 0 88	D11 D10 D9 D8
ttcCtr24 270 0 0 ttcCtr25 271 0 0	D15 D14 D13 D12
ttcCtr26 272 0 0 ttcCtr3 7 0 0	0000000
ttcCtr4 8 0 0 0	
ttcCtr6 10 0 0	Note of caution: those are not the final software, bu
ttcCtr8 12 0 0 0	Note of caution: these are not the linal software, bu
	only evaluation tools to belo you manage the
	only evaluation tools to help you manage the
Read from FIFO Create GBT type Set Default Config Write Read Exit	TEC+ECS part of the firmware in lab

#### LHCD THCD ONLINE

## Ok, now what?

- SODIN and SOL40 ready!
  - Now you can get your preferred GBT or SCA configured with the Mini-DAQ and with some handy tools
    - Just on time for the VDLBs to come out on the market ...
  - Everything is on git, only documentation is missing (sorry, it will come soon ^\_^)
- Next step(s)
  - Sub-detectors experts are very much encouraged to come to me (and/or Ken) to test whichever system you have in your hands
    - We like challenges so we want it as difficult as it can be
  - ECS friends to develop software to control the firmware, so tune up for the LHCb Week online parallel session if you want to hear more.
- ✓ It is vital to test your FE chips as early as possible to discover noncomformities, problems or even if we need to change anything in our architecture/framework.
  - The sooner, the better\*



#### Backup





## Current developments: software

- Will be centrally provided
  - Low-level libraries and command-line tools for the PC of the SOL40
    - $_{\odot}$  Will allow accessing the different FE chips
  - A DIM server running on the SOL40 PC

Will implement higher-level commands to configure and monitor the FE

- A WinCC-OA component(s)
  - Providing the high-level description and access of all electronics components