Status report for TFC and ECS*

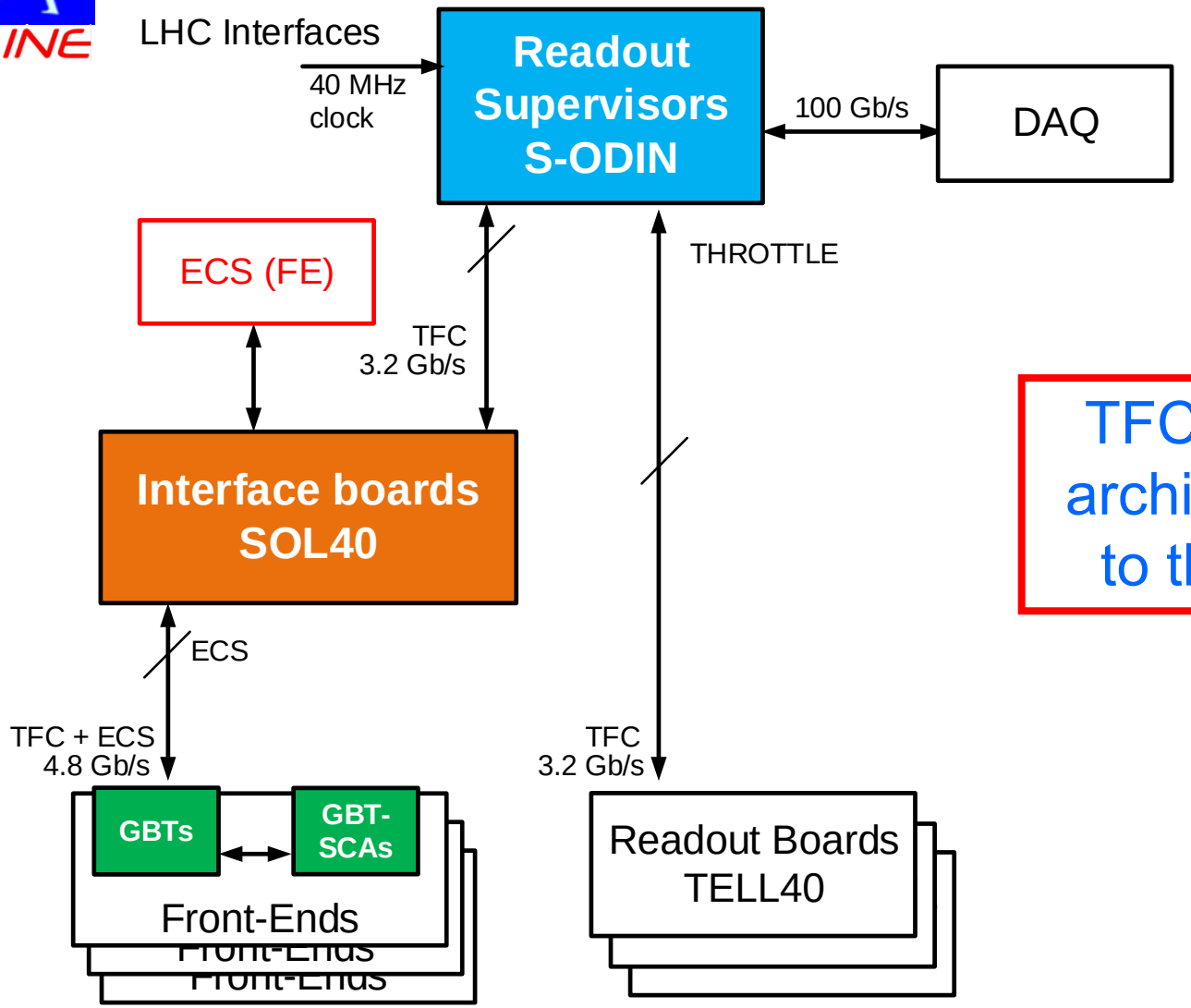
F. Alessio, CERN

with acknowledgements to Cairo (Caplan), Mauricio (Rivello), Luis (Granado), Joao (Barbosa), Clara (Gaspar), Ken & PH-ESE group

LHCb Upgrade Electronics meeting
03-09-2015

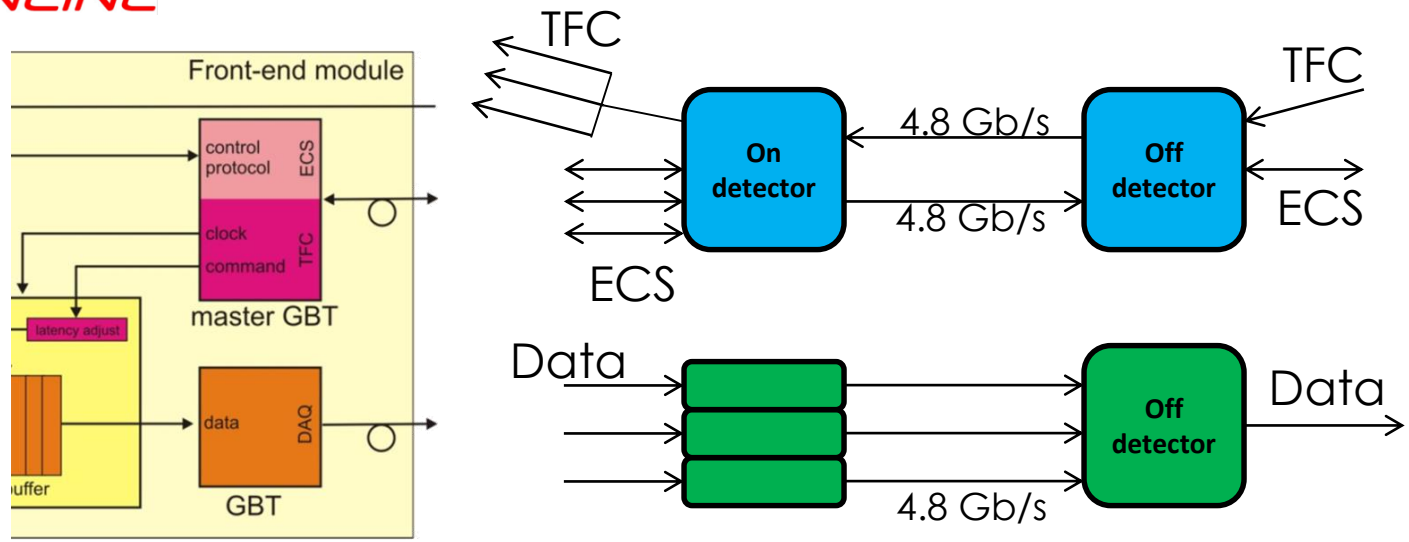
* here only covered firmware developments

Reminder: generic architecture



TFC+ECS architecture to the FE

Reminder: Fast & Slow control to FE



Separate links between controls and data

- A lot of data to collect
- Controls can be fanned-out (especially fast control)

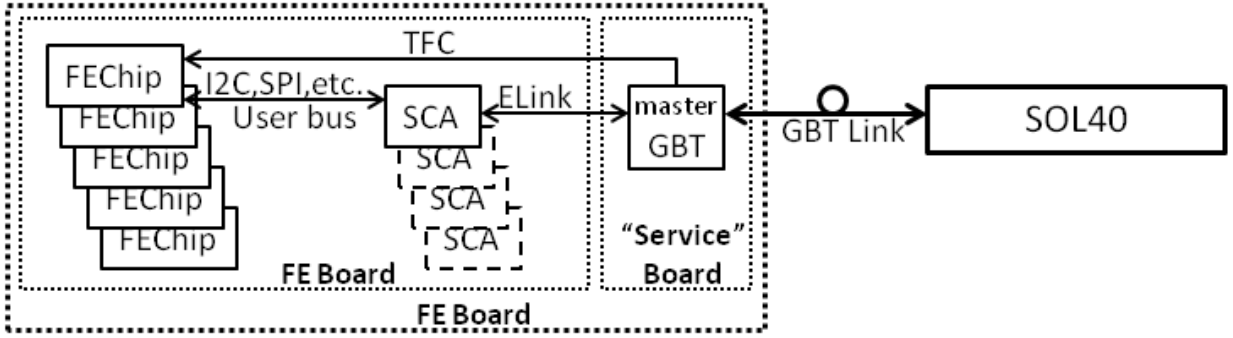
Compact links merging Timing, Fast and Clock (TFC) and Slow Control (ECS).

- Extensive use of GBT as Master GBT to drive Data GBT (especially for clock)
- Extensive use of GBT-SCA for FE configuration and monitoring

Reminder: main features

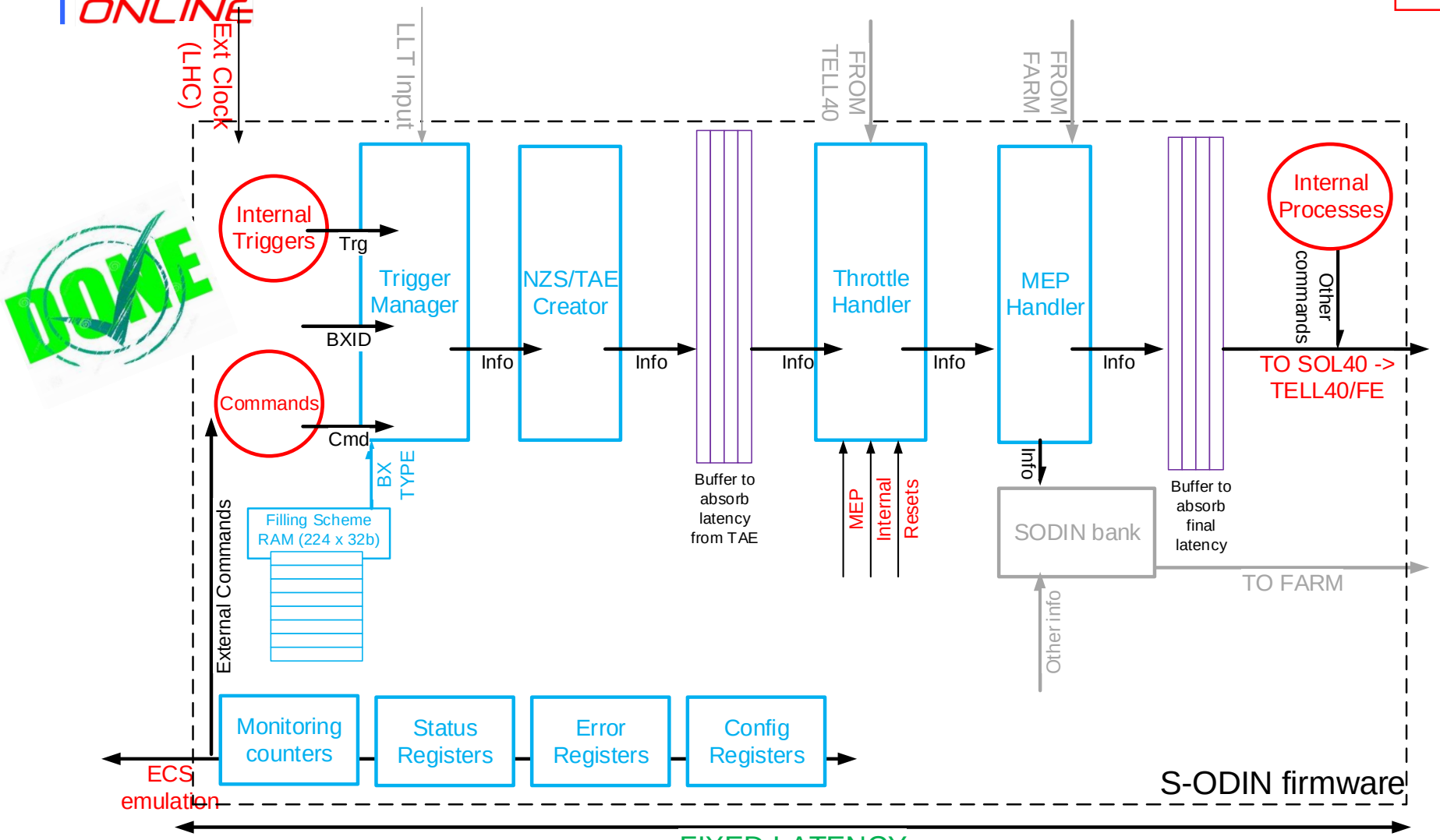
One SODIN as Readout Supervisor +
one or more SOL40 are used to control a slice of your FE:

- Propagate TFC information to the FE
  - TFC triggers and commands, see LHCb-PUB-2012-017 and LHCb-PUB-2012-001
- Propagate ECS information to the FE
  - Configure/control Master GBTX
  - Configure/control Slave GBTXs
  - Configure/control GBT-SCAs
  - Configure/control FE chips
- Receive back ECS information from the FE
  - From all devices at the FE, return path
- Control all of this from WinCC, as usual
  - Within global LHCb ECS

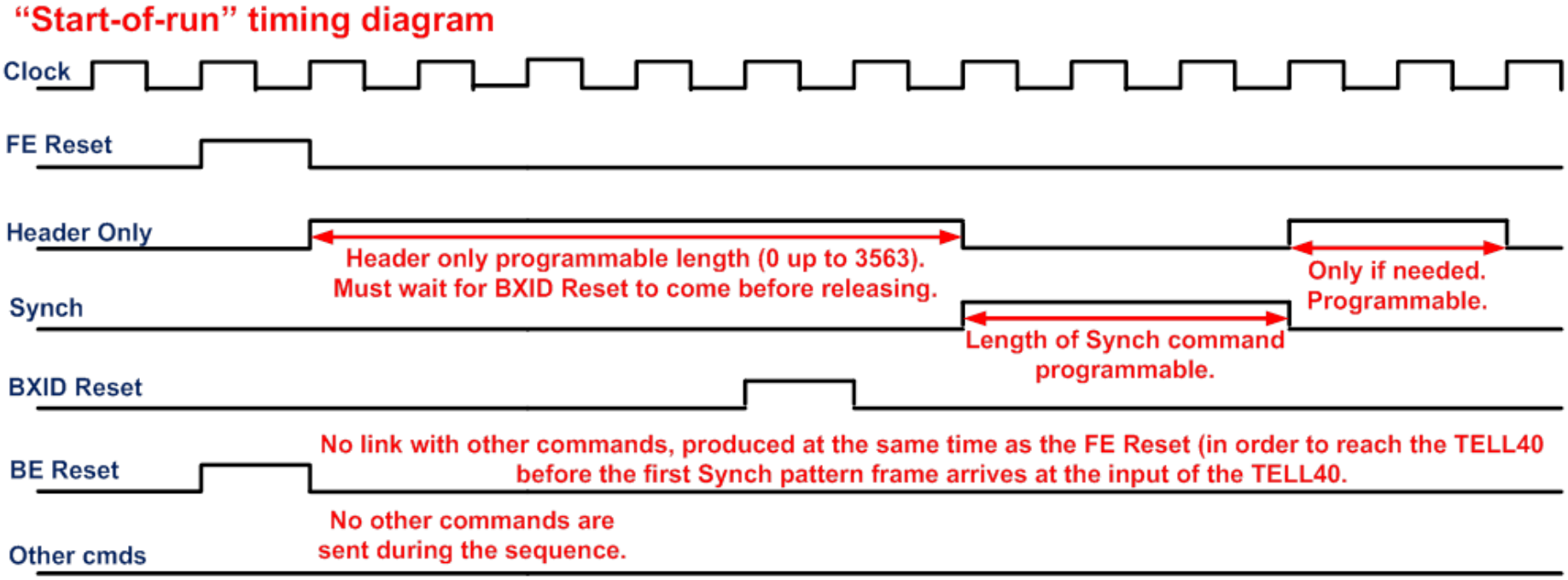


Current developments: SODIN firmware

FA



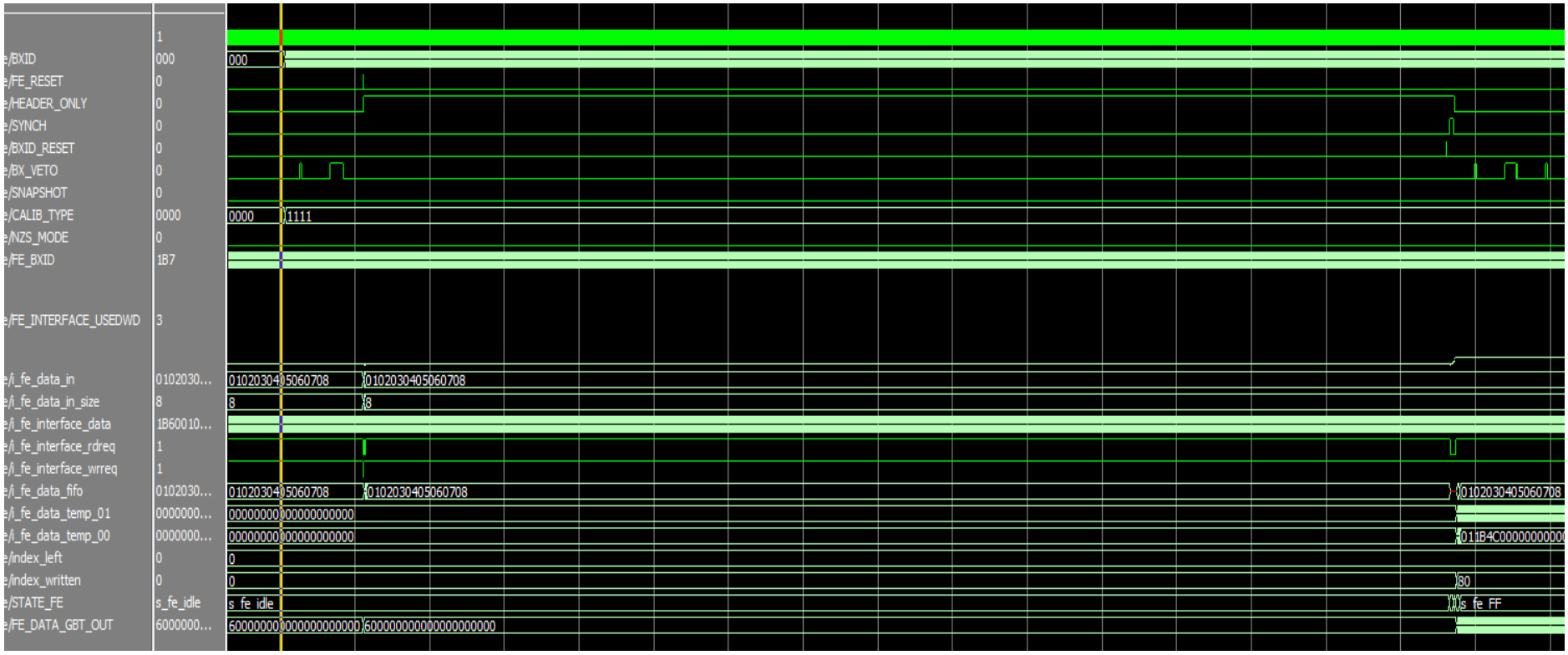
Features:
start-up synchronization mechanism



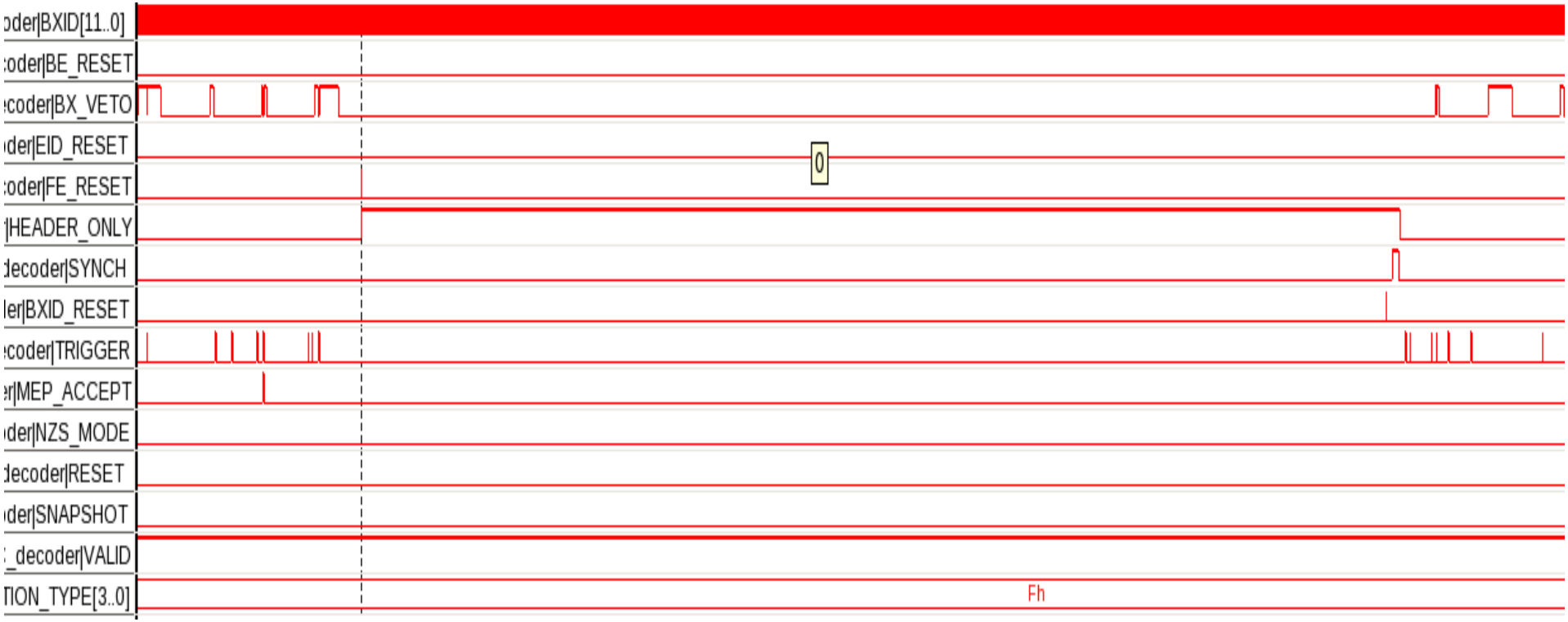
Important mechanism to allow TELL40 to synchronize to the correct event fragment

- See https://indico.cern.ch/event/291719/ for details
- Please comply! And then test it with the firmware on the git repository.

Features:
start-up synchronization mechanism (simulation)



Features:
start-up synchronization mechanism (firmware)



Outlook: SODIN firmware

- First complete and tested version is ready on git: SODIN_v1r06
  - All triggers and commands implemented
  - Including the various synchronization mechanisms for FE-TELL40
  - Including trigger/command decoding block in SOL40
    - **Sub-detectors should come with their favorite bit/command ordering for their Front-End and I will include it in the .vhd**
    - **Based on the mapping at the GBT side**

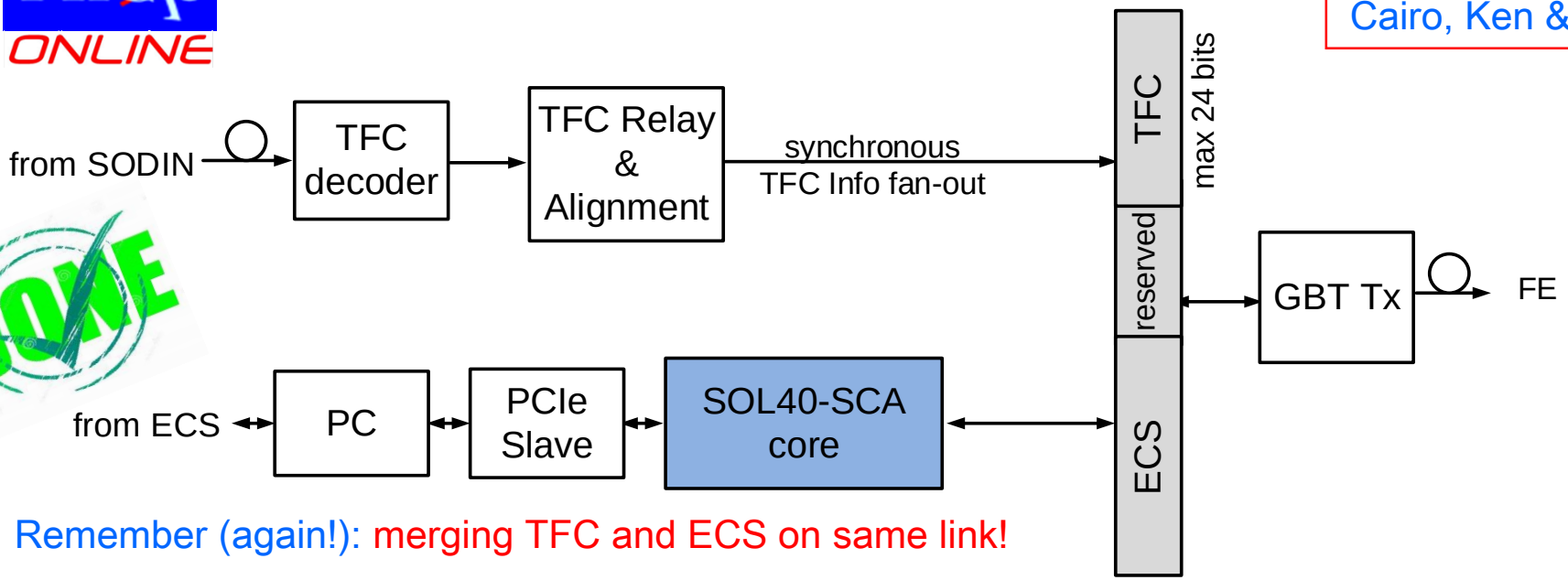
- To-do:
  - Still missing the ODIN bank towards the FARM (for later)
  - Throttle handling between SODIN-TELL40
  - Tests with FE chips/developers

- Next step: architectural developments
  - What technology for TTC backbone? Technologies evaluation with ESE group.
  - Clock and phase tests with PCIe40. To do with Marseille's group.

  - ... test test test ... with you!

Current developments: SOL40 firmware

Cairo, Ken & FA



Remember (again!): merging TFC and ECS on same link!

→ SOL40 firmware will take care of doing all the complicated bit manipulations needed to control GBTs, its SCAs and your FE chipsets

- Single firmware for everybody with all necessary features and requirements
  - → minimize unconformities, highly programmable and customizable
  - → Modular (can get a core and put it somewhere else in an eval board?)
- Centrally provided

→ In addition it will distribute the TFC commands from SODIN to FE with fixed latency.

Features: SOL40-SCA core

Cairo, Ken & FA

It's a firmware core inside the SOL40 firmware which is responsible to:

- control the Master GBT
  - 1 Master GBT per optical link

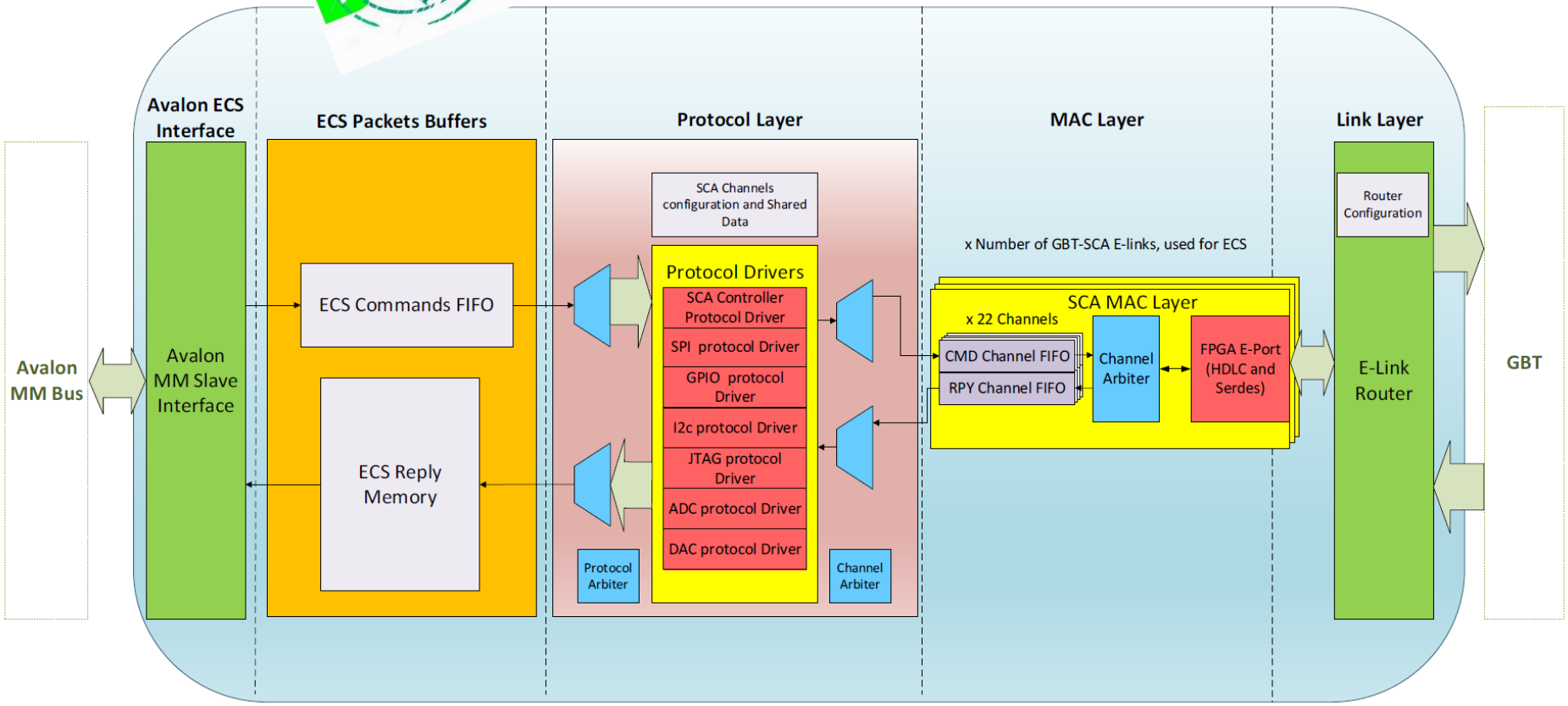
- control all GBT-SCAs associated to that Master GBT
  - Up to 16(+1) GBT-SCAs per GBT link
  - Serialize/Deserialize with proper encoders (HDLC)
  - Targeting 36 GBTs to start with (programmable at compilation)
    → One SOL40 could cover up to ~600 SCAs and ~9000 I2C devices...

- control all the FE chips associated to those GBT-SCAs
  - Including the Slave GBTs connected to the SCAs (I2C dedicated bus)
  - Support for all GBT-SCAs buses in a programmable way
  - Generic in the sense that it is transparent to your FE chip architecture

For more details, see Cairo's presentation at Electronics Meeting in October 2014
https://indico.cern.ch/event/291724/contribution/2/material/slides/0.pdf
The core follows the GBT specs and GBT-SCA specs
  - (see GBT project public webpage for details)

Features: SOL40-SCA core

Cairo, Ken & FA



1 core per GBT, scalable support for SCAs, all SCA buses, *vendor/FPGA independent*, modular control, error detection capabilities

Outlook: SOL40 firmware

- Ready and deployed on git: SOL40_v1r12
  - It also includes the part to control the Master GBTx
  - And SOL40-SCA core with I2C chain fully implemented and validated/qualified, now testing the other protocols
    - We need your FE chip (and you possibly)!
      → We have setup a test-bench in the ESE lab to welcome you with confort. a ready-to-go setup and a close-by cafeteria ☺
    - Basically bug tracking/fixing from now on
- To do:
  - generic matrix to assign GBT-SCA to pair of bits
  - retransmission of packets in case something went wrong
  - checks of transmitted packets, error reporting, semaphores with ECS
  - *Programming of FPGAs via JTAG? SPI?*

- Next steps:
  - Work ha started in ECS team (Joao, Clara, Luis) to develop the necessary software to control the firmware core in an efficient way
    - Ccserv for Mini-DAQ, server for PCIe40
    - WinCC components (+scripts, panels etc)
    - More news from them at LHCb Week!

Resources utilization

Analysis & Synthesis Resource Utilization by Entity

	Compilation Hierarchy Node	LC Combinationals	LC Registers	Block Memory Bits
1	|Q_Top_Level_comp|	64935 (74)	50241 (33)	13870380
1	|Clocks_Generator:Clocks|	44 (12)	38 (6)	0
2	|Q_SODIN_Top_Level:SODIN|	7053 (0)	6610 (0)	195584
3	|Q_SOL40_Top_Level:SOL40|	18677 (0)	10377 (0)	8989072
1	|Q_SOL40:SOL40_link1|	18677 (920)	10377 (427)	8989072
1	|ODIN_counters:SOL40_CNT_01|	363 (0)	704 (0)	0
2	|SC_IC:SC_IC_SOL40|	5899 (6)	2519 (6)	8388608
3	|STFC_decoder:TFC_decoder|	197 (136)	93 (40)	110592
4	|fifo_pipeline_2bits:OUT_FE_VALID_PIPE_FIFO|	61 (0)	53 (0)	4096
5	|fifo_pipeline_84bits:OUT_FE_PIPE_FIFO|	61 (0)	53 (0)	344064
6	|fifo_pipeline_84bits:OUT_SODIN_PIPE_FIFO|	61 (0)	53 (0)	4096
7	|fifo_pipeline_84bits:OUT_TELL40_PIPE_FIFO|	61 (0)	53 (0)	57344
8	|sol40_sca:SOL40_SCA_CORE|	11054 (0)	6422 (0)	80272
4	|mep_top:mep_top_0|	1315 (0)	1167 (0)	1310720
5	|sld_hub:auto_hub|	93 (1)	77 (0)	0
6	|top_level_TELL40:TELL40|	13525 (1513)	12514 (945)	2246144
7	|top_lli_6chs:LLI|	24154 (92)	19425 (36)	1128860

- Mini-DAQ firmware compilation report (24k ALMs / 234 k) Stratix V
  - 1 SODIN
  - 1 SOL40 with 1 core to drive 1 GBT
  - 1 SOL40_SCA core for one GBT and 16(+1) SCAs

→ For a Mini_DAQ to control 6 GBTs and 16(+1) SCAs+FEs each that would mean ~100k ALMs / 230k

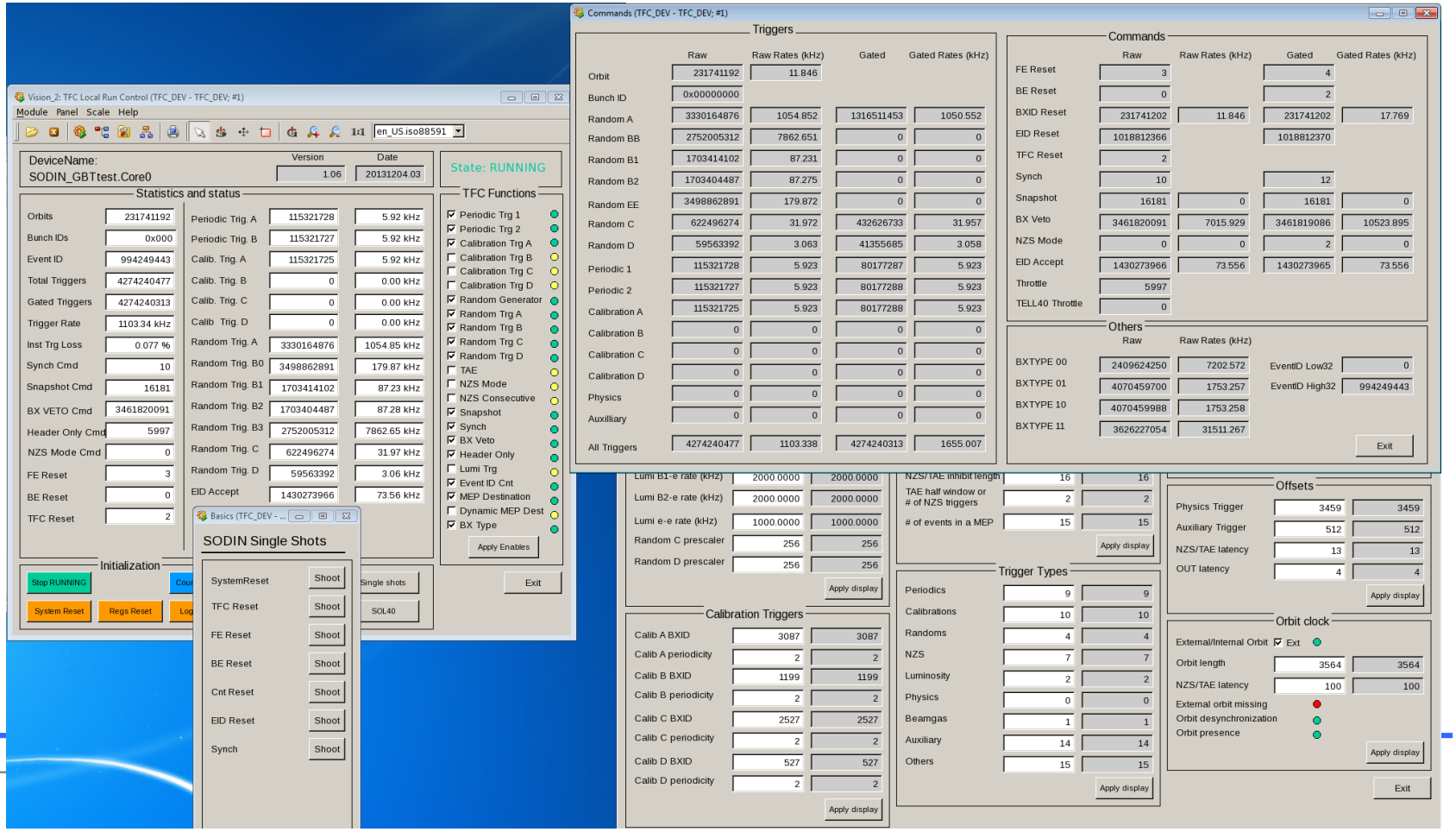
→ OK for an Arria X (# of GBTs and SCAs are programmable, so we can optimize)

X But we can't fill up a full SOL40 with 48 bidir links and fully loaded FE chips

Software tools to get you started

Cairo, Mauricio, Luis & FA

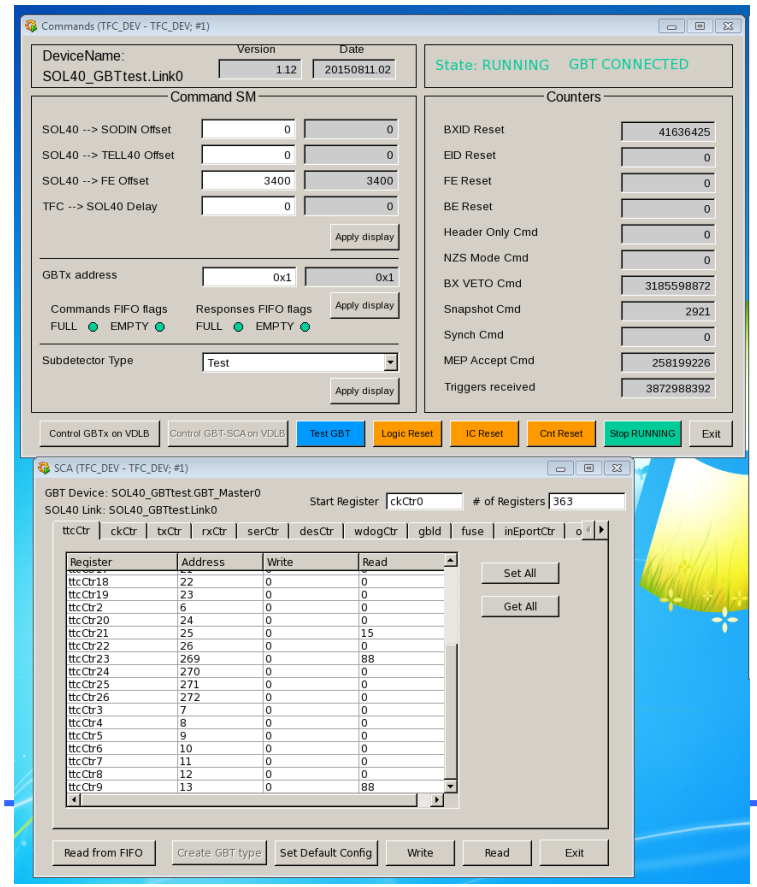
- Developed first software tools to help you get started and use the firmware efficiently on possible test-benches/lab tests
  - WinCC panels to control SODIN

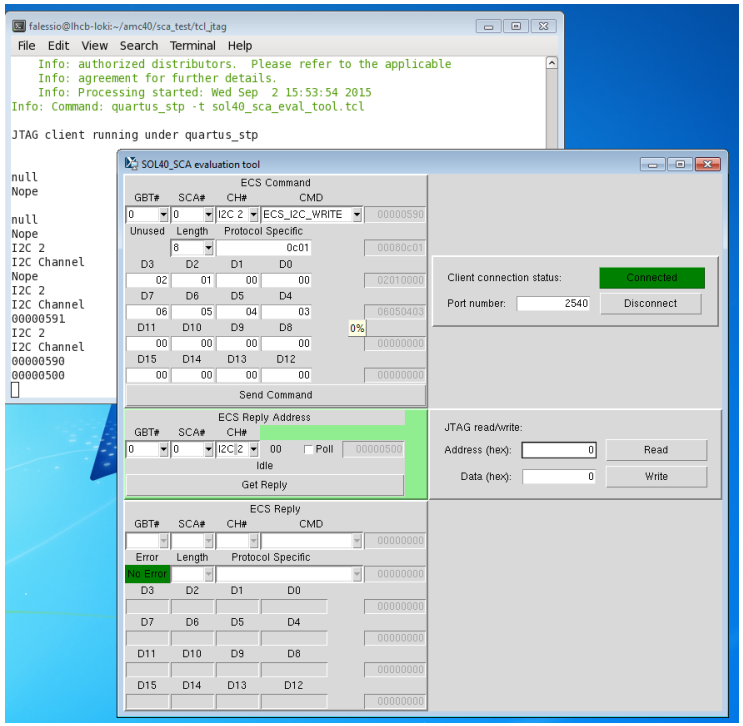


Software tools to get you started

Cairo, Mauricio, Luis & FA

- Developed first software tools to help you get started and use the firmware as efficiently as possible in test-benches/lab tests
  - WinCC panels to control SODIN + SOL40 + GBT + SCAs
  - Altera Quartus tcl/tk scripts/GUIs to control the SCAs and external chips in a generic way





Note of caution: these are not the final software, but only evaluation tools to help you manage the TFC+ECS part of the firmware in lab

Ok, now what?

- SODIN and SOL40 ready!
  - Now you can get your preferred GBT or SCA configured with the Mini-DAQ and with some handy tools
    - Just on time for the VDLBs to come out on the market …
  - Everything is on git, only documentation is missing (sorry, it will come soon ^_^)
- Next step(s)
  - **Sub-detectors experts are very much encouraged to come to me (and/or Ken) to test whichever system you have in your hands**
    - We like challenges so we want it as difficult as it can be
  - ECS friends to develop software to control the firmware, so tune up for the LHCb Week online parallel session if you want to hear more.

✓ It is vital to test your FE chips as early as possible to discover non-comformities, problems or even if we need to change anything in our architecture/framework.

- The sooner, the better*

*I'm going on holidays until the 14th of September, so your request will be taken care of from then on... ☺

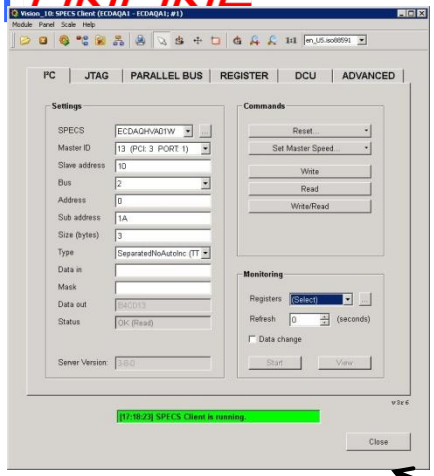
Backup

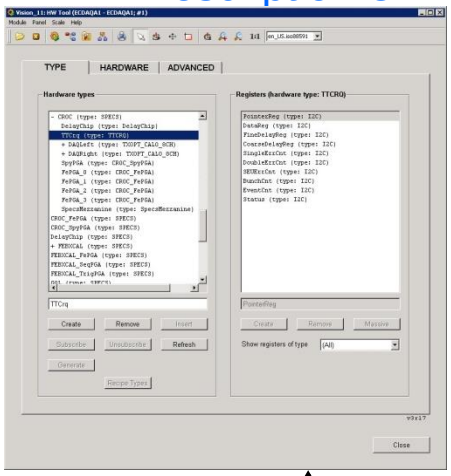
Current developments: software

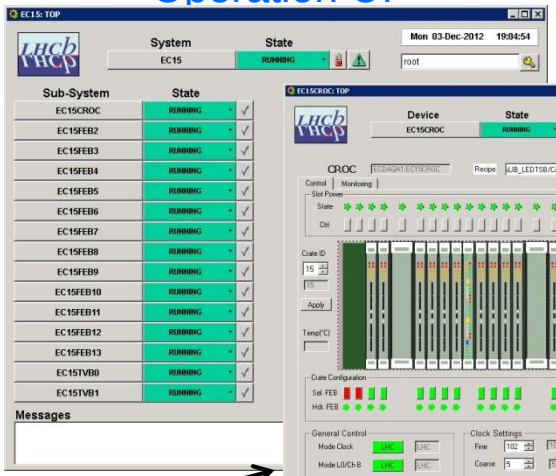
Clara, Luis, Pierre-Yves

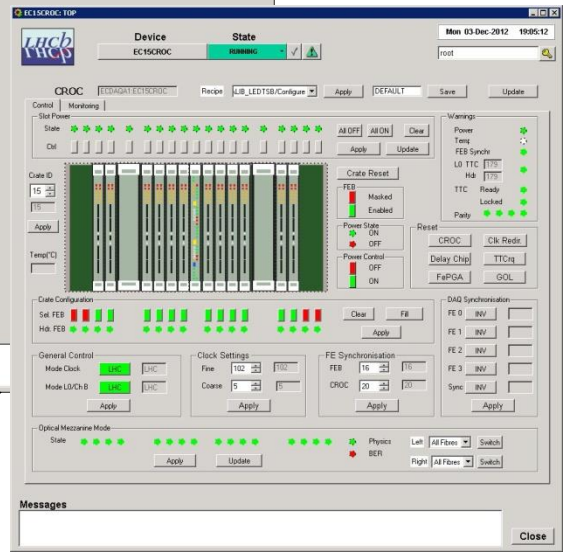
HW Description UI

Operation UI









Test UI

Conf.DB

WinCC-OA

Control PC

FEChip FEChip FEChip FEChip

FE Board

GBT Link

Firmware

FPGA

DIMServer

CCPC

SOL40

Current developments: software

- Will be centrally provided
  - Low-level libraries and command-line tools for the PC of the SOL40
    - Will allow accessing the different FE chips
  - A DIM server running on the SOL40 PC
    - Will implement higher-level commands to configure and monitor the FE
  - A WinCC-OA component(s)
    - Providing the high-level description and access of all electronics components