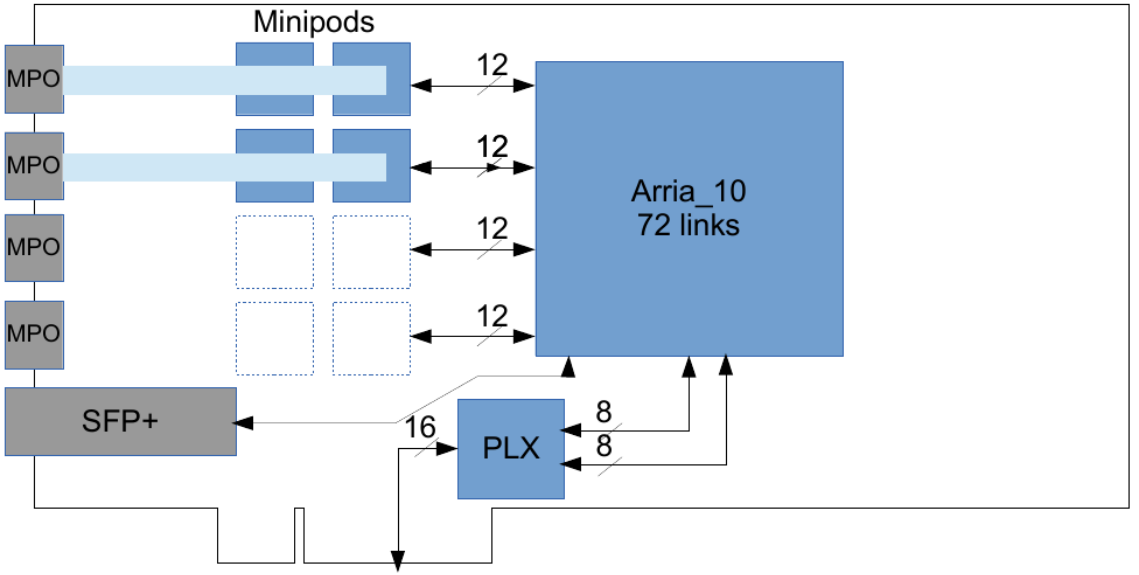
PCIE40
Status of the readout board

K.Arnaud, **J.P. Cachemiche**, P.-Y. Duval,
F. Hachon, M. Jevaud, R. Le Gac, F. Rethore
Centre de Physique des Particules de Marseille

PCIE40 overview

Up to 48 optical inputs/outputs
Serial signal up to 10 Gb/s

Bidirectional serial links for the TFC



output bandwidth ~100 Gbits/s through PCIe Gen3 x16

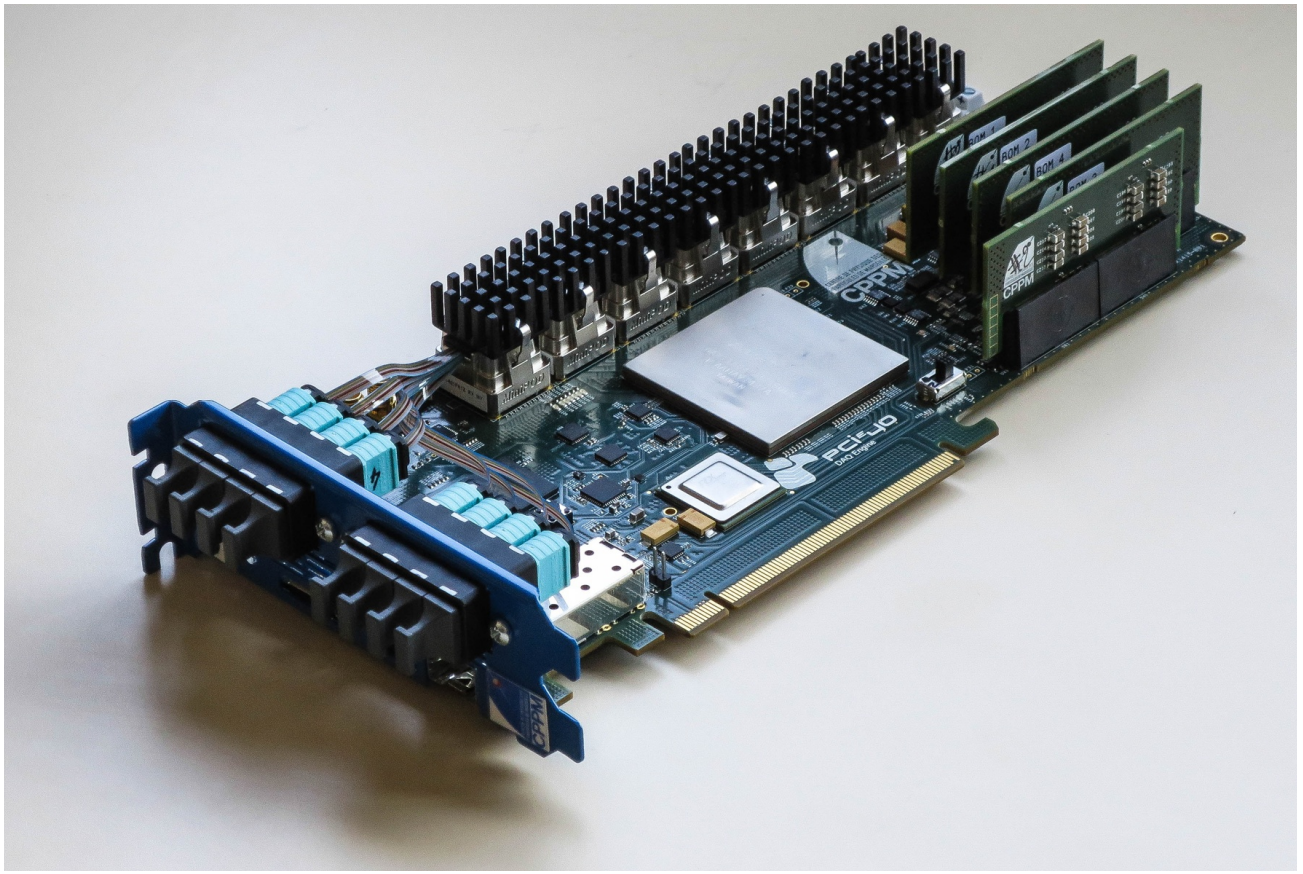
PCIE40 prototypes

First board received end of April 2015.

- *Equipped with an FPGA Arria10 ES1 (limited to GEN2).*

Second prototype received end of June

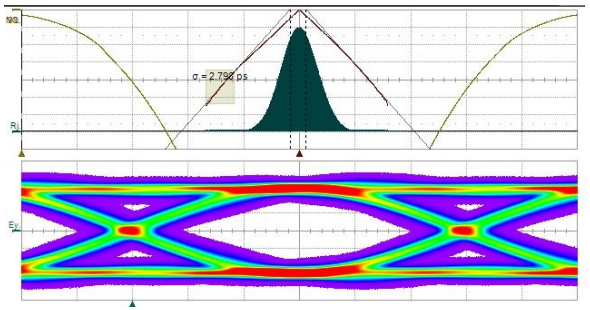
- *Equipped with an ES2 (GEN3)*



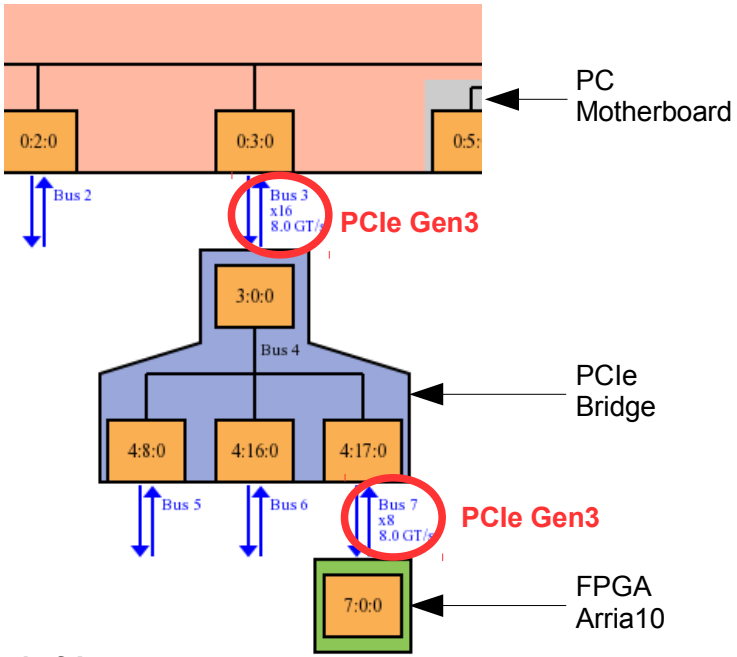
Debug status

Most of data paths and main features validated

Hardware Functionalities	Status
Power	
Power supplies	✓
Power supply sequencing	✓
FPGAs programming	
JTAG	✓
Integrated USB blaster	✓
CVP (through PCIe)	on-going
Flash programming	
Serial	✓
Parallel	✓
FPGA peripherals	
I2C, SPI busses	✓
Main clock PLL	✓
FPGA temperature monitoring	✓
Filtered clock PLLs	on-going
External temperature and current monitoring	on-going
Serial and optical links	
Minipod optical links	✓
SFP+ optical link	✓
PLX PCIe bridge	✓
PCIe interface Gen2 (ES1)	✓
PCIe interface Gen3 (ES2)	✓



Link at 10 gig



→ **Validated end of August**

Specific issue

Bug in Empirion DCDC converter we choosed for core supply

- Will not be fixed by Altera before Q2 2016
  - Too late for miniDAQ2 production

Need to redesign one mezzanine with another component

Server integration

Board is operational in the server

Thanks to Niko, Paolo, Rainer and online team

Next steps on prototype

Functional tests :

- Calibration of optical links (new mandatory feature of Arria 10)
- Access to temperature and current sensors
- Programming the FPGA through PCIe
- Test and qualification of PON interface
  - requires help from Sophie's team
- DMA tests at full speed 100 Mbits/s
  - Requires help from Paolo to implement 2 synchronized PCIe GEN3 busses (firmware and software)
- Fixed lattency clock propagation
  - Federico

Robustness tests

- Measurements and characterization of 48 minipod links and SFP+ link
- Qualification of several heatsinks (commercial, « hand-made », sophisticated …) for cooling
- Measure of FPGA die temperature in function of firmware occupancy and operational frequency
  - With several heatsinks
  - With various air flows and air guides

Next steps for MiniDAQ2

Slight redesign

- Prototype could be dupplicated as is
- Small redesign on main board to ease production
- One of the power mezzanines need a complete redesign, due to issue mentioned before

Production

- Procurement launched for 16 boards
- Availability: end Q1 2016

Contact	Lab	Use	Qty	Comment
Emanuele Santovetti	Universita di Roma	Muon	1	
Tom O'Bannon and JC Wang	University of Maryland	UT	3	
Stéphane TJampens	LAPP	Firmware	1	Already paid
Steve Woton	Cambridge	RICH	2	
Olivier Le Dortz	LPNHE	SciFi	1	
Paula Collins	CERN	Velo	3	
Niko Neufeld	CERN	Online	3	1 DAQ, 1 TFC/ECS, 1 general reference / spare)
Frédéric Machefer	LAL	Calo	0	Can wait final board
Jean-Pierre Cachemiche	CPPM	Readout	2	
		Total LHCb	**16**	

MiniDAQ2 costs

Acquisition board (Tell40 type)

- 24 inputs GBT links for acquisition
- 12 bidir GBT links for control

- *Cost with Server : 14 kCHF*

Control board (Odin type)

- 48 bidir GBT links for control

- *Cost with Server : 16 kCHF*

Funds transfers from groups required ASAP

- TID on CERN account T755020 DAQ-FARM UPG

Note :
Costs based on PC Server = 3942 $ (Upgrade Readout meeting June 17, Paolo)
With current exchange rate : 1,00 USD = 0,97 CHF

PCIe40 LLI status

Already available

- Slow control through PCIe in GEN2
- PCIe DMA full speed on 8 lanes in GEN2 and GEN3
- PLL interfacing and programming
- 24 bidir GBT links (standard mode, wide bus and fixed lattency)
- First QSYS encapsulation, but issues

Next steps

- Serializers calibration
- Slow control in GEN3
- PCIe DMA full speed on 16 lanes

} End Q4 2015

- 48 bidir GBT links
- 48 bidir GWT links
- Encapsulation in QSYS

} End Q1 2016

Conclusion

Prototypes

- The feasibility of a readout board using the PCIe GEN3 standard has been demonstrated
- Still some work for in-depth qualification of current prototype (Thermal aspects, OL quality, PON, …)

MiniDAQ2

- Procurement started
- Funds transfers needed mid-October
- Avalaibility end Q1 2016

Toward the final board

- Market survey on-going
- Decision on PLX removal and power mezzanine suppression to be taken by end 2015
- PRR mid-2016
- Production of pre-series should start in 2016