The upgrade of the CMS Tracker for HL-LHC

Duccio Abbaneo
PH-CMX

Requirements for the High-Luminosity Upgrade

The Pixel detector

- Main challenges
- Sensors
- Readout chip
- Electronics system and detector optimization

The Outer Tracker

- Main challenges and new requirements
- Sensors
- p_T modules
- Electronics system
- Optimization of the detector layout
- Mechanical structures and cooling
- Tracking @ Level-1
- Some performance plots

Requirements for the High-Luminosity Upgrade

The Pixel detector

- Main challenges
- Sensors
- Readout chip
- Electronics system and detector optimization

The Outer Tracker

- Main challenges and new requirements
- Sensors
- p_T modules
- Electronics system
- Optimization of the detector layout
- Mechanical structures and cooling
- Tracking @ Level-1
- Some performance plots

And to conclude... the bill!

Requirements for the High-Luminosity Upgrade

Radiation tolerance up to 3000 fb^{-1}
Keep the possibility to repair the pixel detector
The inner parts could be replaced if needed

Operate up to 200 <PU>
Maintain occupancy at the ~1% level → higher granularity

From the LHC

DAQ compatible with higher L1 rate and longer latency
100 kHz → 750 kHz
3.2 μs → 12.8 μs

Contribution to the Level1 trigger decision
p_T modules in the Outer Tracker

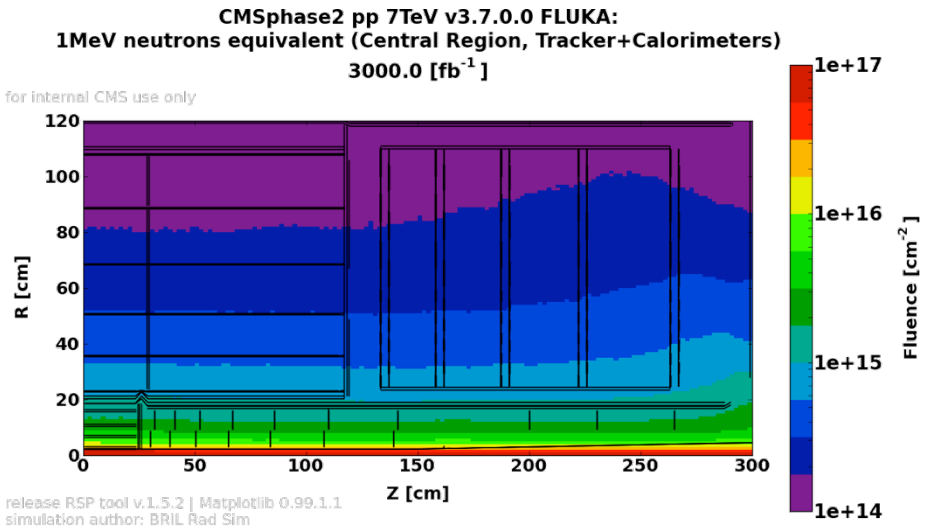
From CMS

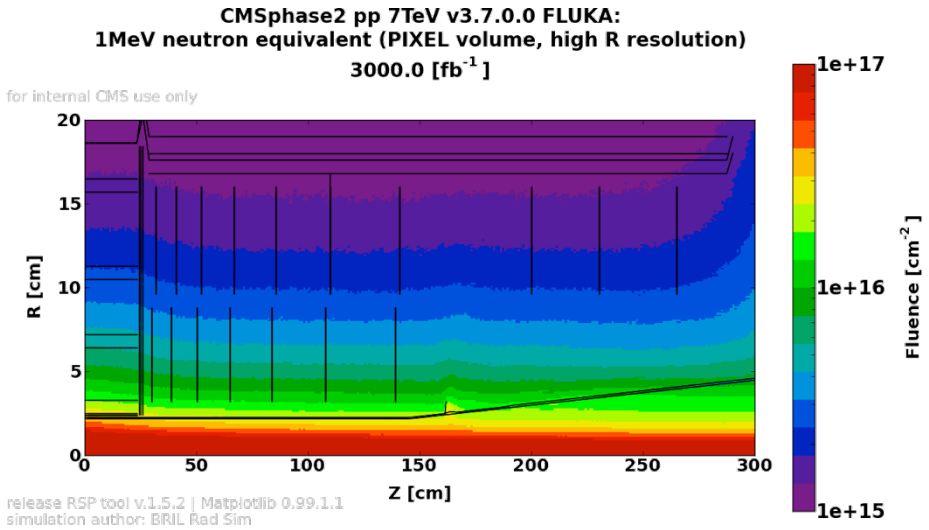
Extended tracking acceptance
Up to η~4 (concerns mostly the pixel detector)
Main purpose: assign jets to primary vertices in the forward region

Reduce material in the tracking volume
The tracker material is a major limitation
to the overall performance of CMS today

Additional improvements

Radiation tolerance





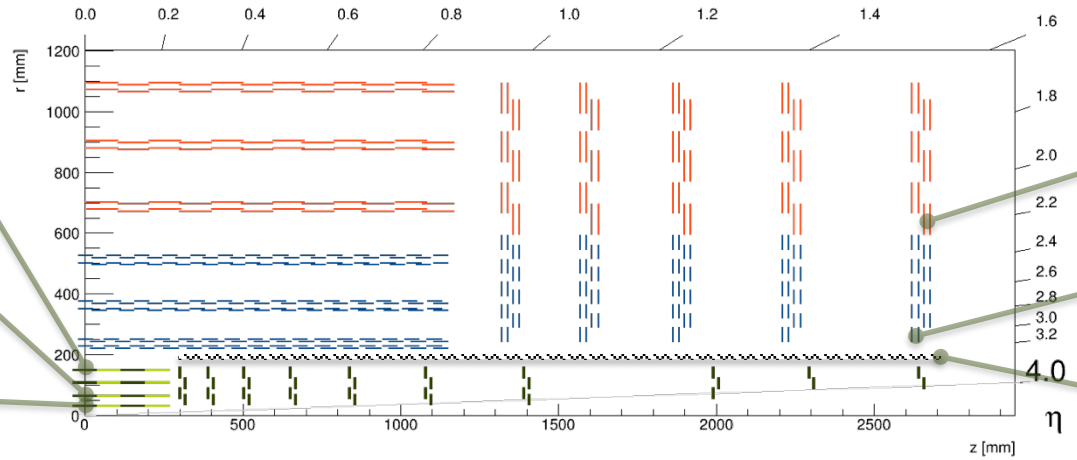
Radiation levels depend essentially on R, not on z

- ✧ The target is 10× present tracker
- ✧ Challenging for silicon sensors and electronics (notably in the pixel region)

Pixel 4th layer
1.6E+15

Pixel 2nd layer
5.8E+15

Pixel 1st layer
2.0E+16



2S modules
3.5E+14

PS modules
9.3E+14

Pixel service cylinder
1.0E+15

Timeline

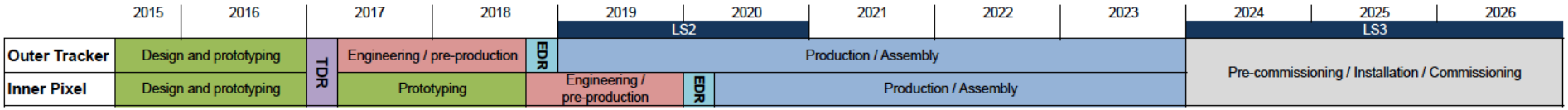
The new Tracking System is due for installation in LS3

The official timeline has still ample margin

Production time can be shorter

Notably for Inner Pixel

Installation will be towards the end of LS3



Next big milestone

The phase-2 pixel upgrade

Radiation tolerance is a major worry, not only for sensors but also electronics!

Huge ongoing effort in RD53 to qualify TSMC 65 nm technology
R&D on thin n-in-p planar sensors, 3D sensors, (n-in-n thin sensors)

Rapidity extension

Main requirement is to match jets to vertices in the forward region
(Anything else is a bonus)

Operate at 200 PU x 750 kHz

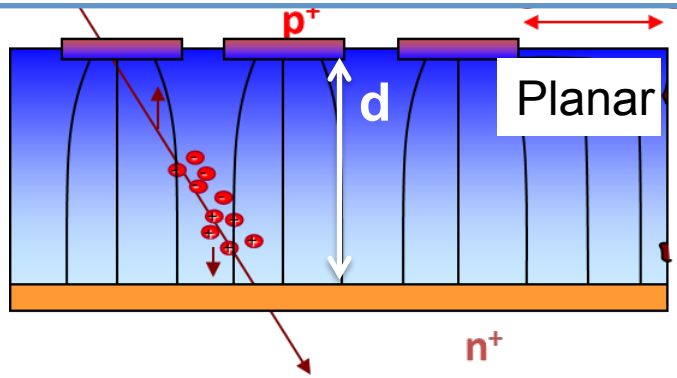
Maintain/improve single hit resolution and two-track separation

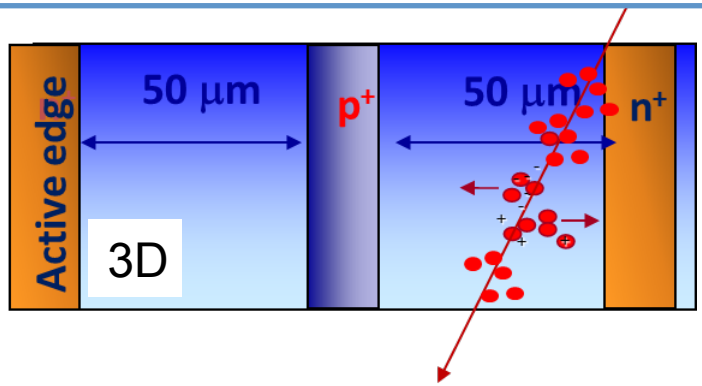
Rad tolerance requirements implies thinner sensors, less charge (100 ÷ 150 μm active thickness).
Achieve hit resolution with less charge sharing and smaller pixels.
Rectangular pixels give lower occupancy and mitigate requirement on pixel chip threshold
(around 1000 e-, under study)

Pixel sensors: thin planar (n-in-p) and 3D

Developing small-area pixels 25 x 100 μm^2 or 50 x 50 μm^2

The most promising for layers with very high radiation damage:
3D and thin planar pixel sensors (100 μm < d < 200 μm)





Common advantages:
- Short drift path
- Higher fields at same V_{bias}

→ Lower operation voltage
→ Less power consumption

Common problem:
- Bump bonding

Thin planar sensors:
- Low total leakage after irradiation
- Less material (multiple scattering)
- Lower occupancy at high η

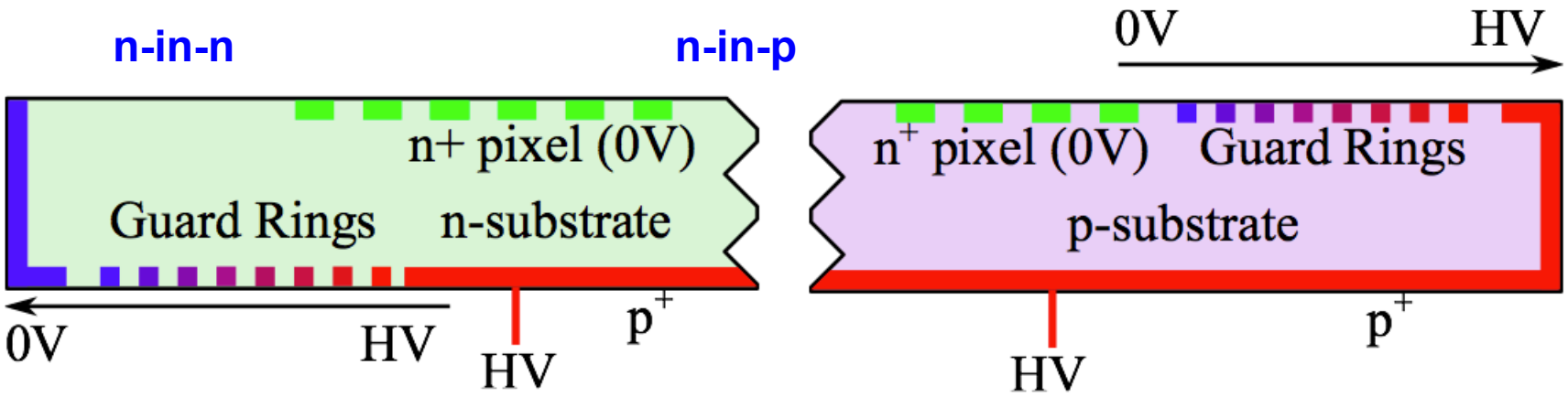
Drawback:
- Smaller initial signal (76e^-/μm)
- Thinning step required
- Thin sensors "bow"

3D sensors:
- Thicker sensor possible

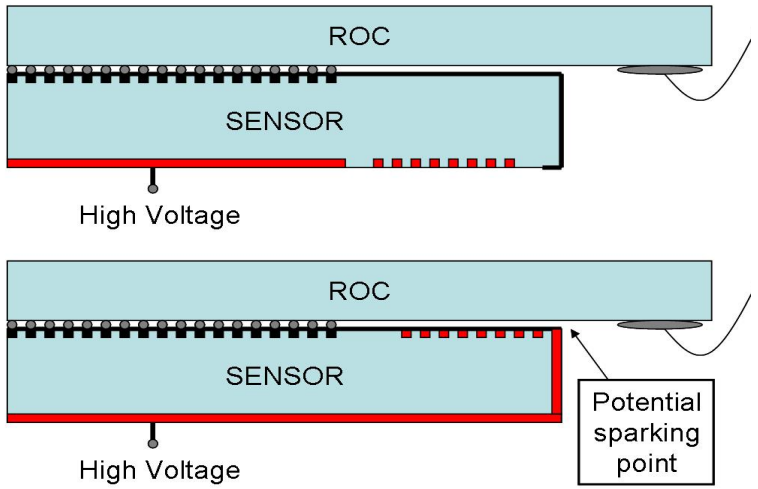
Drawback:
- Higher capacity
- Lower yield
- Higher cost
- Are very small pitches possible?

N.B. Planar n-in-n remains as a valid back-up (more expensive than n-in-p!)
Thinning being investigated

n-in-n vs n-in-p

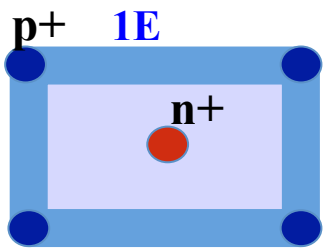


Compare radiation hardness
Address spark protection problem
Consider production issues

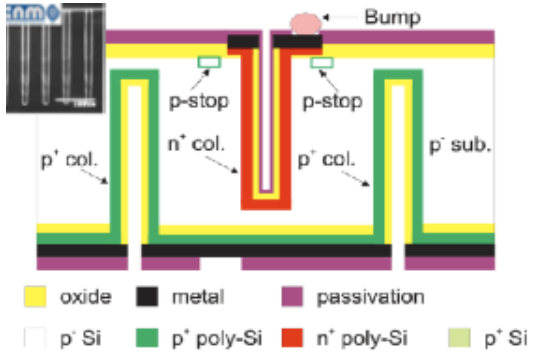


3D sensors

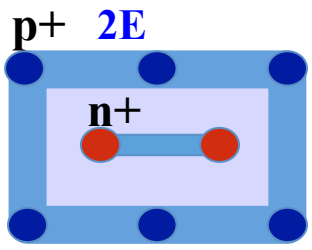
Different techniques to realize the electrodes, and different possible geometrical configurations
- Often linked to different vendors….!



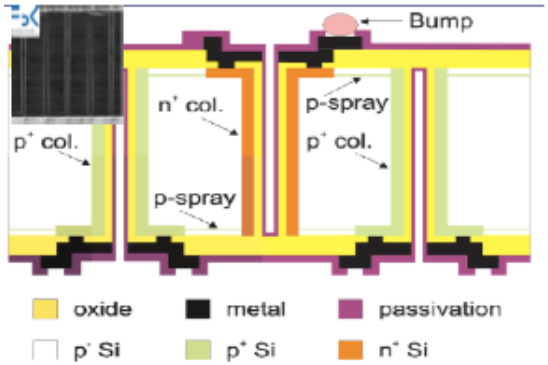
CNM



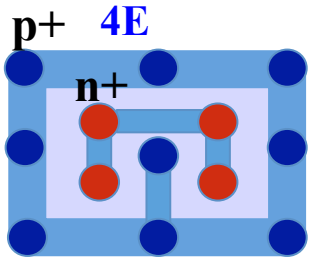
Double side, not passing through columns but **slim edges** (200 μm)



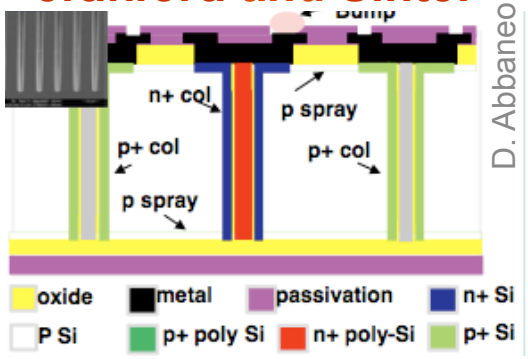
FBK



Double side, full 3D with **slim edges** (200 μm)



Stanford and Sintef



Single side, full 3D with active edges (it requires a support wafer which is removed later)

Specific issues:
- Inefficiency around electrodes
- Advantages progressively reduced for thinner sensors
- Fabrication difficult for small pixels
- COST…

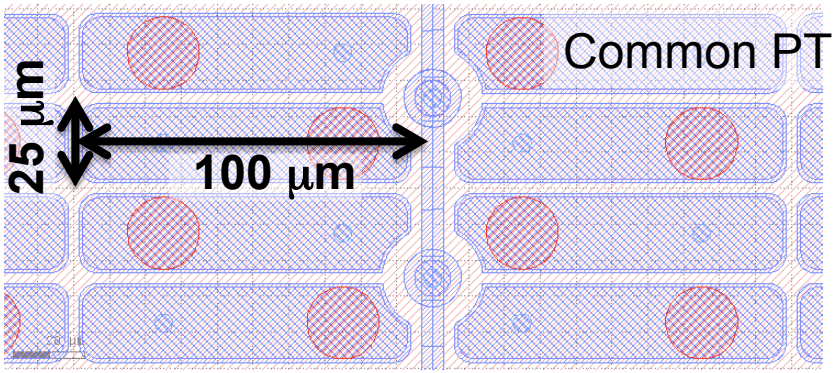
Pixel sensors submissions

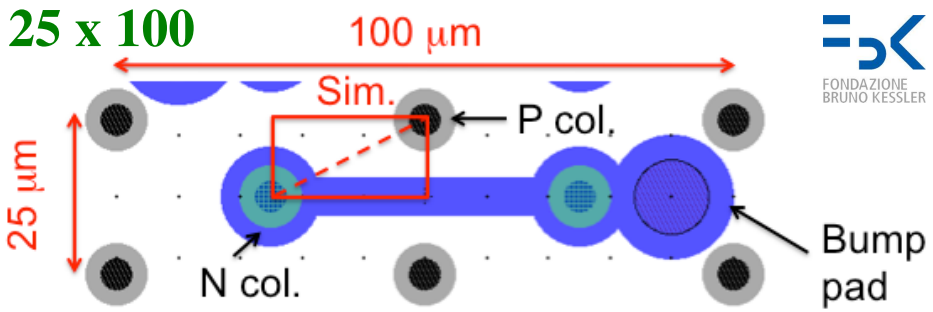
Planar n-in-p
Test of design options and production technologies for fine pitch pixel (25 x 100 μm^2)
- Feasibility of small pitches
- Resolution (in test-beam)
- Radiation tolerance up to which layer?
- Spark protection

Details on the submission:
- N-in-p on 6" wafer
- 150 μm active, 200 μm physical thickness
- Comparison of p-spray and p-stop

3D
Two joint ATLAS & CMS submissions:
1. CNM
- Test of new etching process (DRIE) to increase aspect ratio of columns
- Trial with thicker 3D wafers
- Radiation tolerance with fine pitch

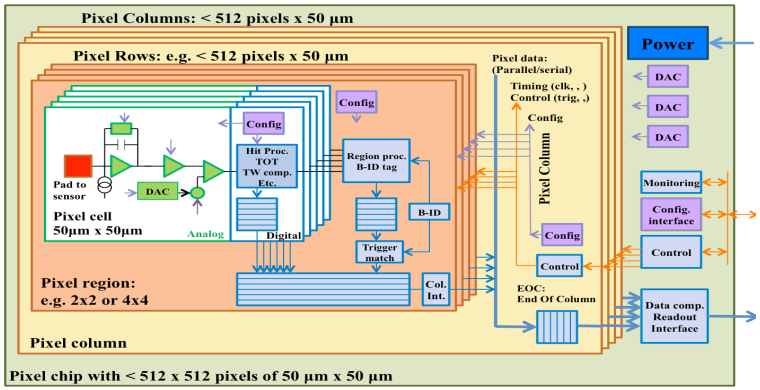
2. FBK
- Test of thin 3D sensors (100 μm & 130 μm)
- Production on handle wafer
- Radiation tolerance with thin 3D





Layout by G.-F. Dalla Betta, presented by R. Mendicino Trento Workshop 2015

Pixel ROC



Developed in RD53

Radiation qualification studies converging

Large effort involving many Institutes
Testing to unprecedented levels (1 Grad)
Finding effects never observed before!
Coherent picture emerging

Outlook:

Wrap up findings, derive design rules for optimal radiation tolerance
Likely achievable goal: chip that functions up to at least 500 Mrad
1 Grad is not (yet) excluded

Design of chip structures continuing
Small demonstrator about to be submitted

Next steps:
Finalize ROC specifications ~ mid 2016
Full-size ROC demonstrator ~ end 2017

Electronics architecture - concept

Envisage modules with 1×4 and 2×4 chips in the barrel, possibly ½ length in the forward (1×2 and 2×2)

1.2 Gbps e-links up to 2m length (or possibly 2.4 Gbps) from FE chips to LP-GBT (on the service cylinders)

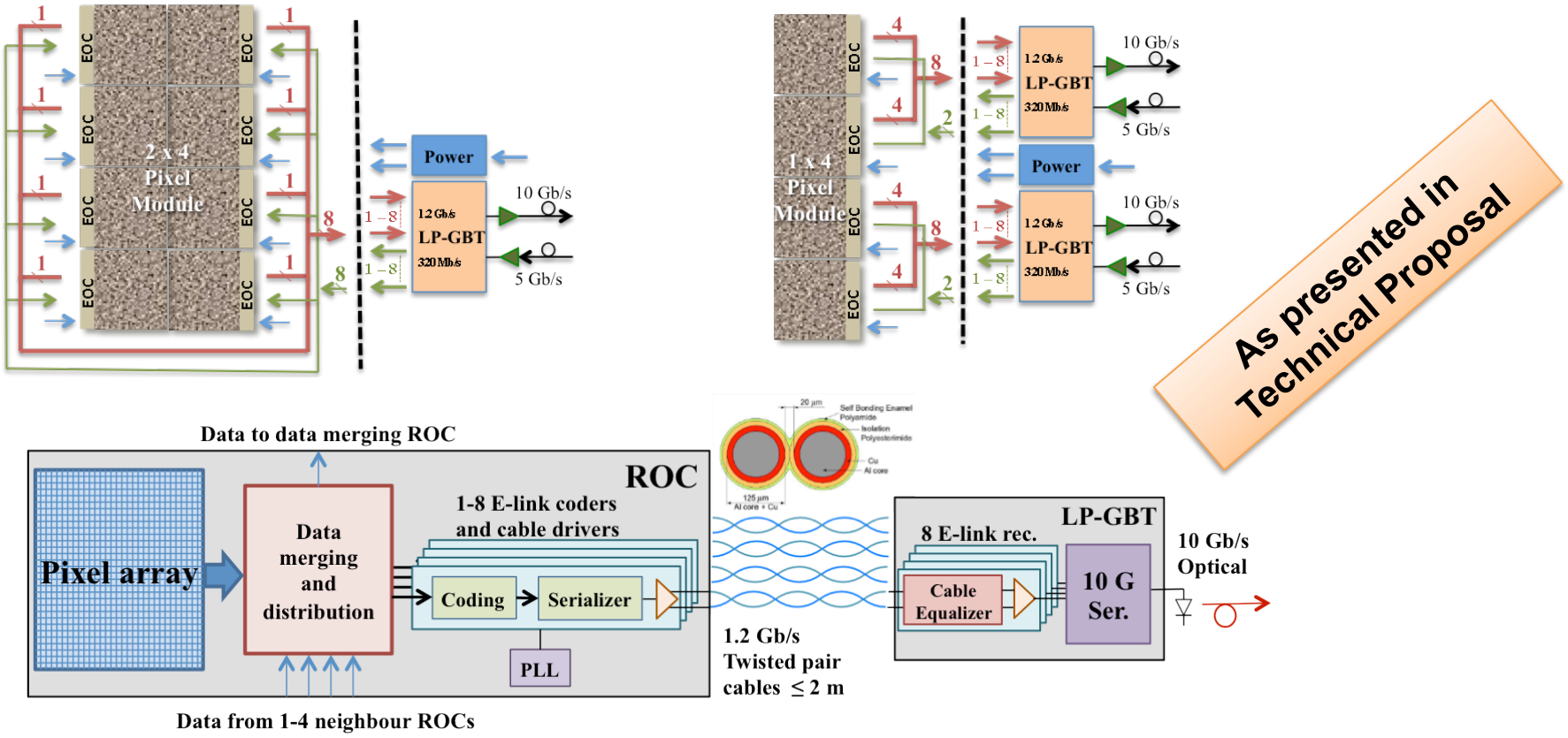
The chip implements data merging functionality

2 or 4 links / chip in the innermost regions (chip can support up to 8); multiple chips into one link in the outer layers

The chip can work with ½ or ¼ of the channels operational

Fine-tune channel density and the link density in the different layers to reduce power and mass

Very flexible architecture!



Electronics system challenges - I

200 PU x 750 kHz → x 30 increased bandwidth wrt to phase-1!

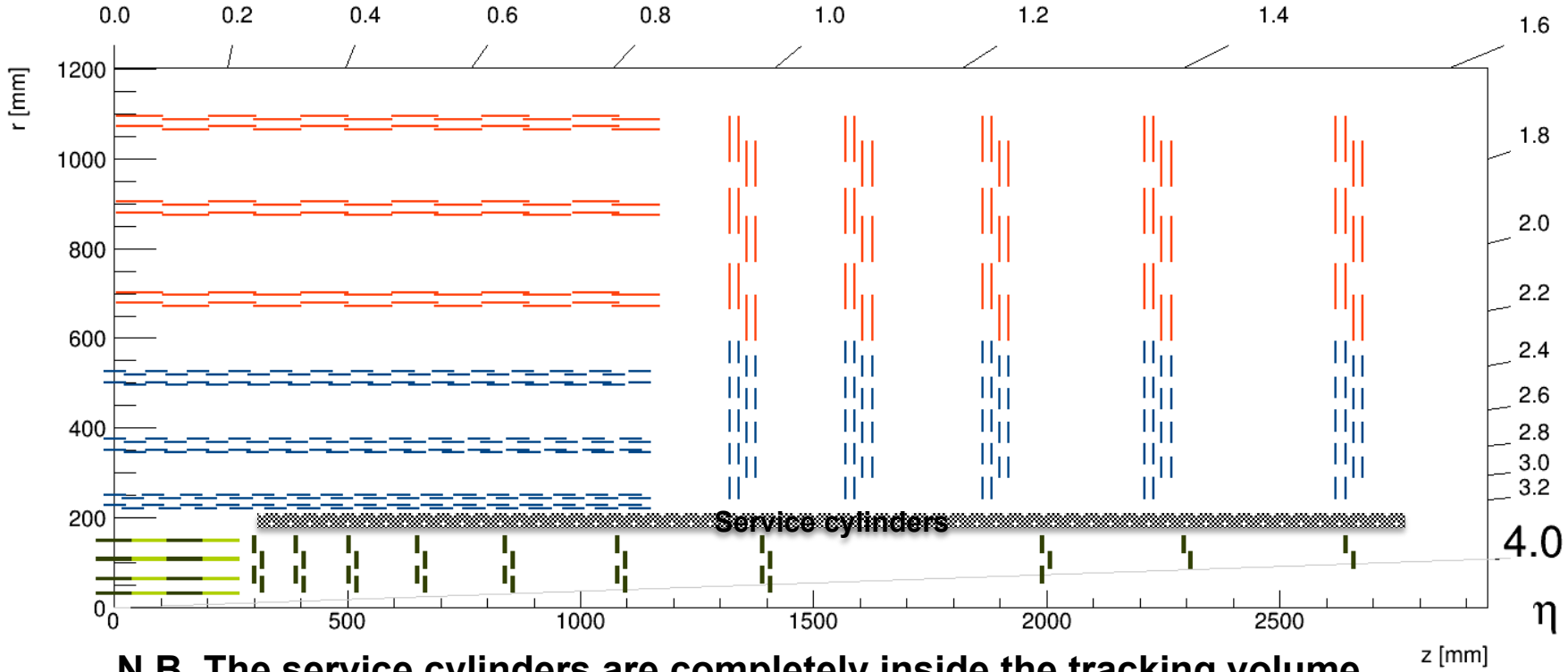
Huge increase of the cross section of electrical links

Optical converters can be integrated on the service cylinders – but not on-module

Need very efficient lightweight e-links!

Implement Feed Forward Equalization

R&D ongoing – simulations and lab tests: early results very encouraging



N.B. The service cylinders are completely inside the tracking volume

Electronics system challenges - II

Higher power, with lower operating voltage → large conductors

DC-DC conversion not very appealing in this case

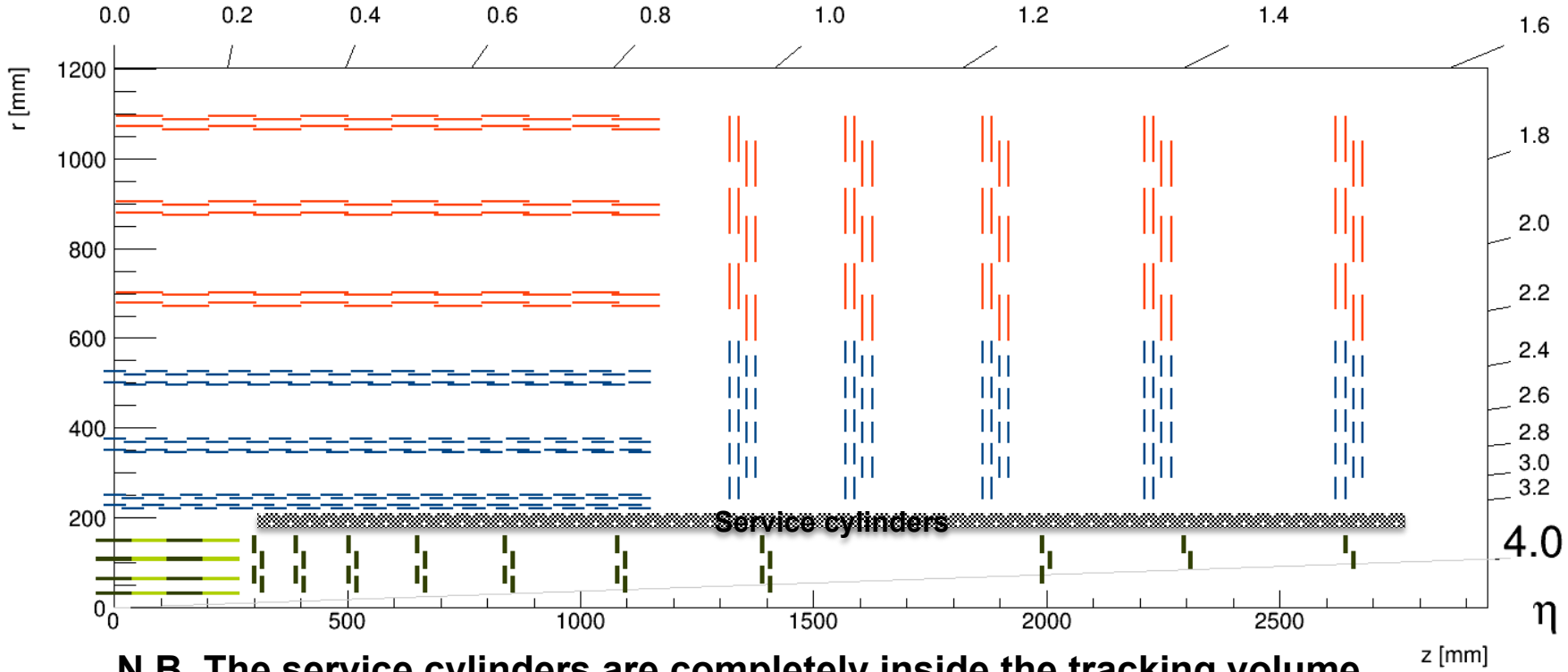
Inductor-based converters are too bulky for a pixel module, and in any case would not survive

If implemented far away from the load (service cylinder) they do not help much

On-chip converters maybe possible with x2 conversion factor – not good enough for material budget

Conclusion: resume R&D on serial powering!

Work just started – collaborate with ATLAS



N.B. The service cylinders are completely inside the tracking volume

Phase-2 data links

Discussion on specs for phase-2 data link is converging
Highly optimized link for use in high radiation
Asymmetric up/down link rate with different forward error correction in the two directions
- High bandwidth required in the downstream (data) link
- High robustness required in the upstream (control) link

"Low-speed " version

Downstream bandwidth 12 /14 links @ 320 Mb/s (3.84 or 4.48 Gb/s)
- (depending on error correction scheme)

Or else 6 /7 links @ 640 Mb/s
Upstream link reduced to 4 links @ 320 Mb/s
- With increased SEU robustness

"High-speed " version

As above with x2 bandwidth in the links
- Some (moderate) penalty in power

E.g. maximum 7 links @ 1.28 Gb/s → Total 8.96 Gb/s

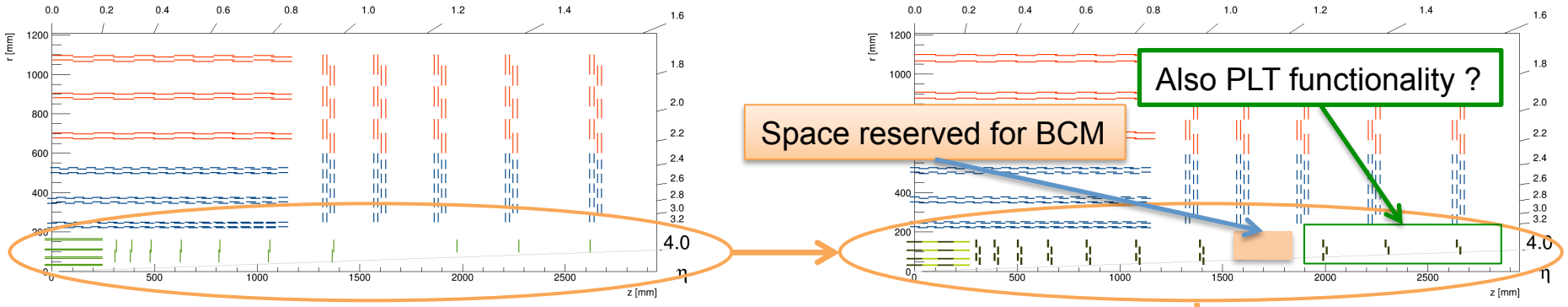
Implementation in a small-size package: huge leap compared to the 400 Mb/s DOH used for phase-1
Suitable development to cope with the x 30 increase in bandwidth requirement
(Suitable also for Outer Tracker)
Limit at 7 links / GBT does not ideally fit our initial Pixel electronics system concept
… some more thinking required… !!

Detector optimization

Geometry used for TP studies: straightforward extension of the phase-1 geometry

Detector optimization ongoing:

- Detailed analysis of achievable hit resolution for different pixel sizes and aspect ratios in the different part of the detector
- Effect on track parameter resolution
- Optimization of geometry to improve rapidity coverage



- Study of routing of services and modelling of material under different assumptions
- Detailed implementation of electronics system concept
- …

Medium-term goal: coherent baseline concept for TDR, with well understood performance

The phase-2 Outer Tracker upgrade

Increased granularity and radiation tolerance

~ one order of magnitude wrt to present tracker

Participate to Phase-1 Trigger decision

"p_T modules" with online data reduction

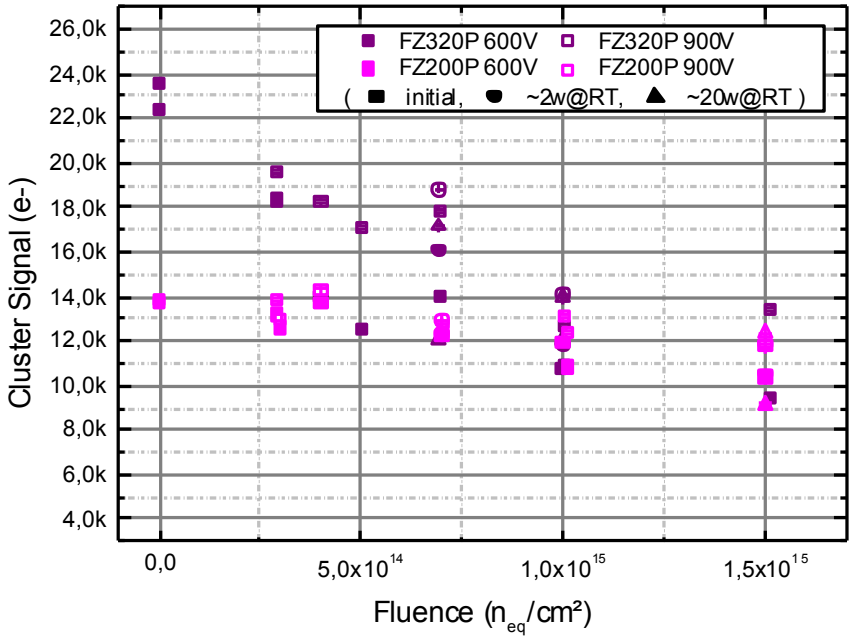
Allows tracking of charged particles with p_T > 2GeV at every bunch crossing

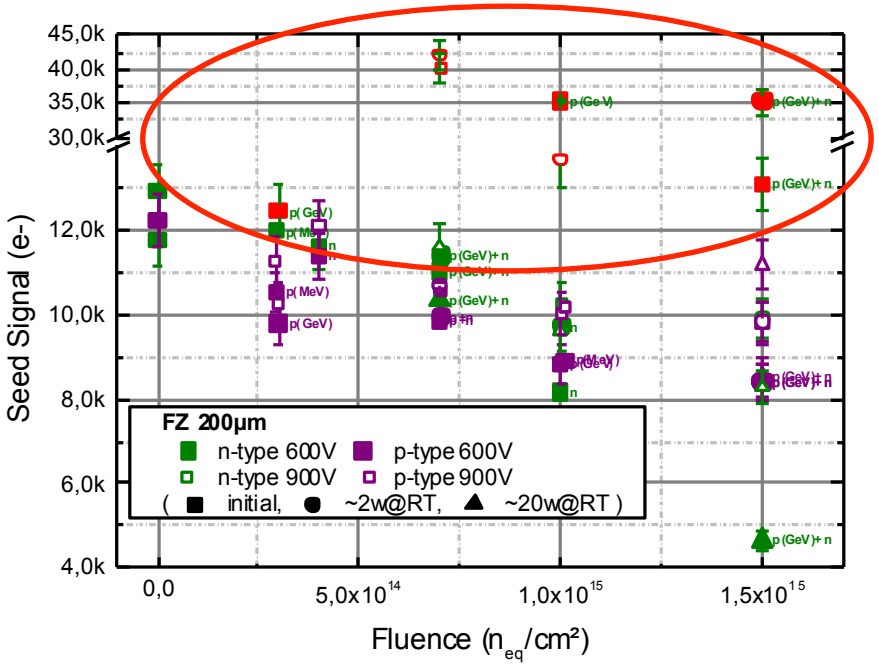
Novel concept of silicon detector modules

Drives design of modules and overall detector concept

Sensors for Outer Tracker

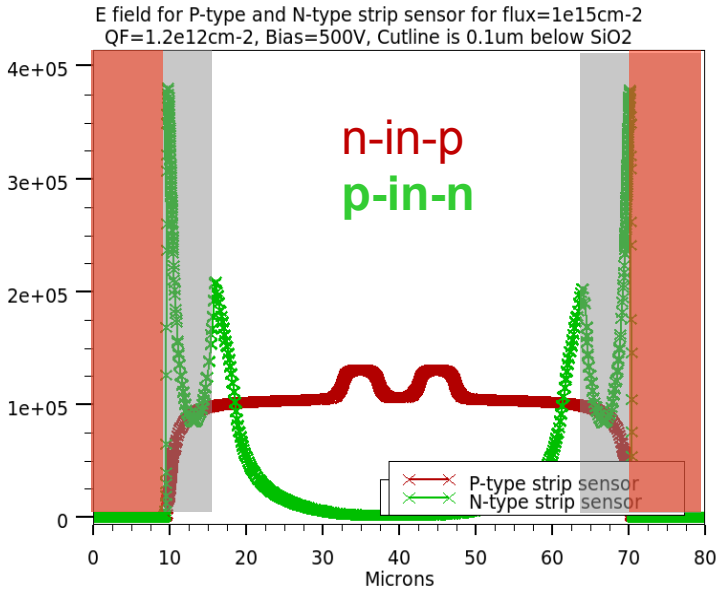
- After heavy irradiation (~10^{15}) charge from 320 µm thick sensors drops down to the same level as 200 µm
  - More trapping
  - In 200 µm the leakage current is smaller, and can be operated at smaller V_{bias}: mitigate requirement on cooling!
- In p-in-n sensors observed spurious signals (random non-gaussian noise, a.k.a. **R**andom **G**host **H**its)



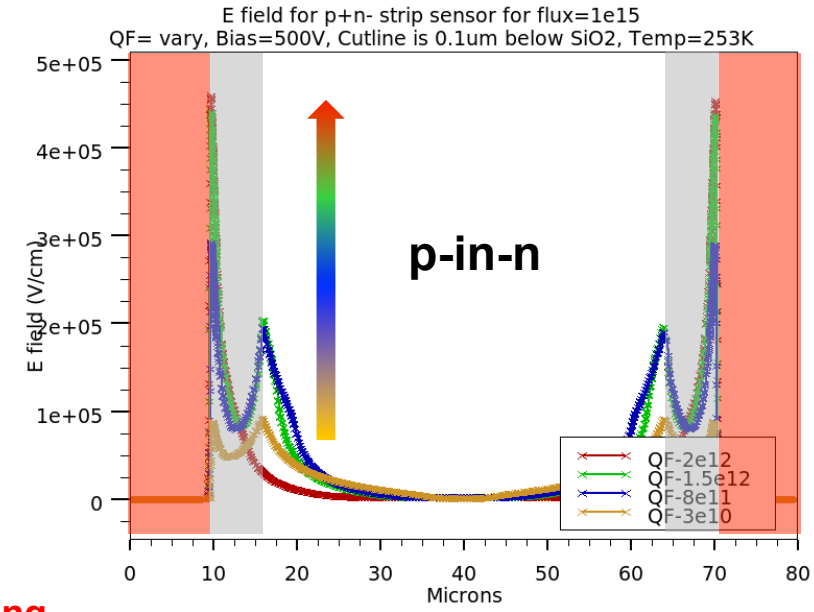


Understanding RGH

- T-CAD simulations show higher electric fields at the strip edges for irradiated p-in-n sensors than for p-type sensors with same geometry
  - Suggests the occurrence of “micro-discharges” in p-in-n
- Increasing oxide charge…
  - increases max. electric fields in p-in-n, reduces max. electric fields in n-in-p
  - Observation: rate of RGHs are smaller for neutron than for proton irradiation
    - ★ less ionization, less surface damage



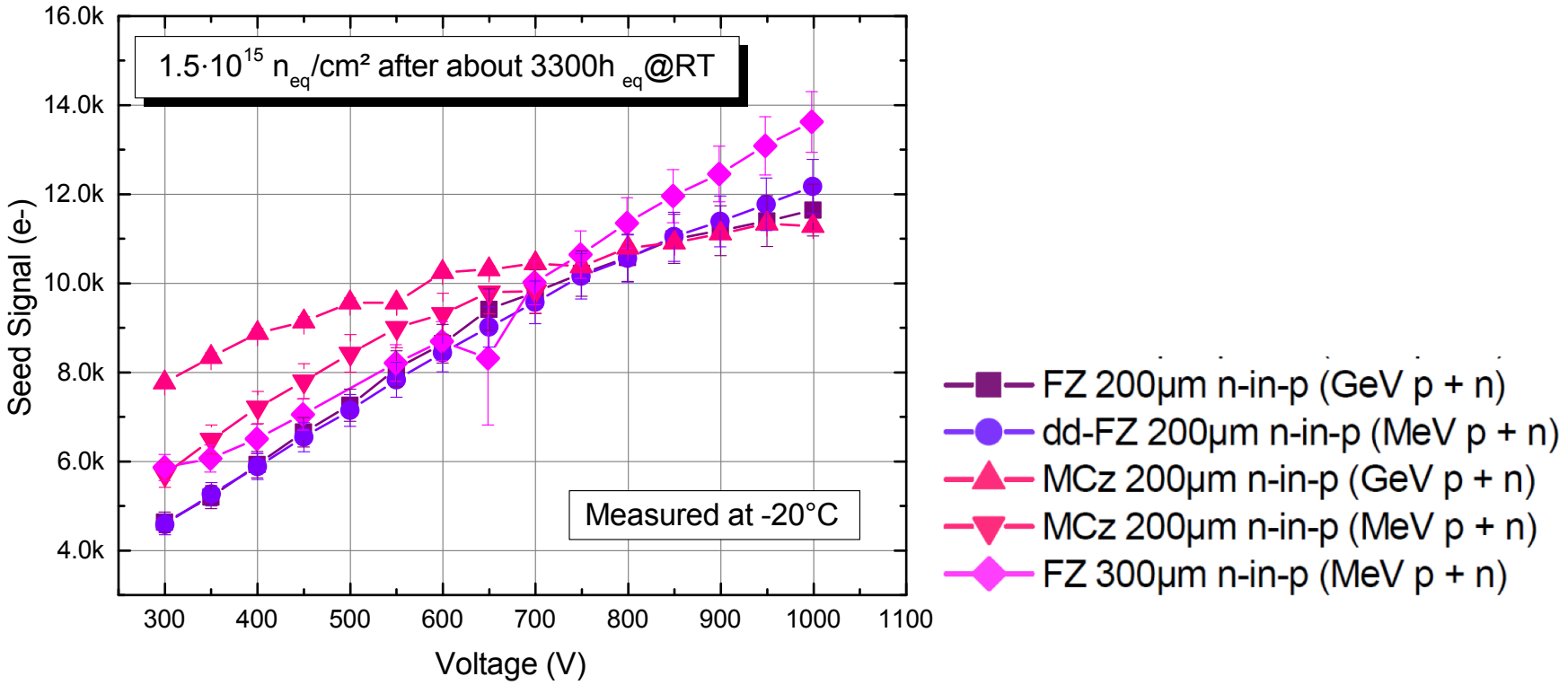
F=1x10^{15}cm^{-2} ; Q_F = 1.2x10^{12}cm^{-2};
U = 500 V; **5-trap model (Silvaco)**



strip doping
aluminum

Annealing

- All thin p-type samples work well and show seed signals >8ke- at 600V until about 20w@RT
- Can be used to reduce the leakage current by keeping the detector at RT for 2 weeks each year, e.g. during YETS
- MCz material shows significantly better behaviour after long annealing time

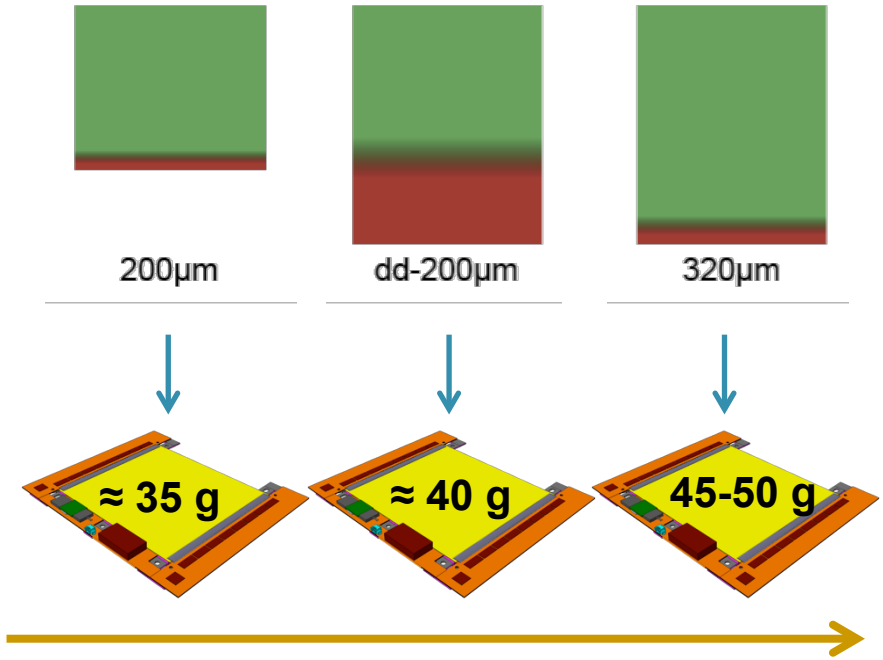


Sensor thickness

- 200 µm active thickness provides sufficient charge
  - Due to smaller charge loss after irradiation
- Adding (inactive) silicon thickness increases the mass
- With larger active thickness the leakage current is larger
  - … and most likely V_{bias} would have to be larger, eventually

→ additional material for thermal management

Example for 2S modules, where the effect is largest



Outer Tracker sensors summary

Basic R&D essentially finished: the main properties of the sensors are defined

- Polarity
  - n-in-p is the selected option, as it offers robust performance (i.e. graceful degradation) after heavy irradiation
- Material
  - MCz is the preferred option (but FZ is OK)
    - Allows for long annealing times with no adverse effects
    - Could be (eventually) operated at lower V_{bias}, mitigating the requirements on the cooling
- Thickness
  - 200 μm active and physical thickness is the preferred option
    - Sufficient charge, good annealing behaviour, lower I_{dark} and V_{bias}
  - 200 μm active 320 μm physical is a good backup
    - Adds 60 kg of inactive material uniformly distributed in the tracking volume
    - Active thickness can also be fine-tuned…

Outer Tracker sensors outlook

Ongoing: qualification of vendors and production options, fine-tuning of sensor design parameters, preparation of Market Survey (with ATLAS)

HPK: well-established reliable vendor, consistently delivering excellent quality; dd-320 μm FZ 6" material available at good price, thinning expensive

Infineon: development ongoing for several years; produced 300 μm p-in-n sensors with adequate quality; now moving to n-in-p, exploring thinning and production on 8"; dd-FZ material also available

Work with other possible vendors (Novati, CiS…)

Procurement of sensors to support module prototyping

Preparation for sensor QA in several labs

Evaluation of new irradiation sources

Tracker input to Level-1 trigger

- μ, e and jet rates would substantially increase at high luminosity
  - ★ Even considering other trigger upgrades
- Increasing thresholds would affect physics performance
  - ★ Performance of algorithms degrades with increasing pile-up
    - Muons: increased background rates from accidental coincidences
    - Electrons/photons: reduced QCD rejection at fixed efficiency from isolation
- Even HLT without tracking seems marginal
- Add tracking information at Level-1
  - ★ Move part of HLT reconstruction into Level-1

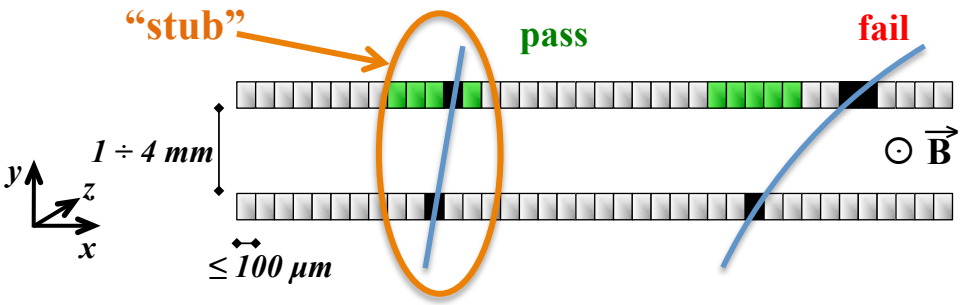
➢ Goal for “track trigger”:

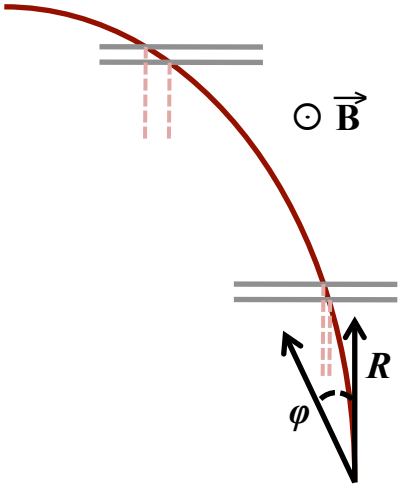
- Reconstruct tracks above 2 GeV
- Identify the origin along the beam axis with 1÷2 mm precision
  - ★ Enables vertex discrimination

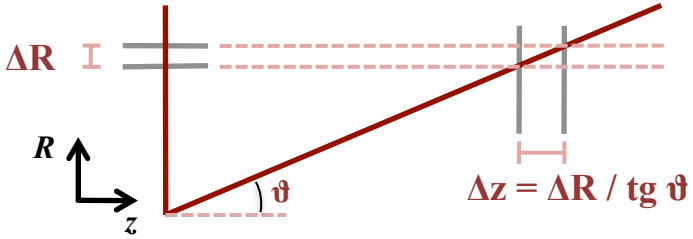
General concept

- Silicon modules provide at the same time “Level-1 data” (@ 40 MHZ), and “DAQ data” (upon Level-1 trigger)
  - The whole tracker sends out data at each BX
- Level-1 data require local rejection of low-p_T tracks
  - To reduce the data volume, and simplify track finding @ Level-1
  - Threshold of ~ 2 GeV $\Rightarrow$ data reduction of ~ one order of magnitude
- Design modules with p_T discrimination (“p_T modules”)
  - Correlate signals in two closely-spaced sensors
  - Exploit the strong magnetic field of CMS
- Level-1 “stubs” are processed in the back-end
  - Form Level-1 tracks, p_T above ~2 GeV
  - To be used to improve different trigger channels

Working principle of p_T modules

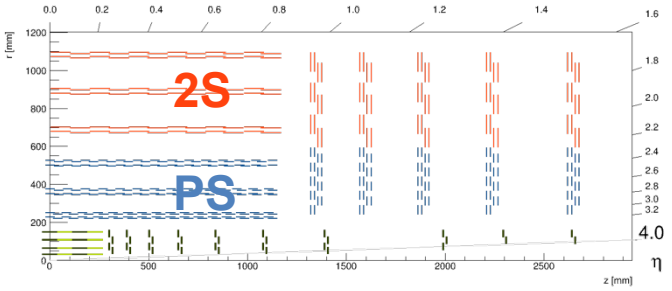




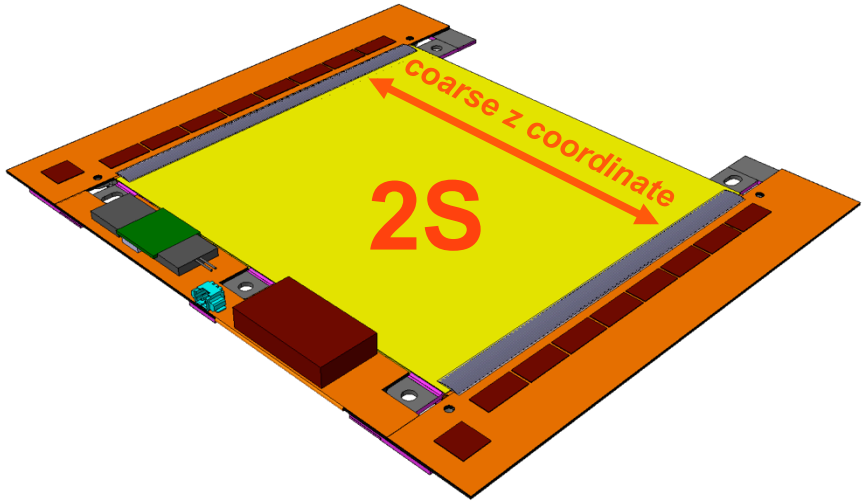


- Sensitivity to p_T from measurement of Δ(Rφ) over a given ΔR
  - For a given p_T, Δ(Rφ) increases with R
  - In the barrel, ΔR is given directly by the sensors spacing
  - In the end-cap, it depends on the location of the detector (tgϑ)
    - End-cap configuration typically requires wider spacing, and yields worse discrimination
- Optimize selection window and/or sensors spacing
  - To obtain, as much as possible, consistent p_T selection through the tracking volume
- The concept works down to a certain radius
  - 20÷25 cm with the CMS magnetic field and a realistic 100 μm pitch

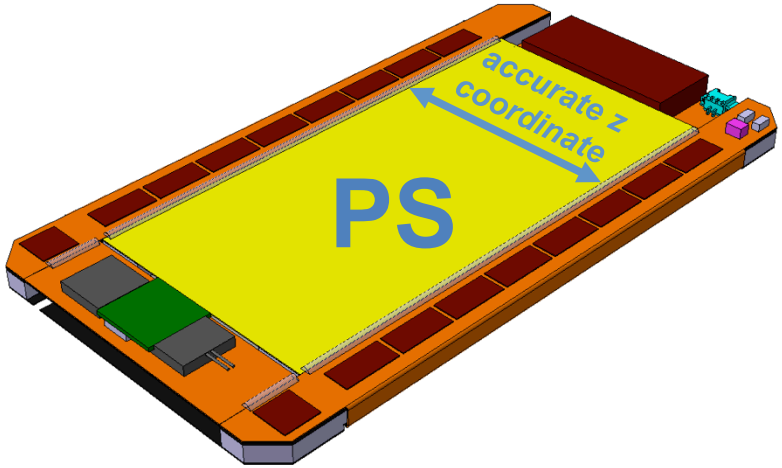
p_T modules



2 Strip sensors
2×1016 Strips: 5 cm × 90 µm
2×1016 Strips: 5 cm × 90 µm
P ~ 5 W
~ 90 cm^2 active area
For R > 60 cm
Spacing 1.8 mm and 4.0 mm



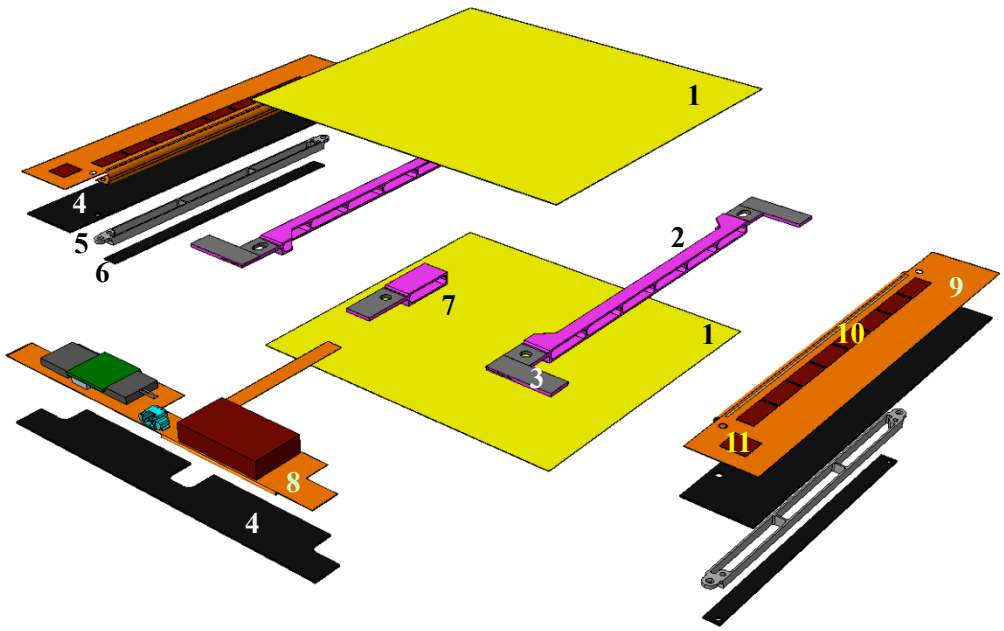
Pixel + **S**trip sensors
2×960 Strips: 2.5 cm × 100 µm
32×960 Pixels: 1.5 mm × 100 µm
P ~ 7 W
~ 45 cm^2 active area
For r > 20 cm
Spacing 1.6 mm, 2.6 mm and 4.0 mm



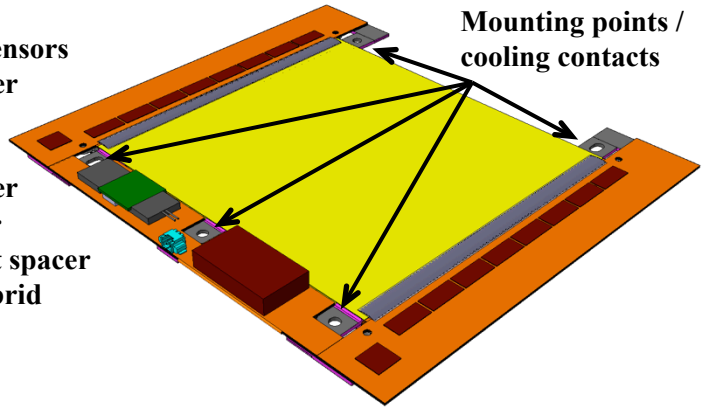
Operate sensors at about −20°C with cooling set point at −30°C

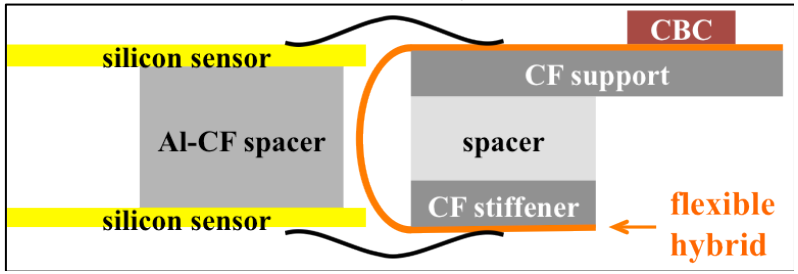
2S module

- Five mounting/cooling points – peripheral cooling
  - Concept similar to modules of the present tracker
- Al-CF spacers provide good thermal conduction, and enable simple, high-precision assembly with ~ no CTE mismatch
- Hybrids are laminated on the CF supports by the company



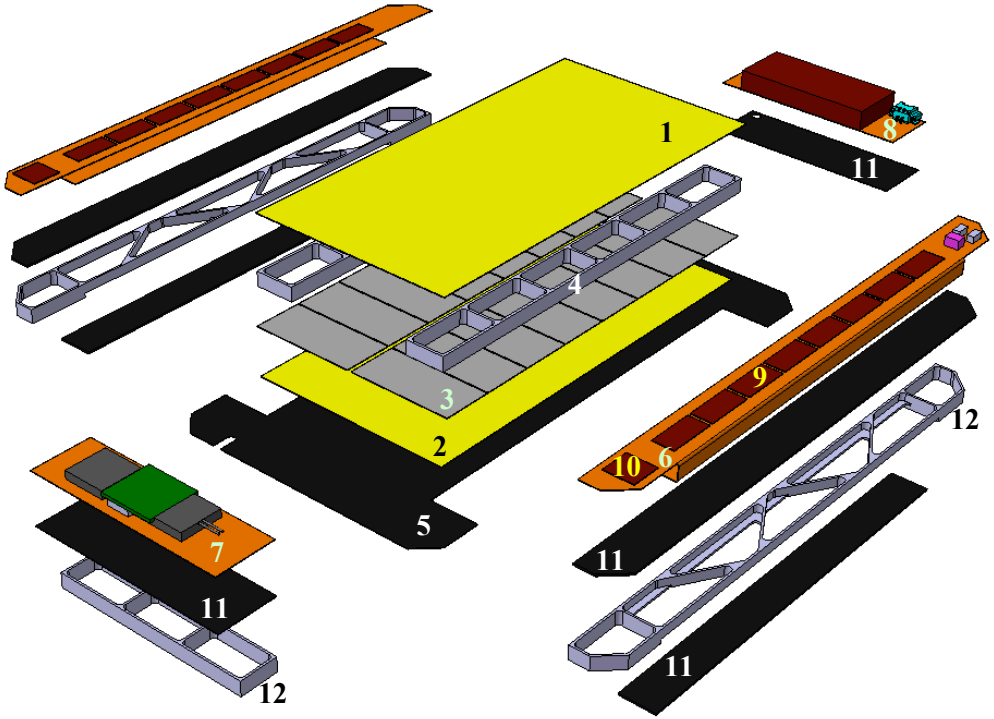
1. 2S silicon sensors
2. Al-CF spacer
3. Al-CF tab
4. CF support
5. Al-CF spacer
6. CF stiffener
7. Al-CF short spacer
8. Service Hybrid
9. FE Hybrid
10. CBC
11. CIC



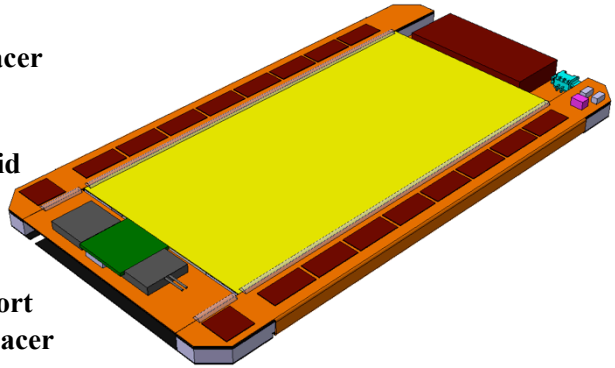


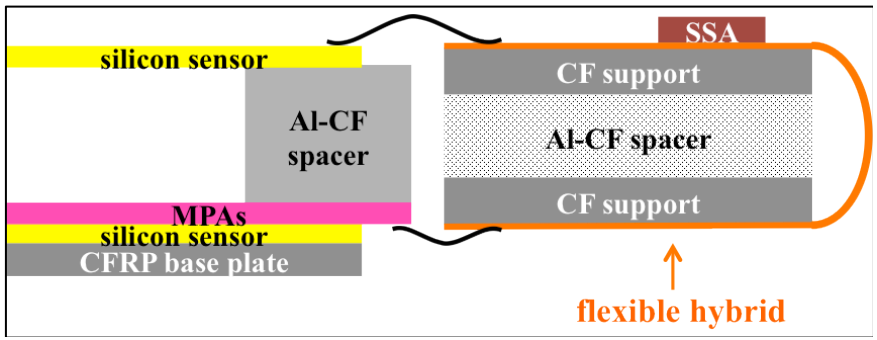
PS module

- Heat dissipation in the MPA requires large area cooling contact
- Cooling through CF base plate, glued on a cold surface on the supporting mechanics
- Module assembly starts from the base plate
  - Additional spacer under the Opto-Link Hybrid, wire-bonded to the FE Hybrids



1. PS-s silicon sensor
2. PS-p silicon sensor
3. MPAs
4. Al-CF sensor spacer
5. CFRP base plate
6. FE Hybrid
7. Opto-Link Hybrid
8. Power Hybrid
9. SSA
10. CIC
11. Hybrid CF support
12. Al-CF Hybrid spacer





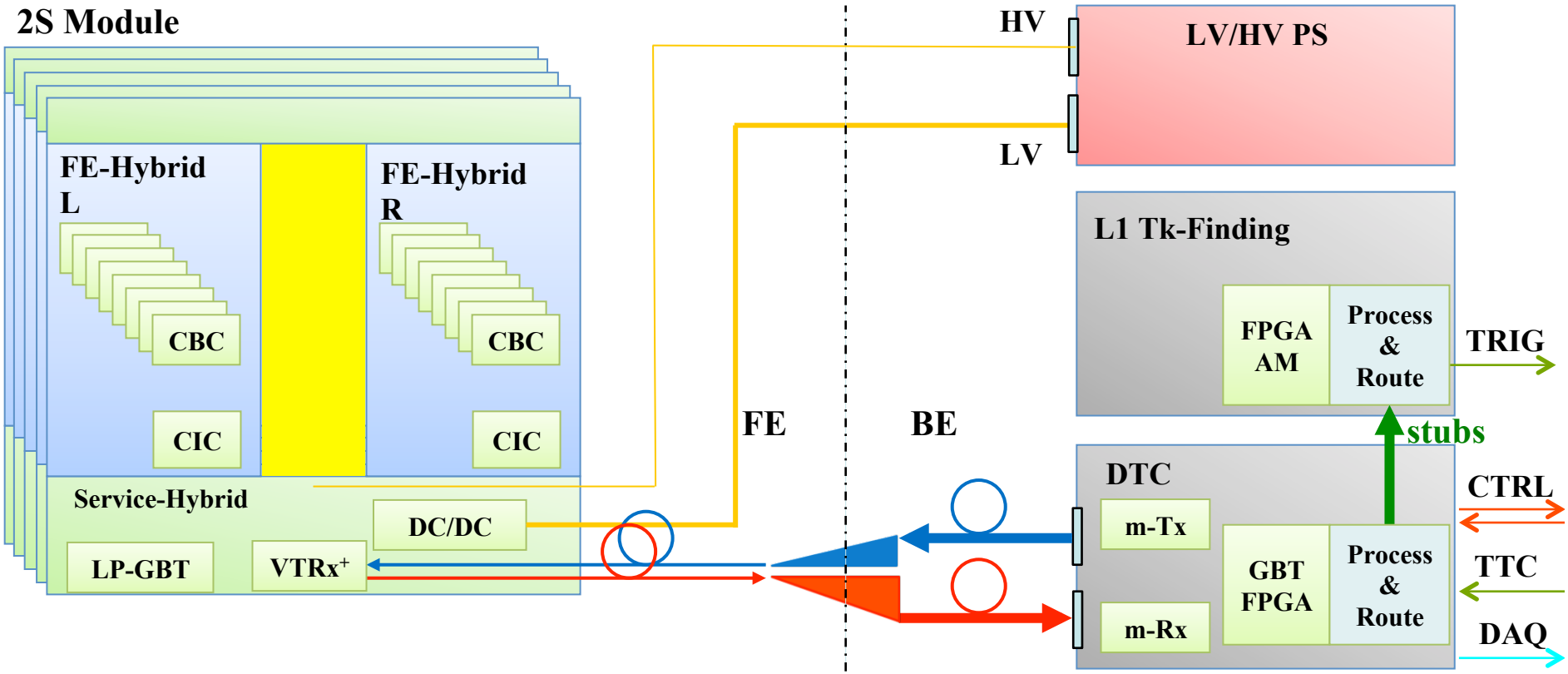
Al-CF composite

Aluminium with embedded carbon fibers, randomly oriented in a plane
Excellent combination of mechanical and thermal properties
Easy to machine
Breakthrough in the design of p_T modules!

Property		Al-CF V2-4	Al
Density [g cm^{-3}]		2.4	2.7
Thermal conductivity [W m^{-1} K^{-1}]	In plane	230	237
	Through plane	120	
CTE [ppm K^{-1}]	In plane	4	23
	Through plane	24	

Electronics architecture

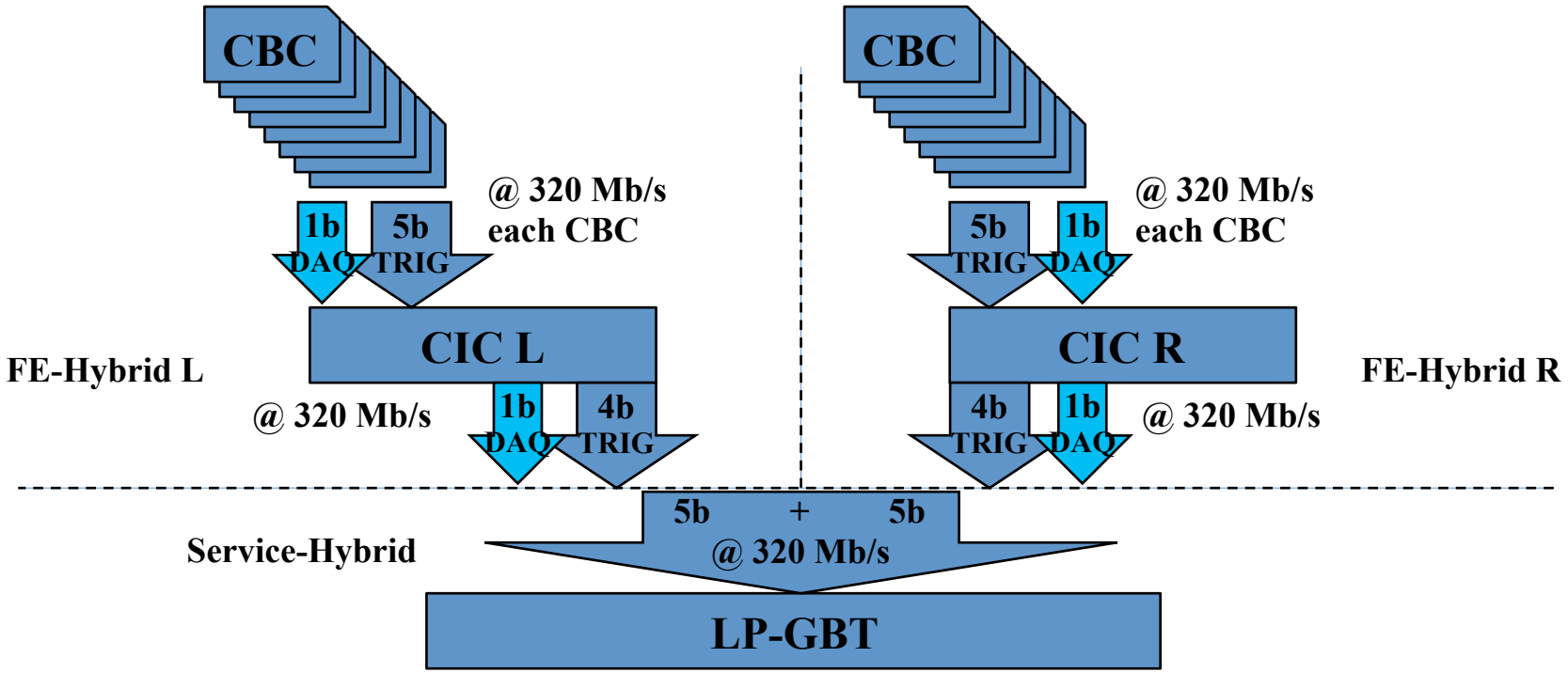
shown for 2S modules



- 8 CBCs / side, 130 CMOS, bump-bonded on the flex hybrids together with the passive components
  - ★ 800 bumps @ 250 μm pitch
  - ★ 127×2 channels, performs top-bottom correlations
- Sensors wire-bonded to high-density FE hybrid
- Wire bonds from FE Hybrid to Service Hybrid
- FE hybrid implements all line routing (data, control, power)
  - ★ Sensors → CBCs, CBCs → CIC, CIC → GBT on Service hybrids
  - ★ Power from Service Hybrid to all chips

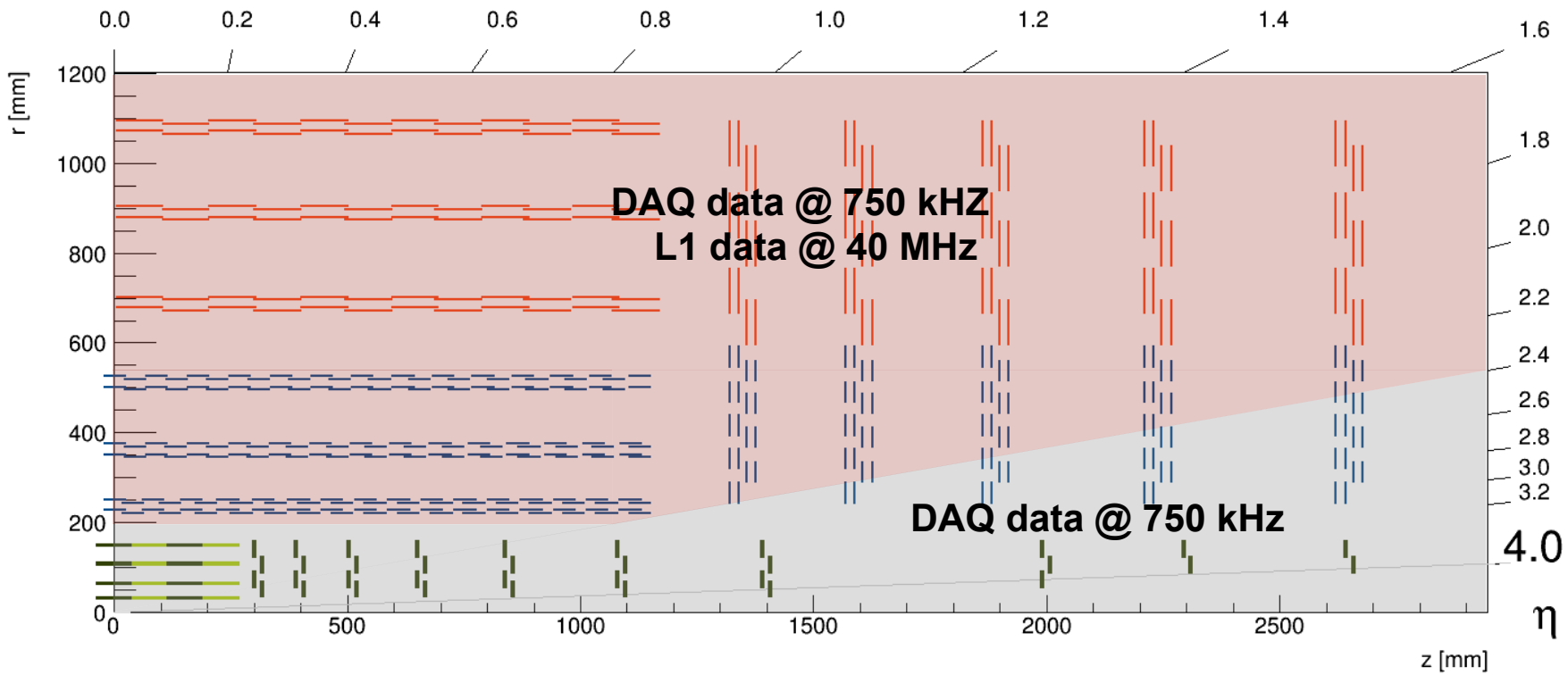
Data flow (2S modules)

- The Concentrator IC combines data from 8 CBCs and for 8 consecutive BX
  - ★ "Block synchronous" system. Efficient use of bandwidth with fixed latency



Initially based on a conservative assumption of 3.2 Gb/s available bandwidth in the phase-1 GBT
The real value will be higher
→ 3.84 Gb/s or 4.48 Gb/s, depending on error correction scheme chosen
Option to use the high-speed version (2 × bandwidth) at the cost of some extra power
→ Can be useful in the first layer of PS modules

N.B. L1 tracking acceptance is limited at η~2.4



The L1 data output is disabled for modules located at low angle in the End Caps
(p_T discrimination insufficient to achieve reasonable bandwidth and stub purity)

FE electronics for PS modules

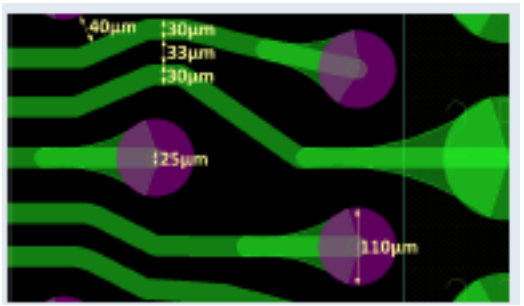
- Two different chips: Macro-Pixel ASIC (MPA) and Short Strip ASIC (SSA). TSMC 65 nm.
  - Correlation in the MPA
  - 2×8 MPA per module, ~2000 bumps / MPA, ~30,000 macro-pixels
  - Connectivity and data formats as for 2S modules
- Service Hybrid split in two boards (readout and power) since the module is ½ length
  - Sensors → CBCs, CBCs → CIC, CIC → GBT on Service hybrids
  - Power from Service Hybrid to all chips
- System fully efficient in layers 2-3
- Limited by bandwidth in layer 1 for the stub data
  - With <PU> = 200 as design goal, the high speed version of the LP-GBT will be needed!

High density flex hybrids

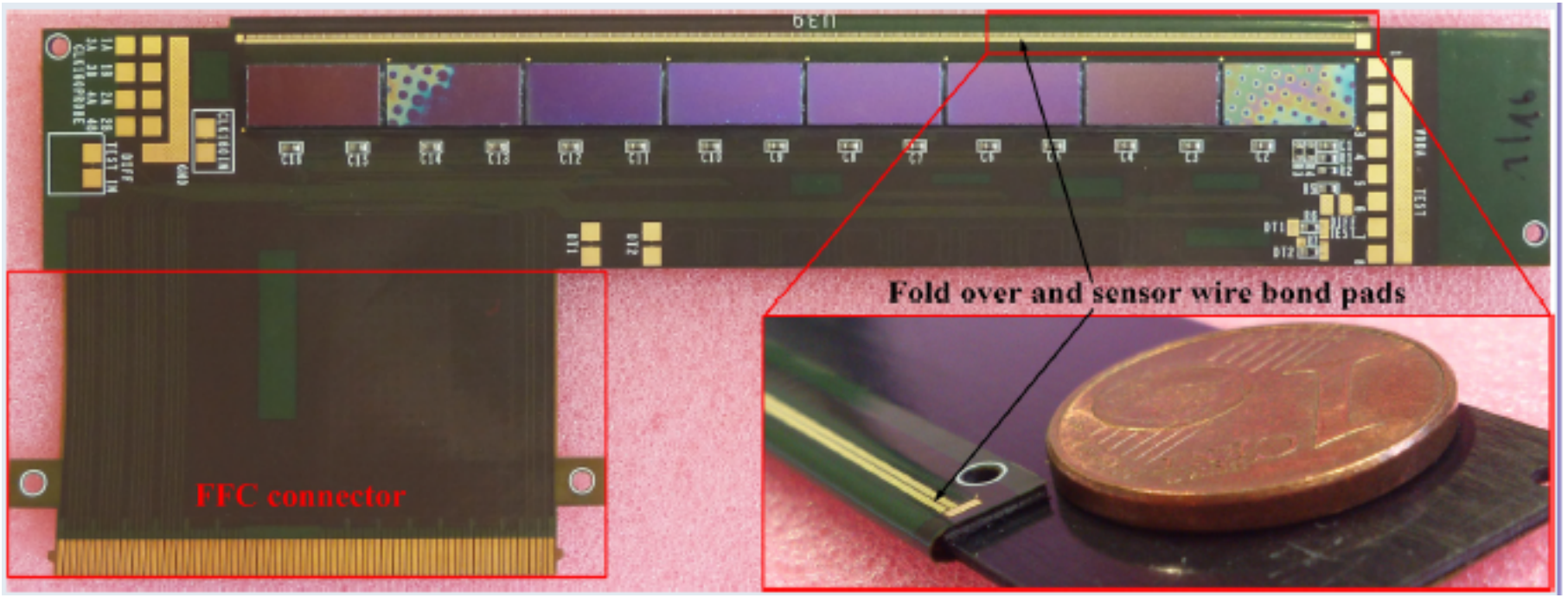
25 μm double-sided polyimide core layer, plus two single-sided 12.5 μm polyimide layers on either side. 25 μm coverlay on the bottom, solder mask on the top. Total thickness ~130 μm.

2S hybrid. Wirebonding pitch to sensor 90 μm × 2 sensors. Bump bonding pitch of CBC 250 μm, 800 bumps × 8 chips. High-density routing: thinnest line 30 μm with spacing 33 μm.

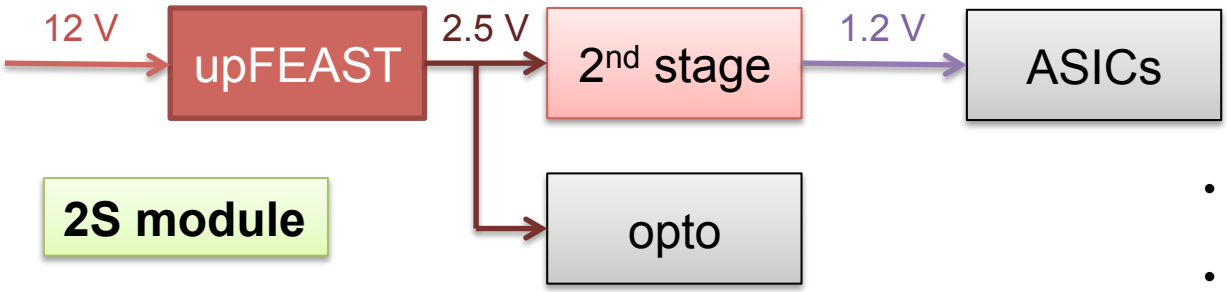
Prototype with Flat Flexible Connector (CIC not yet available).
Eventually will be wire bonded to the Service Hybrid.



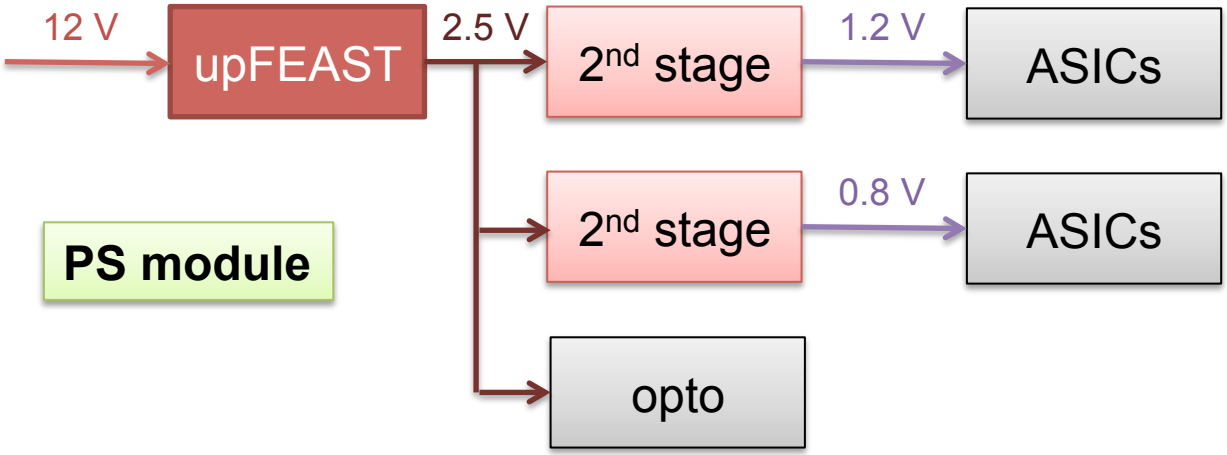
Key element for a lightweight module design!

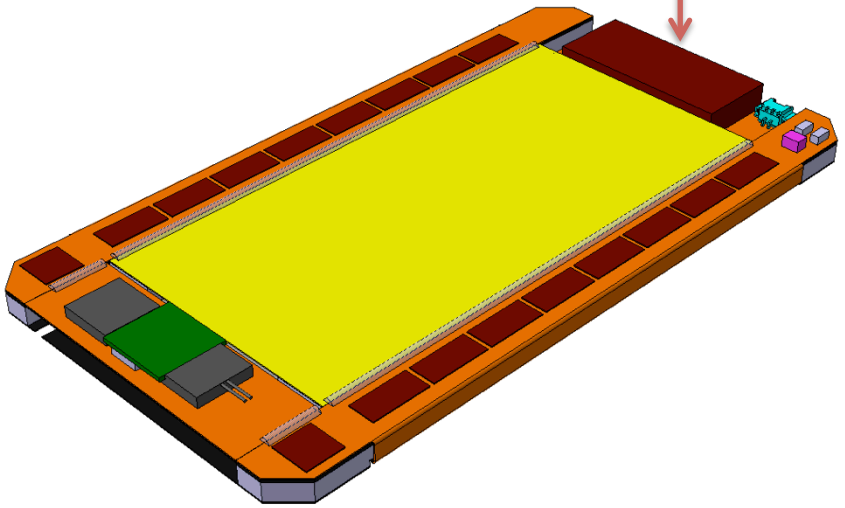


Front-End powering with on-board DC-DC converters



- upFEAST improved version of existing FEAST
- 2nd stage to be designed - technology chosen TSMC 130 nm

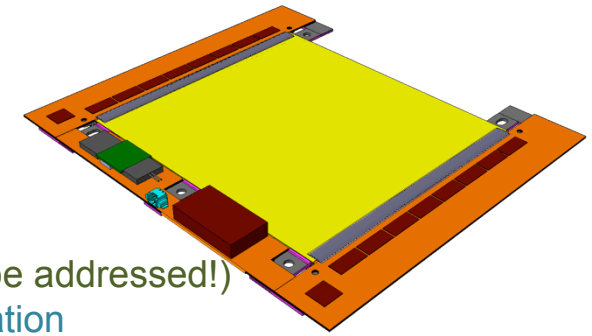




The module is a self-contained functional unit

Individually connected to the back end with power lines and optical fibers for readout and control

FE ASICs



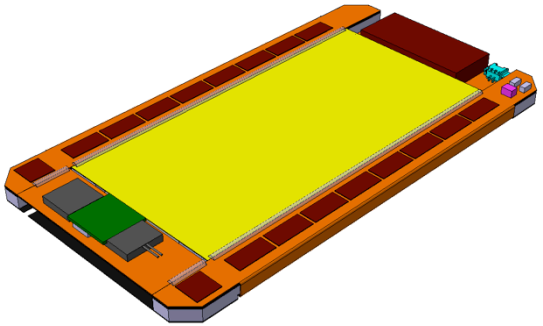
2S module

Design of CBC3 in progress

Specification document prepared and being discussed (...a lot of details to be addressed!)

In principle the final chip – although there is contingency for one further iteration

Submission next year.



PS module

MPA-light qualification well advanced, specs fully met!

- Small-size chip, analogue front-end final, part of the digital logic

Structures for clock distribution and SLVDS data link OK

Memory cell subcontracted to a company, first iteration not fully successful

- Work in progress…

Started working on the definition of the SSA specifications

Common

CIC specs almost fully defined, good progress in the design

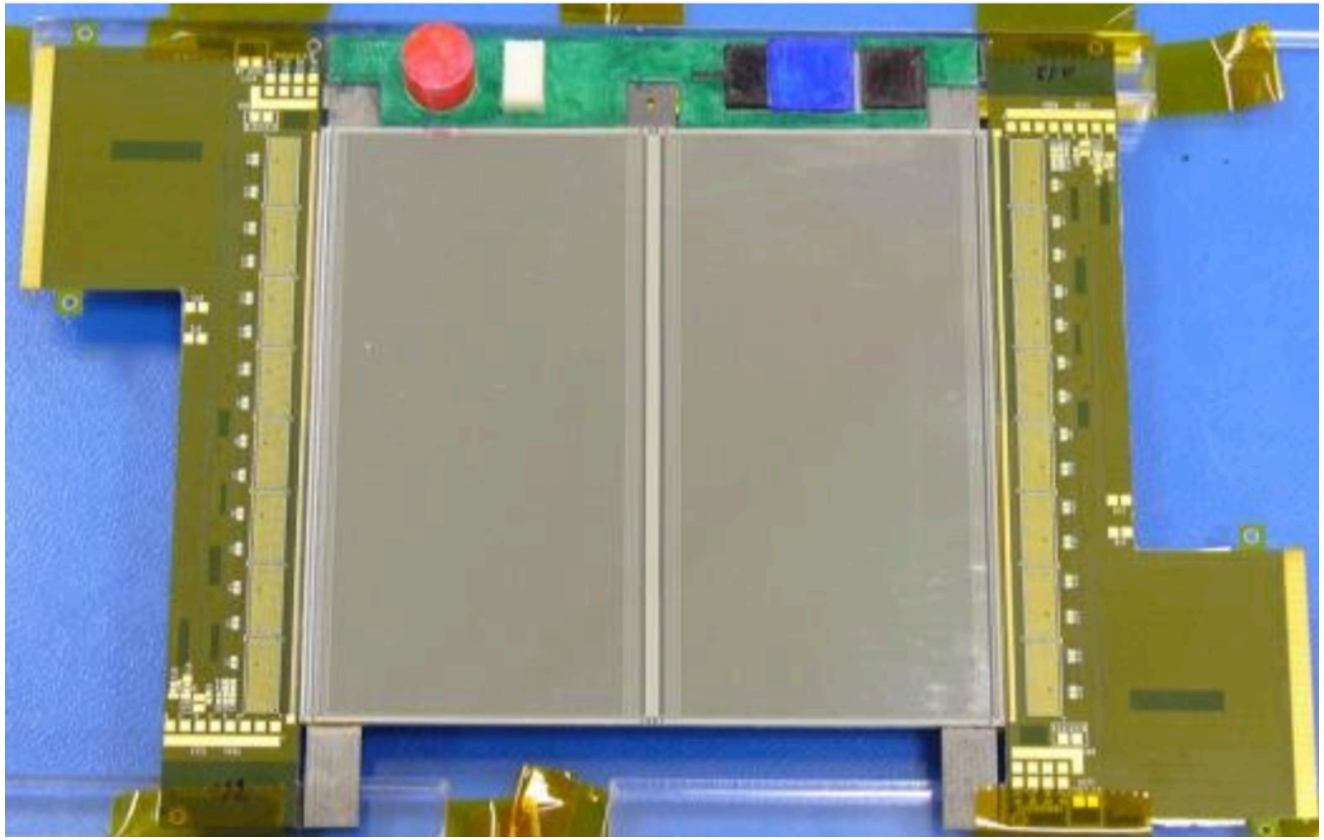
Implementation in Verilog

Plan to submit first prototype in 2016 (funds available)

2S module prototyping

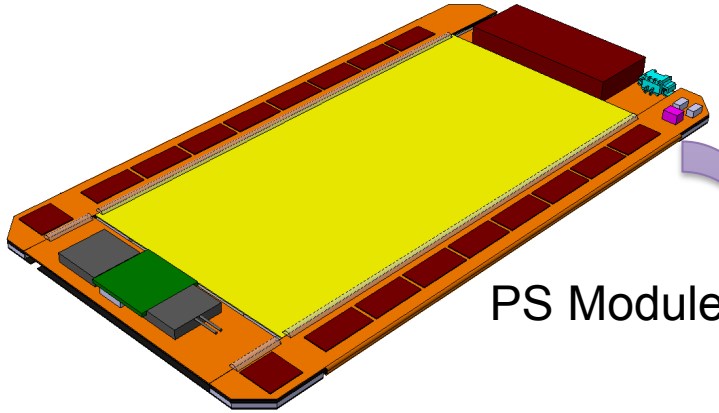
Dummy module built for assembly studies

Prototype readout hybrids with 8xCBC2
Inactive dummy sensors
3d-printed service hybrid dummy

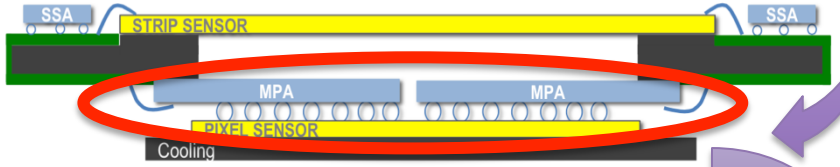


PS module prototyping: MaPSA-light

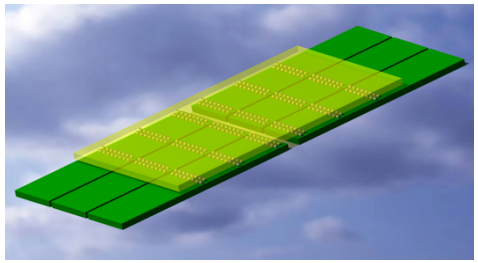
- **Ma**cro**P**ixel **S**ub**A**ssembly: **MaPSA**
- **Scaled down** version of the pixel part of the PS module
- MPA-light chip
  - # of pixels: 3 x 16
  - Pixel size: 100 x 1446 µm
  - Chip size 1.7 x 6.5 mm^2
  - Process: 65 nm TSMC
- PS-p light sensor
  - Material: FZ p-type
  - Thickness: 200 µm
  - # of pixels: 48 x 6
    → 6 x MPA-light chips
  - Sensor size 7.8 x 12 mm^2
  - Produced at: CiS, Erfurt DE



PS Module



Pixelated part: MaPSA



Small prototype: MAPSA light

Status: assembly ordered from 3 different vendors
Test system under development

Next (if successful): build a PS-light module

Outlook

All parts coming together to assemble full-size functional 2S modules

Without service hybrid and without CIC, based on CBC2 hybrids

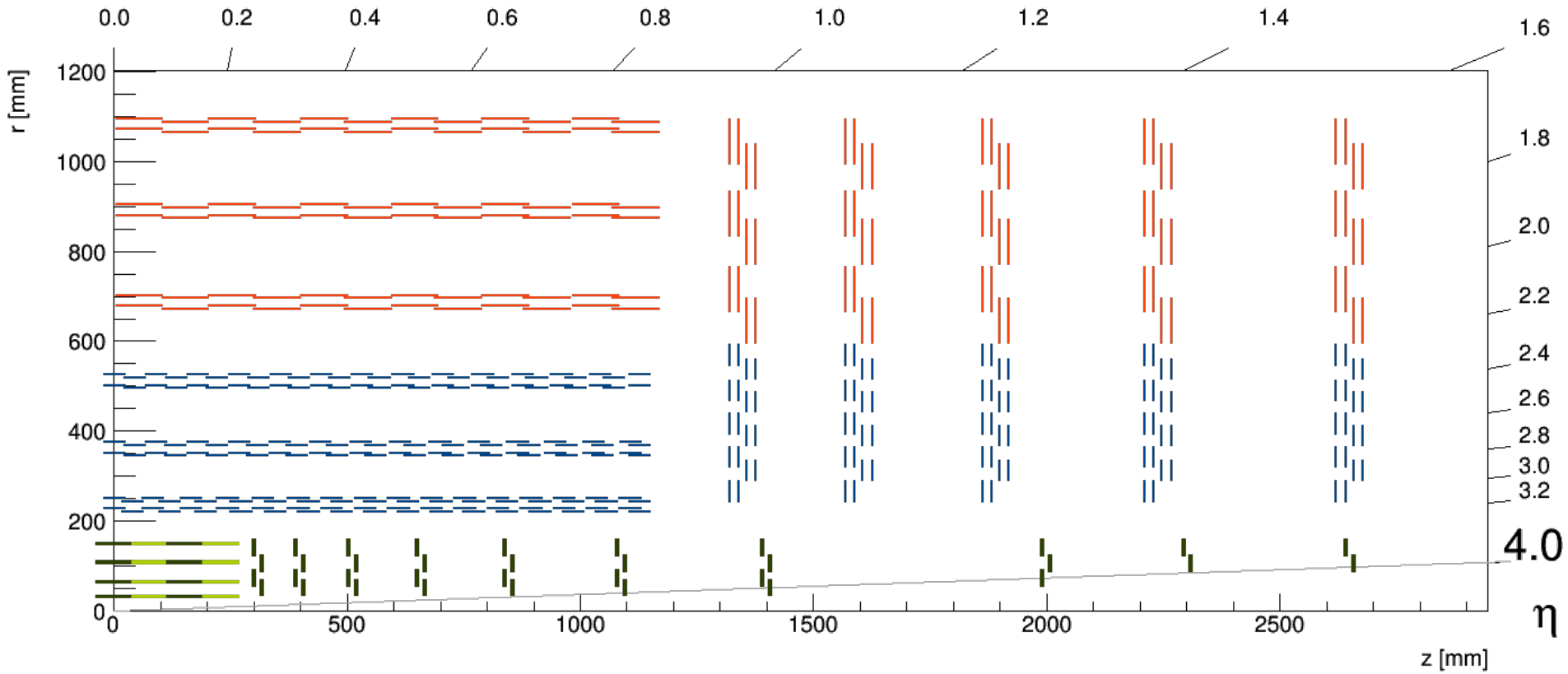
Full-size 2S module prototypes very soon!

… in the beam in November?

Following successful MPA-light → MaPSA-light being assembled

If all OK, small-size PS modules prototypes next year

Optimization of the detector

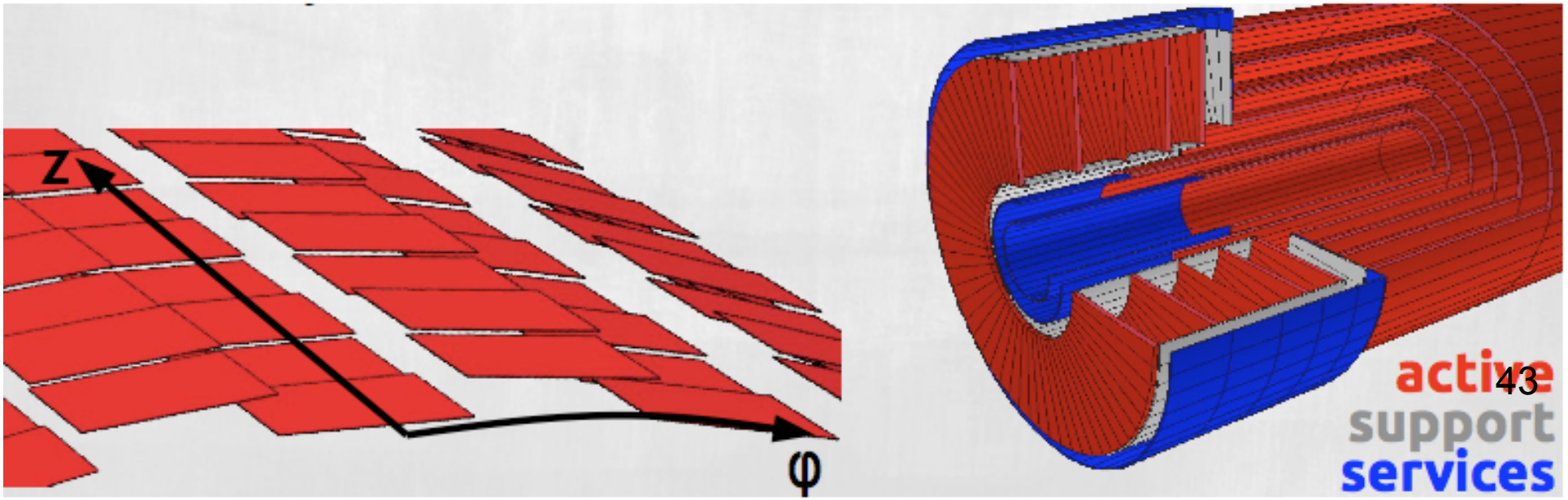


Optimization of the detector

Detector standalone modelling: tkLayout

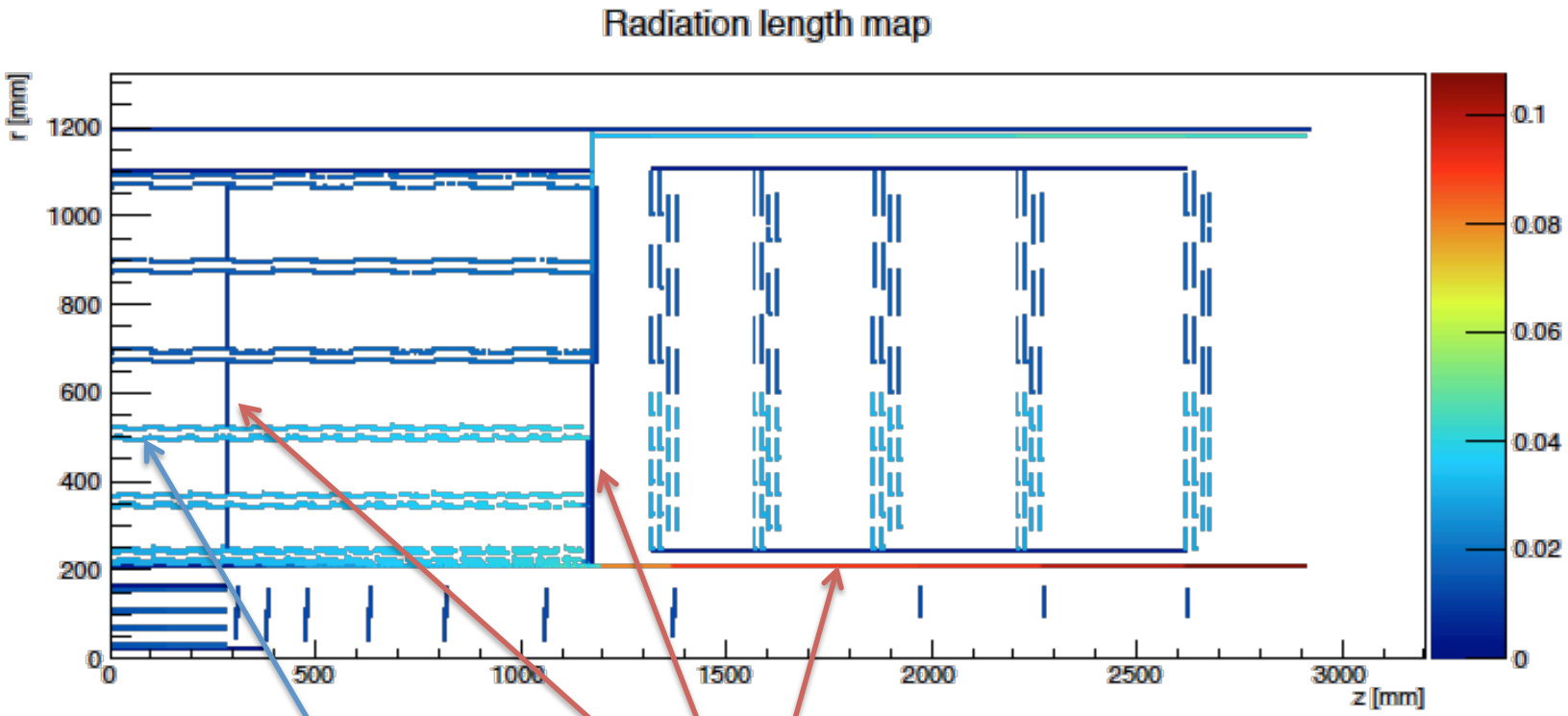
Flexible tool to create 3D models of the tracker from simple configuration files and user-defined rules

Includes both active surfaces and inactive materials



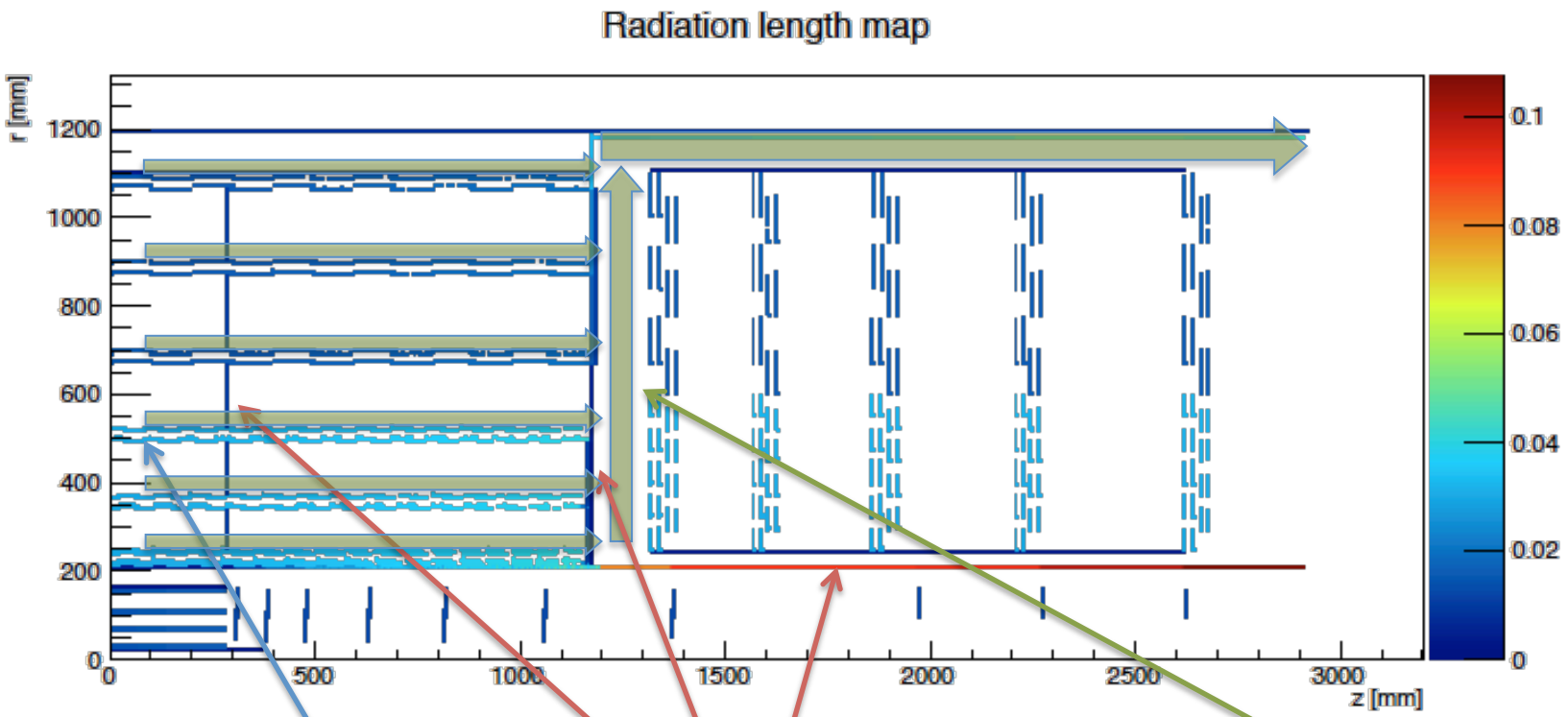
Detector standalone modelling: tkLayout

Simple (semi-automatic) modelling of services



Detector standalone modelling: tkLayout

Simple (semi-automatic) modelling of services



Material of sensitive elements

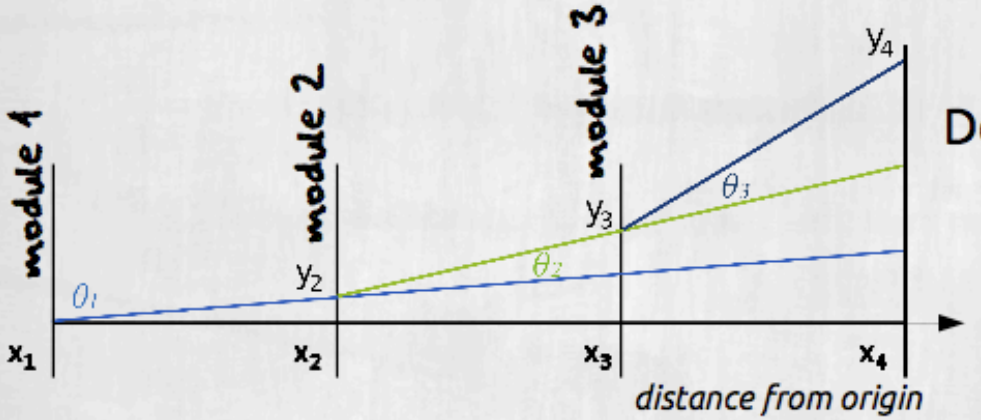
Dedicated volumes for supports and services

Automatic routing of outgoing services

Detector standalone modelling: tkLayout

Implements estimates of tracking performance

- Use measurement errors to estimate the errors in track fit parameters
- **Multiple scattering** treated as (correlated) a measurement error



Deviation due to scattering:

$$y_n = \sum_{i=1}^{n-1} (x_n - x_i)\,\theta_i$$

Error correlation matrix:

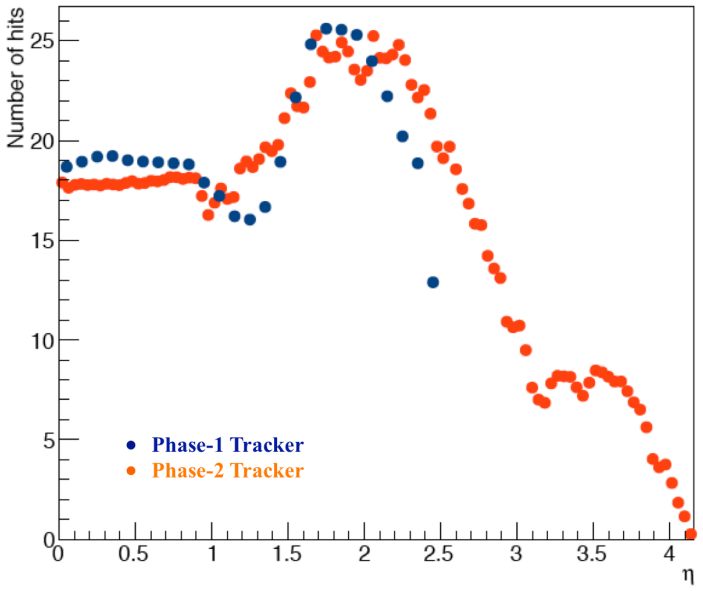
$$\sigma_{n,m} = \langle y_n y_m \rangle = \sum_{i=1}^{n-1} (x_m - x_i)\,(x_n - x_i)\,\langle \theta_i^2 \rangle$$

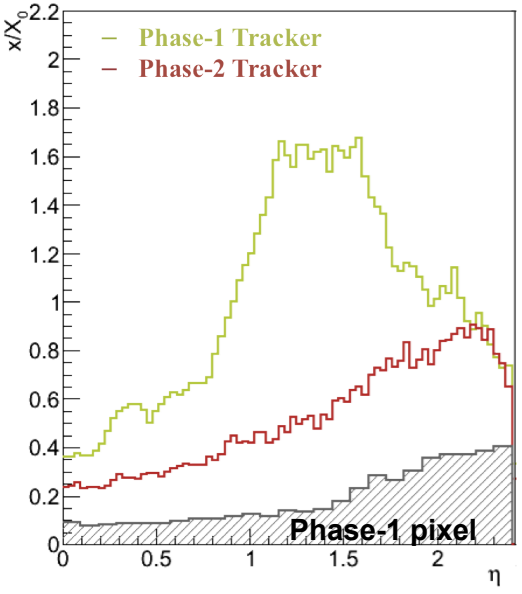
$$\sigma_n^2 = \frac{p^2}{12}$$

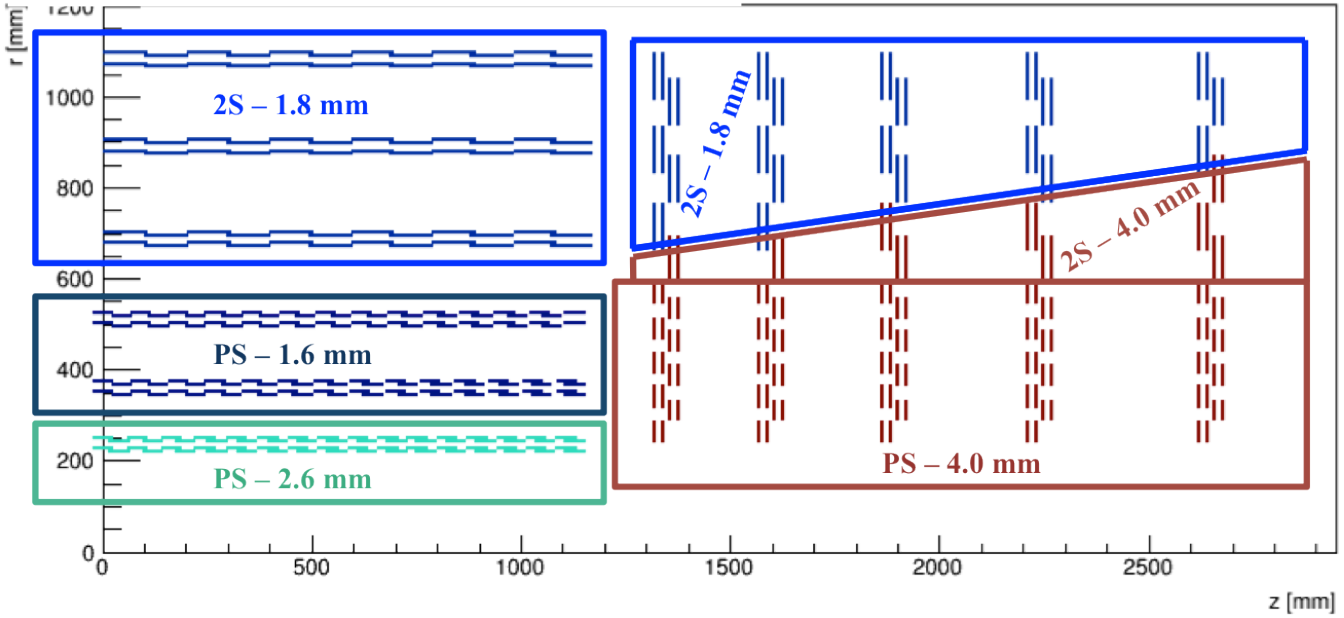
Detector standalone modelling: tkLayout

- Provides:
  - Estimates of the tracking precision including multiple scattering
    - For both offline tracking and L1 tracking
  - All useful summaries/statistics
    - # of modules, active surface, # of channels, total power, total weight, etc etc….
  - Radiation length and interaction length vs rapidity
  - Map of leakage current in all modules after irradiation
    - Input from FLUKA – used to optimize module cooling
  - Stub p_T resolution for each module location
    - Used to optimize distribution of sensor spacing in the Tracker volume
  - … and more…
- Outputs:
  - Mini web-site with full information
  - Geometry files for CMSSW
  - Module coordinate files for the 3D modelling of the detector structures
  - Geometry files for FLUKA

Some infos from tkLayout

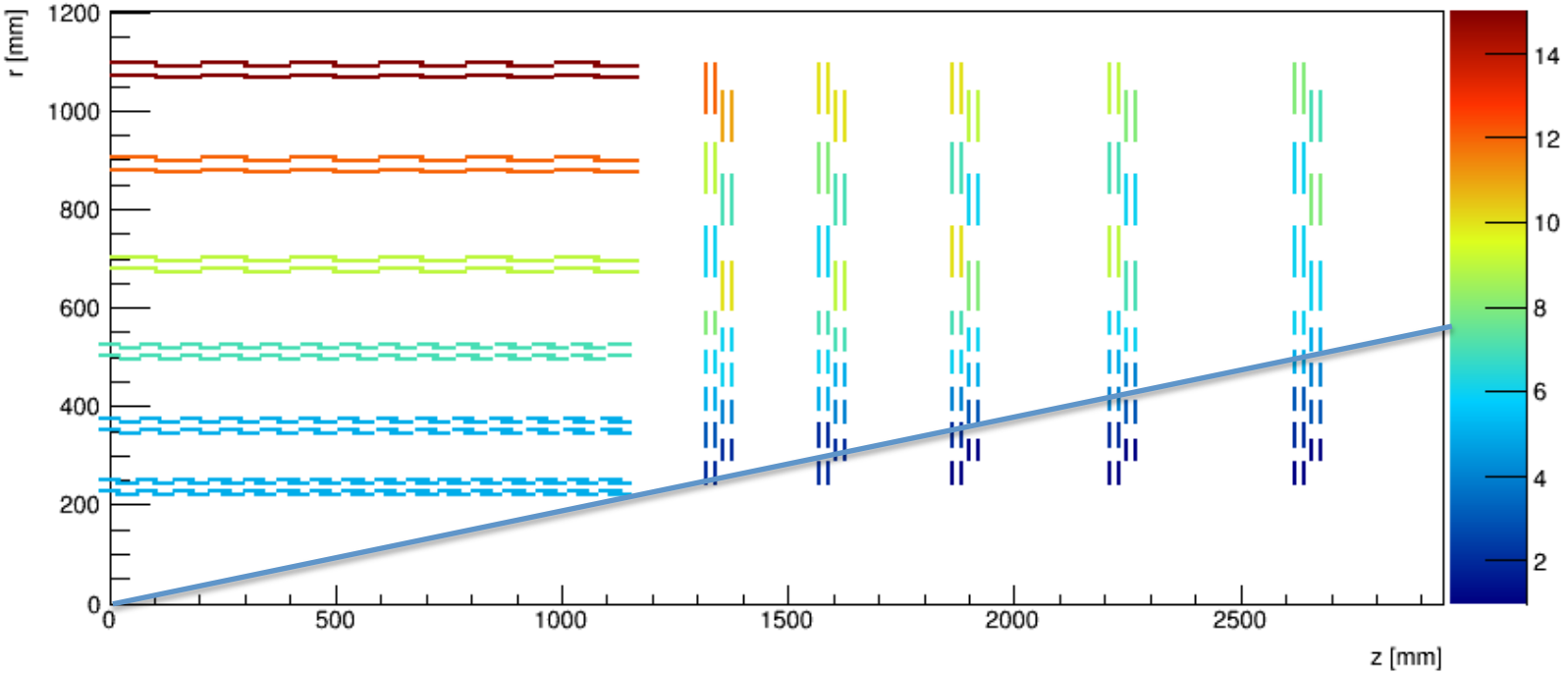




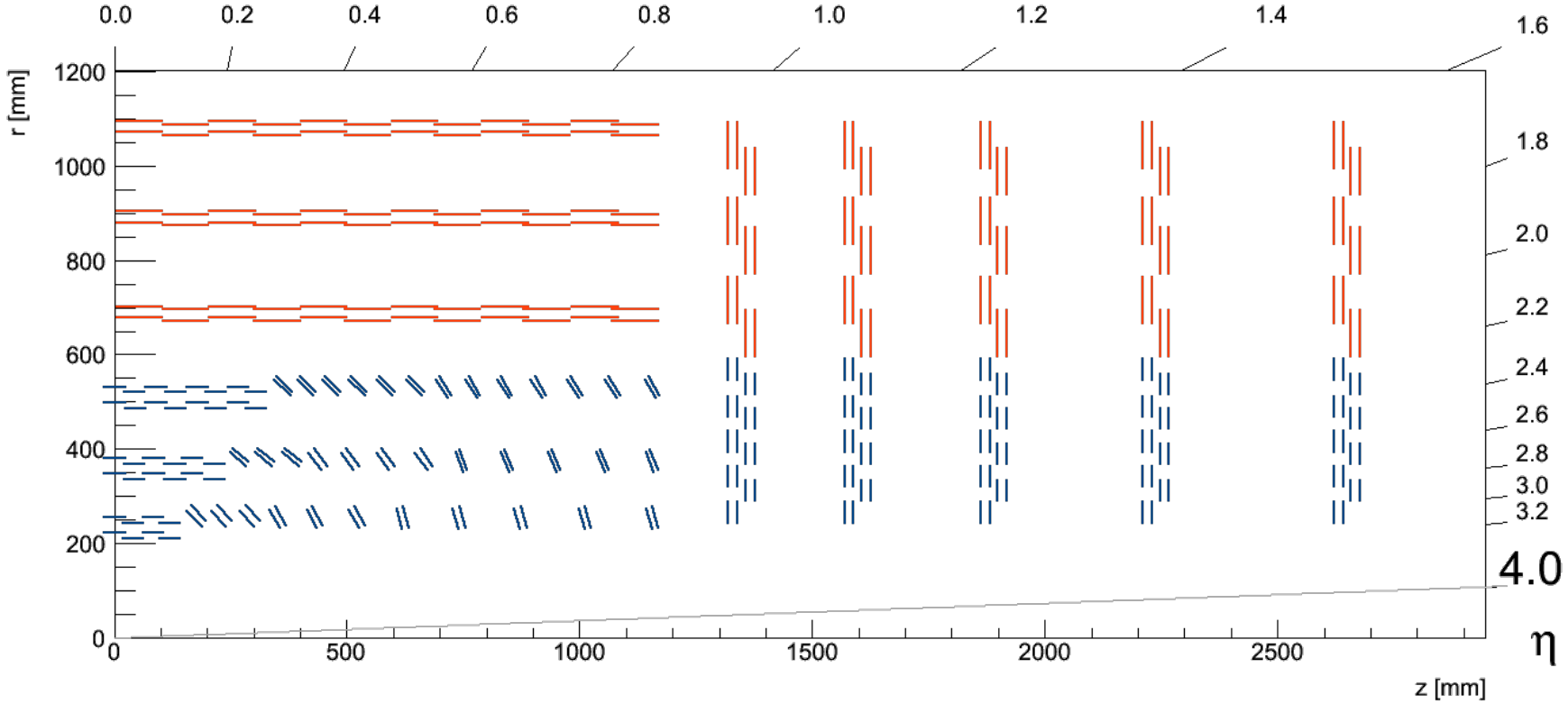


Acceptance window

- Width 5÷15 channels in the barrel, 2÷12 in the endcap



Beyond baseline



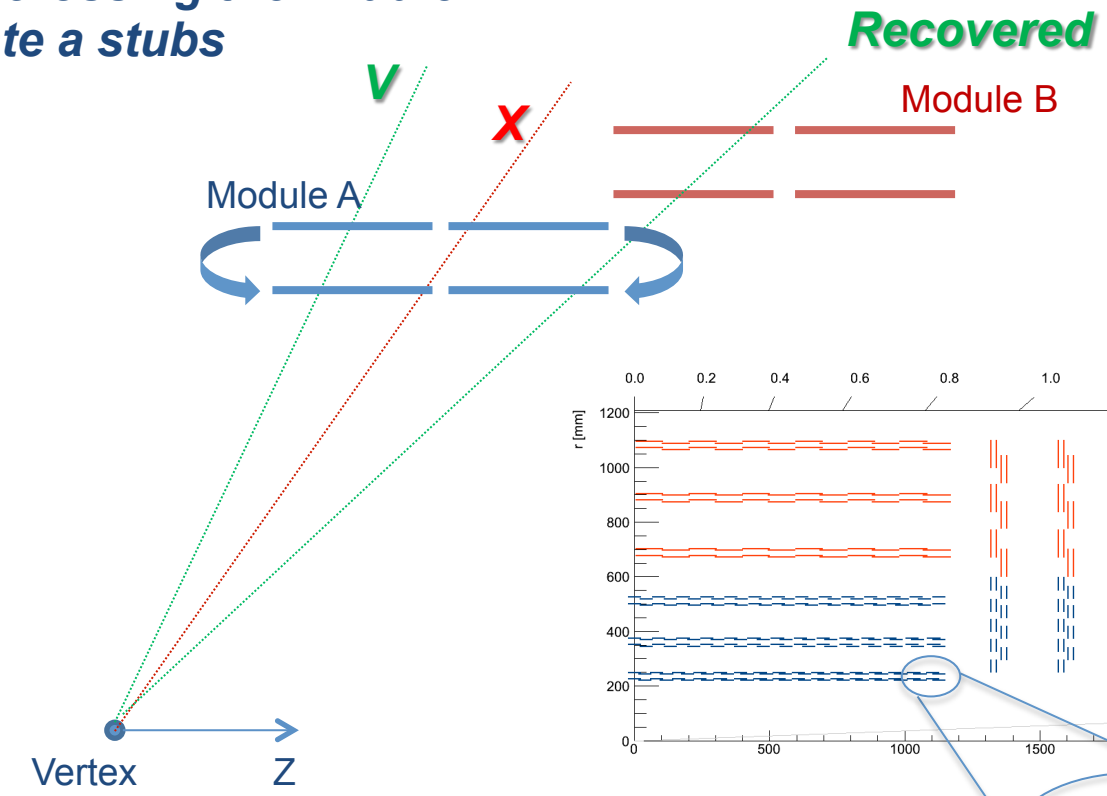
- Variant of TBPS with progressively tilted modules
- Short central section followed by groups of rings with same tilt
- Same coverage and ~same tracking performance with a smaller number of modules

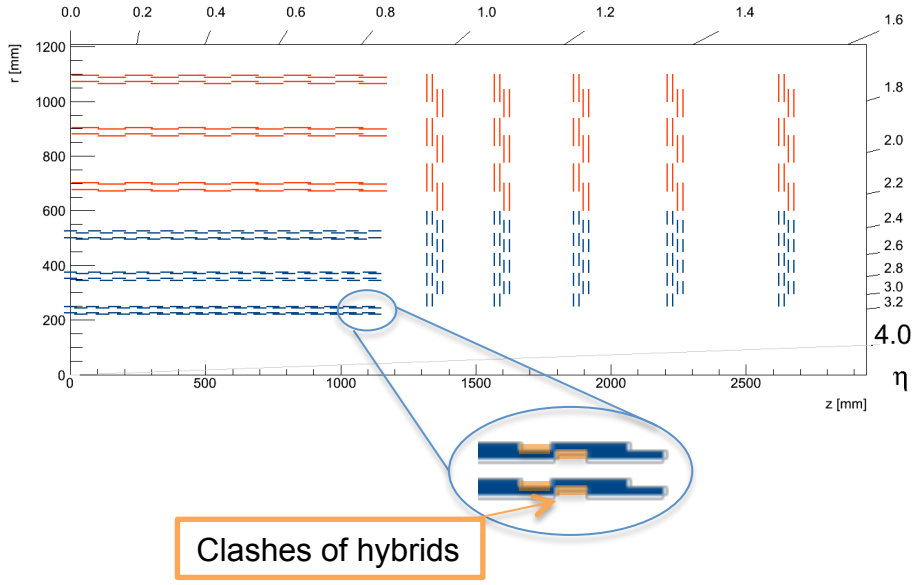
Is it really a good idea???

Many tracking detectors have been designed and built…
… and they don’t look like that!

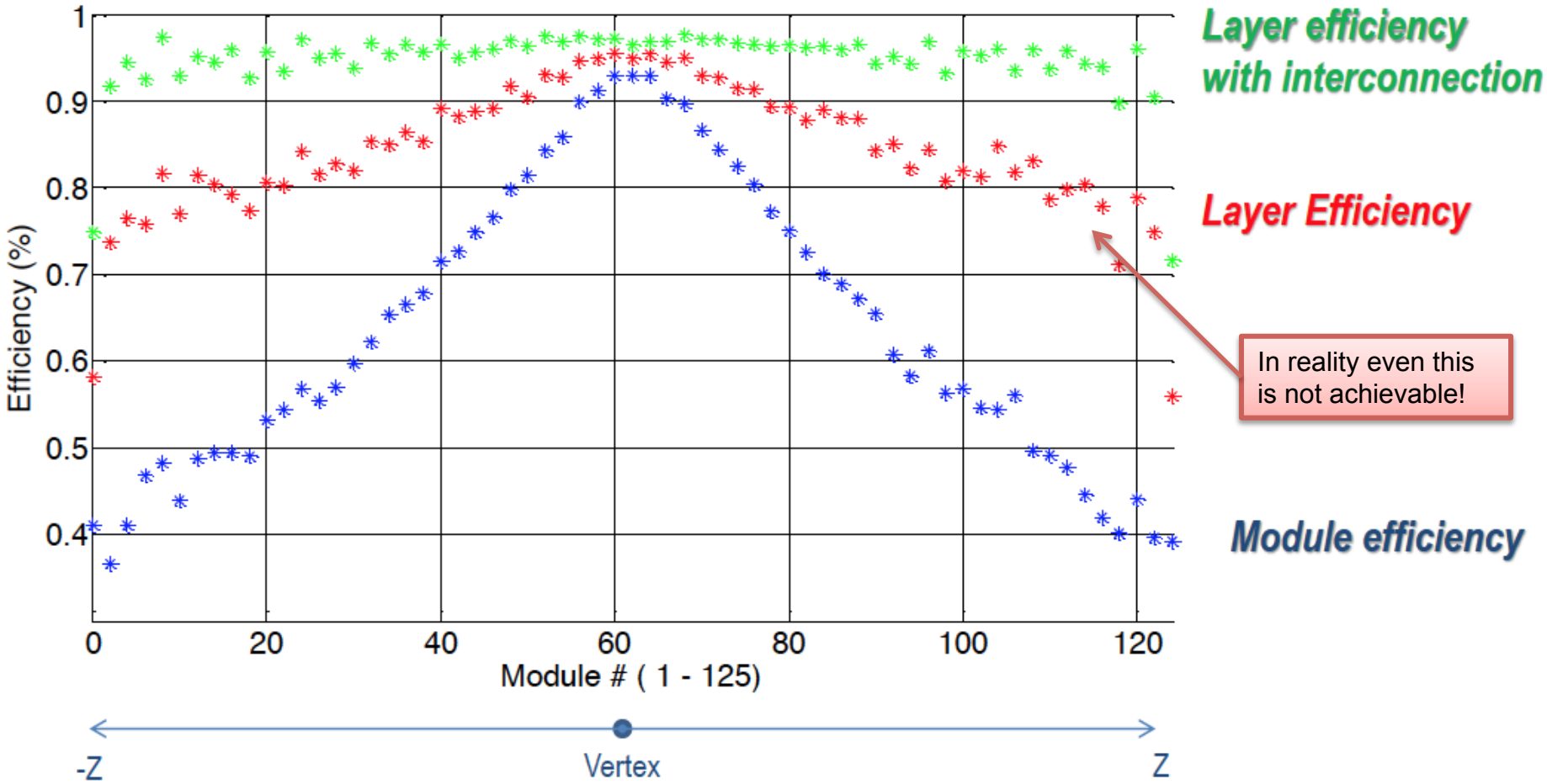
Stub Finding logic efficiency results

*Without an **interconnect technology*** (ex: TSV) *between the two sides of the module, **tracks crossing the middle will not generate a stubs***

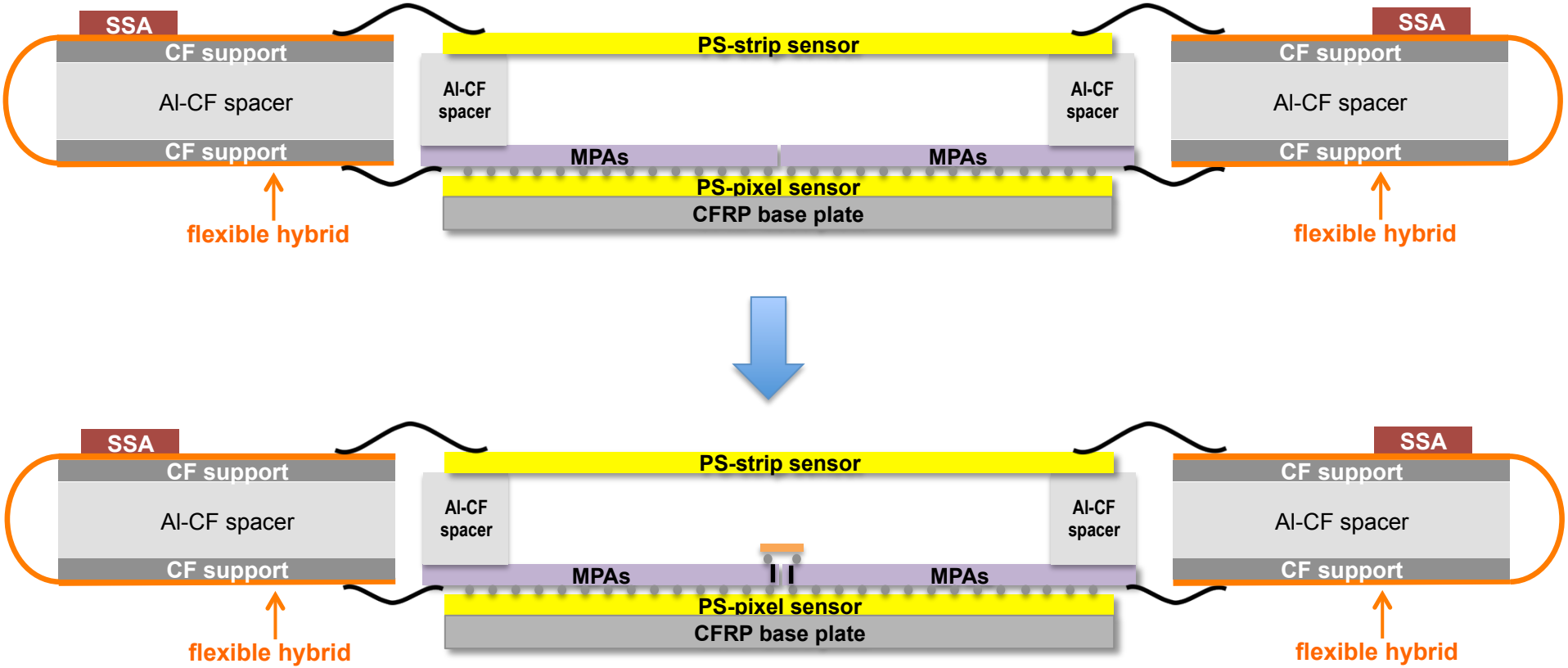




Stub Finding logic efficiency results

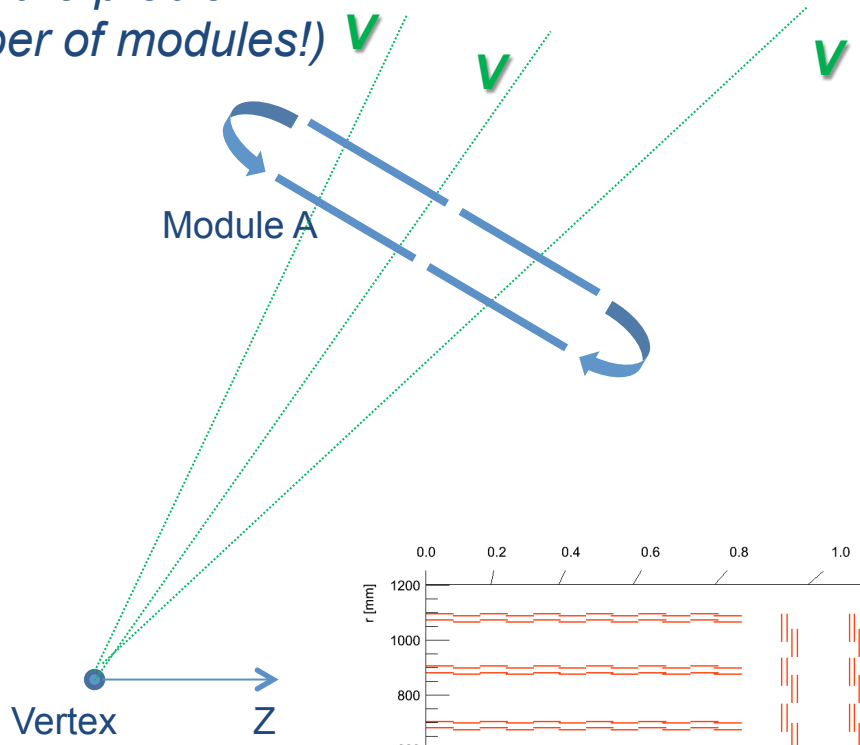


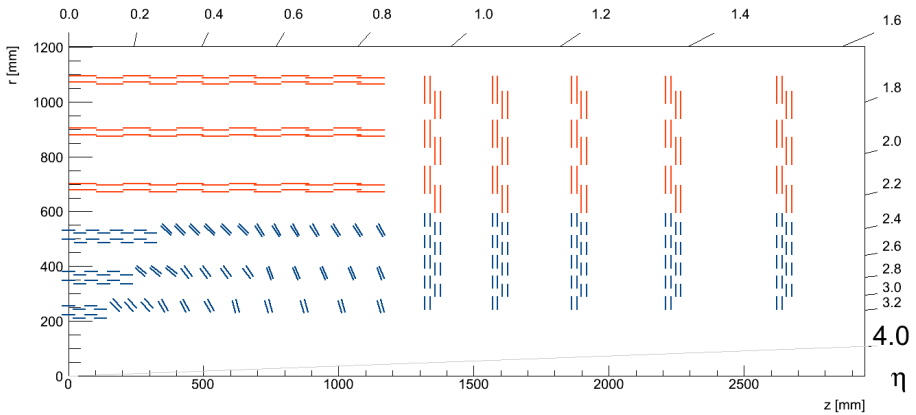
Through-Silicon Vias would be required to achieve acceptable efficiency in the “flat” layout



Stub Finding logic efficiency results

The tilted layout *solves the problem*
(with a smaller the number of modules!)





Three specific facts favour the tilted layout

Stub finding efficiency

(1) Avoids needs of TSVs to interconnect the two halves of a PS modules

(2) Avoids huge overlaps between consecutive modules in z

Impossible to implement at the edge of the barrel anyway

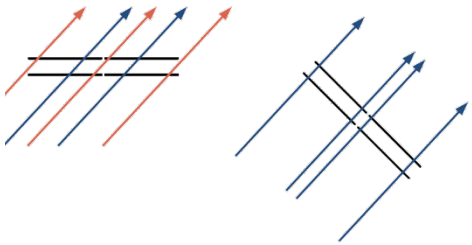
Module length

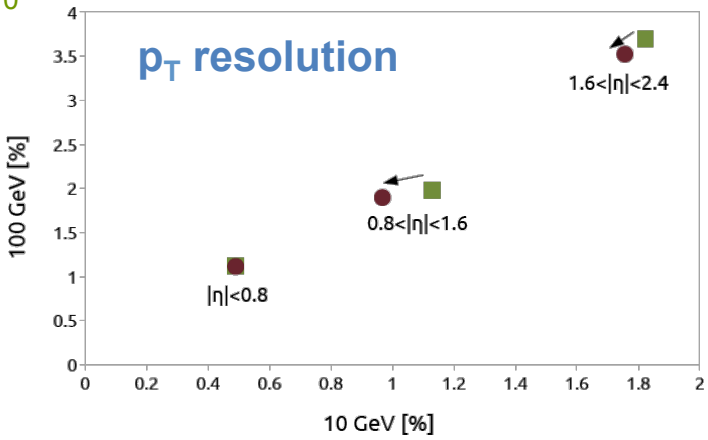
(3) Modules only 5 cm long in the z direction because of technology limitations

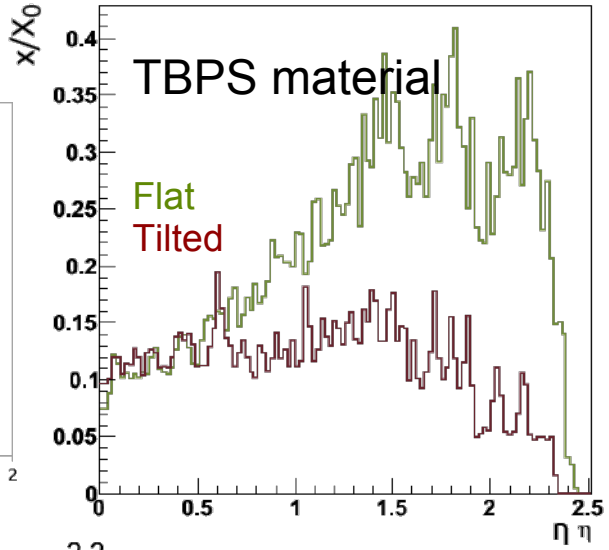
Aggravates effects (1) and (2), but makes tilt possible!

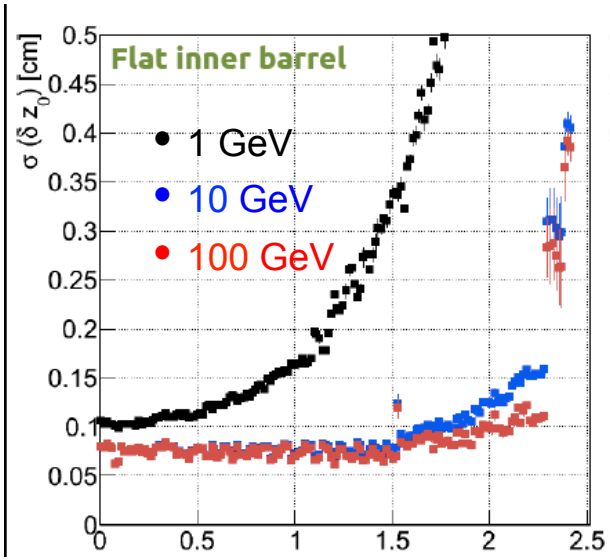
Tilted TBPS - performance

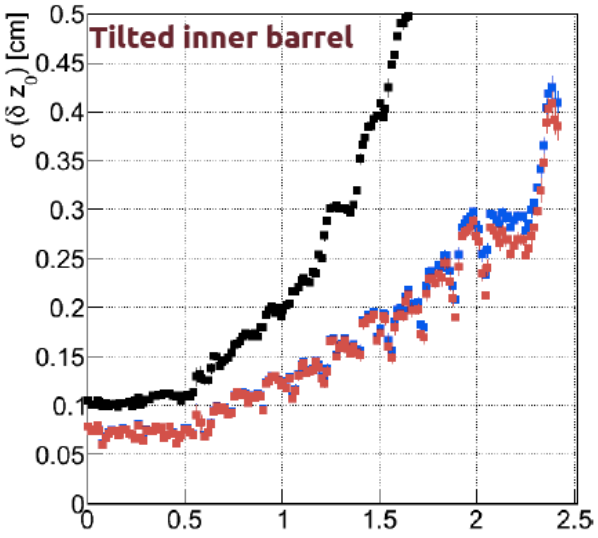
- Less material, equal or better tracking performance, better stub coverage, no need of TSVs
- Less modules, cost saving
  - 1200 modules, 10 m^2 of silicon
- Slightly degraded z_0 resolution for L1 tracks

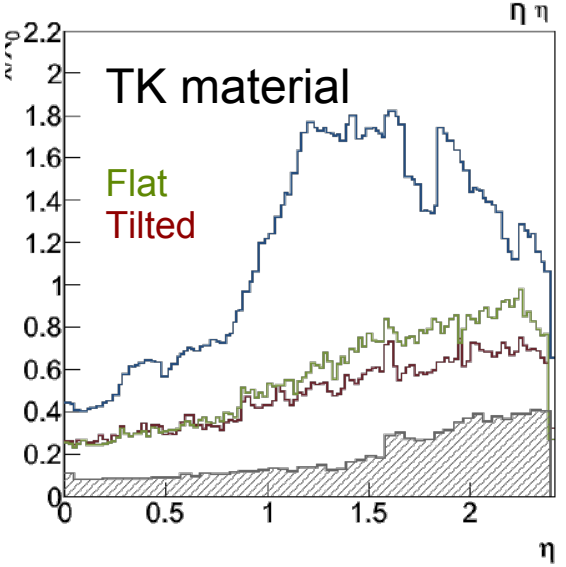




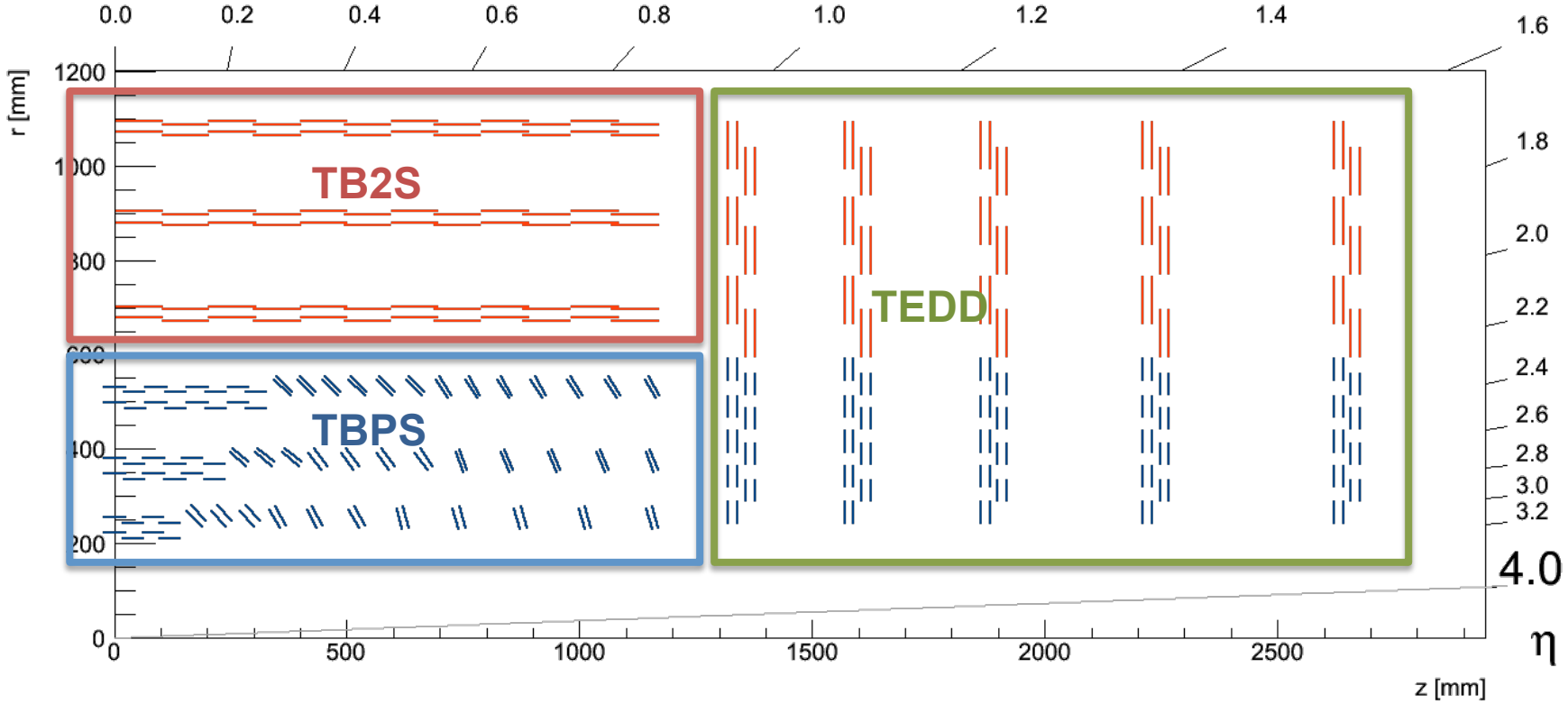








Mechanics

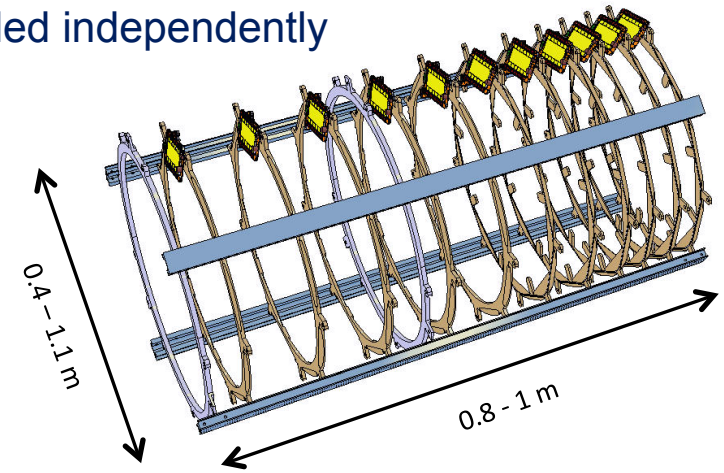

TB2S
TBPS
TEDD
r [mm]
z [mm]
η
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
3.2
4.0
0
500
1000
1500
2000
2500
1200

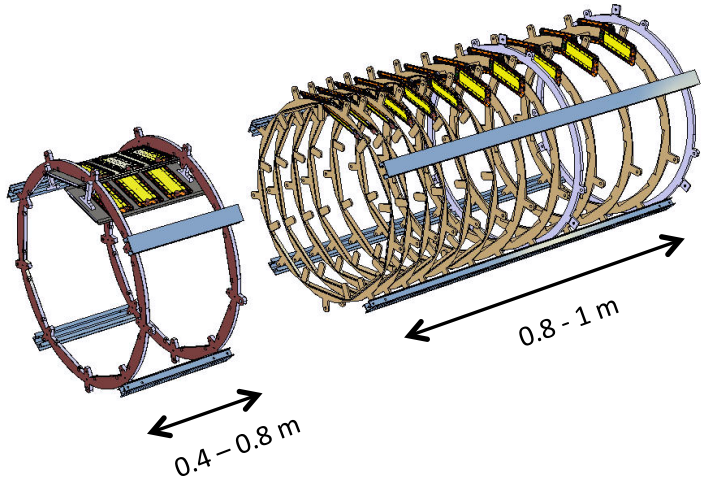
TBPS- tilted geometry

Central flat section made of “staves”

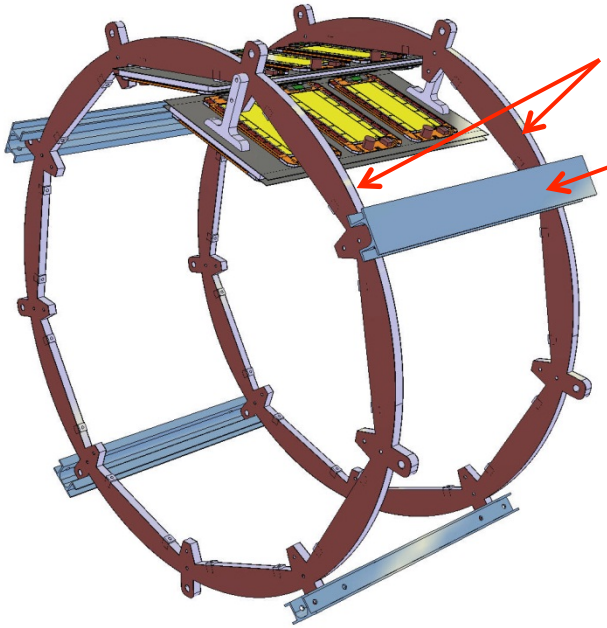
Tilted sections made of “rings”

Three layers assembled independently



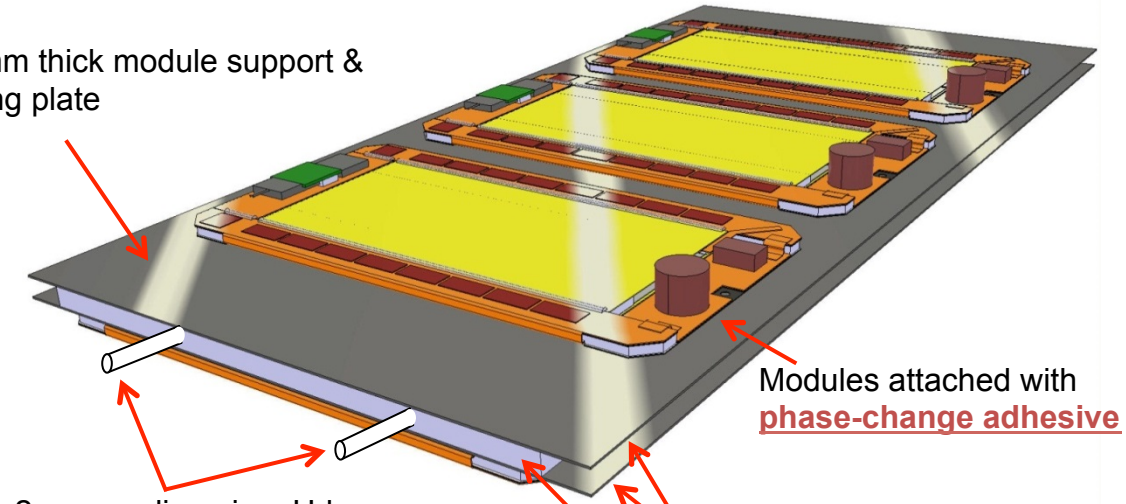


Stave: modules glued on CF/foam panels



Space frame made of end rings
and longitudinal profiles

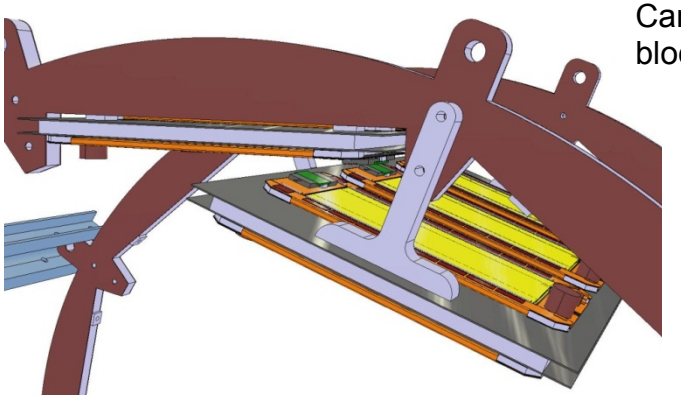
4-6 mm thick module support &
cooling plate



Modules attached with
phase-change adhesive

Diam ~2 mm cooling pipe, U-loop
Carbon foam or aluminium/carbon-fibre
block next to cooling pipe

~0.5 mm high-conductivity
carbon-fibre composite skins
Foam core



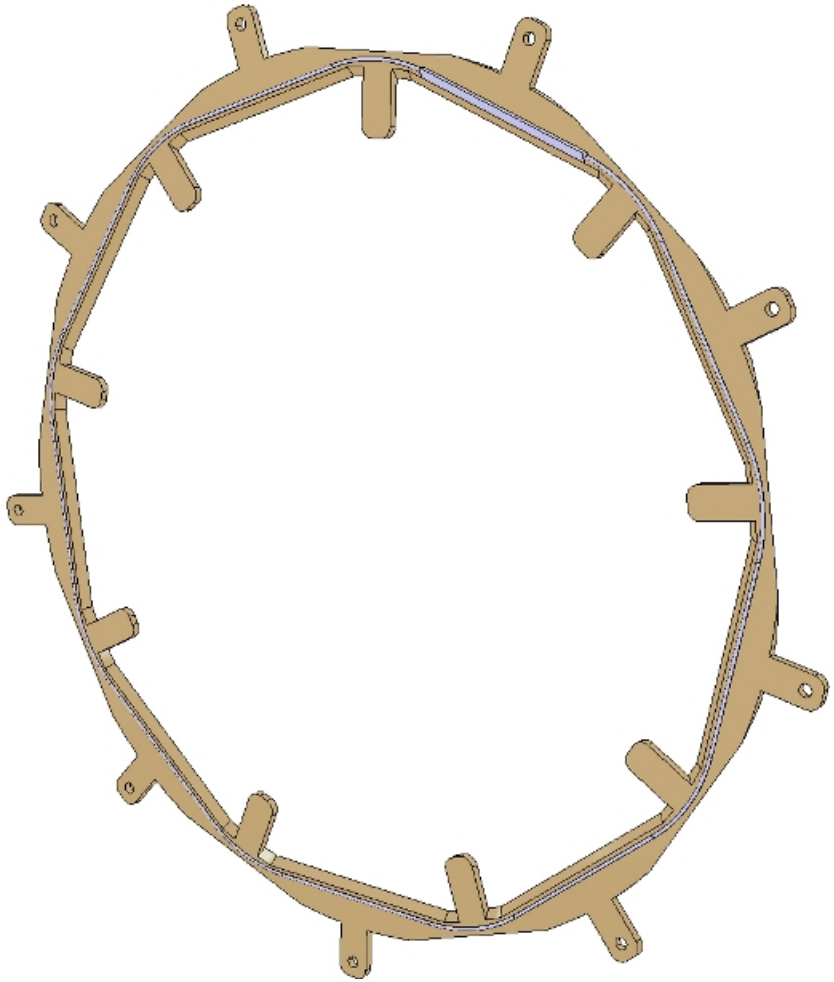
Geometrically simple building blocks

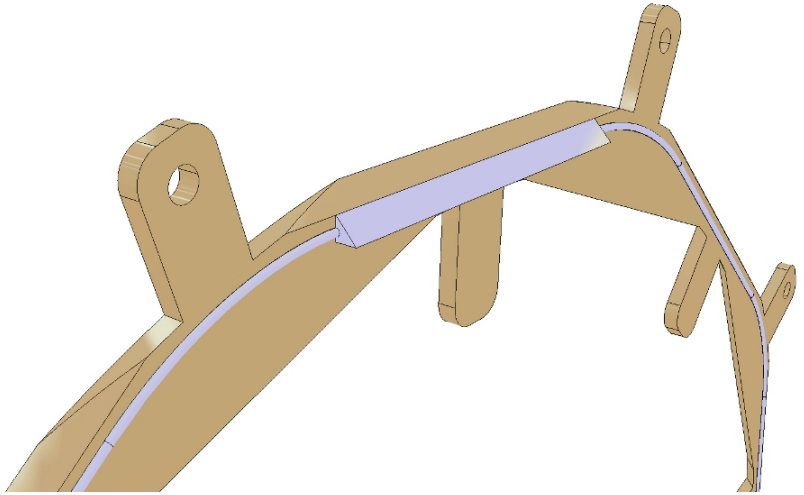
Main challenges:

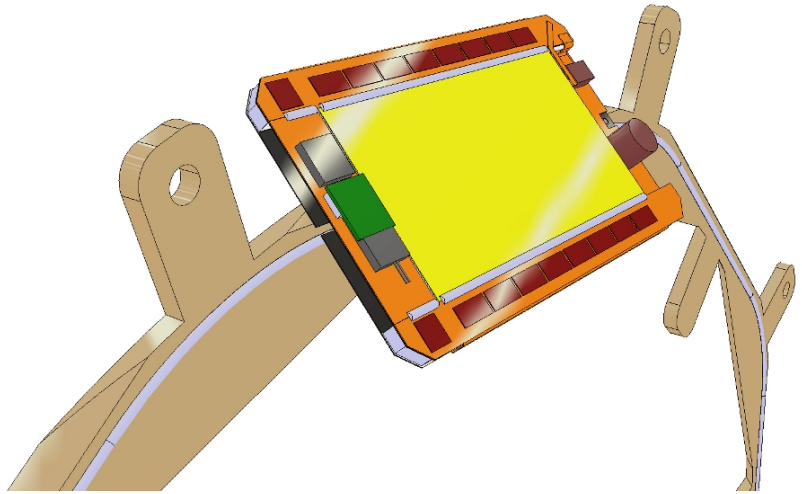
- Precise and light plates with integrated cooling
- Thermal and mechanical connections

CF/foam “rings” support modules with the required tilt angle

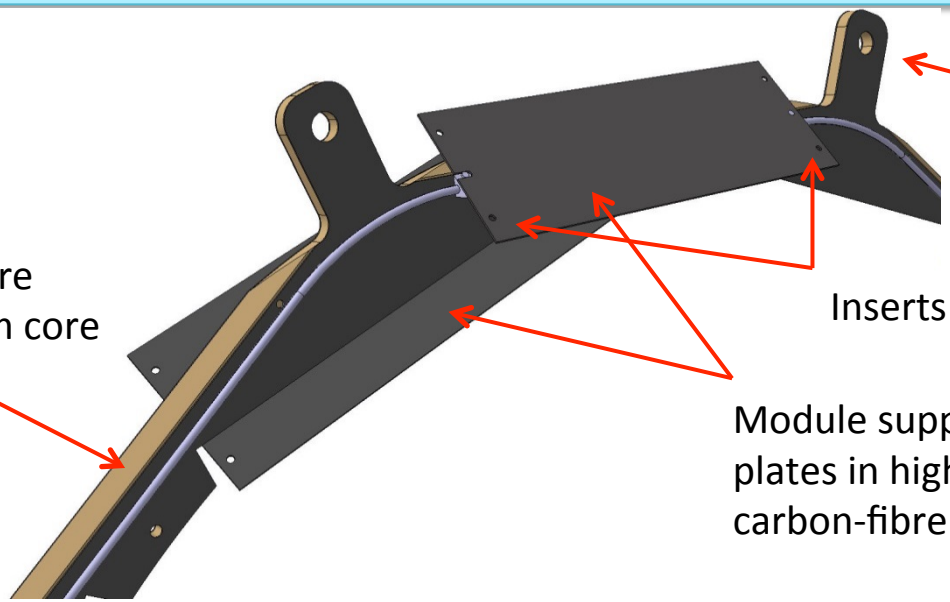
- Flat disk with cooling pipes and module supports on each side.







The Ring

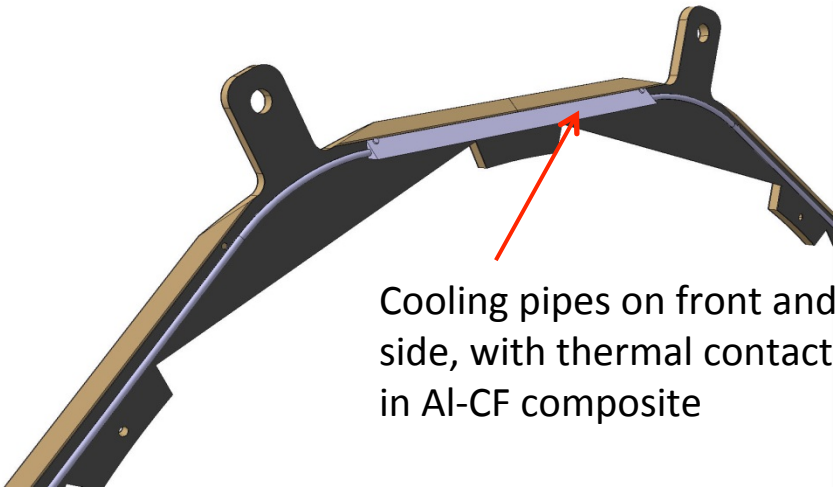


Ears for joining the Ring to the other Rings of the Layer

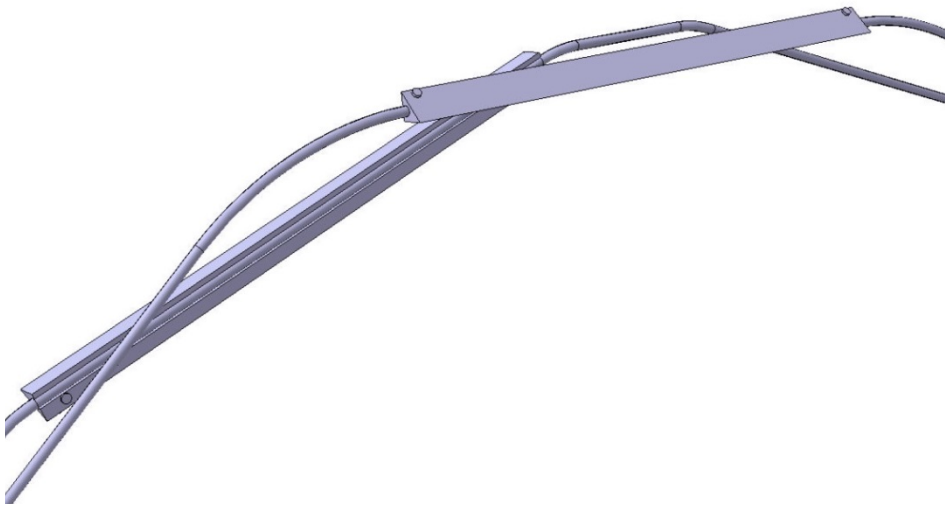
~5 mm thick sandwich structure with carbon-fibre composite skins and foam core

Inserts for module positioning

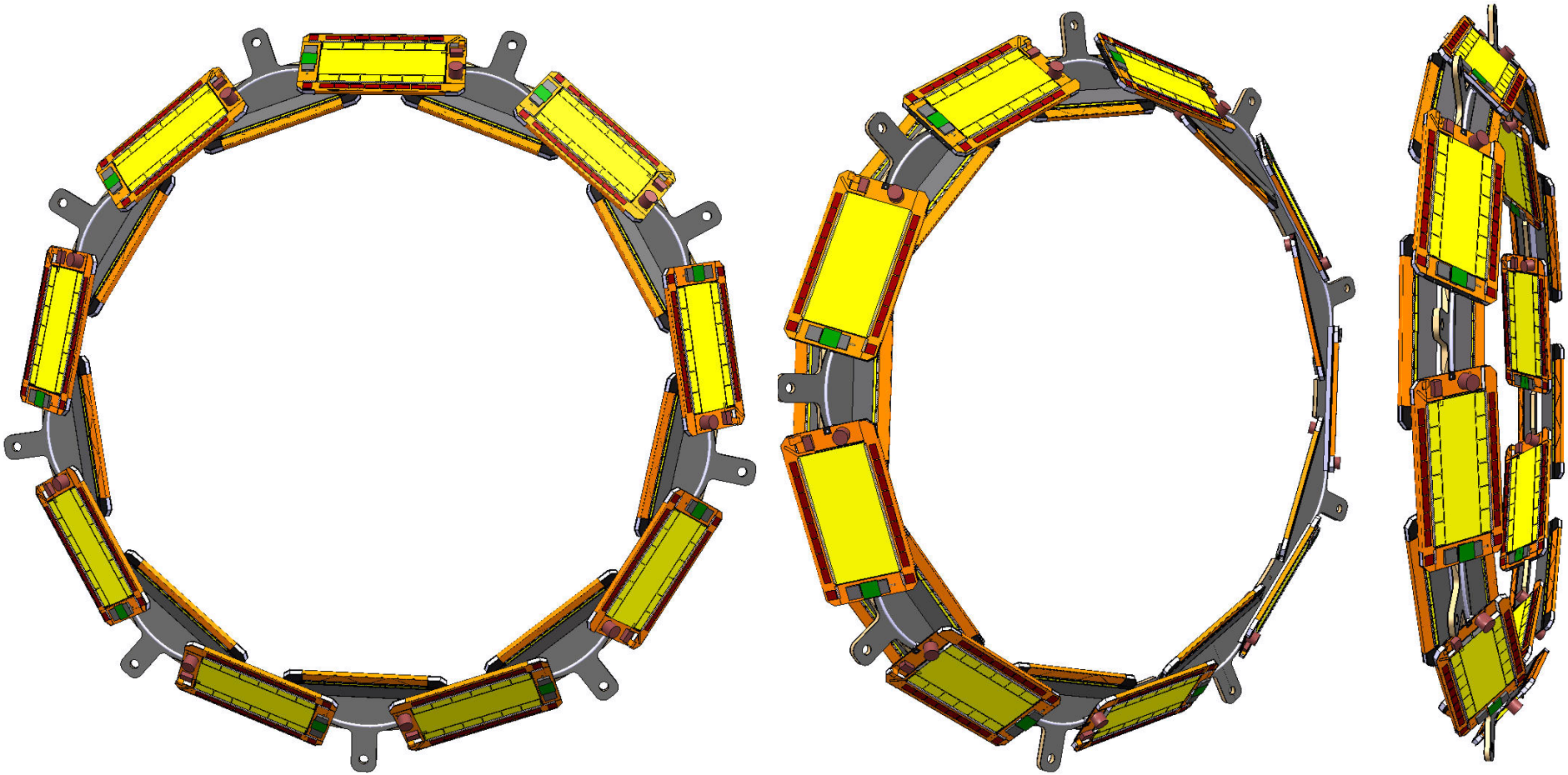
Module support / thermal contact plates in high thermal conductivity carbon-fibre composite



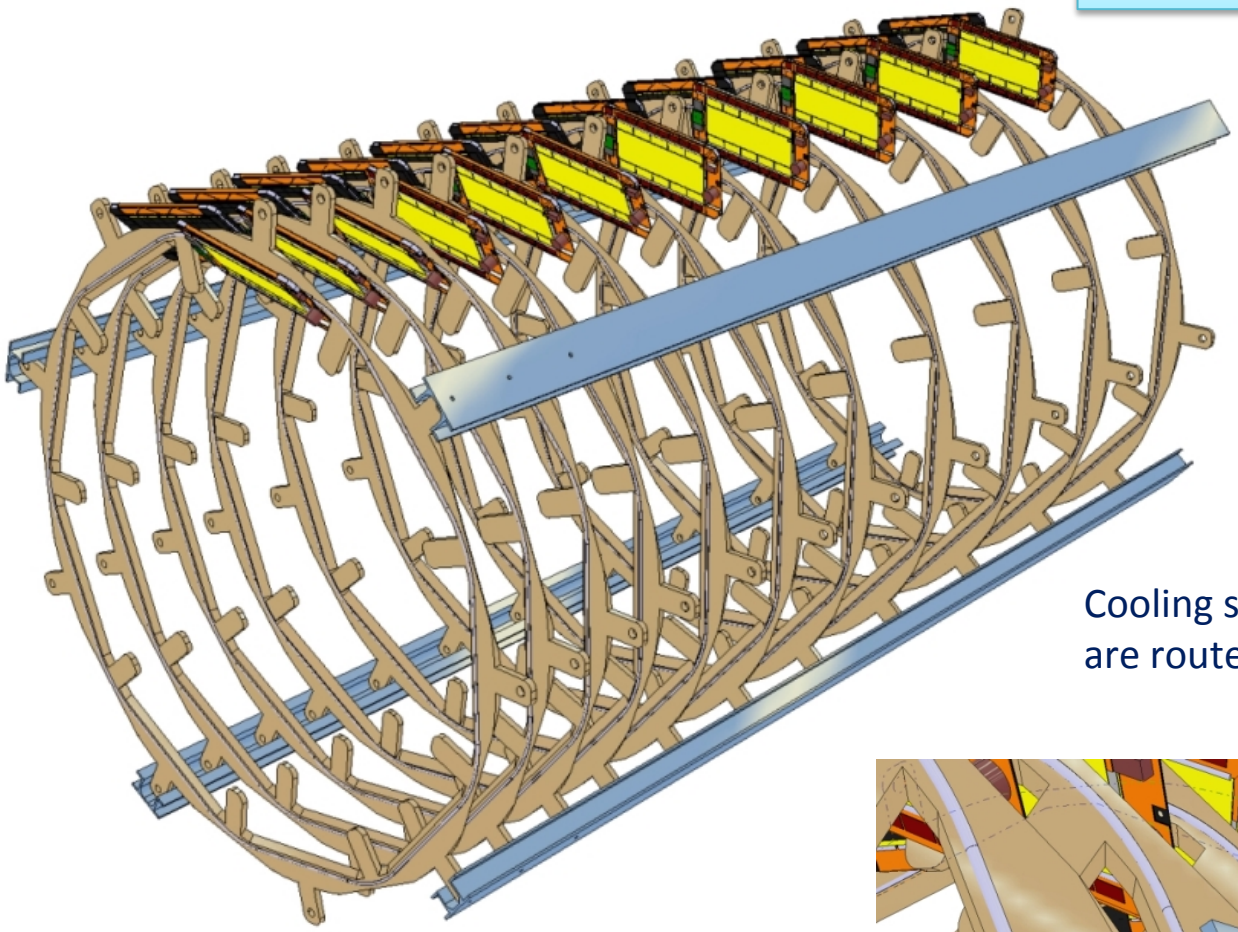
Cooling pipes on front and back side, with thermal contact pads in Al-CF composite



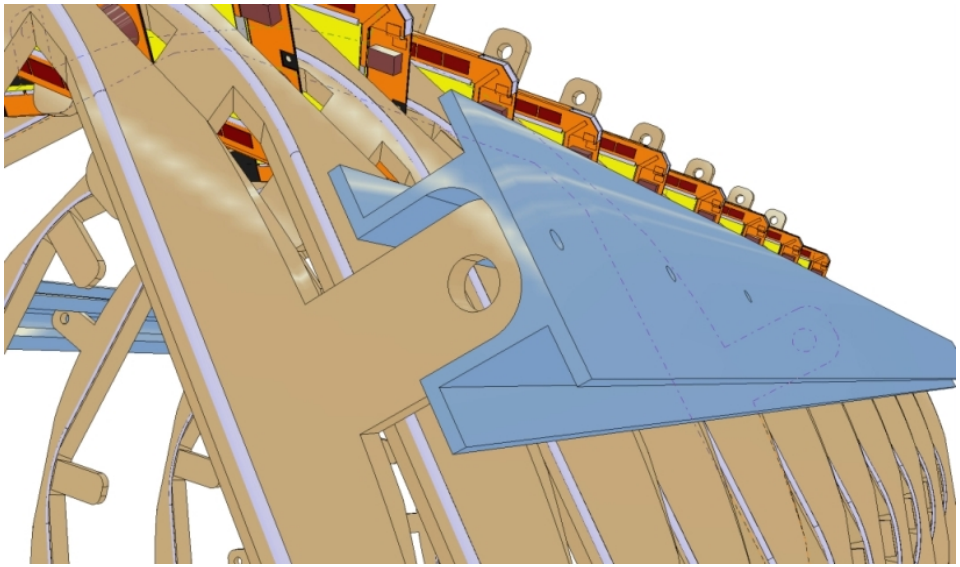
Ring with modules



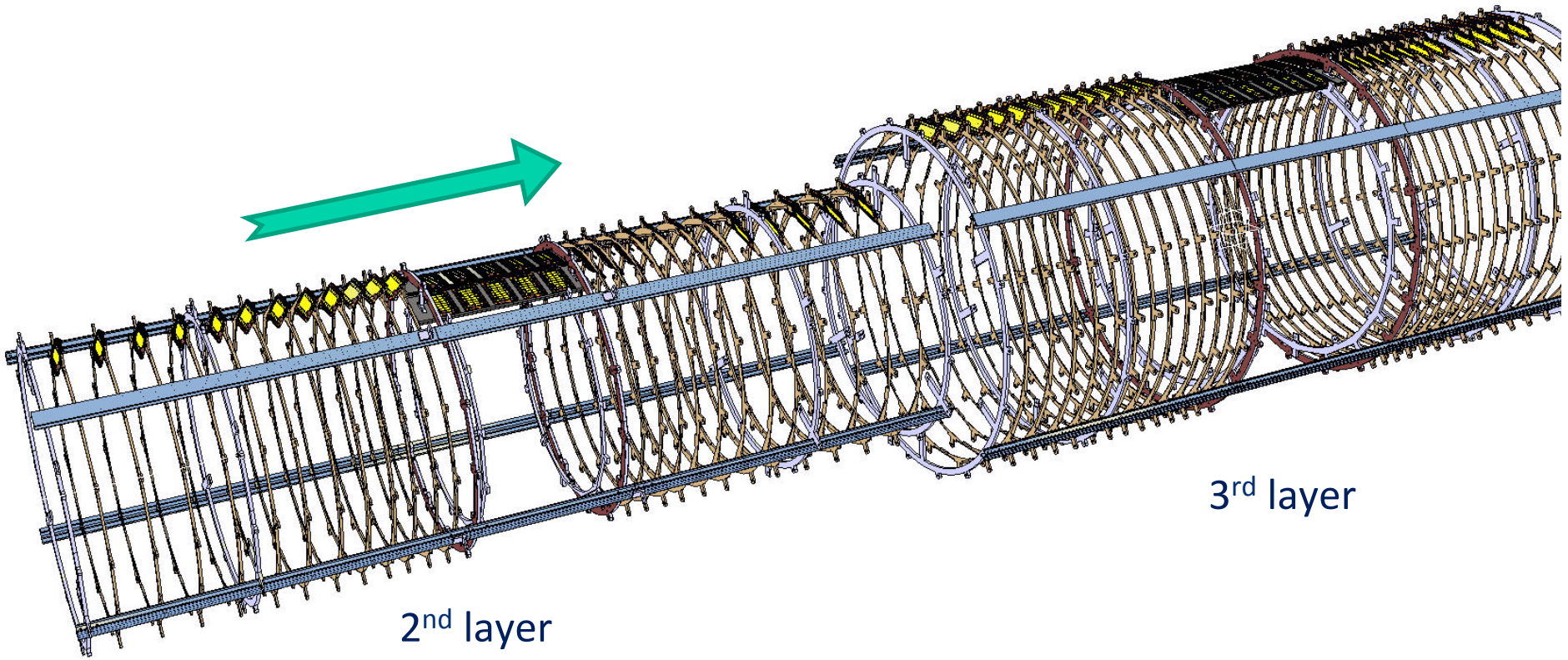
Rings joined by longitudinal bars

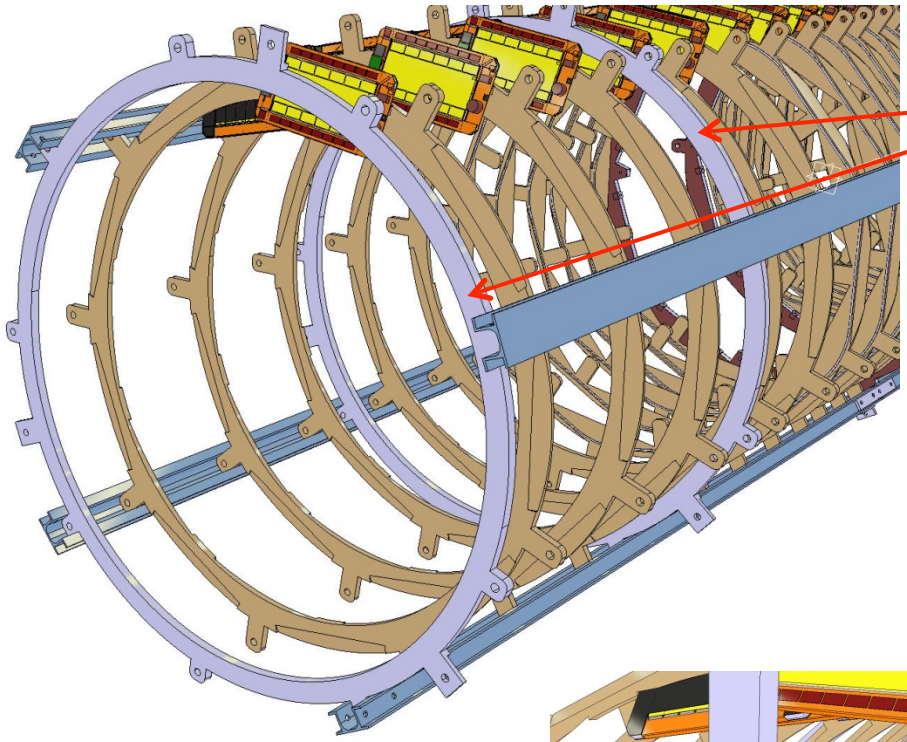


Cooling supply pipes, wires and fibres are routed along the bars.

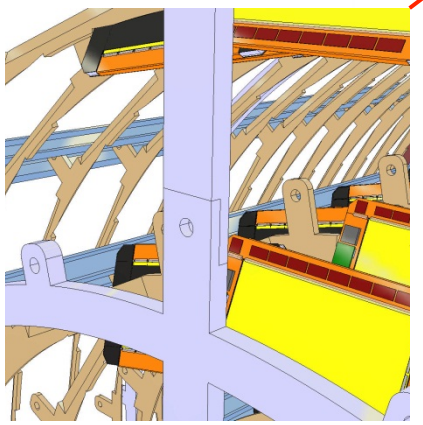


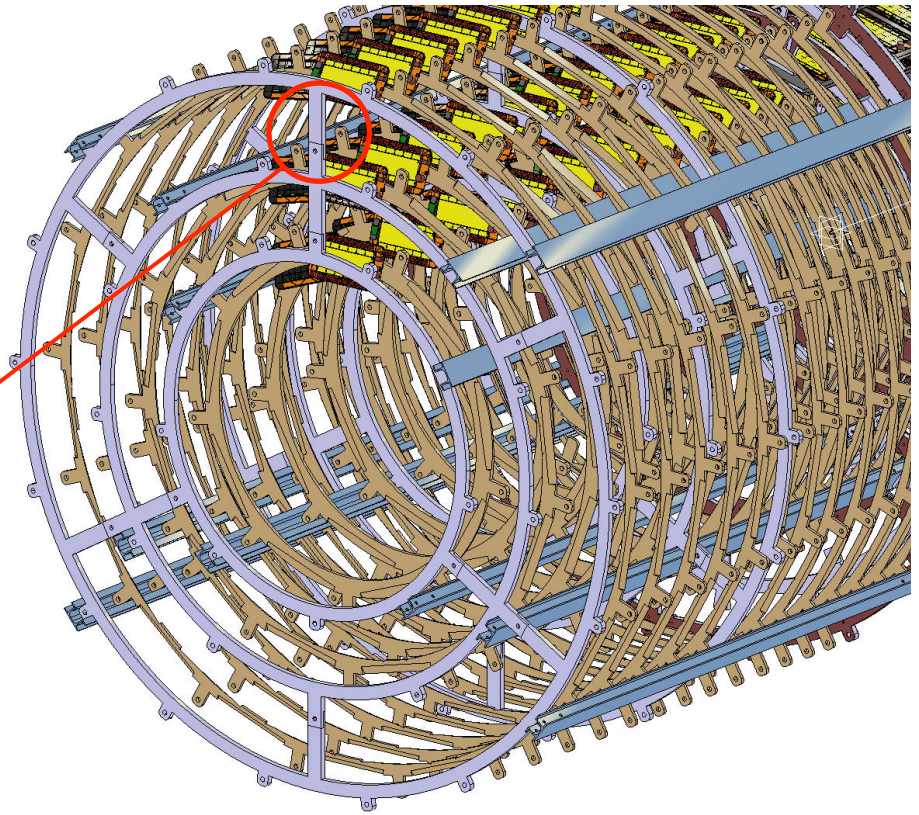
Joining layers

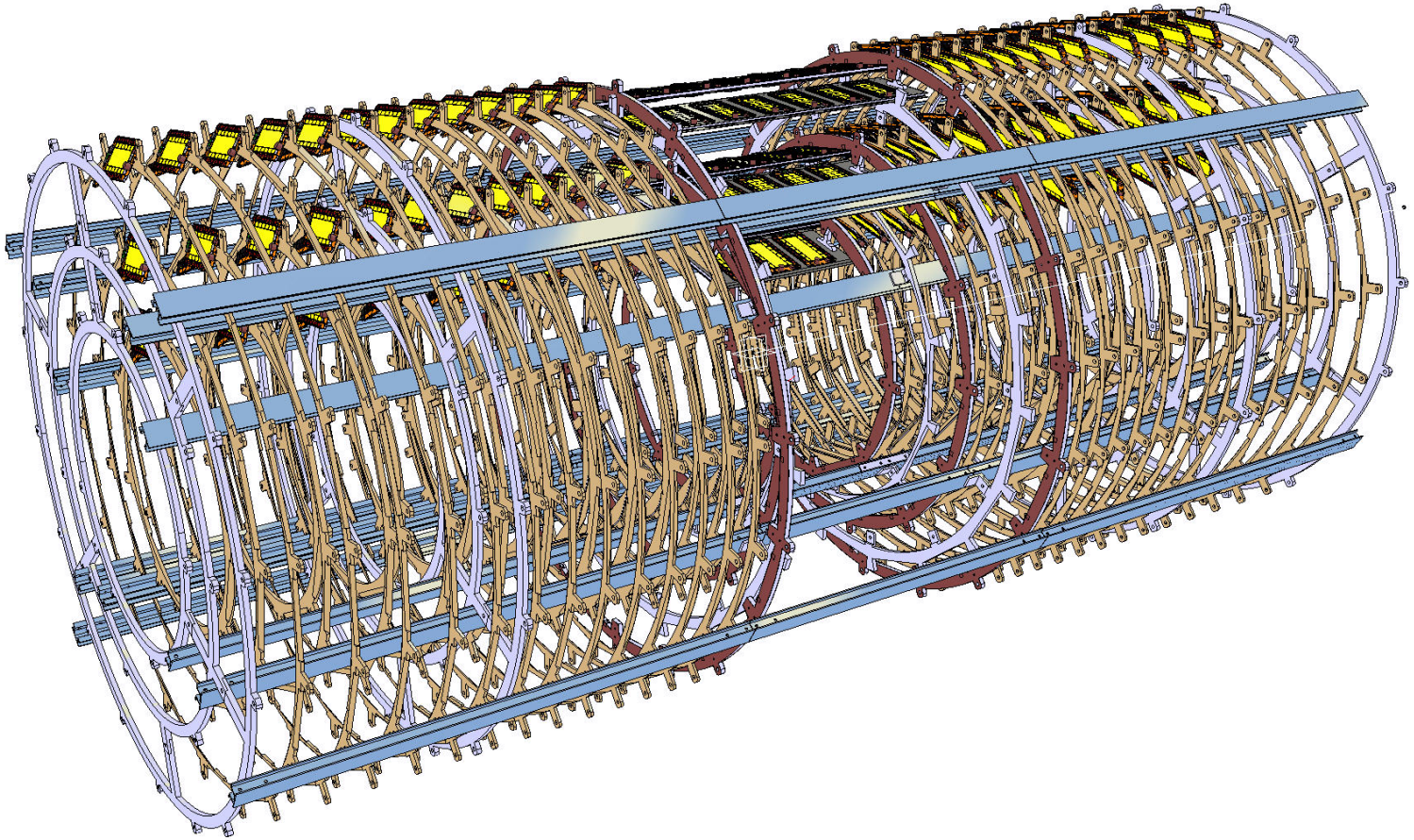




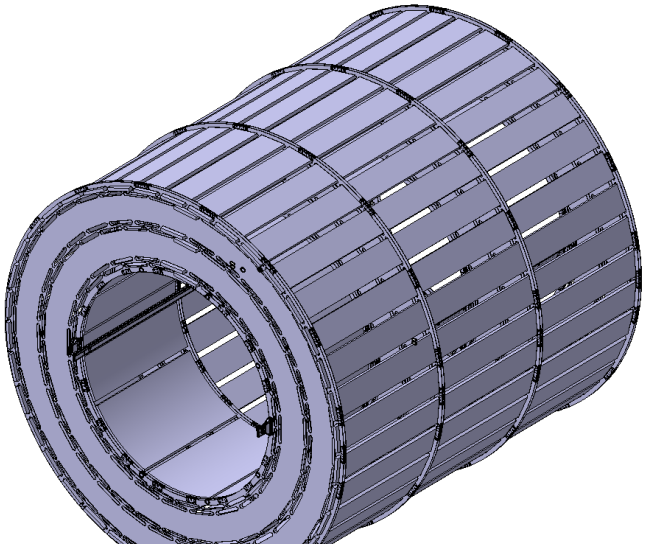
Additional rings for joining layers together

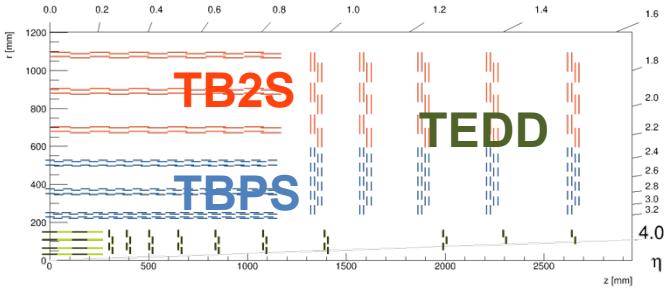


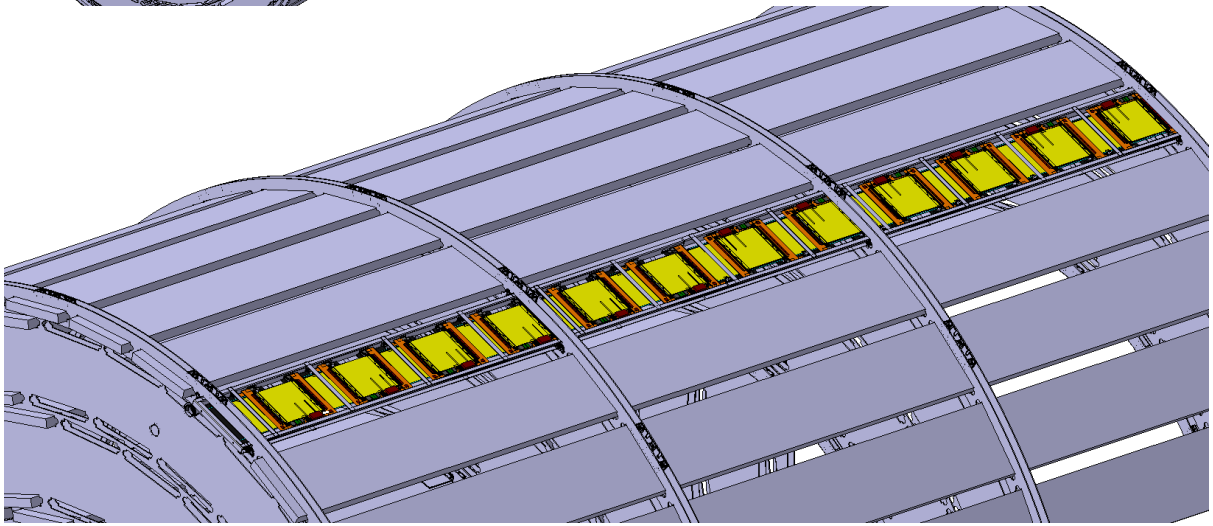


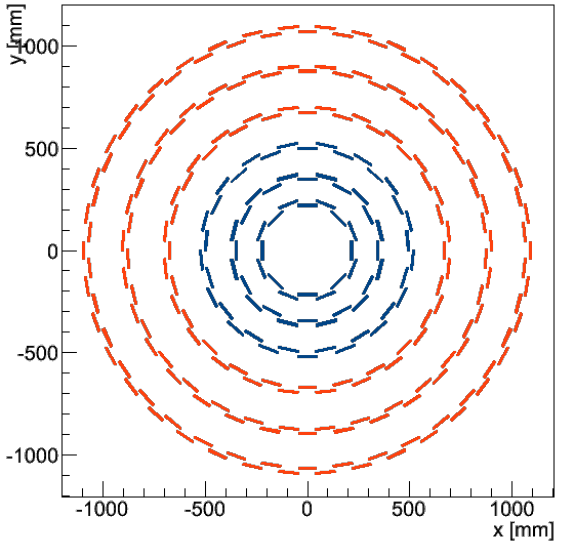


TB2S





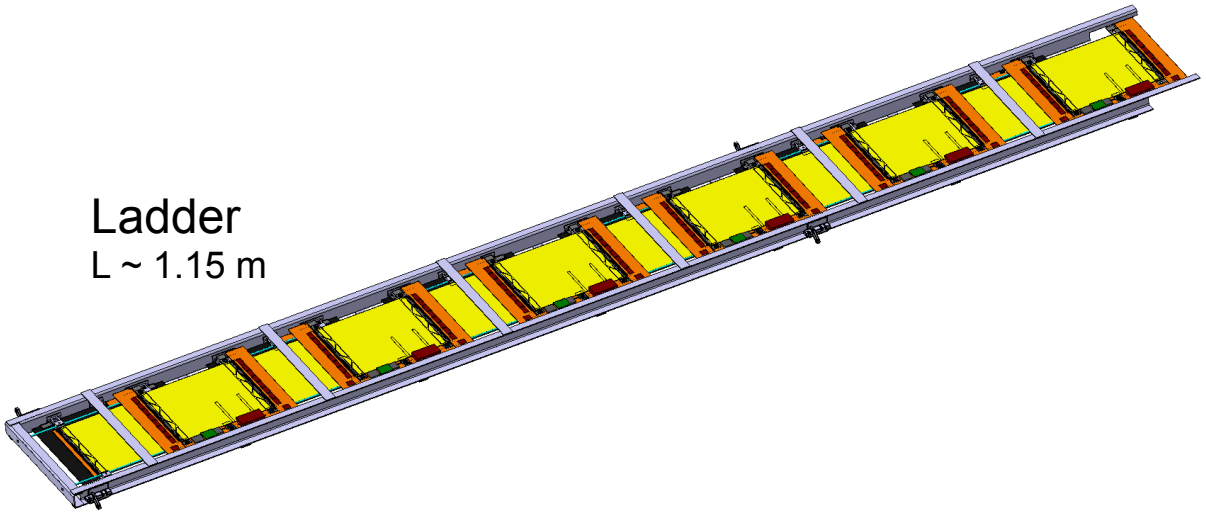




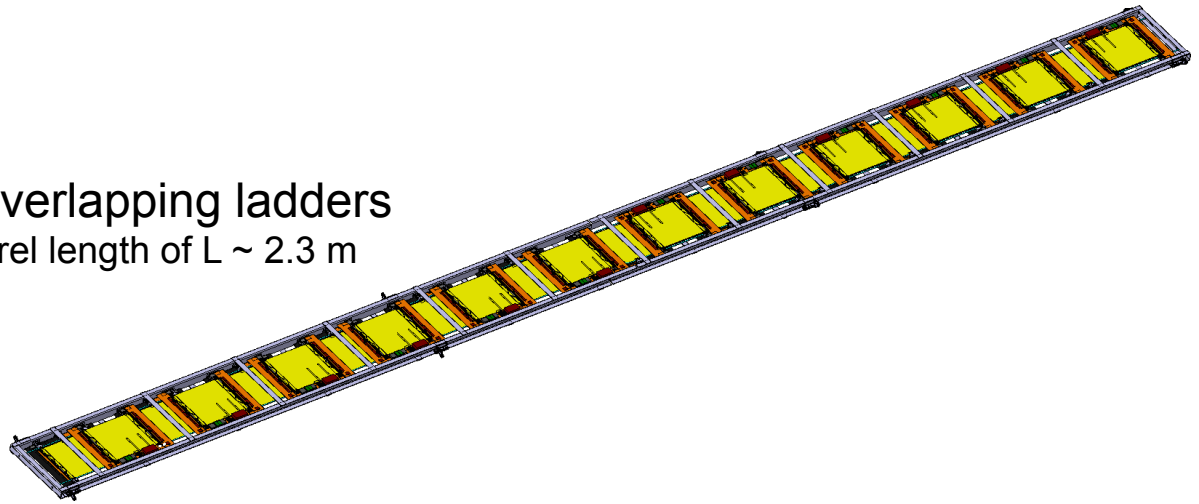
Z overlap within one “ladder”

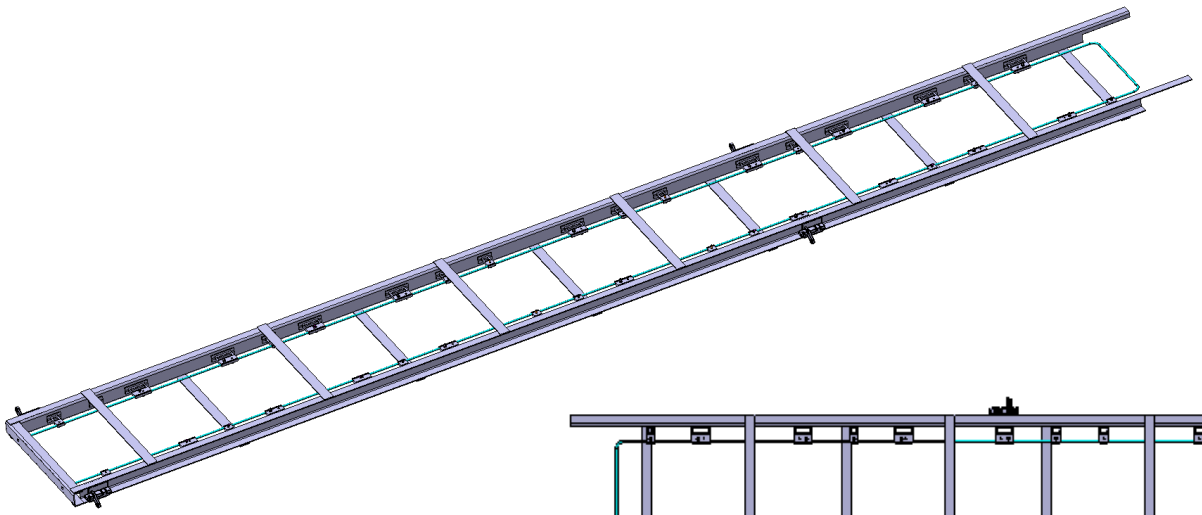
ϕ overlap between consecutive ladders

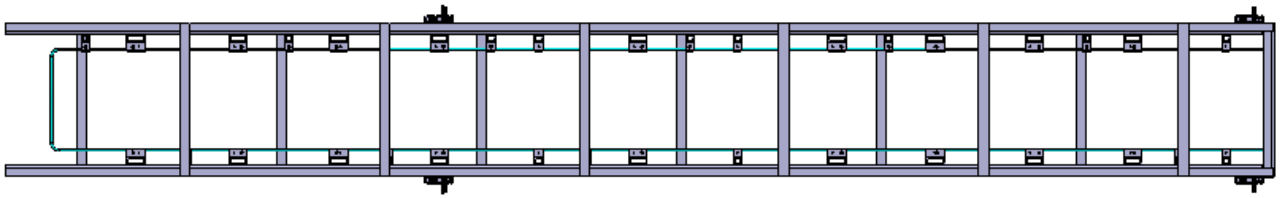
Ladder
L ~ 1.15 m

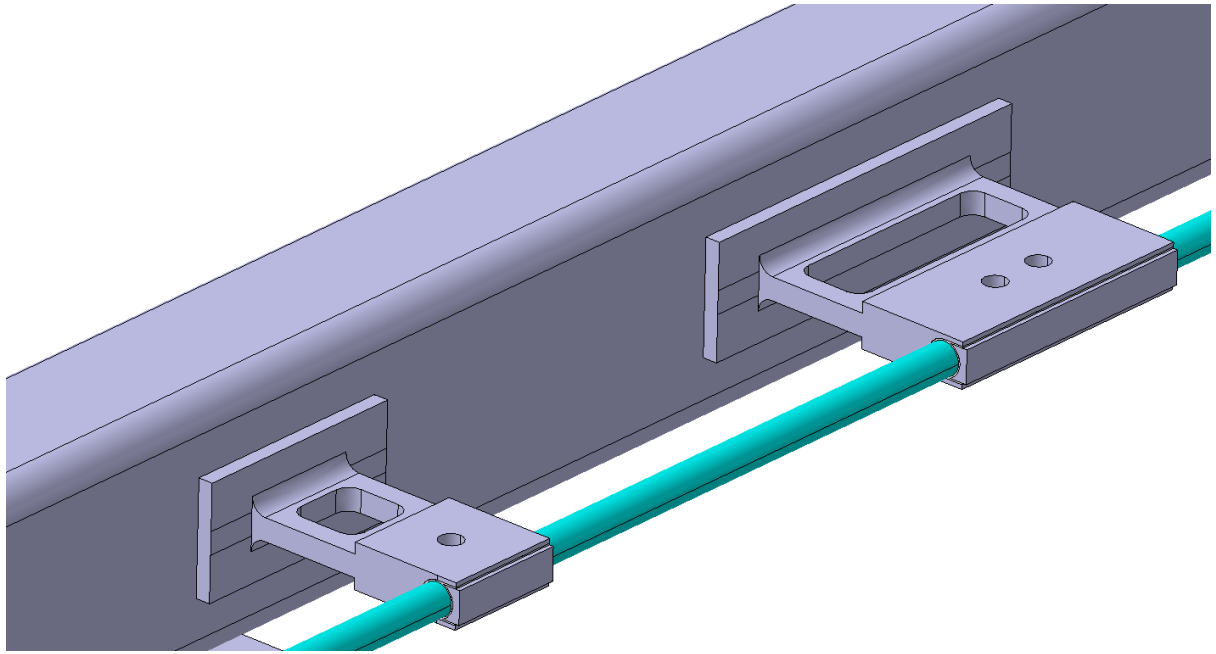


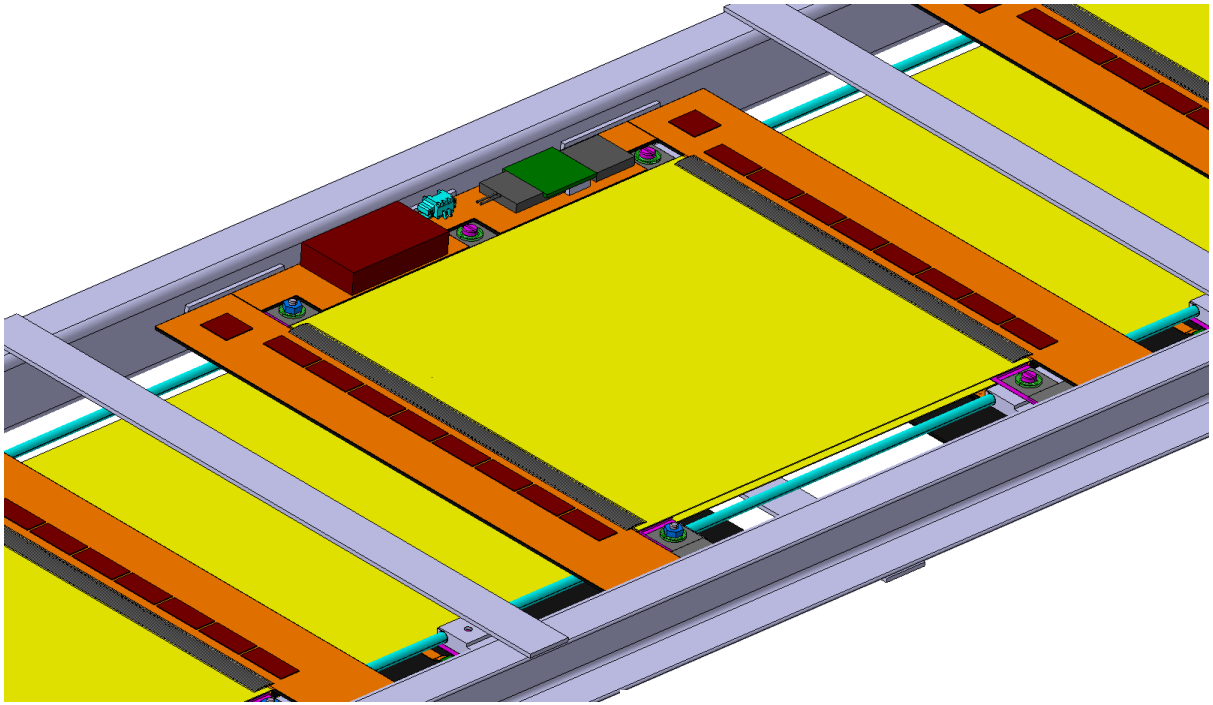
Two overlapping ladders
Full barrel length of L ~ 2.3 m

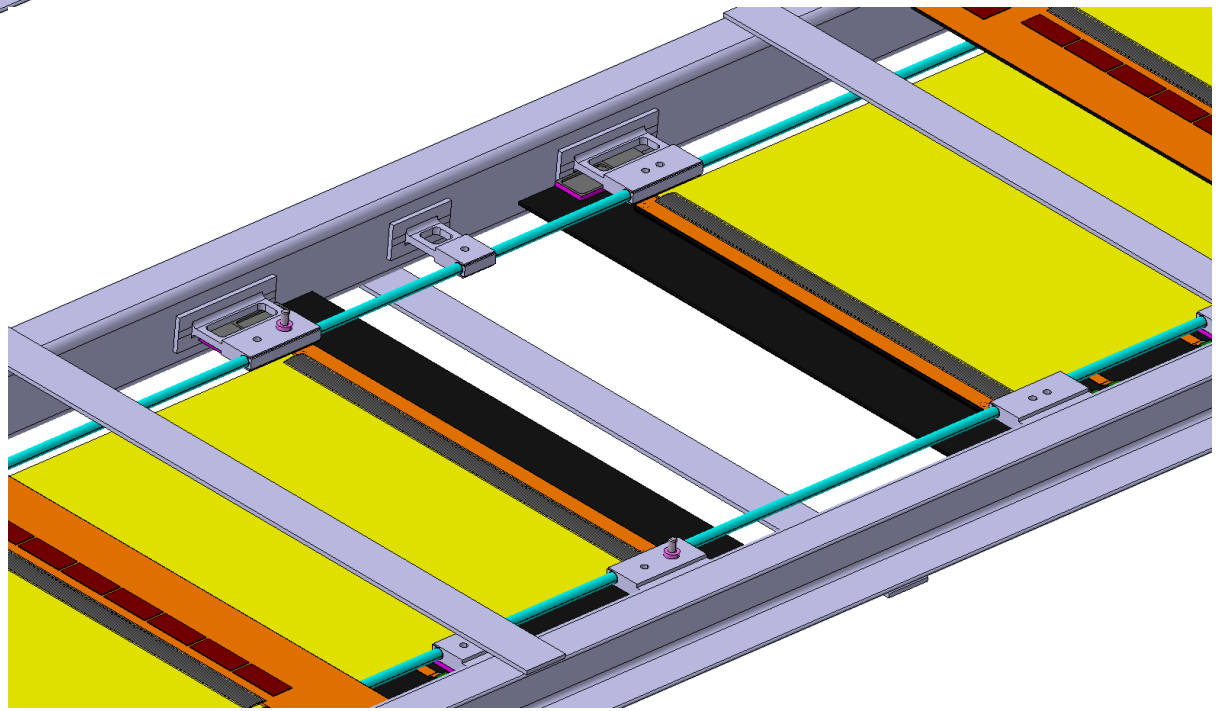






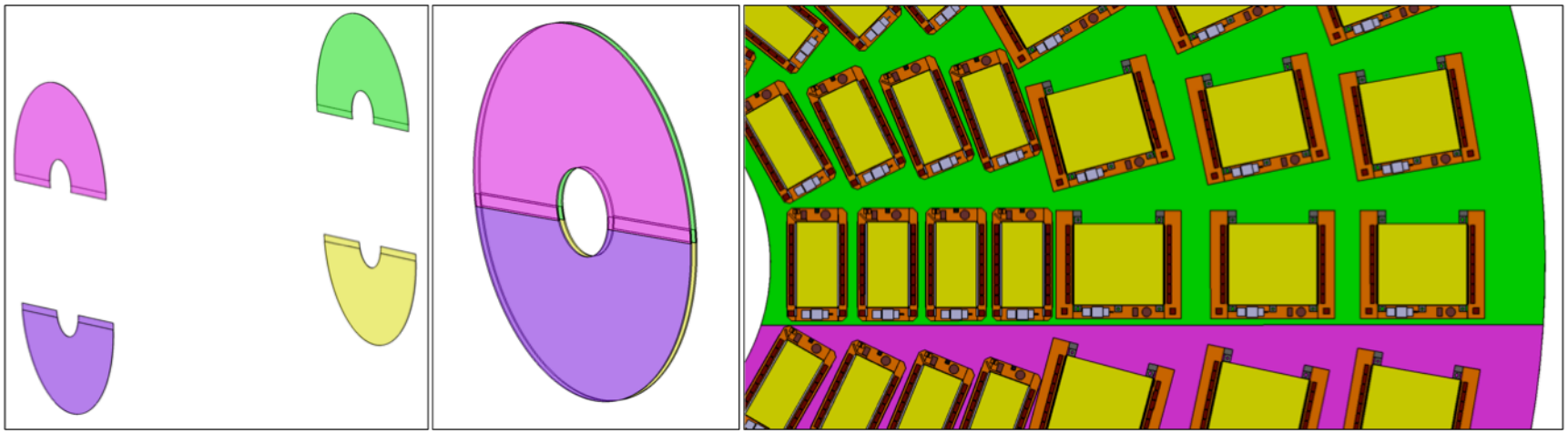


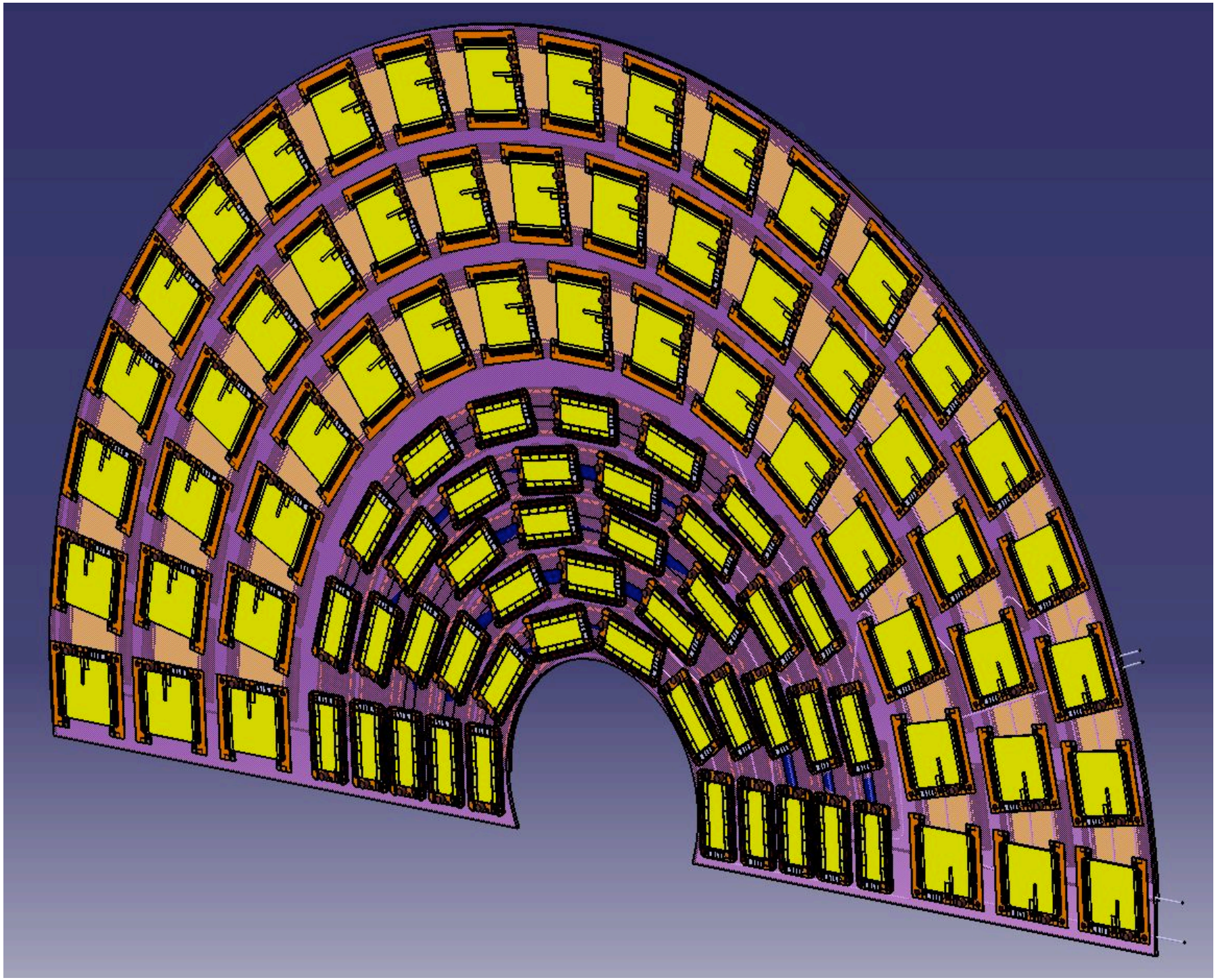


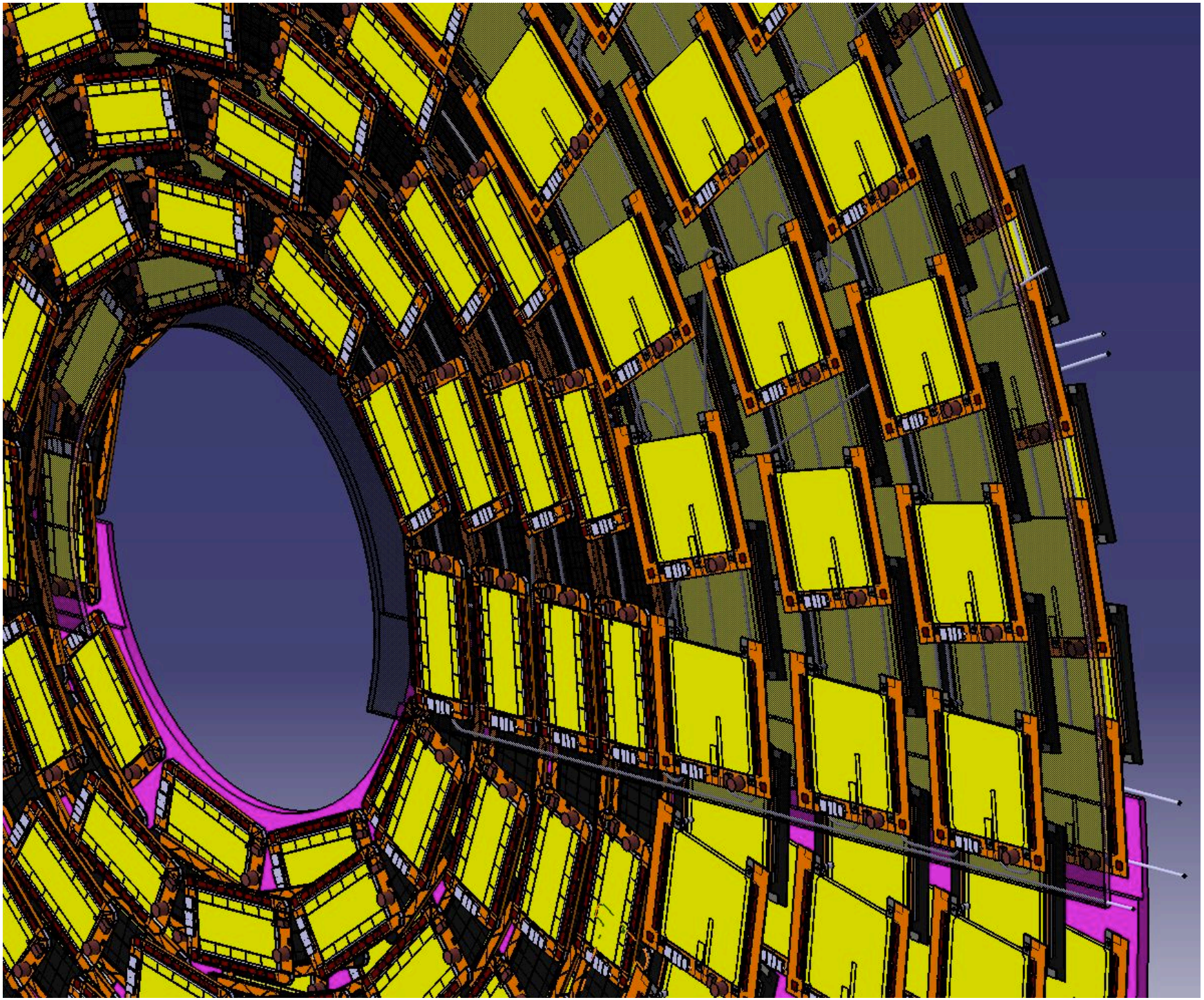


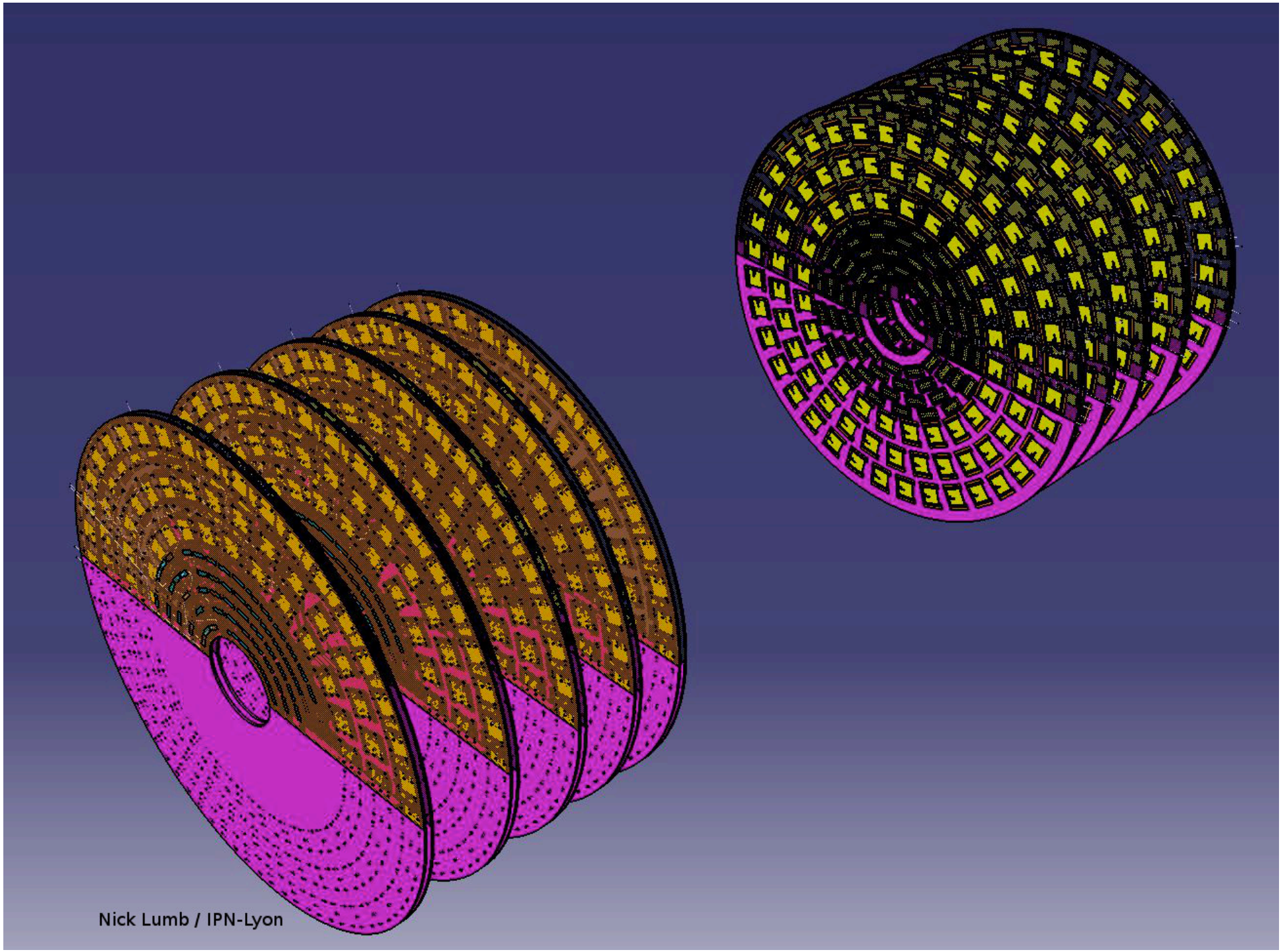
Tracker End-Cap Double Disks (TEDD)

- Modules mounted on four surfaces on two disks, each made of two dees
  - ⊙ φ overlap within disk, R overlap with next disk
- **Same rectangular modules as in the barrels**
- 9 rings of PS modules + 6 rings of 2S modules
- Cooling pipes embedded in the disk structure, wires and fibers running above and between the modules

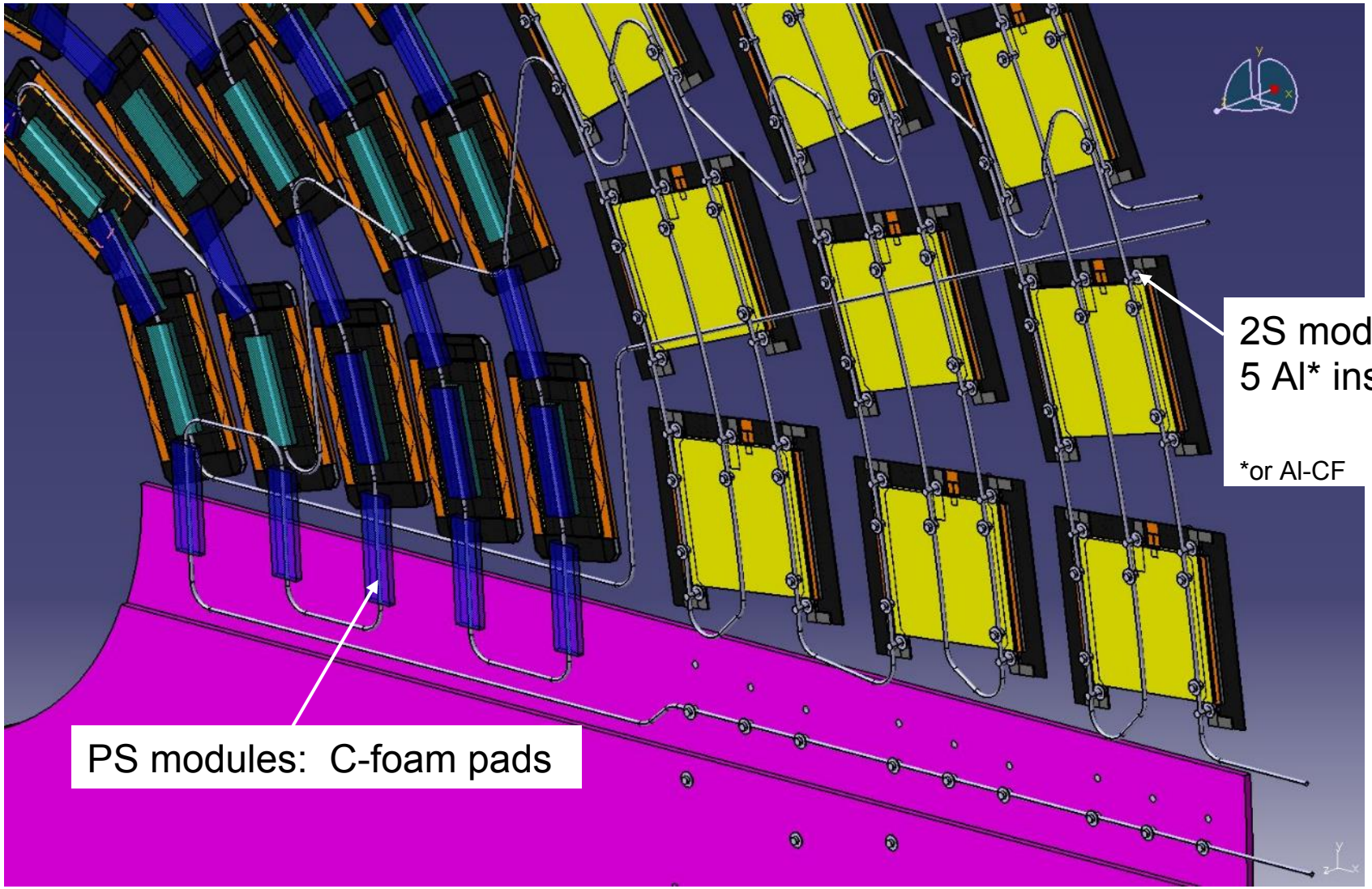


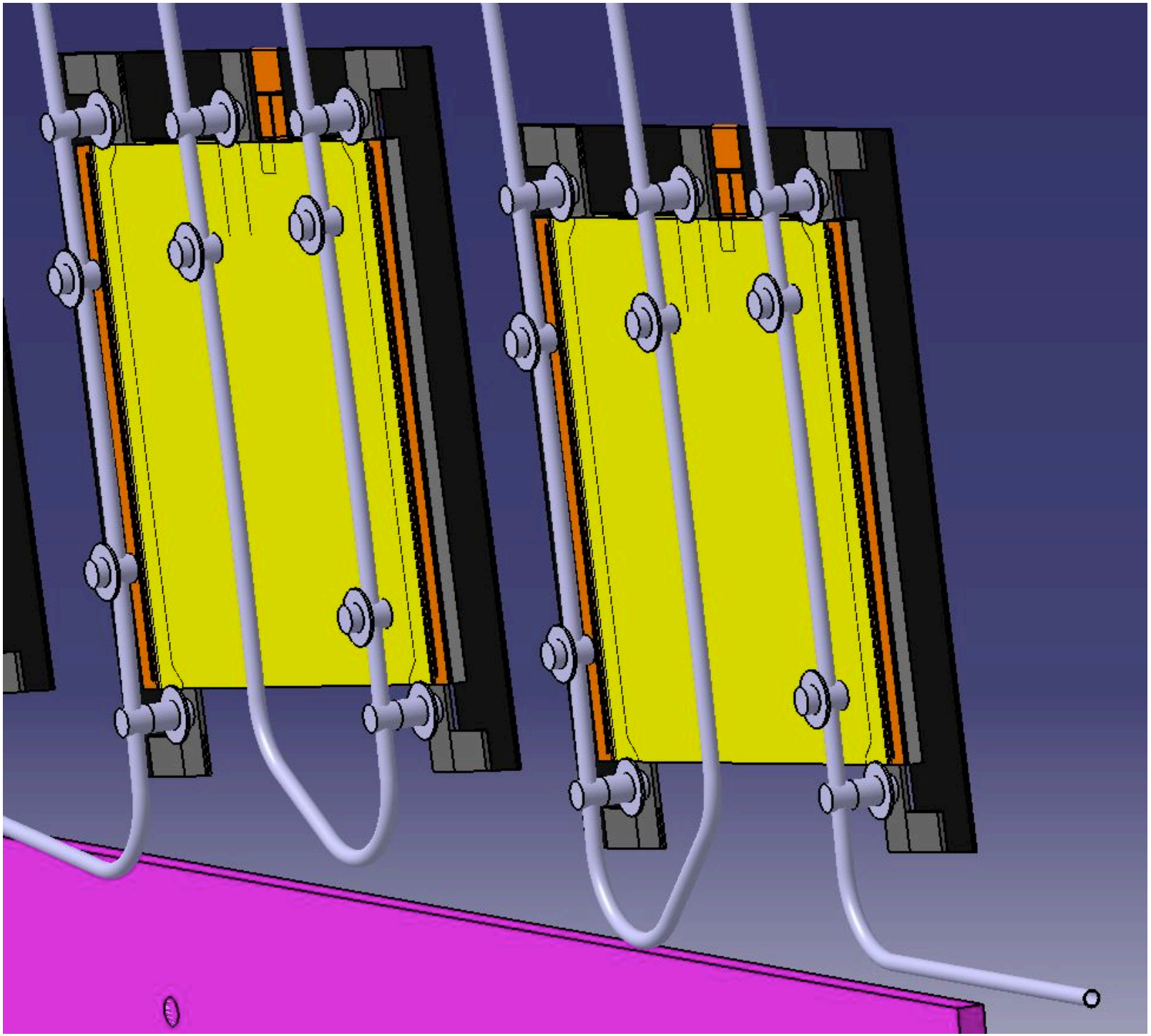


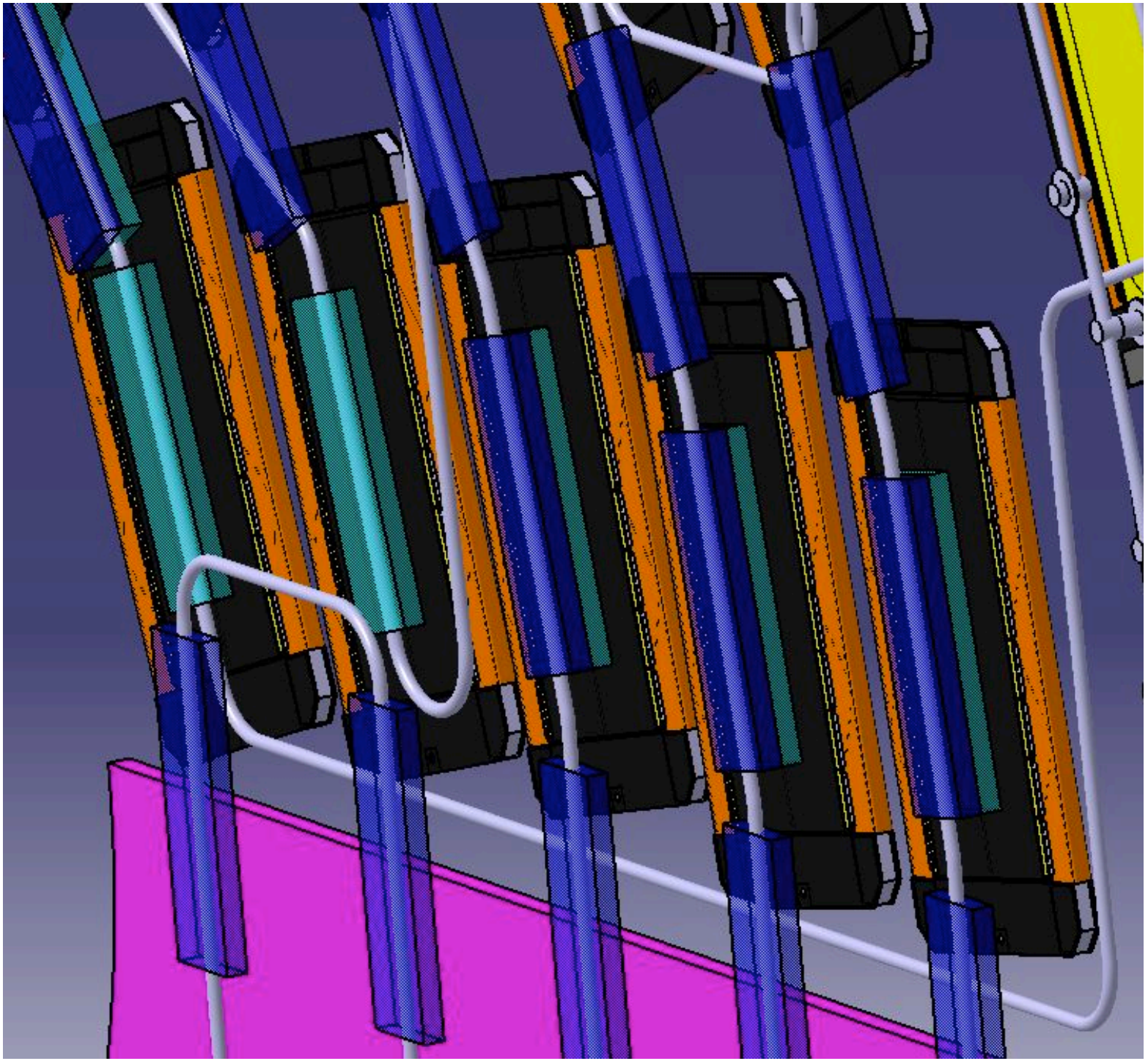



Nick Lumb / IPN-Lyon

TEDD: sector-wise cooling loops

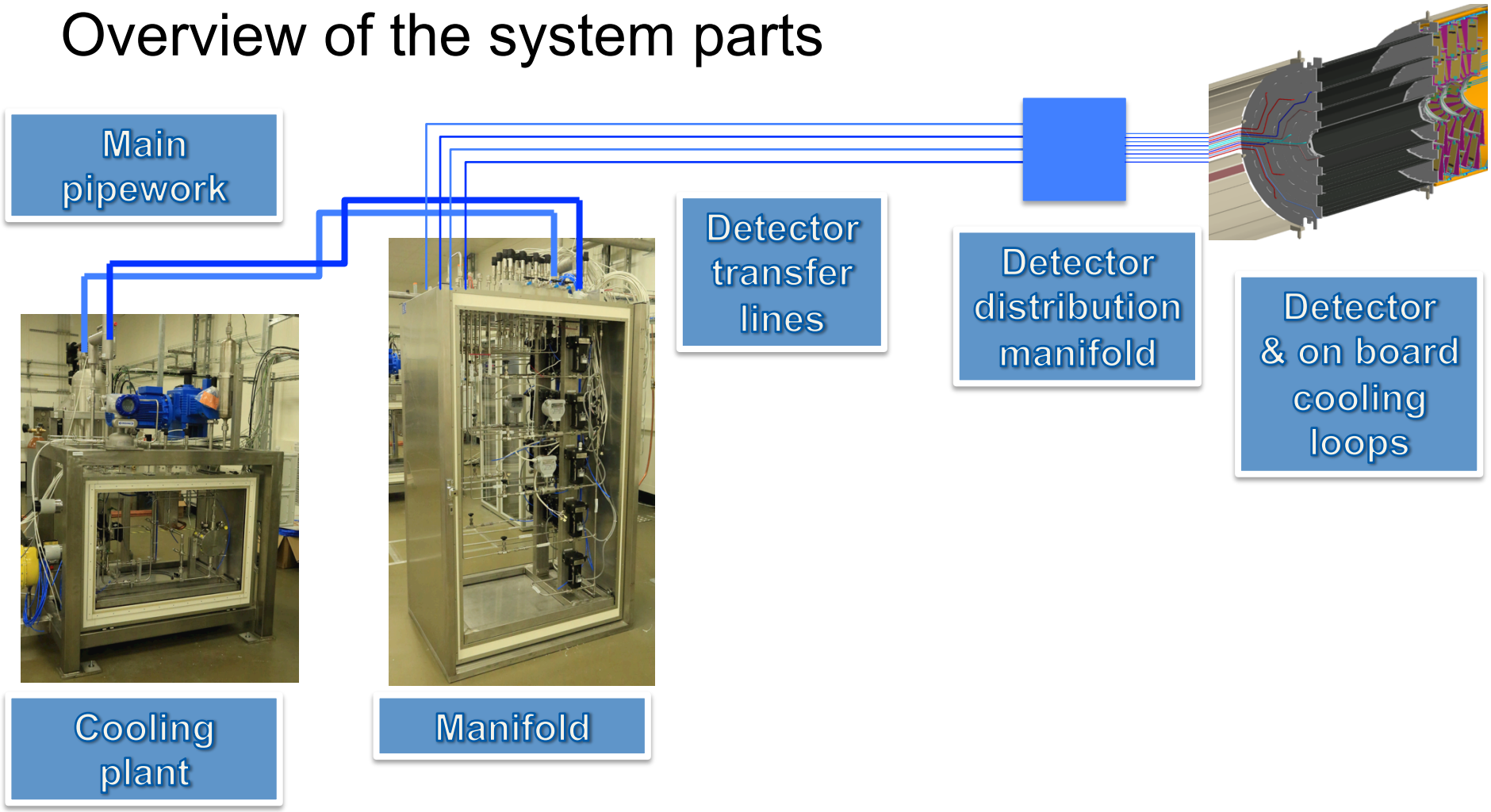






Detector cooling system

Overview of the system parts



Chosen cooling technology: two-phase CO_2

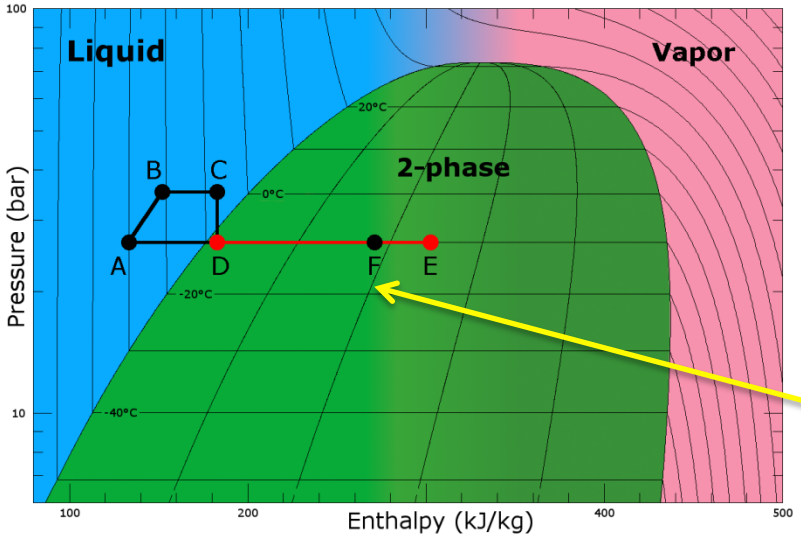
Advantages of evaporative cooling

- Heat Transfer Coefficient higher than for liquid cooling
- Limited temperature excursion on the detector
  - (isothermal evaporation – cooling exploits latent heat)

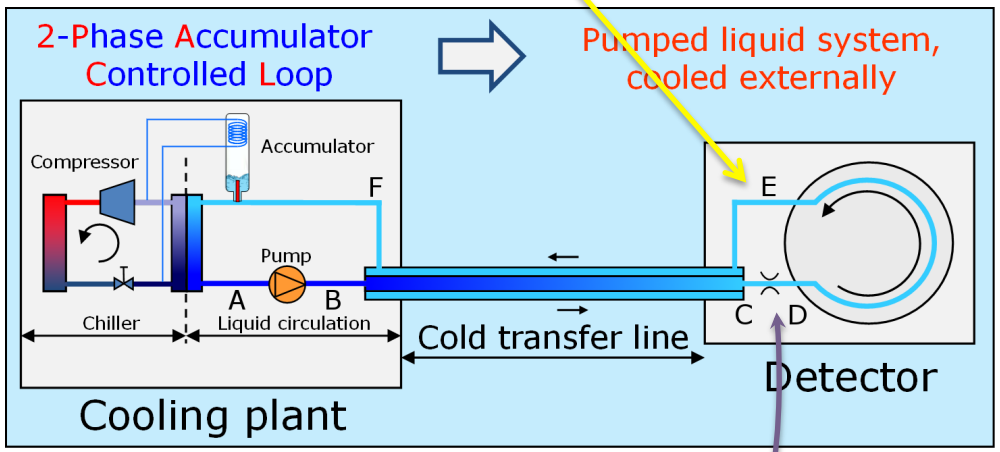
Advantages of CO_2

- Large latent heat of evaporation
- Low liquid viscosity
- Particularly high heat transfer coefficient
- Very convenient fluid to work with (environmental friendly, not activated)
- Convenient range of operating temperature −45°C to +25°C
  - Easier at low temperature

The 2PACL process



Ideal lines with no pressure drop



Capillaries

In practice a quite complex system…

Detector loops must be properly sized (avoid dry out)

Flow distribution must be stable wrt to load changes

In reality there is pressure drop along the detector loops

May require some pre-heating to ensure that the CO_2 boils…

Higher operating temperature → higher pressure rating

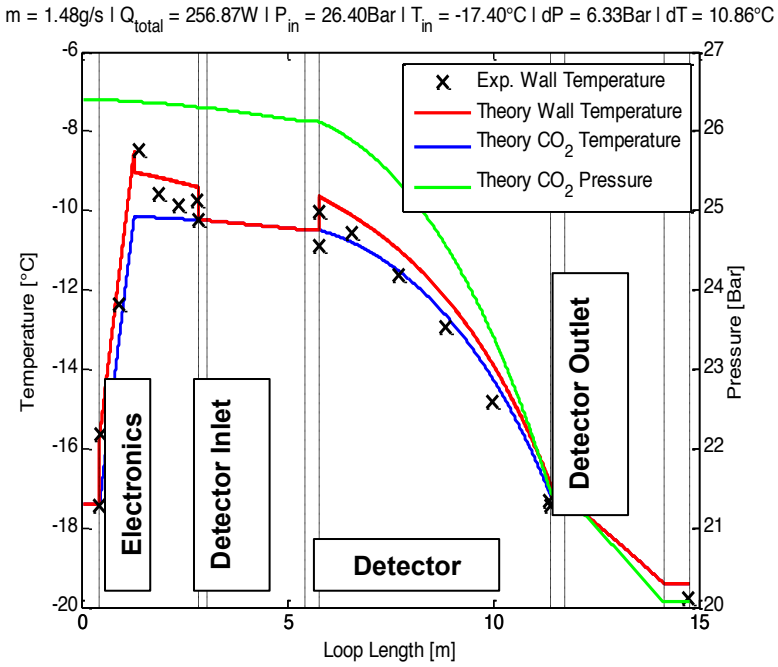
Just started reflection on system parameters

Evaporation temperature −30° C, with operational margin to about −40° C

Total power ~100 kW, about 50 cooling lines splitting to ~600 detector loops

On-detector pipes typically 2.0/2.2 mm (maybe larger in TEDD)

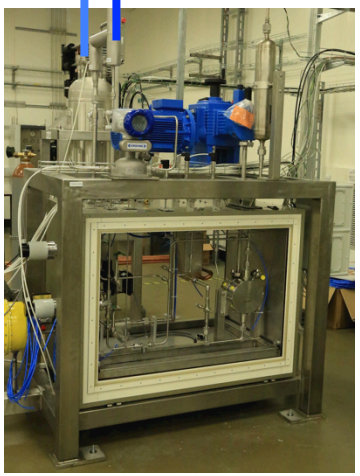
Realistic case: Pixel "phase-1"



Study of cooling system started

Reasonably solid estimate of power consumption - Detector modularity defined
Common system for Outer Tracker and Pixel

Main pipework



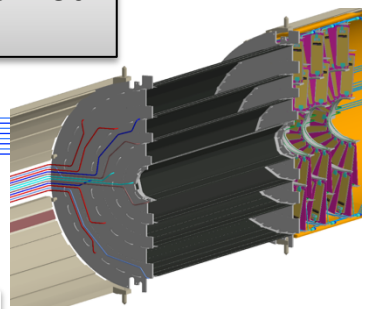
Cooling plant

Connected to a commercial chiller

Manifold

Detector transfer lines

Detector distribution manifold



Detector & on board cooling loops

Inventory of detector loops, their lengths and power
Nearly 600 loops

Possible grouping into independent cooling lines
Aim at ~50÷60 lines

L1 tracking

Three methods

- Associative Memories + track fitting
- Time-Multiplexed architecture – Hough Transform + track fitting
- Tracklet-seeded road search

AM concept

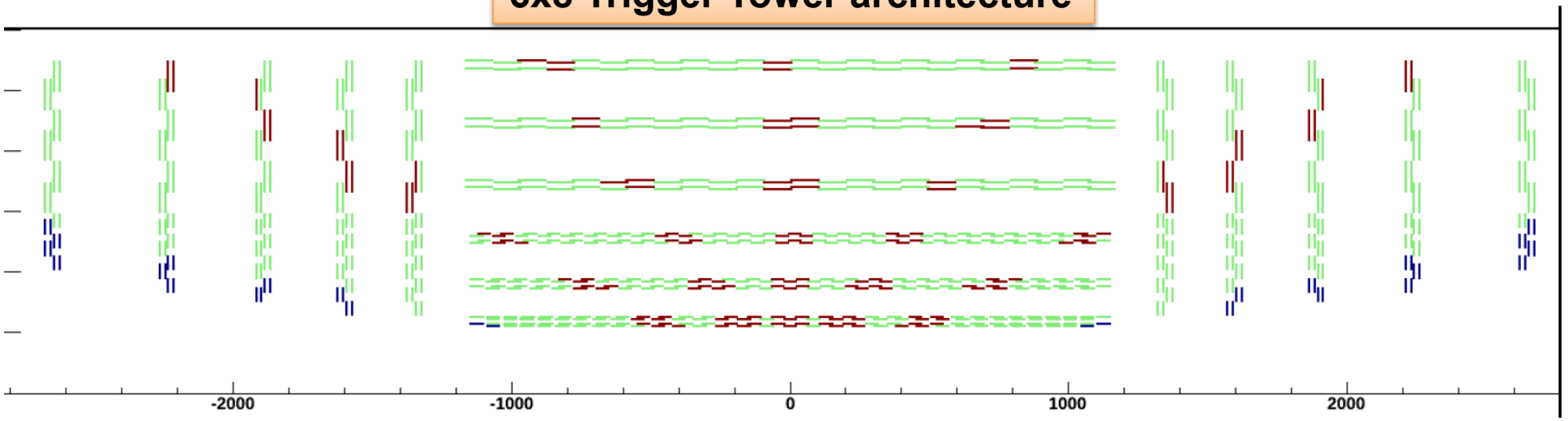
Large bank of patterns (“roads”) stored in a dedicated Associative Memory chip

- Roads are defined with coarse-resolution coordinates
  - → *Keep the number of patterns manageable*
- Stub coordinates are loaded in the Memory
- Matched patterns are the track candidates

Refit track candidates with full-resolution coordinates

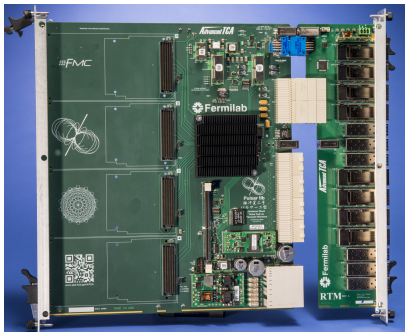
- Achieve ultimate resolution, remove fake combinations / duplicates

6x8 Trigger Tower architecture

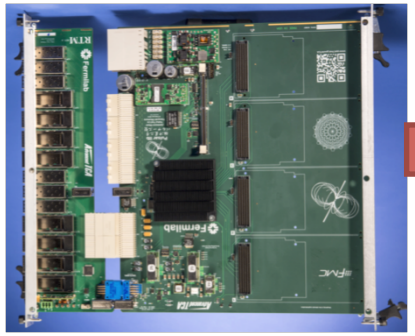


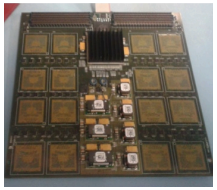
AM + FPGA approach: Data Flow Stages/Hardware

FNAL Pulsar 2b

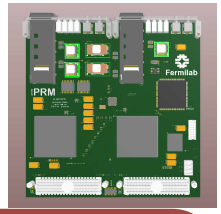


FNAL Pulsar 2b





INFN Mezzanine card
for AMchip05/06



FNAL Mezzanine card
for protoVIPRAM02

Data Sourcing

Emulate trigger data from upstream

Pulsar- 2b/RTM/
IPMC
DS Firmware/ software

Data Formatting/ Delivery

Deliver stubs to the pattern recognition engine

Δt1

Pulsar- 2b/RTM/
IPMC
PRB Firmware

Pattern Recognition

Fast PR using AM chips

Δt2

PR Mezzanine Card
Data Organizer firmware
+ AM Chips
Followed by Track Fitting firmware

Track Fitting

Calculate track parameters in FPGA

Δt3

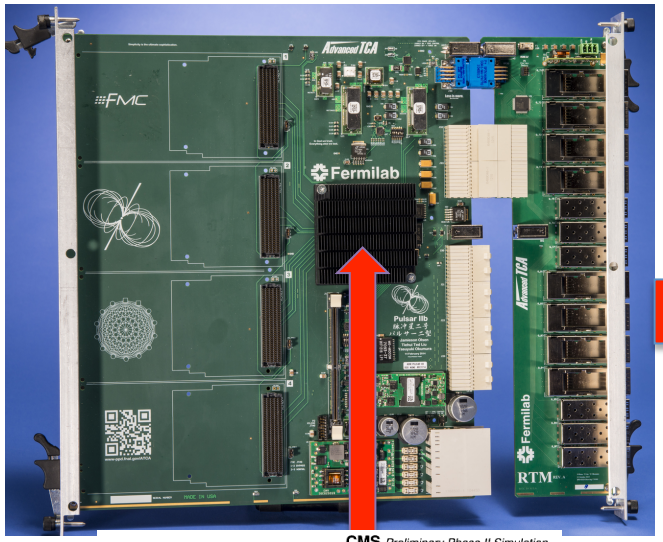
AM + FPGA on PR mezzanine

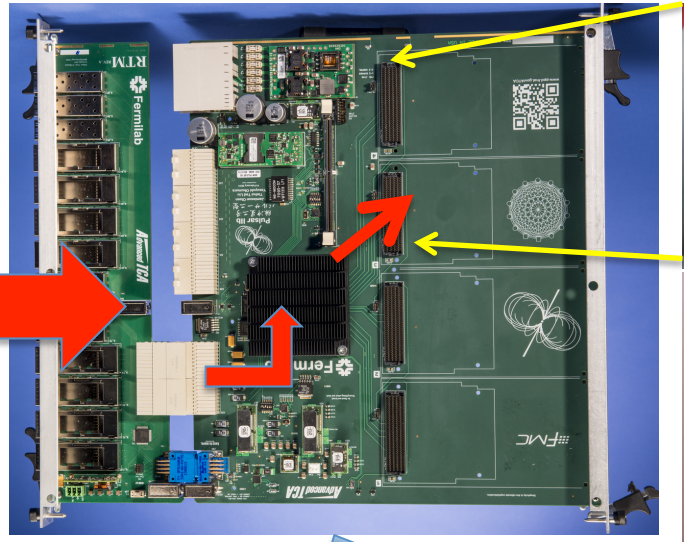
Board Level Demonstration in 2015

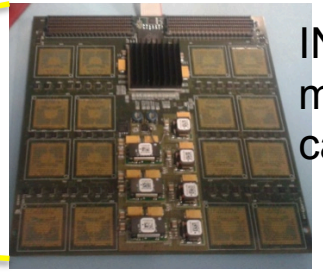
Data Source (FNAL/Brazil): emulating ~40 modules

PRB

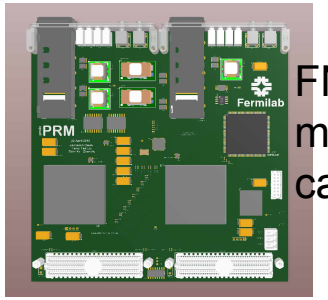
Δt1 (Data Delivery) + Δt2(AM) + Δt3 (TF)



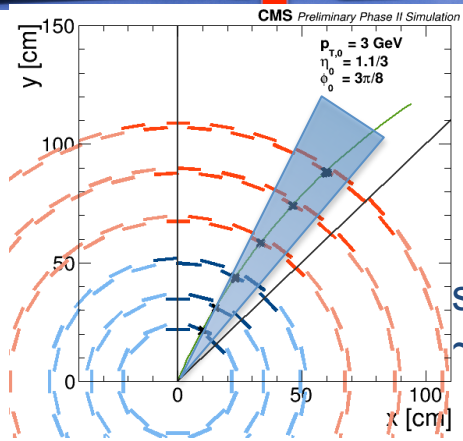




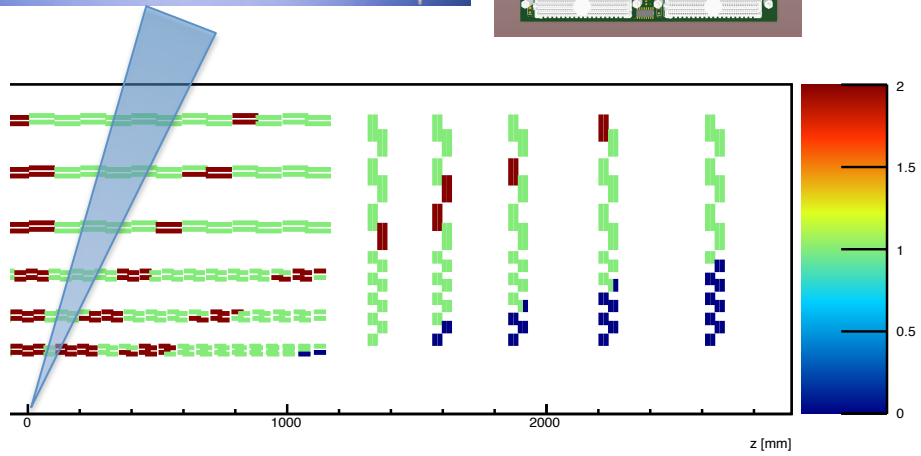
INFN mezzanine card



FNAL mezzanine card



select ~40 modules



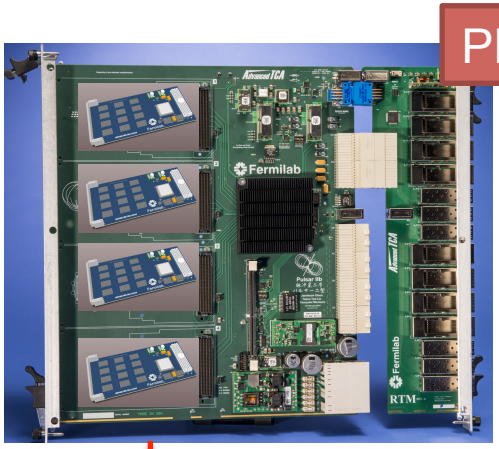
Details are being worked out

Full-Scale Demonstration (goal of 2016)

Data Source crate

- 400 fibers worth of data from one Trigger Tower
- Includes neighbor data needed for this Trigger Tower

All 10 PRBs take turn to process events



Data Sourcing

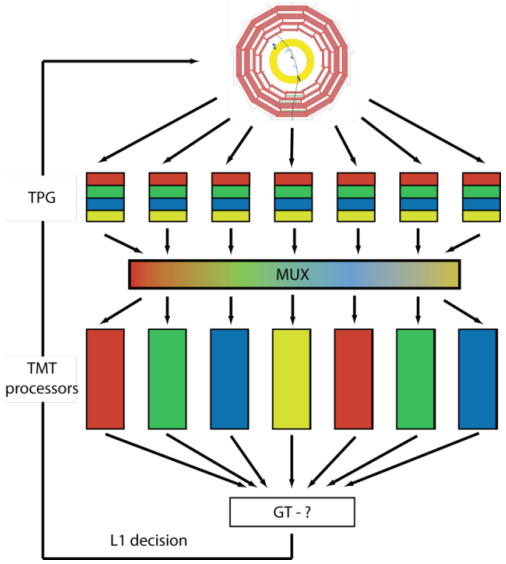
400 optical links

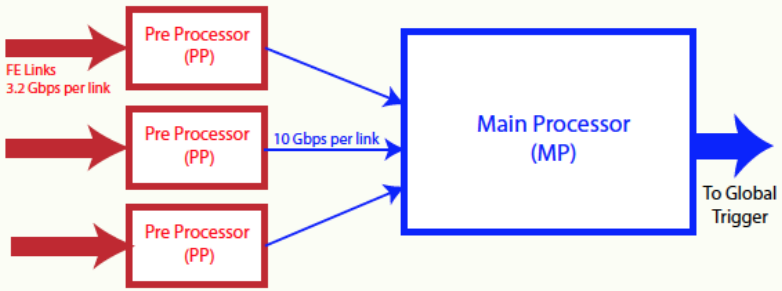
via full-mesh backplane

Target PRB

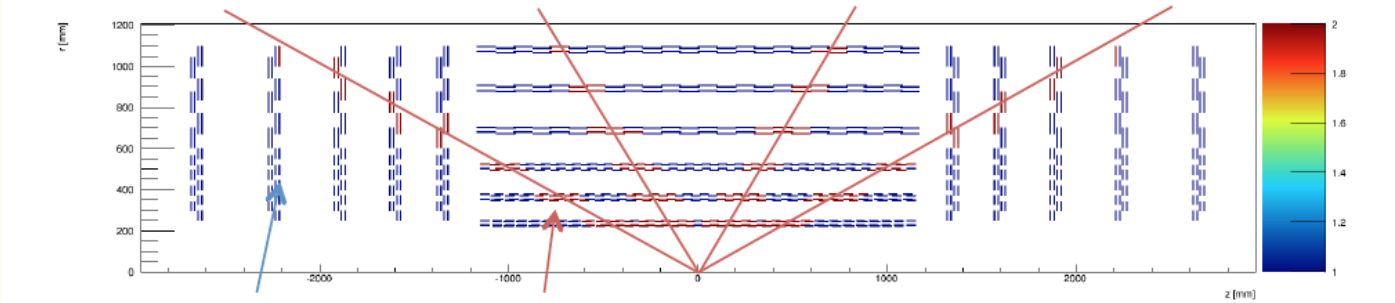
TMT architecture

Principle:
- all data from one event arrives in one processing node, over N BX (the time multiplexing period)
- round-robin scheduling over N nodes, each node processing one event



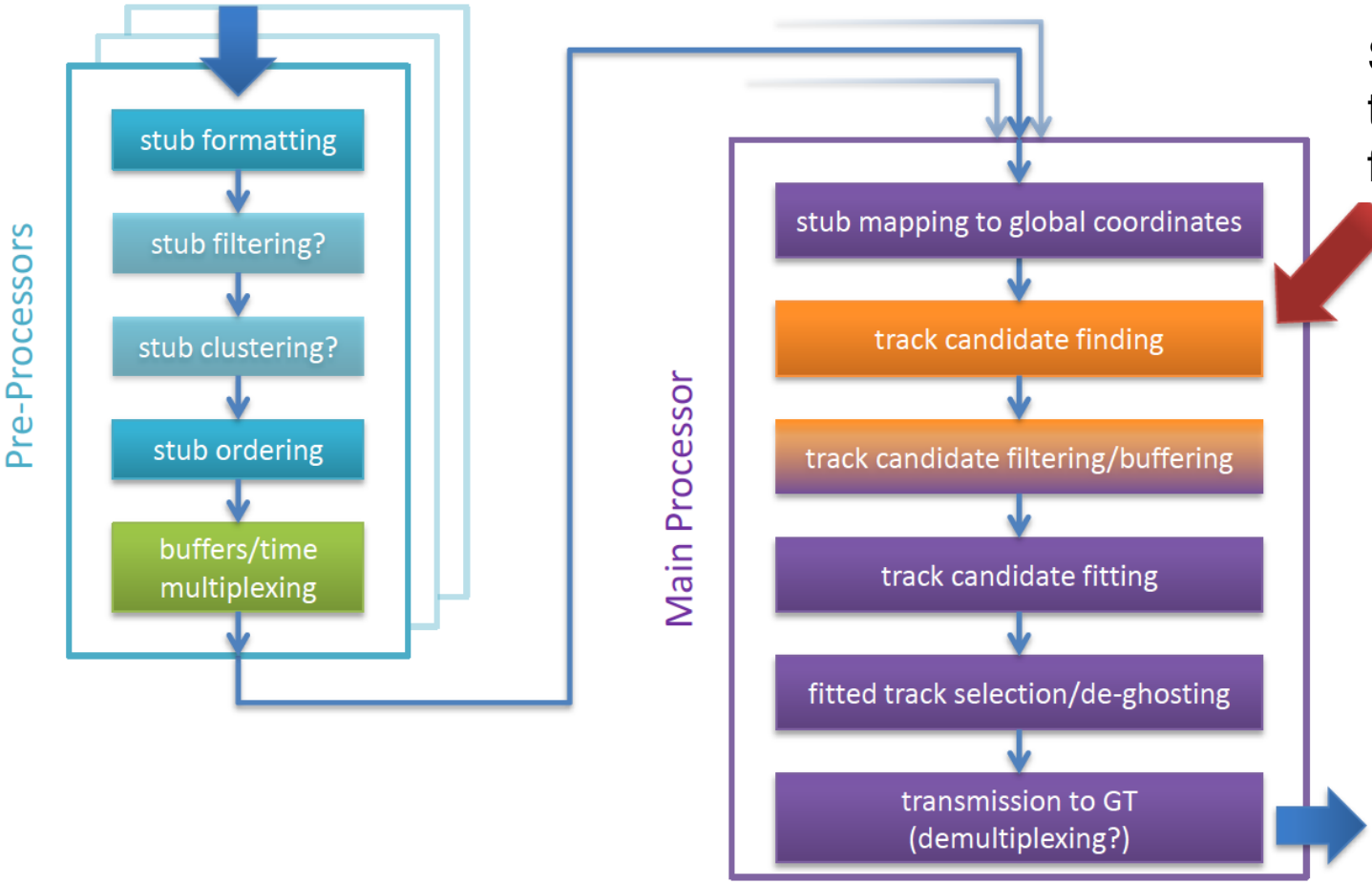


- Maximum # links to the MP (72) limits # PP connected
- Need to divide tracker into 5 trigger regions in η (Δη ~ 1.0)



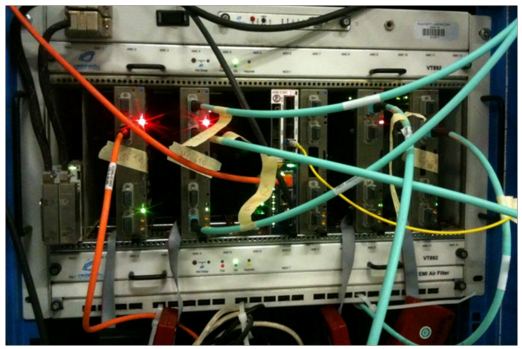
TP definition (σ_z=5cm) for luminous region in z

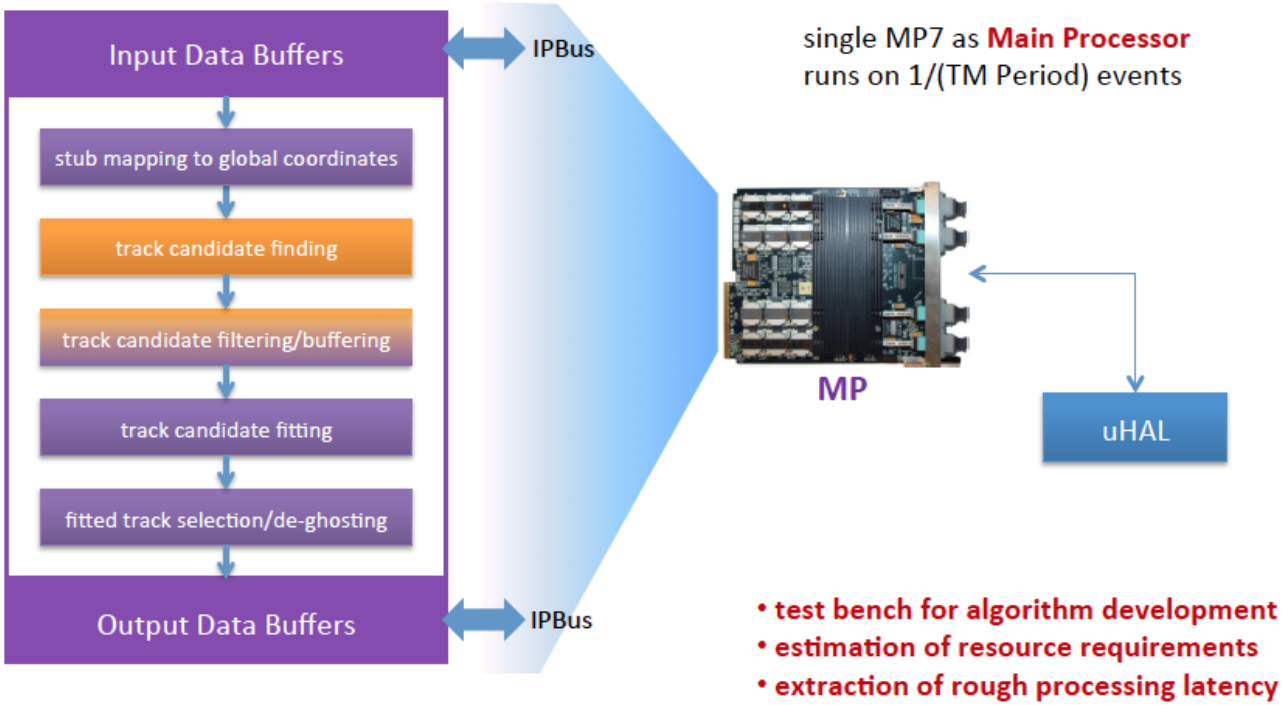
Main steps


Pre-Processors
stub formatting
stub filtering?
stub clustering?
stub ordering
buffers/time multiplexing
Main Processor
stub mapping to global coordinates
track candidate finding
track candidate filtering/buffering
track candidate fitting
fitted track selection/de-ghosting
transmission to GT (demultiplexing?)
Studying Hough transform as track finding algorithm
Fill a histogram in the track parameter space

TMT demonstrator

System available in 904, use MP7 as main processor





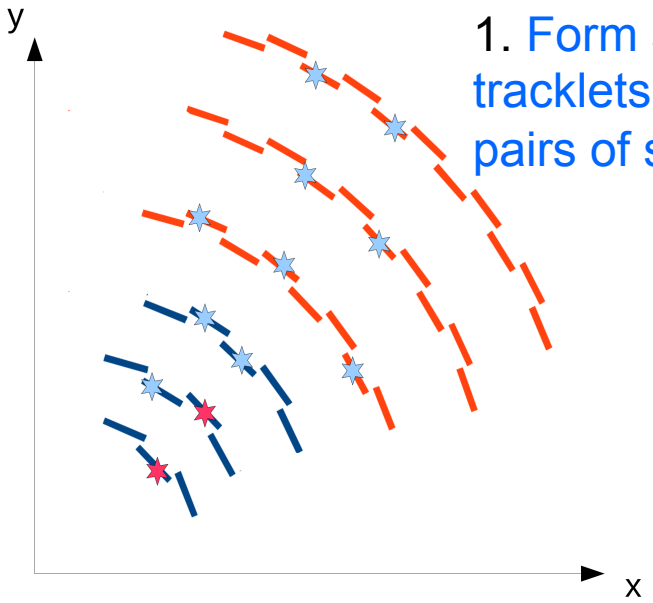
Firmware implementation of Hough Transform array ready

being integrated with infrastructure firmware

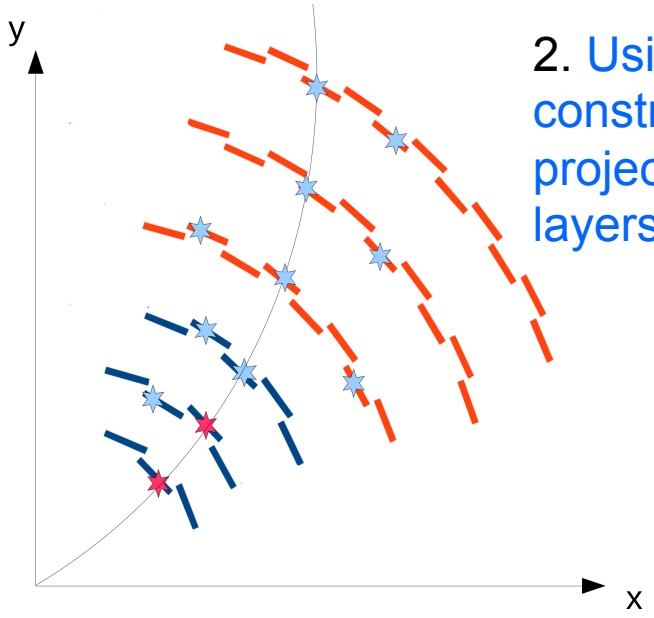
First tests with single board during the summer

Expect first slice tests towards the end of the year

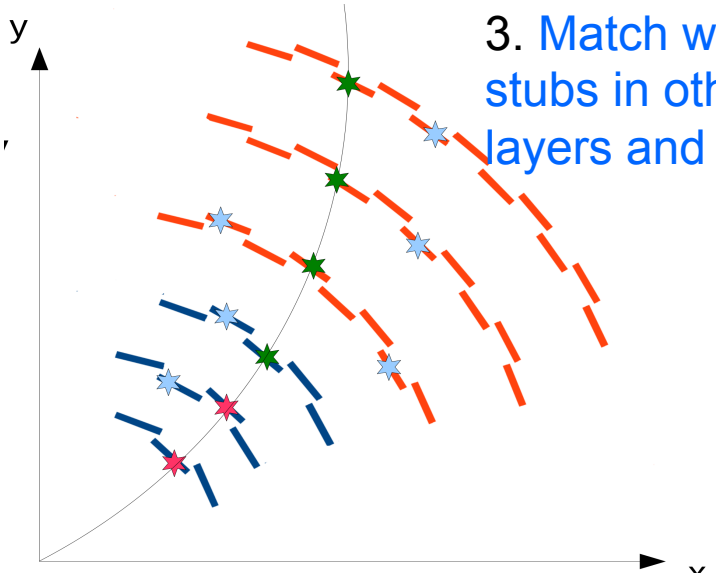
Tracklet Algorithm: Road Search



1. Form seeds, tracklets, from pairs of stubs



2. Using IP constraint project to other layers



3. Match with stubs in other layers and fit

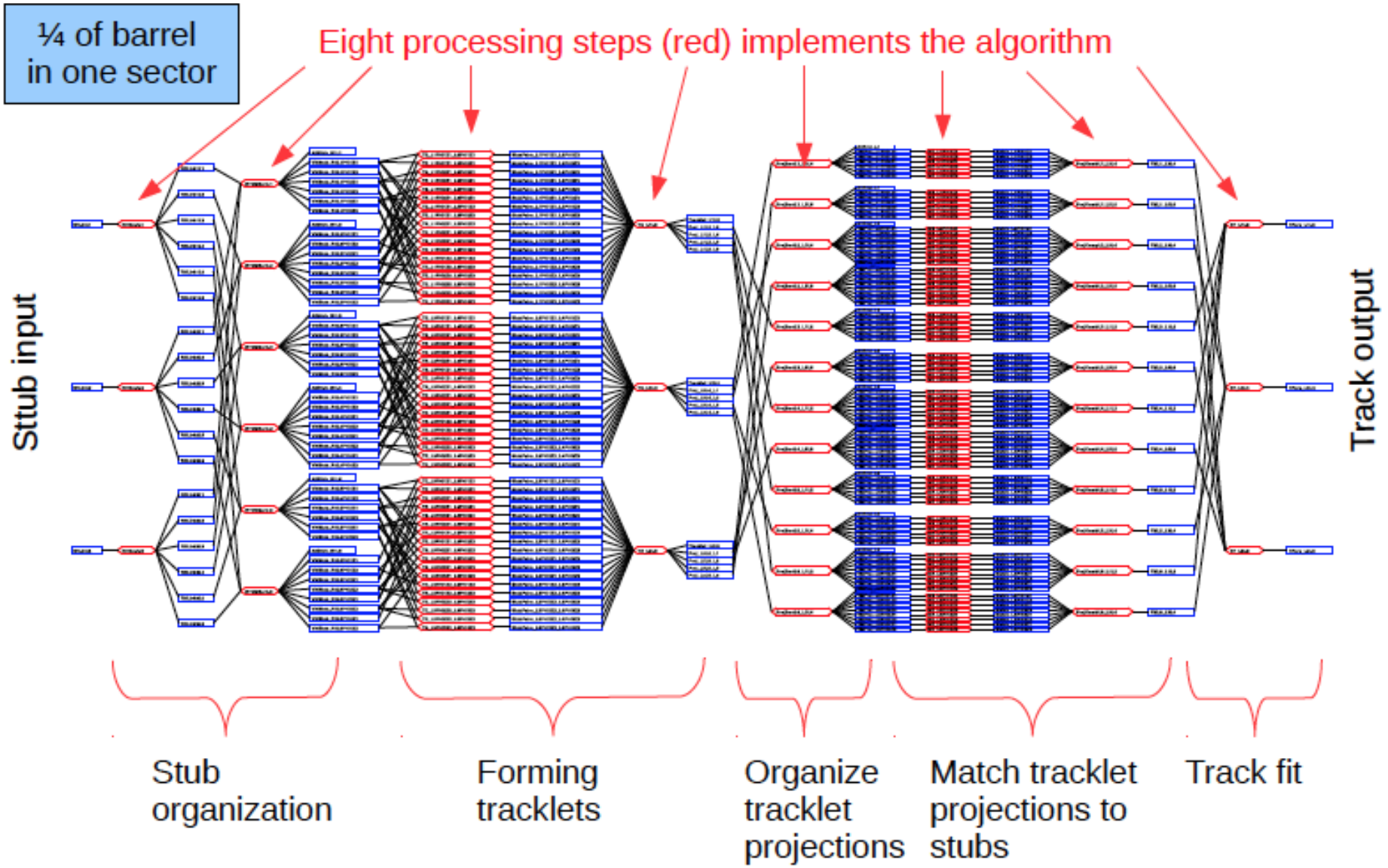
Extensive simulation program:

- High level simulation – used in TP studies
- Low-level (bitwise) C++ emulation of algorithm
- Implementation in Verilog for FPGA

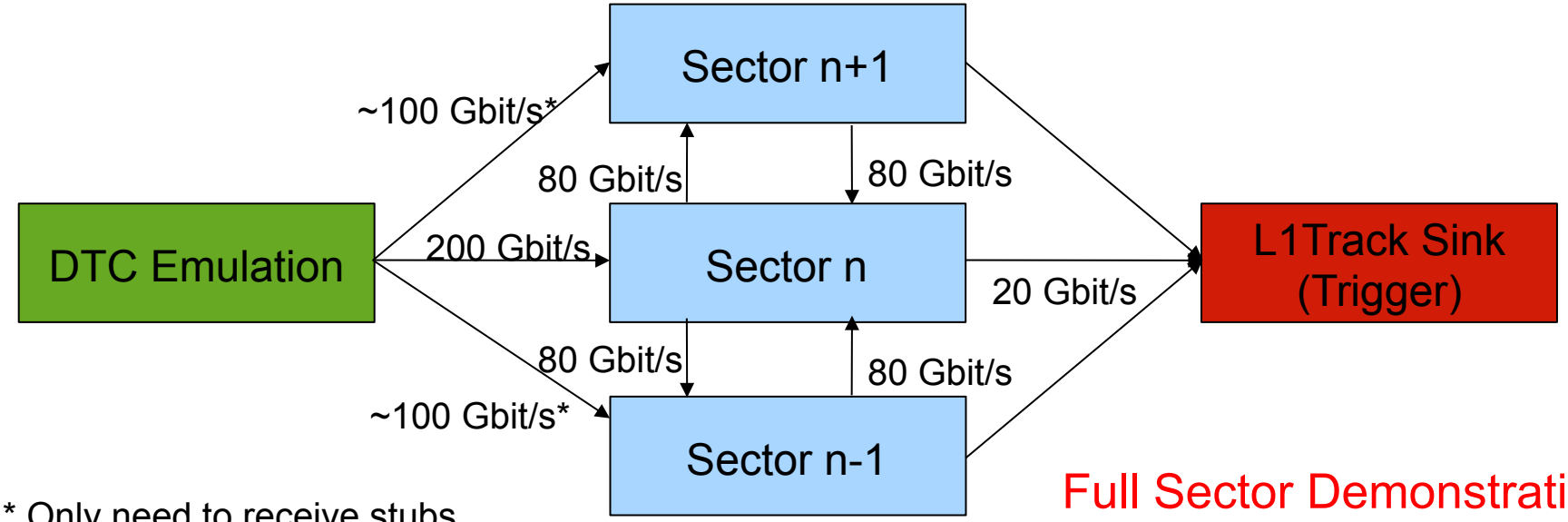
Steps validated against each other

28 phi-sectors
Corresponding to the size of a sector containing a 2 GeV track

FPGA implementation



Tracklet Demonstrator



* Only need to receive stubs needed to demonstrate functionality of the central sector

Board used for DTC emulation and the L1Track receiver can be the same

Sector board
Input: 360 Gbit/s
Output: 180 Gbit/s

Full Sector Demonstration:

- Covers $|\eta|<2.4$
- Uses factor 4 time MUX
- $p_T>2$ GeV

Demonstrator based on CTP7 board developed for phase-1

Demonstrate full tracking in a sector, including communication with neighbour sectors
Measure latency from DTC output to L1 tracks available

L1 tracking

Three methods

Associative Memories + track fitting
Time-Multiplexed architecture – Hough Transform + track fitting
Tracklet-seeded road search

Hardware demonstrators under development – goals:

Provide evidence that L1 tracking is feasible
Support statement that L1 tracking will fit in 5 μsec

Timeline

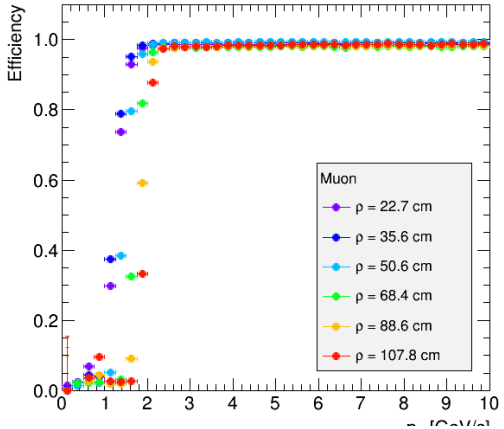
First exercises within this year
Full sector demonstrator before the end of next year (in time for TDR)

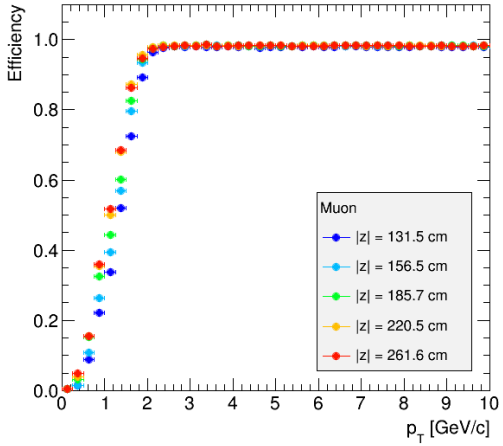
Review of demonstrators will (hopefully) provide insight on best way forward

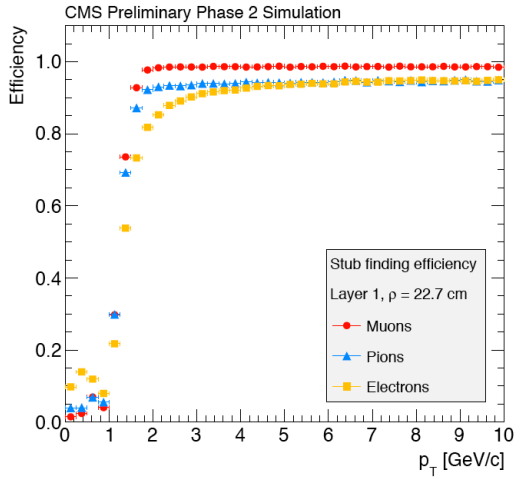
Some performance plots

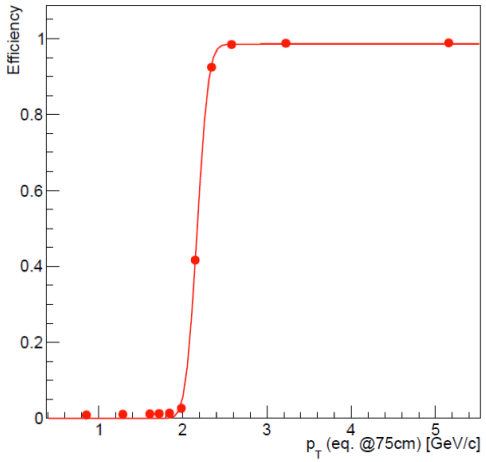
Stub finding performance

- Muon stub finding efficiency in all layers (barrel, endcap)
- Barrel layer 1 for muons, pion electrons
  - Effect of interactions
- Efficiency measured on DESY beam with 2-CBC2 module prototype









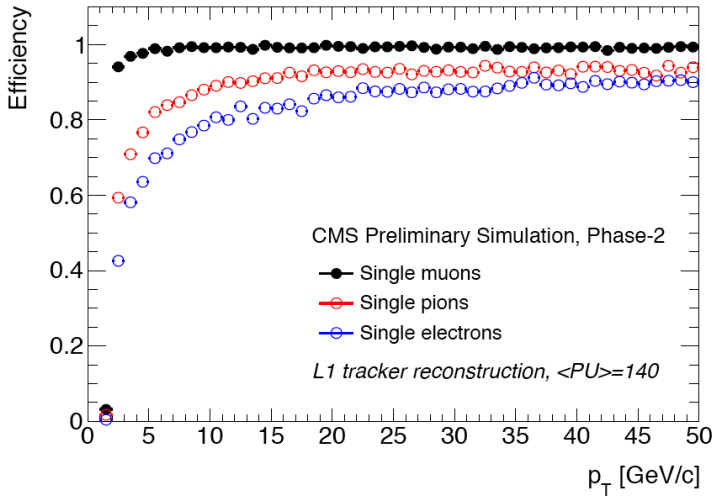
p_T simulated with module tilt

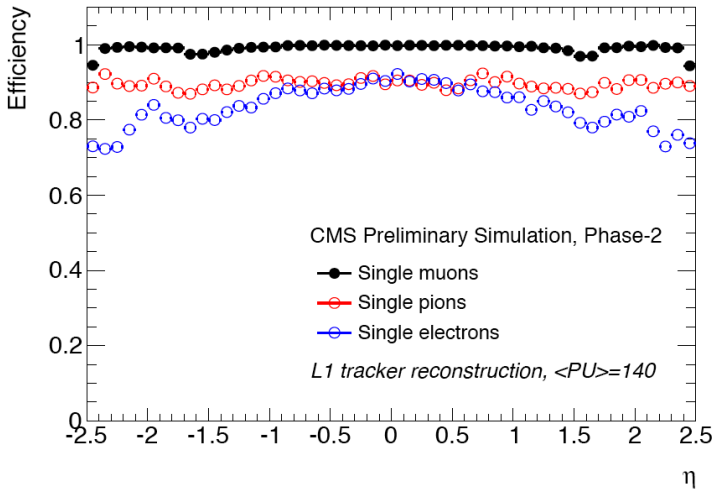
Selected threshold equivalent to a nominal p_T cut of 2.14 GeV @ 75 cm

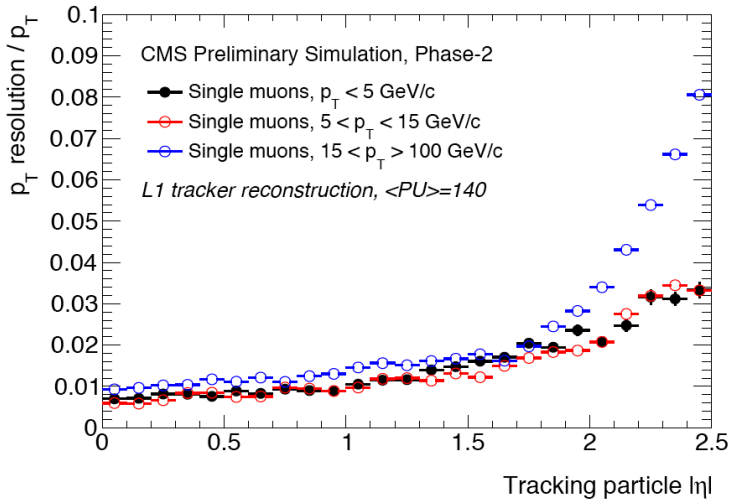
Fit to data gives effective threshold of 2.2 ± 0.1 GeV

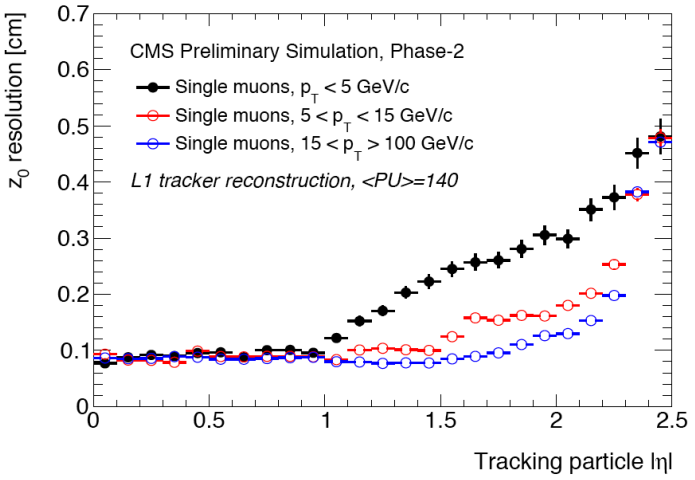
Level-1 track finding

- Track finding performance taken from “tracklet” method
  - N.B. Track finding not demonstrated in hardware
    - Indication of the performance that should be achievable



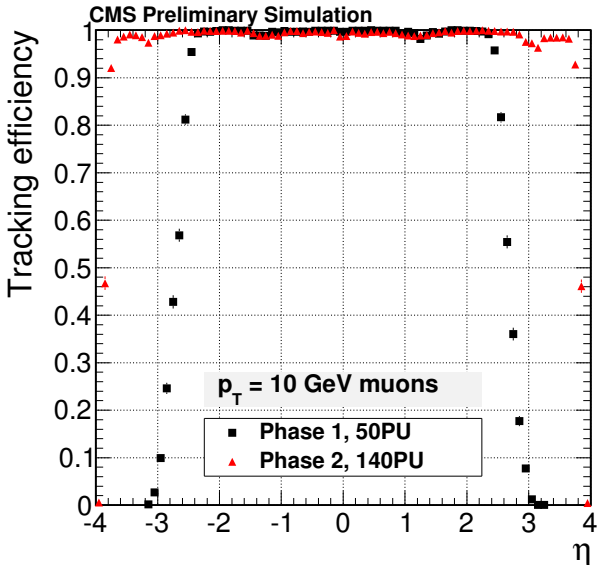


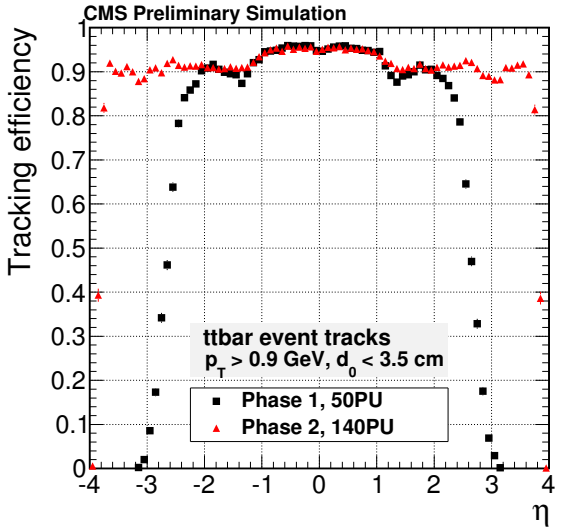


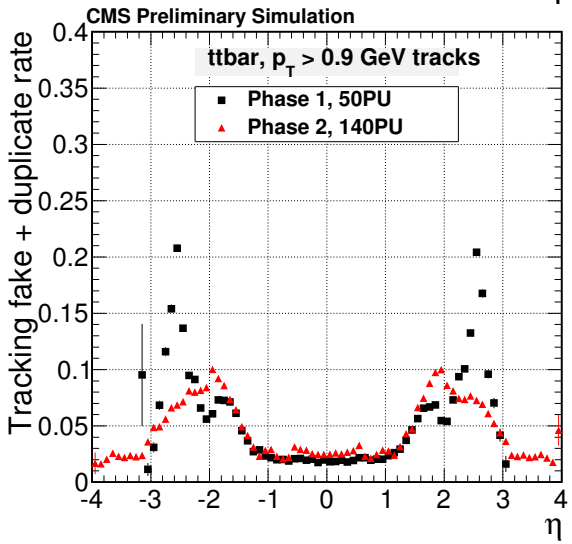


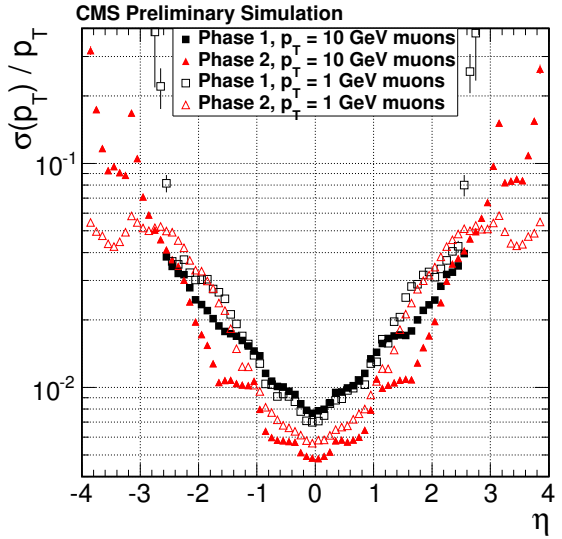
Offline tracking

- Compare Phase-1 @ 50 PU with Phase-2 @ 140 PU









The Outer Tracker in numbers

OLD

- N of modules 15,148
- Total active surface 210 m^2
- Total n of strips 9.3 M
- Power in the tracking volume ~ 30 kW

NEW

- N of modules 15,508
  - 7084 PS modules (-1200 if tilted)
  - 8424 2S modules
- Total active surface 218 m^2
  - 155 m^2 strips (2S)
  - 31 m^2 strips (PS)
  - 31 m^2 macro-pixels (PS)
- Total n of strips 47.8 M
- Total n of pixels 218 M
- Power in the tracking volume ~ 80 kW

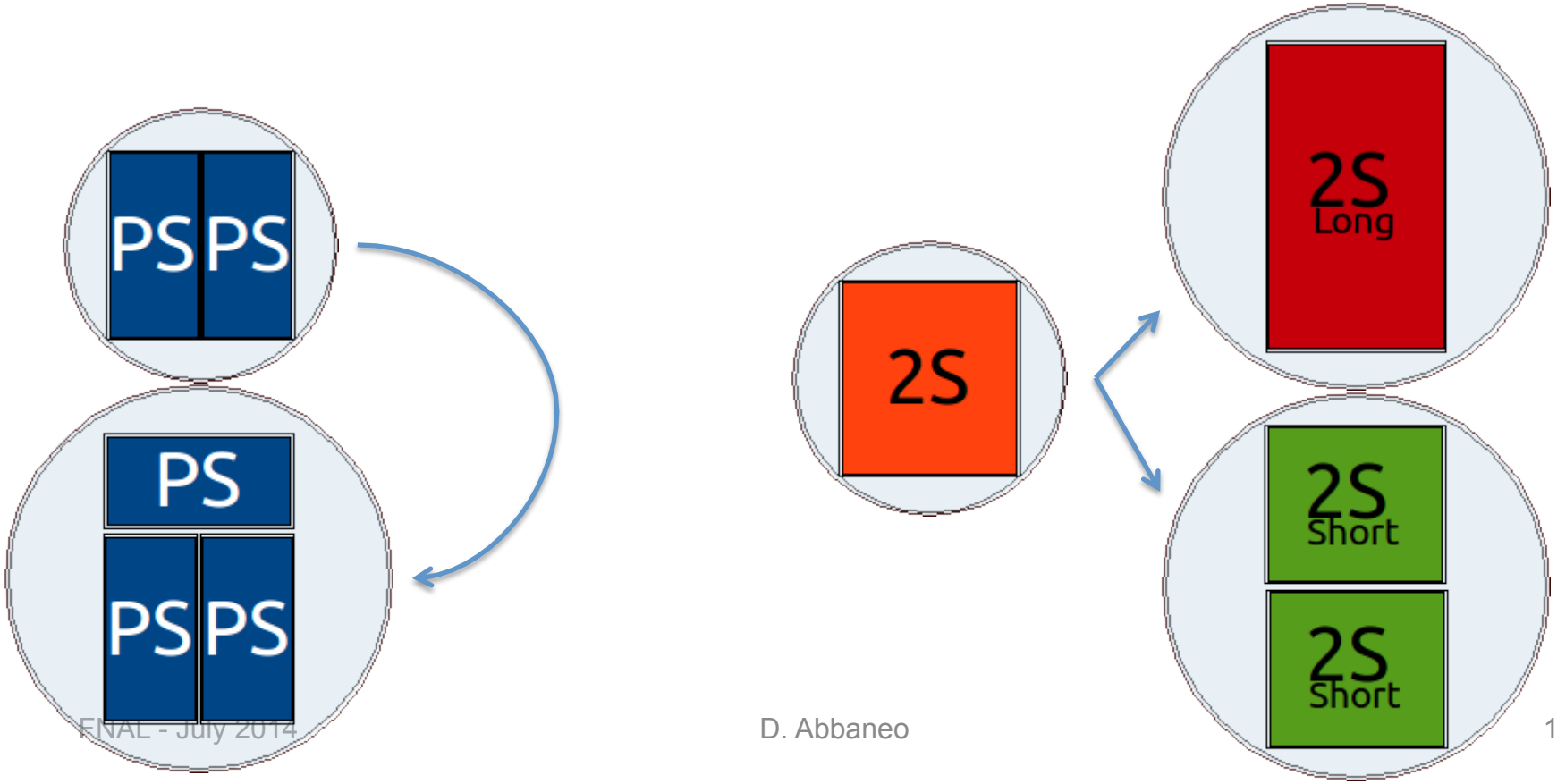
Estimated CORE cost in MCHF			
	Outer Tracker		Inner Pixel
Modules	2S	27.9	11.8
	PS	22.8	
Mechanics		6.6	3.6
BE electronics		12.4	2.0
Power system		6.1	1.4
Services, cables and pipes		5.5	1.1
Cooling system		4.2	0.6
Infrastructure and installation		3.5	2.7
TOTAL		**89**	**23**

	Outer Tracker	Inner Pixel
Austria	X	
Belgium	X	
CERN	X	X
Finland		X
France	X	
Germany	X	X
Greece	X	
India	X	
Italy	X	X
Pakistan	X	
Spain		X
Switzerland		X
UK	X	
US	X	X

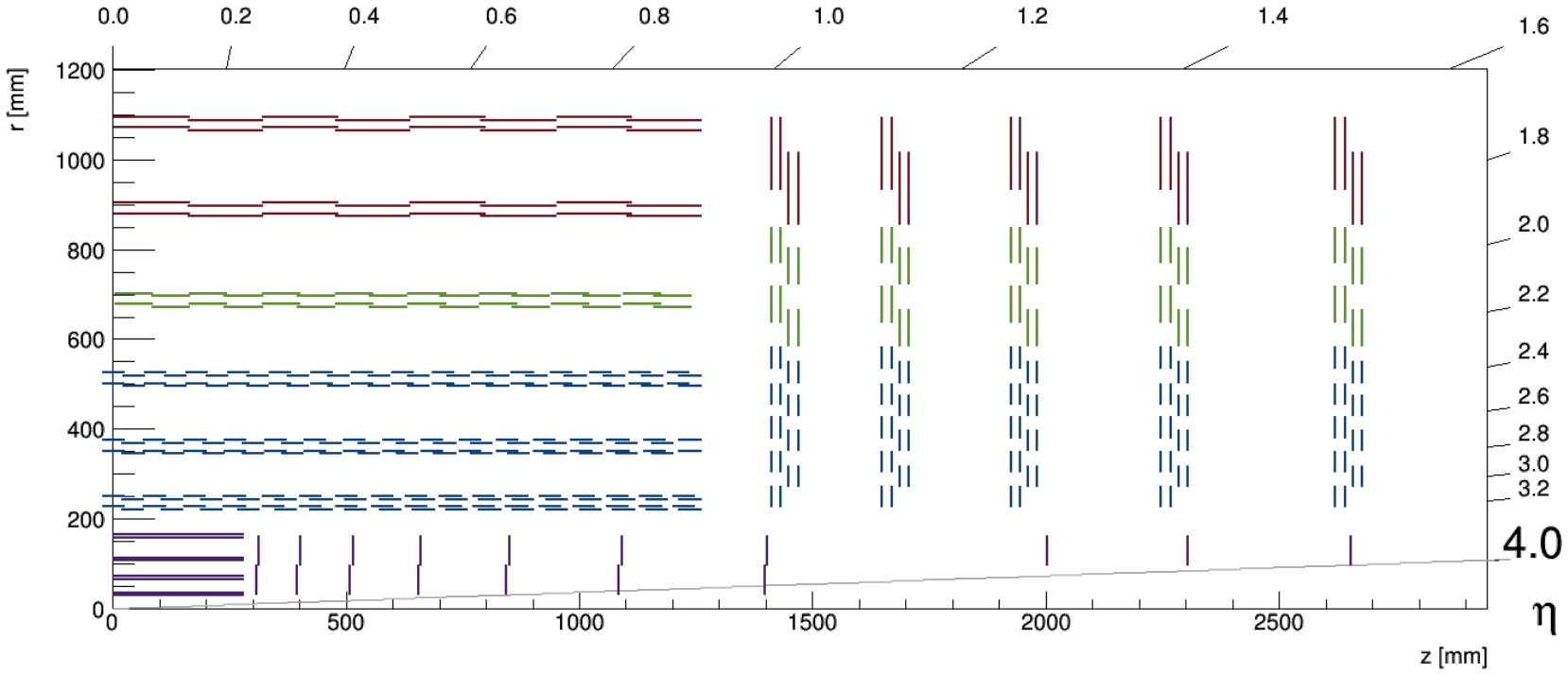
BACKUP

A variant: sensors from 8”

- PS module: keep the same design, produce 3 sensors from 1 wafer
  - Sensors surface could be slightly enlarged if decision taken soon enough (960 → 1024 channels)
    - Possibly small reduction in N of modules
- 2S module: modify module design by changing strip length
  - **2S_long:** stretch to wafer edges. Sensor 10 cm → 16 cm (strips 5 cm → 8 cm).
  - **2S_short**: shorten to fit two sensors in one wafer. Sensor 10 cm → 8 cm (strips 5 cm → 4 cm).



Layout for 8” production



- 2S_long used in the outer region
- 2S_short used in the intermediate region
  - E.g. Outer barrel half-length goes from 12 modules to 16 modules (2S_short) or 8 modules (2S_long)
- Further optimization possible!

Summary: 6” vs 8”

- Layout with flat TBPS
  - 27400 6” wafers or 18450 8” wafers
    - Ratio 1.485
- Layout with tilted TBPS
  - 25950 6” wafers or 17400 8” wafers
    - Ratio 1.491
- The potential interest for the TK is mostly financial
  - The designs are basically equivalent
- Bottom line: 8” is interesting if $(8”) << 1.5 × $(6”)
  - Taking into account yield of all steps, up to module assembly