

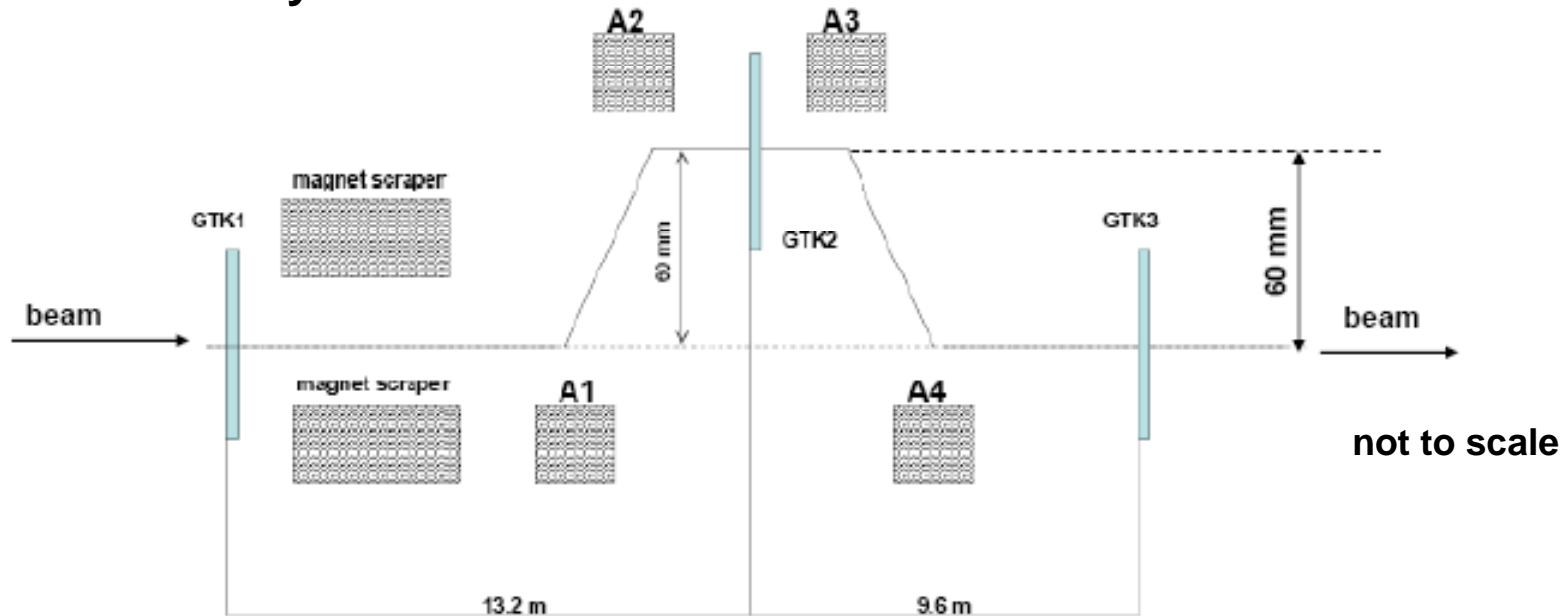
# GigaTracker: status report

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- **Introduction : detector generalities and specifications**
- **Progress report about:**
  1. Final and prototype sensors
  2. Bump bonding
  3. Cooling
  4. Chip prototype design
  5. DAQ for chip prototype

## Introduction : detector generalities and specifications (1)

### Detector layout



- Three same Si-pixel stations: each station  $(60 \times 27) \text{mm}^2$
- pixel dimensions:  $(300 \times 300) \mu\text{m}^2$ ; thickness:  $200 \mu\text{m}$

To measure the following quantities of the beam particles:

- direction ( $\sigma_{\text{RMS}} \sim 14 \mu\text{rad}$ )
- momentum ( $\sigma_{\text{RMS}} \sim 0.15 \text{ GeV}/c$ )
- track time ( $\sigma_{\text{RMS}} \sim 200 \text{ ps}/\text{station} \rightarrow \sim 150 \text{ ps}/\text{track}$ )

## Introduction : detector generalities and specifications (2)

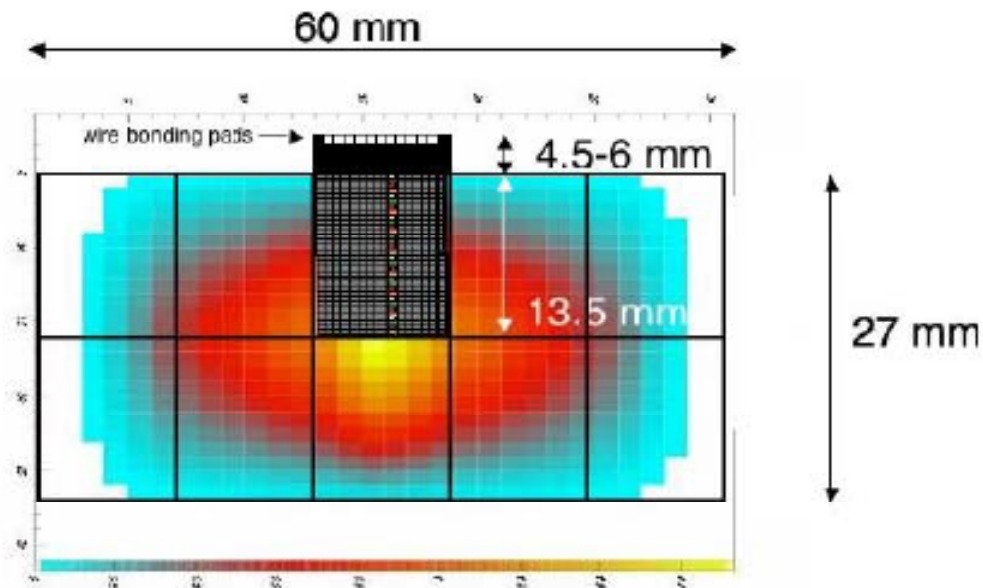
Mounted inside the vacuum tube

Dimensions of the stations to match the beam shape

Sensor technology: p-in-n

18000 pixels/ station -> 54000 pixels grand total

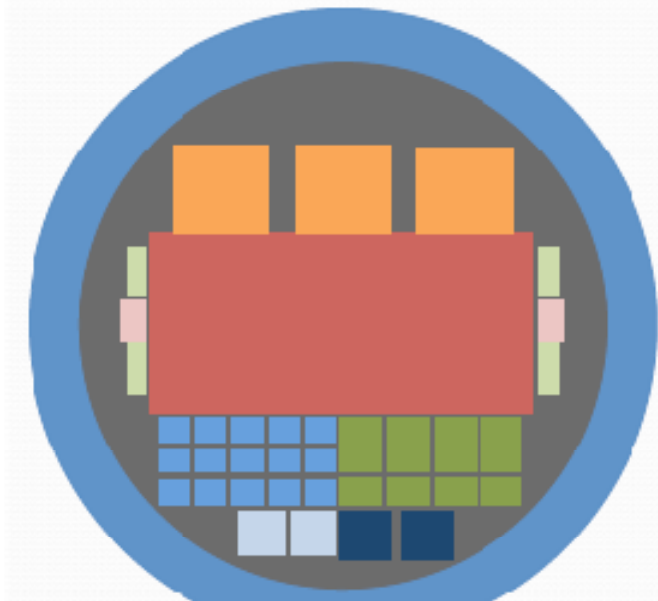
Sensor read-out via 10 chips



# Progress report: final and prototype sensors

- a batch of 20 wafers (-> 20 sensors) has been ordered to FBK-Trento,Italy
- wafer layout is ready
- bump details (dimensions and position) defined
- wafer to be processed before the end of the year

## Wafer layout



### Legend for sensors:

- ◆ 1 full size  $27.0 \times 60.0 \text{ mm}^2$  [ $29.0 \times 62.0 \text{ mm}^2$ ]
- ◆ 3 chip-size  $12.0 \times 13.5 \text{ mm}^2$  [ $14.0 \times 15.5 \text{ mm}^2$ ]
- ◆ 12 TO-demo  $2.1 \times 4.5 \text{ mm}^2$  [ $4.1 \times 6.5 \text{ mm}^2$ ]
- ◆ 15 CERN-demo  $1.8 \times 2.7 \text{ mm}^2$  [ $3.8 \times 4.7 \text{ mm}^2$ ]
- ◆ 2 CMS diodes  $7.0 \times 7.0 \text{ mm}^2$
- ◆ 2 RADMON diodes  $8.0 \times 8.0 \text{ mm}^2$
- ◆ 4 no-bump-bonding test structures  $0.9 \times 6.0 \text{ mm}^2$  [ $2.9 \times 8.0 \text{ mm}^2$ ]
- ◆ 2 VTT alignment structures  $4.0 \times 7.0 \text{ mm}^2$

## Progress report: bump-bonding

- Development of the processes with VTT (Finland)
  1. **Bump-bonding of the final chip to the sensor:** standard technique
  2. **Bump-bonding of the prototype:** how to bond a diced chip to a sensor ?

This is a technical problem related to the lack of room on diced chips for galvanic contacts for electroplating and thus it is impossible to apply the standard bump-bonding technique.

**Two solutions are however available:**

1) *Reverse rework*: most promising and preferred solution

2) *Au stud bumps* practical only for ~100 pixels: technique off-shelves (backup solution)

# Progress report: cooling

Power to be dissipated:  $2\text{W}/\text{cm}^2 \rightarrow 32\text{ W}$

Target chip temperature  $< 5\text{ }^\circ\text{C}$

Base solution: two half-cylinders of carbon fiber enclosing the sensor+chip

## CONFIGURATION 2 – COOLING ANALYSIS

COOLING FLUID : NITROGEN		K	°C
Delivery temperature	$T_i$	100	-173
Wall temperature	$T_w$	275,6	2,6
dT	$T = (T_w - T_i)$	175,6	175,6
$T_m$	$T_m = (T_w + T_i)/2$	187,8	-85,2

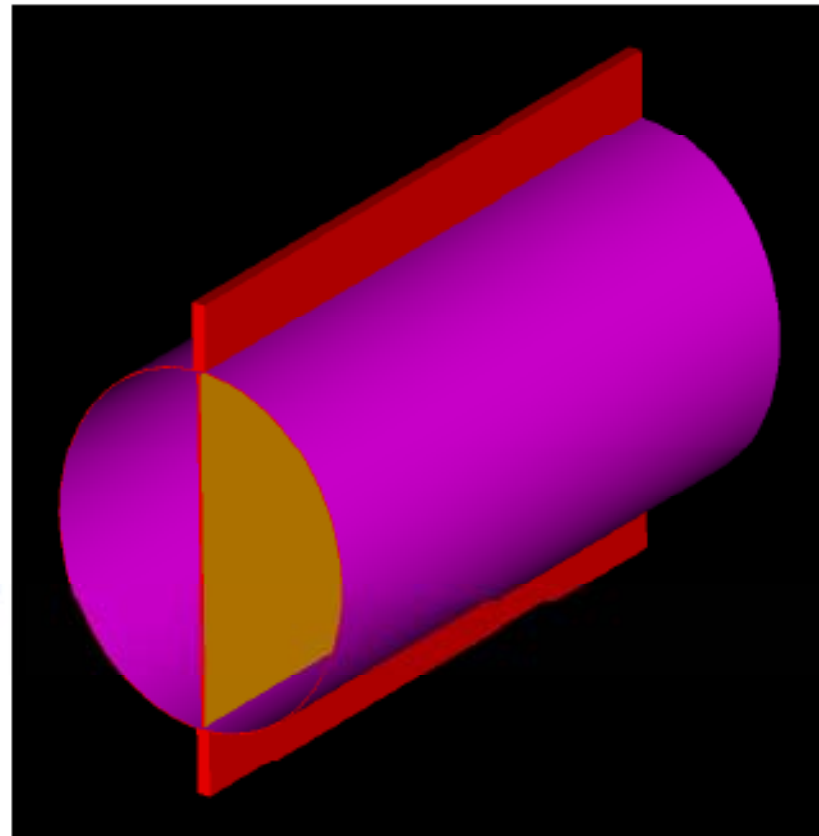
NITROGEN PROPERTIES @ $T_m$ and atmospheric pressure		
Specific weight ( $\text{Kg}/\text{m}^3$ )	$\rho$	1,79
Specific heat ( $\text{J}/\text{KgK}$ )	$C_p$	1041
Thermal conductivity ( $\text{W}/\text{mK}$ )	$\lambda$	0,024
Kinematic viscosity ( $\text{m}^2/\text{s}$ )	$\nu$	1,34E-05

GENERATED POWER (W)

$$Q = q \times A = (2\text{E}+04) \times (27\text{E}-03 \times 60\text{E}-03) = 32,4$$

COOLING SURFACE ( $\text{m}^2$ )

$$S = 2 \times (27\text{E}-03 \times 60\text{E}-03) + 0,35\text{E}-03 \times 2 \times (27\text{E}-03 + 60\text{E}-03) = 3,34\text{E}-03$$



# Progress report: chip prototype

## Introduction:

- The challenging specification of the project is the hit time resolution we are aiming at:  $\sim 200$  ps (rms) per station
- The sensor, bump-bonding technique, and the DAQ are well within reach with the actual status-of-the-art in this field.
- Also the mechanics and the cooling system, though complex, do not necessitate outstanding effort.
- To summarize: the design of the front-end to beat the jitter and the time walk (which are the main sources of errors) and to get to the specified time resolution is the crucial point.

# Front-end: introduction

We are following two design options to cure the time walk:

1. Constant Fraction Discriminator, which recovers hardware-wise the time walk of the signal due to the energy deposit fluctuations
2. Determination of the Time-over-Threshold of the signal and offline correction of the time walk.



Concerning the architecture two configurations are under study:

- a) All the electronics dedicated to a pixel (preampli-CFD-TDC ) is on the pixel itself. The technology that has been chosen (130 nm) allows to comfortably fit all the components into the (300x300)  $\mu\text{m}$  pixel area.
- b) Preampli and Time-over-Threshold discriminator is on every pixel and TDC is at the end-of-column and serves 5 pixels.

For each option, in 2007, a prototype has been developed and tested on the bench.

Results have been shown in previous meetings and reports and they resulted to be promising:

$$\sigma < 100 \text{ ps (rms)}$$

# More information about the front-end design status

Option a): on-pixel-TDC option: preampli->CFD->TDC within the pixel area (Torino)

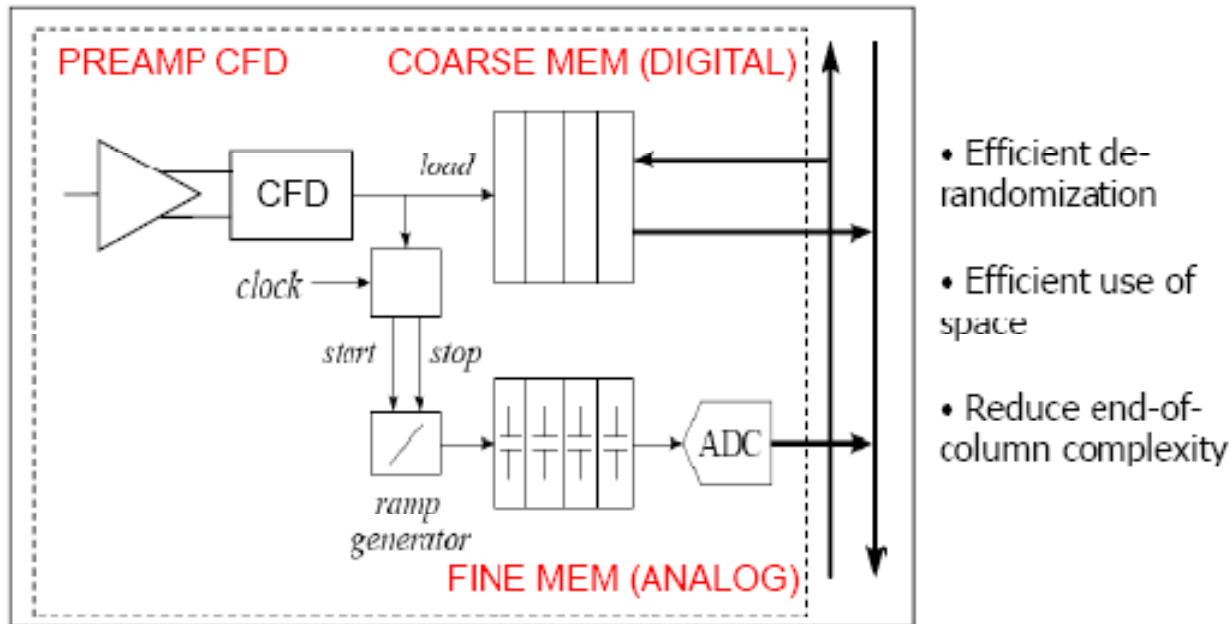
Option b): end-of-column TDC: preampli → ToT discriminator → TDC serving 5 pixels placed at the end-of-column.(CERN)

Remark: nothing would prevent to mix the two options, for example CFD with the end-of-column TDC.

- To insist on more than two options seemed not easy to be sustained.
- This possibility, mix of the two options, will be exploited only if the tests will show it is necessary.

## Some more info about the On-pixel-TDC option

### CFD-FE Overview



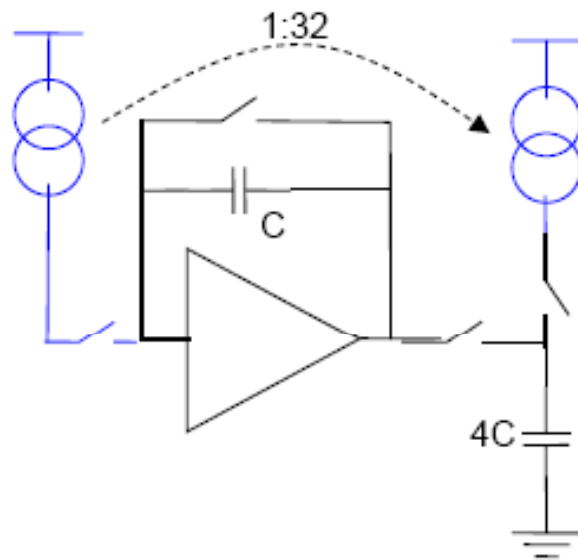
Sorin Martoiu, GTK Meeting, CERN

2

## Some more info about the On-pixel-TDC option (cont'd)

### Wilkinson TDC variant

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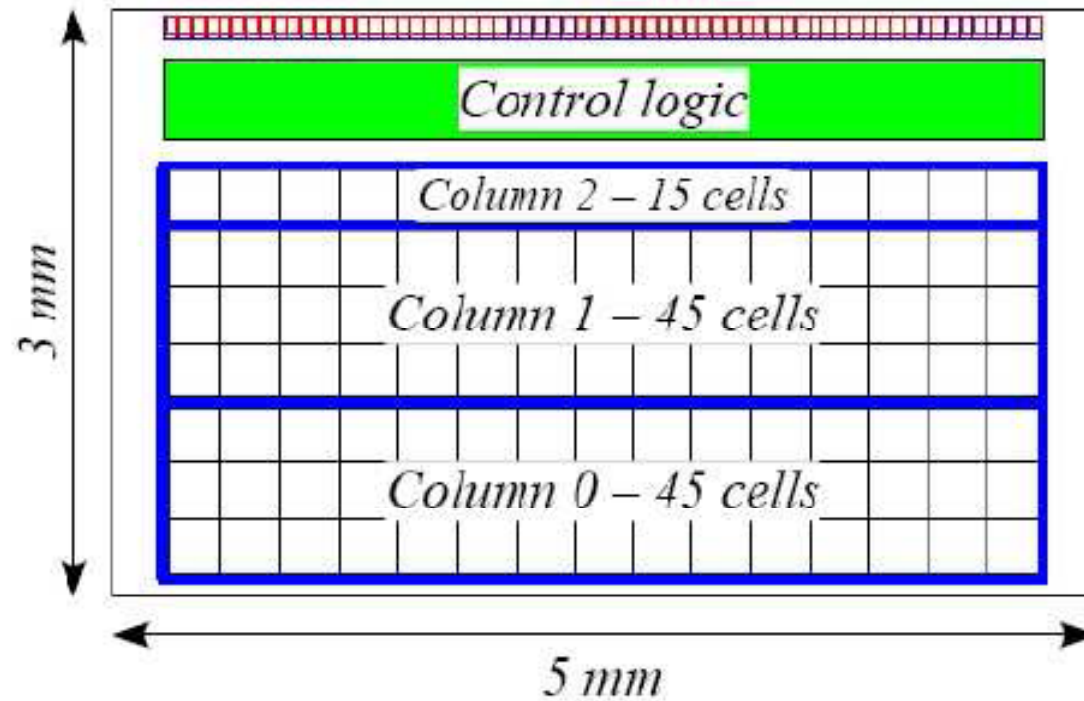
- Lower current ratio
- Use same source polarity
- Rely also on cap matching
  
- < 4 LSB range mismatch
- 2-3 bit calibration DAC
- VNCAP (LM option)
  - parasitic cap – systematic offset
- MIM (DM option) –
  - no systematic offset;
  - better matching;
  - lower area

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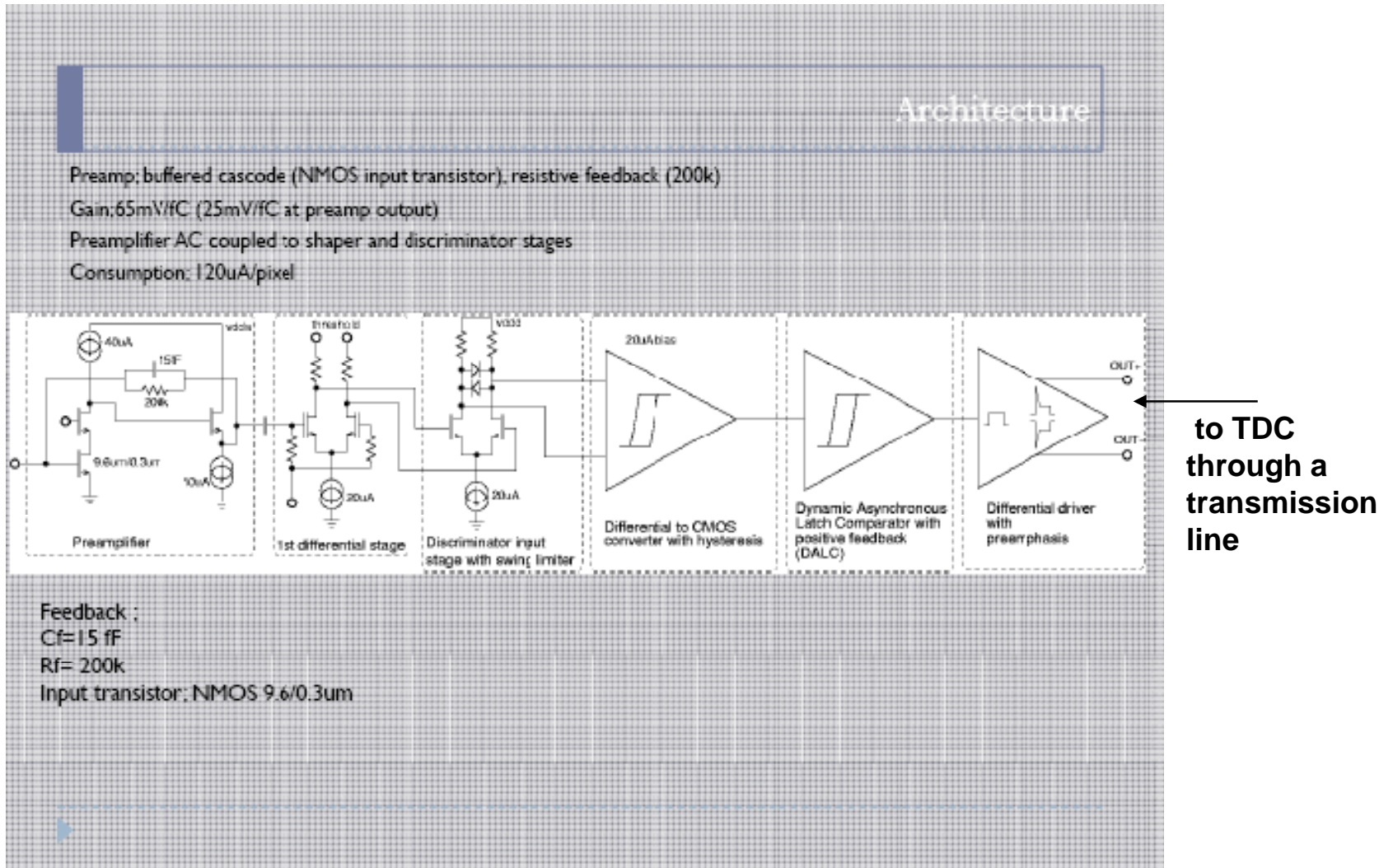
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- The baseline design of the full chain is frozen
- Layout is underway

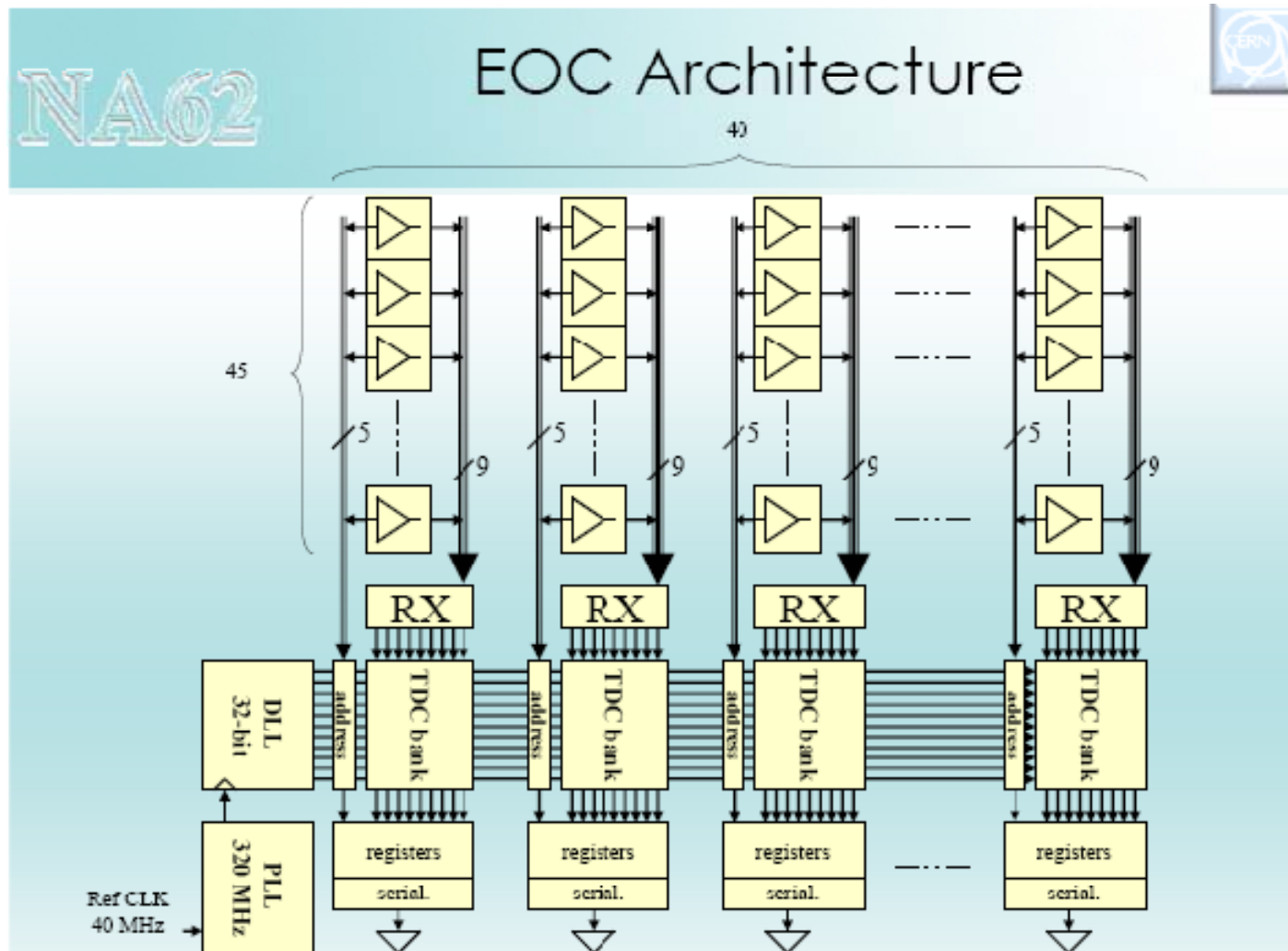
## On-pixel-TDC architecture: chip layout



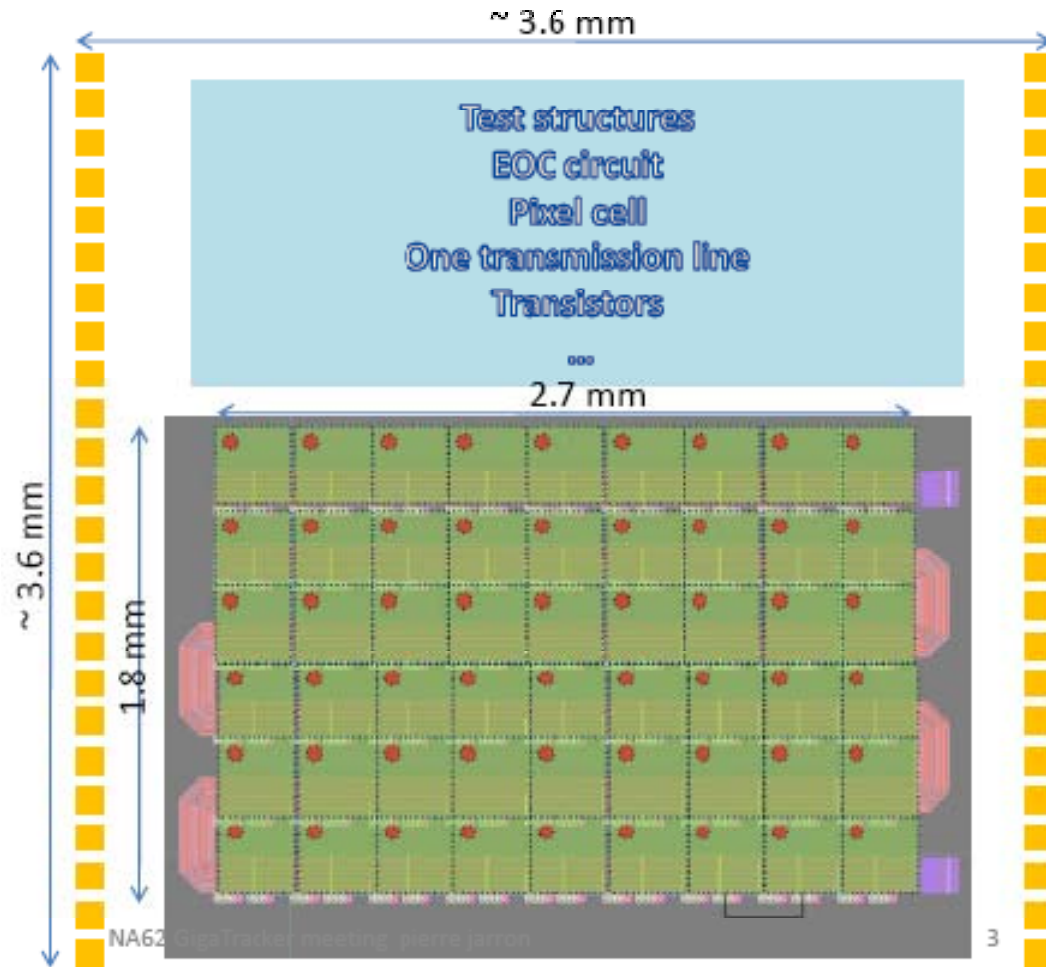
## Some more info about the End-of-column-TDC option



## Some more info about the End-of-column-TDC option (cont'd)



# EOC architecture: chip layout





# Status of the chip prototypes

- **Two options:**
  - **on-pixel-TDC**
  - **End-of-Column TDC (EOC)**

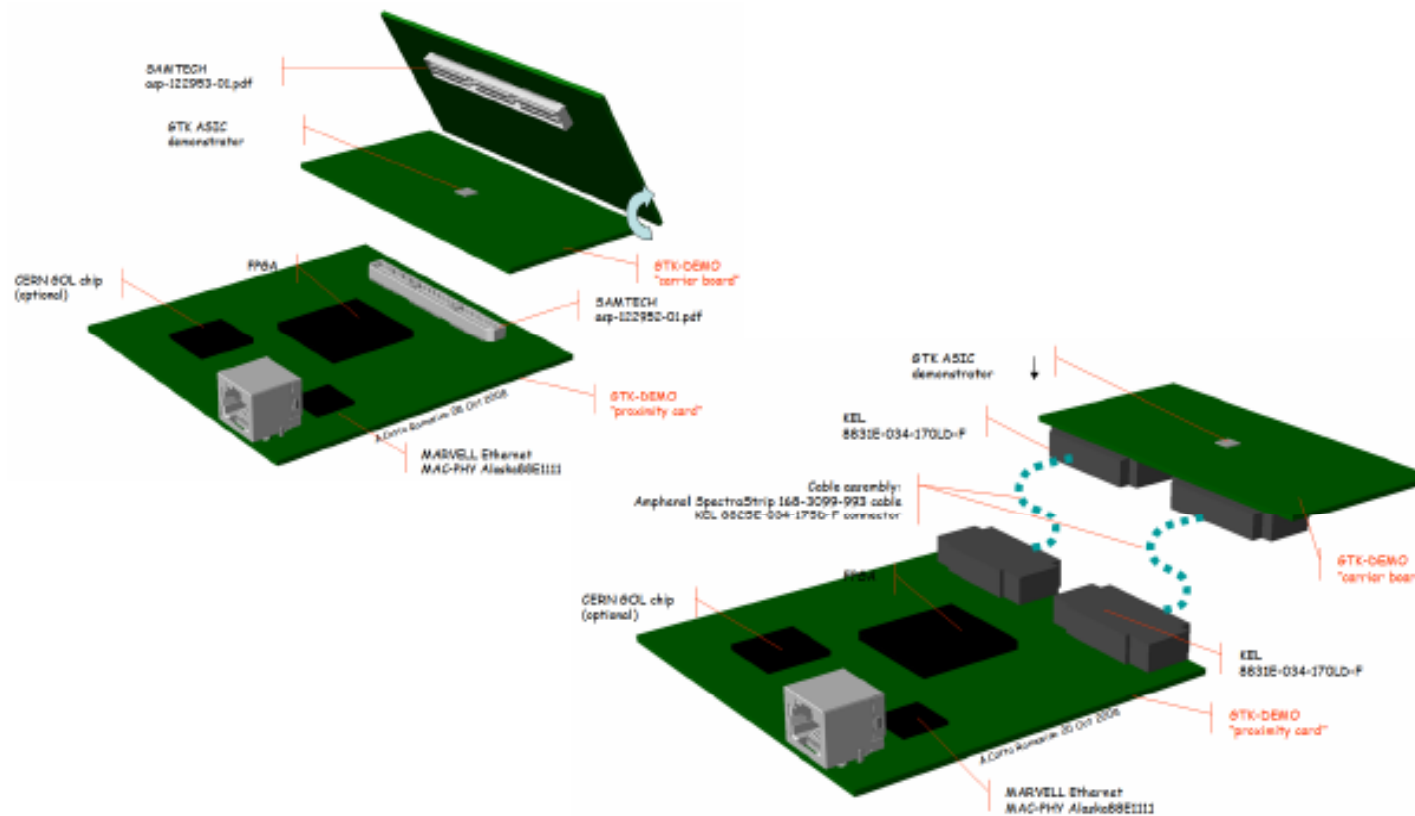
**Design review on Oct. 7-8th with several CERN-LAL designers**

- **all the building blocks are ready**
- **no flaws have been spotted**
- **some further checks to be performed**
- **layout underway for both options**
- **submission moved to Jan. 20th 2009, delivery expected by middle of March 2009.**

## Tests on prototypes in Spring-Summer 2009

- before bump-bonding: electrical test and measurements of the jitter+time-walk with charge injection method
  
- after bump-bonding: test with source/laser and beam.

# Progress report: DAQ for chip prototype



Testing of the GTK demonstrators