NA62 TDAQ progress report

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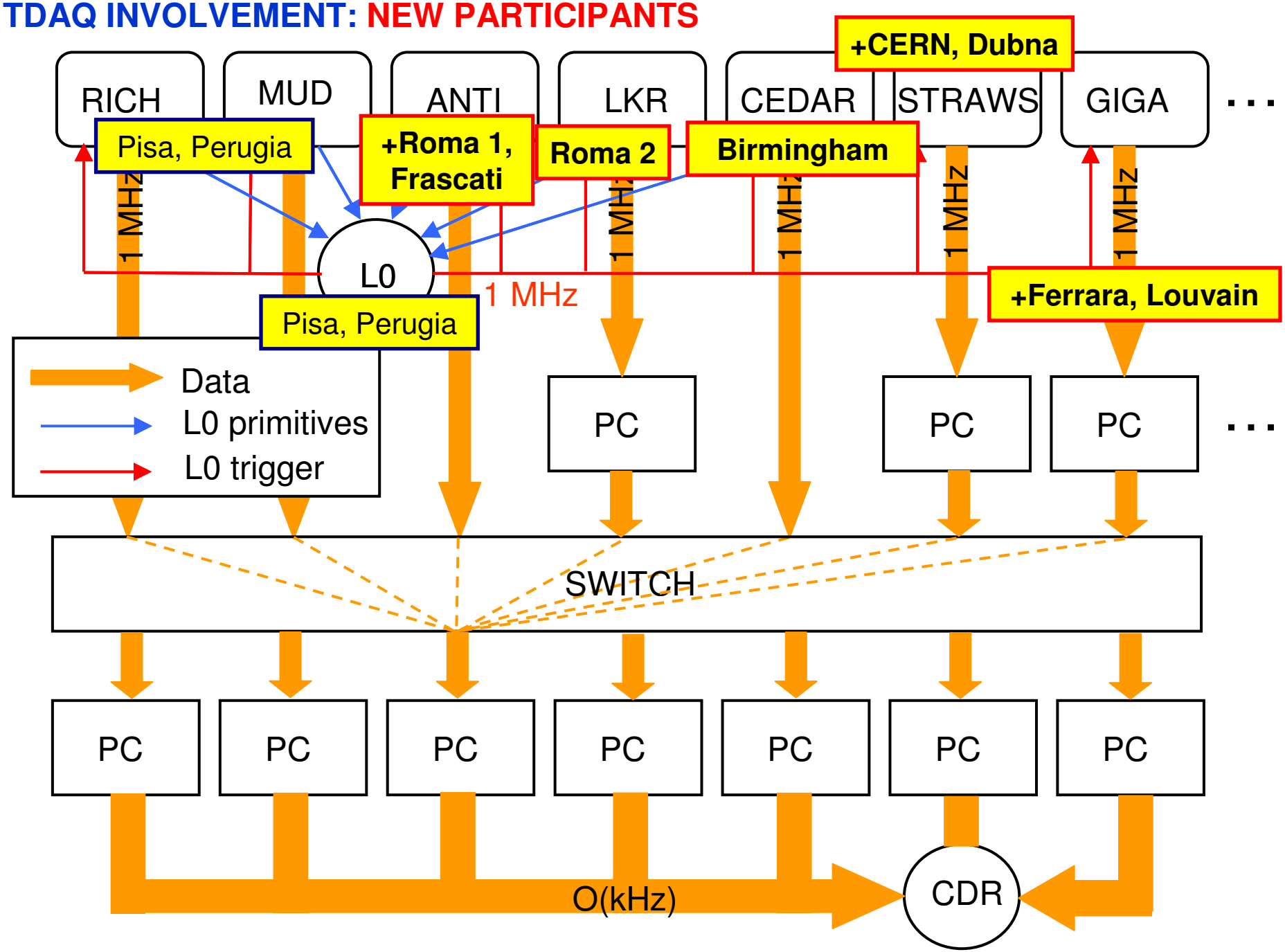
for the TDAQ Working Group

4.11.2008 - CERN

TDAQ INVOLVEMENT: NEW PARTICIPANTS

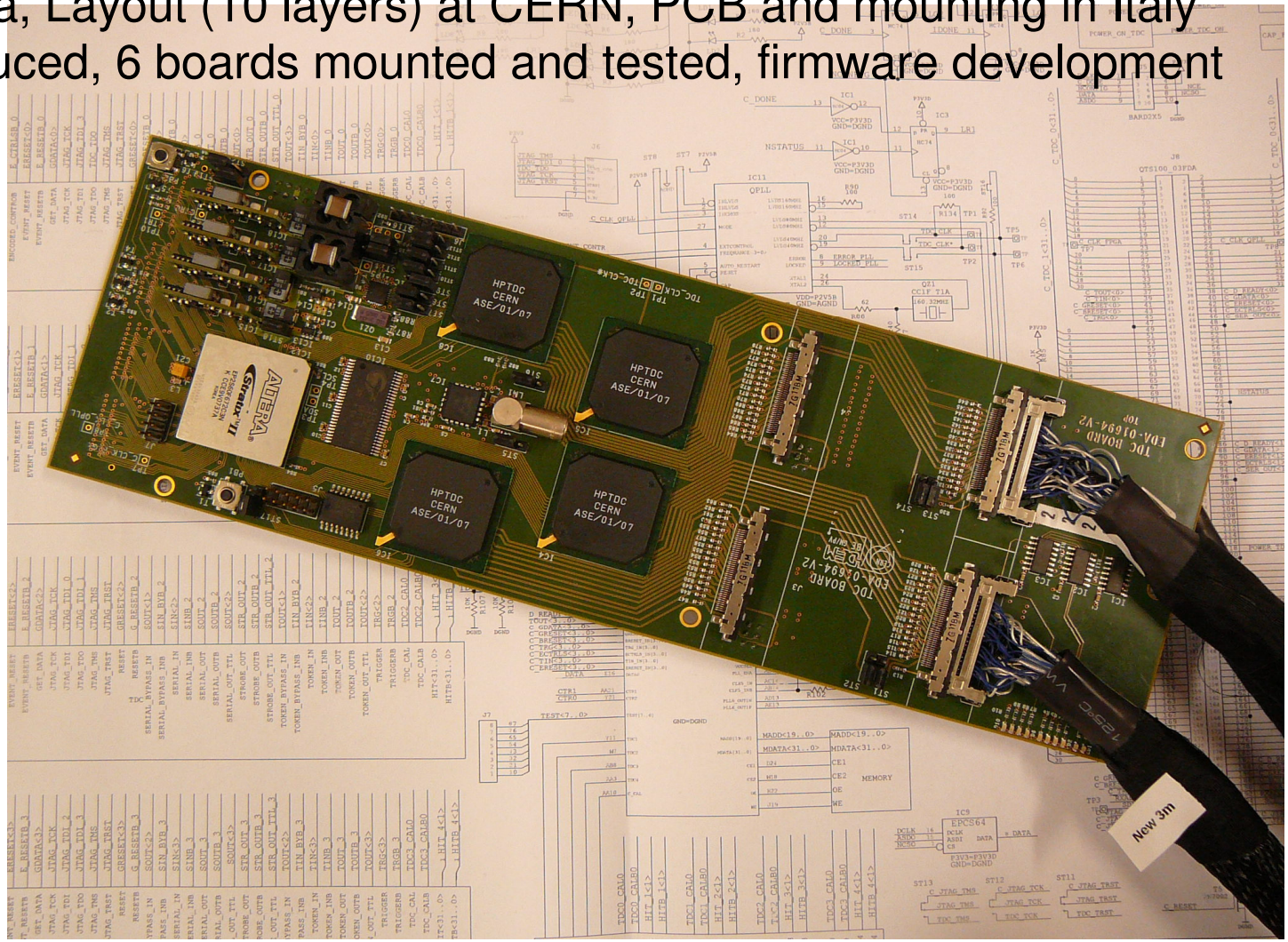


TDC Board V2 (Pisa)

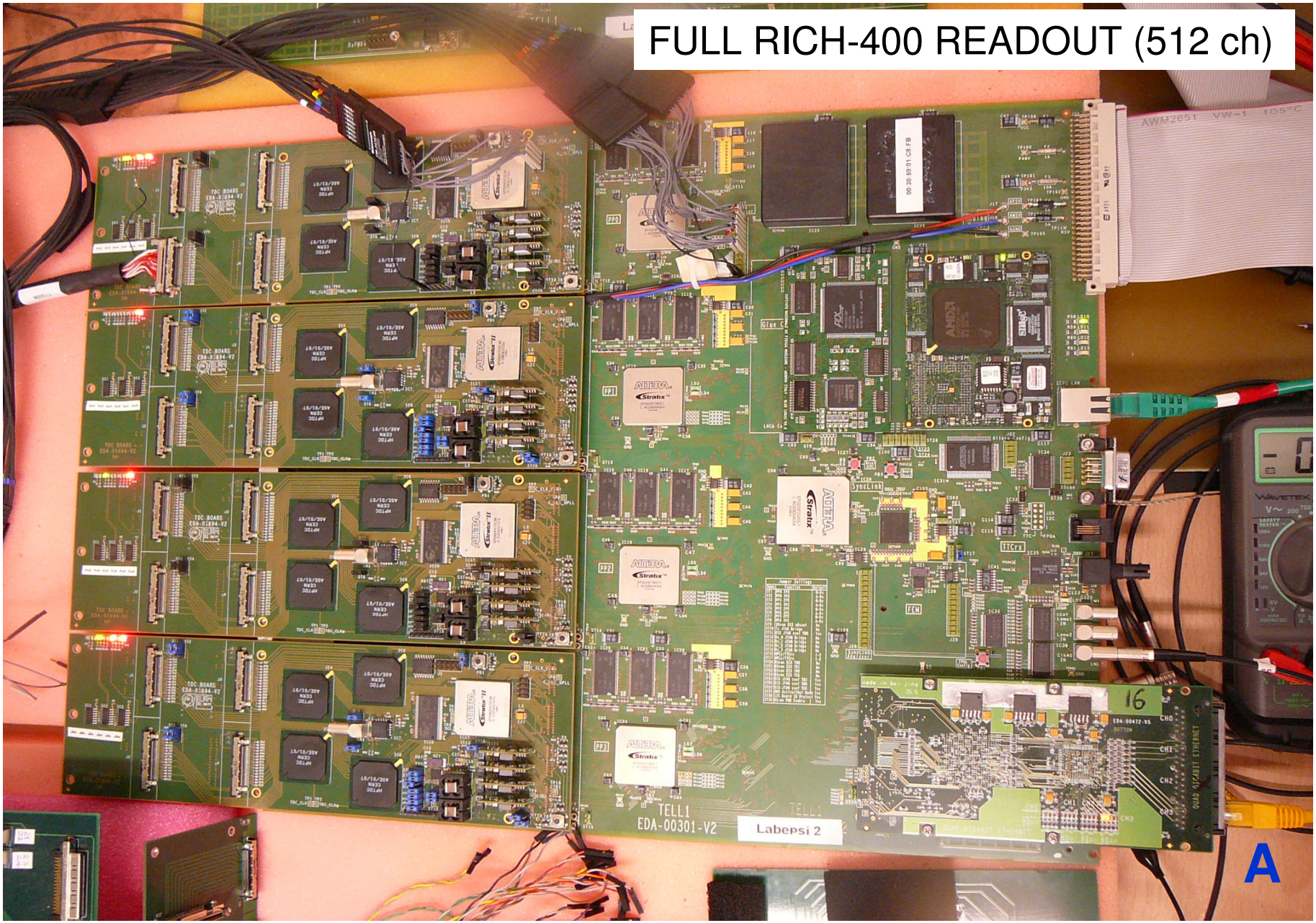
- Reminder: 128 HPTDC channels/board
- Changes in V2: noise reduction (power distribution), monitoring input/output, static RAM for future use
- Design in Pisa, Layout (10 layers) at CERN, PCB and mounting in Italy
- 18 PCB produced, 6 boards mounted and tested, firmware development

Clock jitter performance slightly improved < 30ps

No more random glitches which degraded the jitter

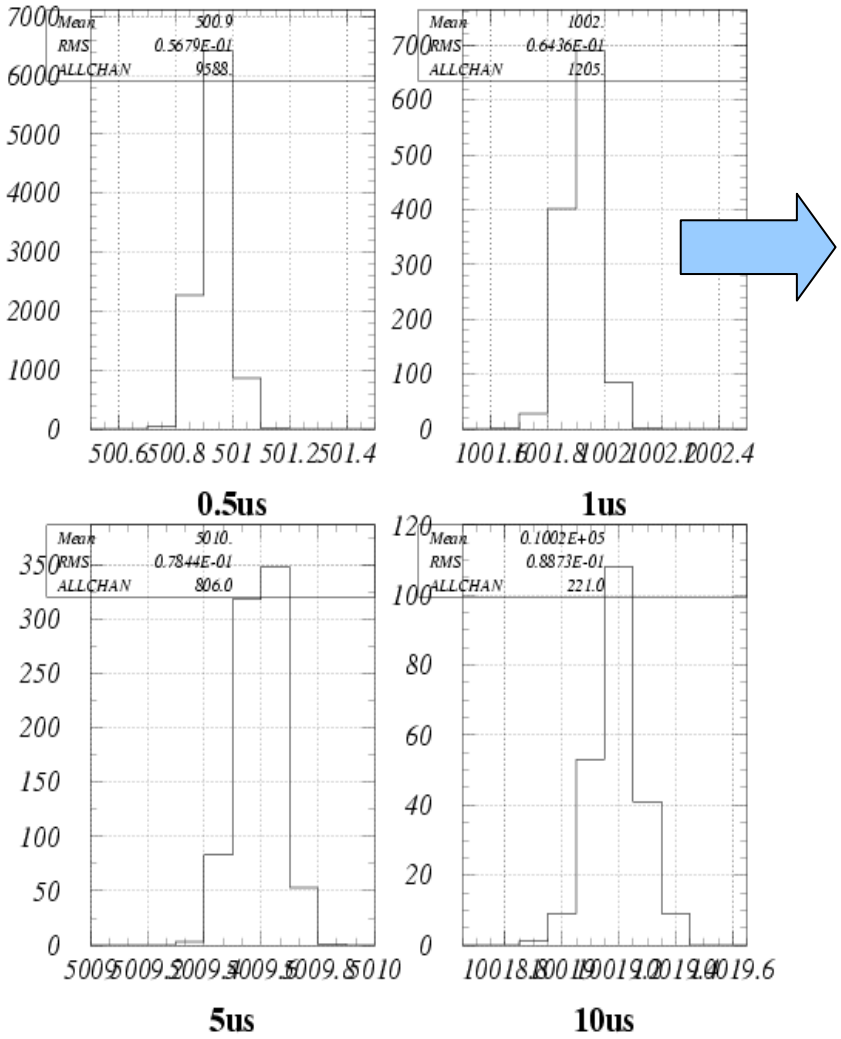


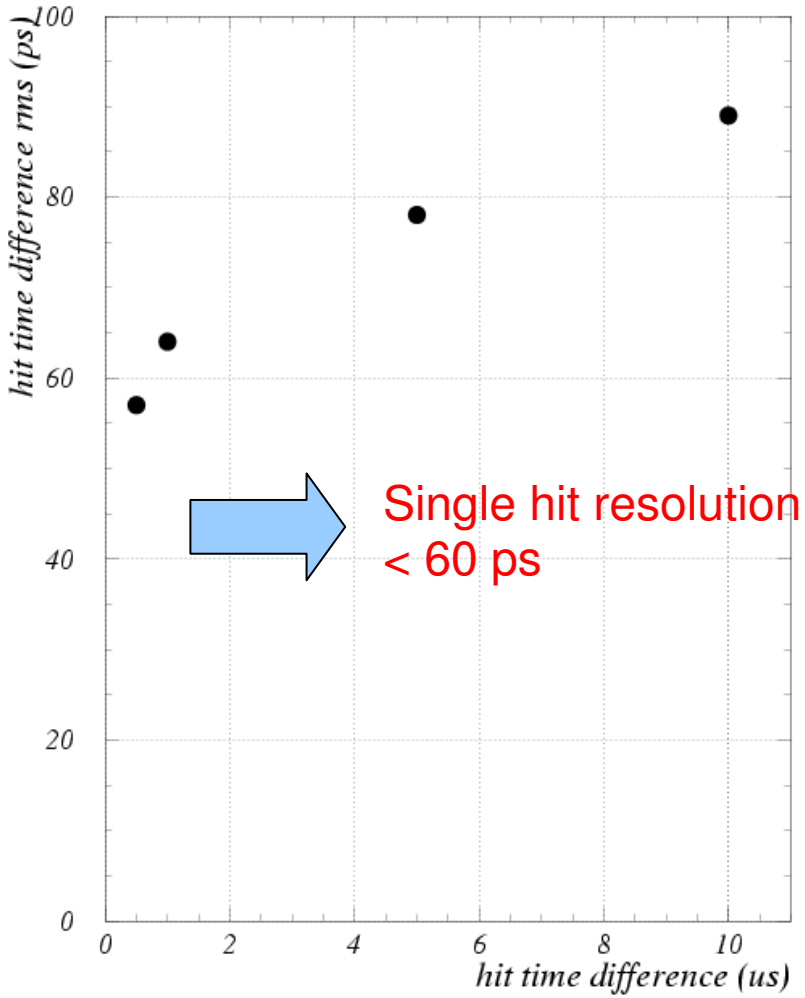
TELL1 fully equipped with TDCs



TDCB-V2: time resolution

Rms of time difference between 2 hits (same channel, fixed delay)





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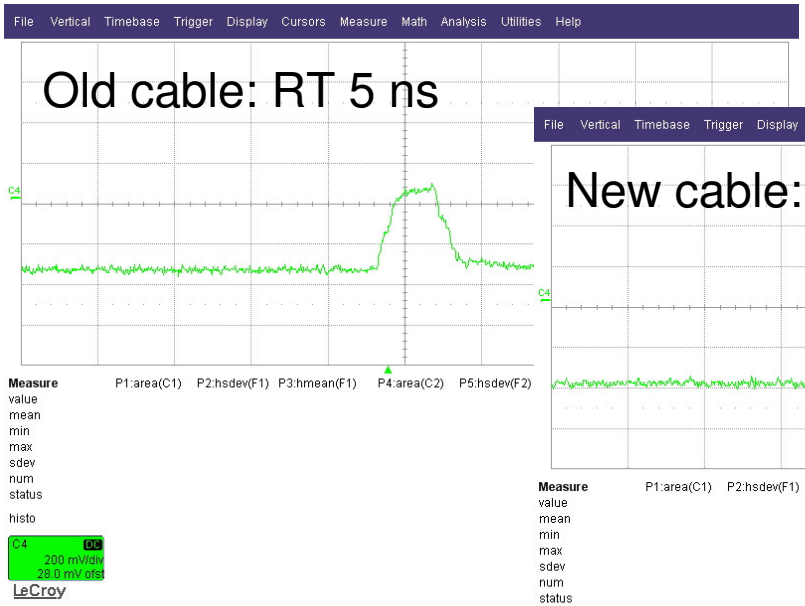
Cables

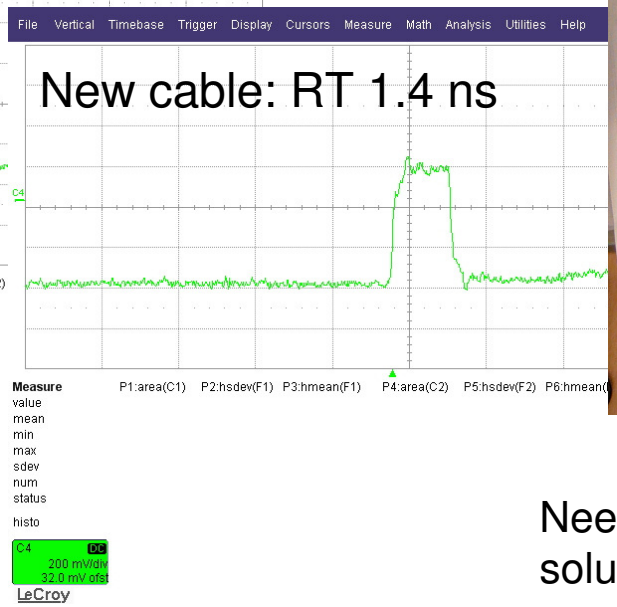
Reminder: high performance + high integration + mechanically not stiff = difficult!

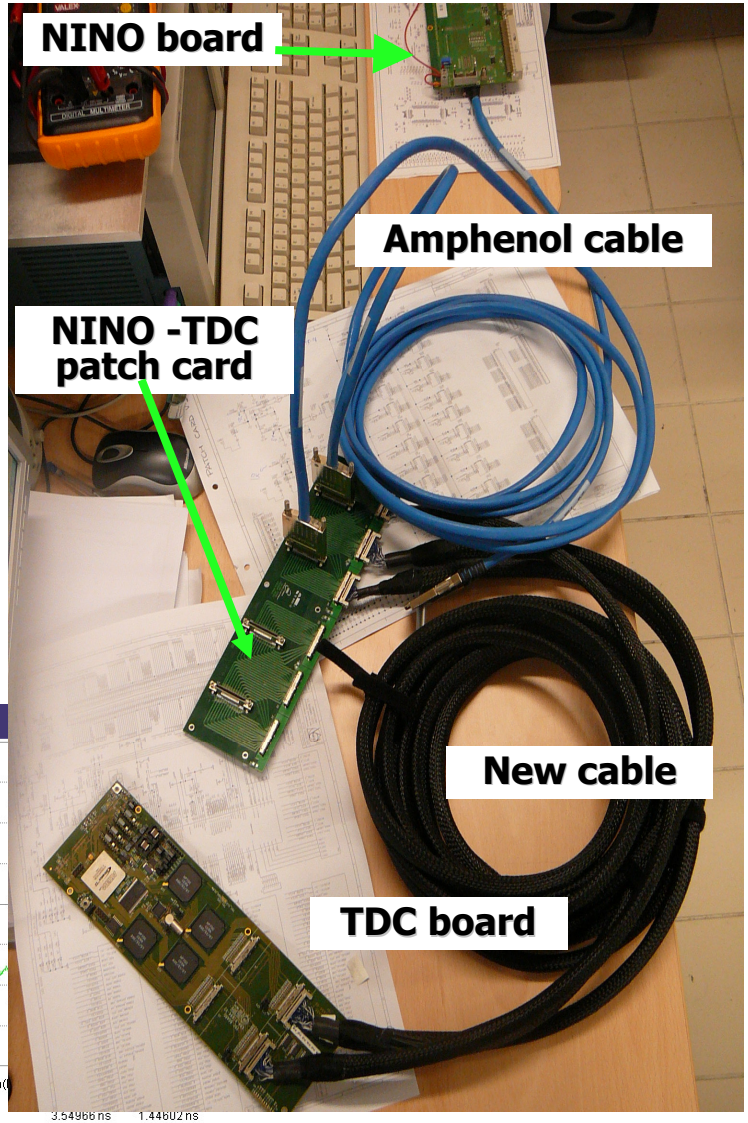
"Old" cables not produced to specifications !!!
(poor bandwidth, wrong impedance)

(1) Found new cable manufacturer (mounting by old manifacturer): prototypes OK, 40 cables available

(2) Other solution Amphenol (ALICE/TOF cable) proposed: waiting for prototypes







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Need to finalize cable and solutions for connectors and shielding

TDC project evolution

• **Software** development for hardware control, SPS interfacing, Gb ethernet readout and monitoring, overall configuration ready
• Basic DAQ design: fast enough to collect 10^6 events/spill at 100kHz
• "Naïve" **firmware** at the moment: no use of data buffer memory, readout of data buffered at trigger time
• Data buffering (external memory) and online triggering **algorithms** under development (tested on hardware development system) for testing this year
• SPS **test** with RICH-400 canceled: rescheduled laboratory test in Perugia (end of November) with 24 PMs, in spring with 400 PMs
• **Crate**: cheaper commercial solution (10 slot mini-crate) found, 2 bought (might be considered also for the experiment)

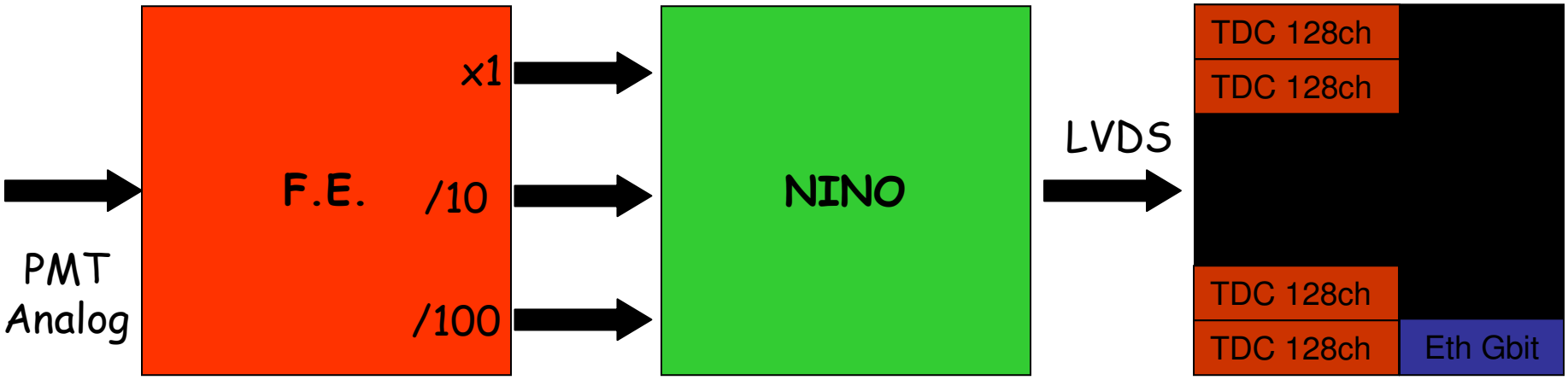
WORK TO DO:
• Develop final TDCB and TELL1 firmware
• Interconnecting TELL1 boards
• Experiment with TTC clock/trigger system

Future **firmware development** should be a collaborative effort

TELL1-based TDAQ for RICH, MUD, STRAWS, VETO, CEDAR, GTK(?)

- Problems with LHCb TELL1 problems solved (some delay): waiting for new boards soon
- More groups are buying TELL1 for evaluation and development (Louvain, Roma 2, Ferrara, Birmingham, Roma 1)
- 1-day “workshop” in Pisa (with Perugia, Roma, Frascati, Ferrara, Birmingham), 1 Birmingham engineer 3 days in Pisa
- One “special” TELL1 board with larger FPGAs (40K L.E. vs. 25K) being produced for evaluation

LAV: TELL1-based readout (Roma 1, Frascati)



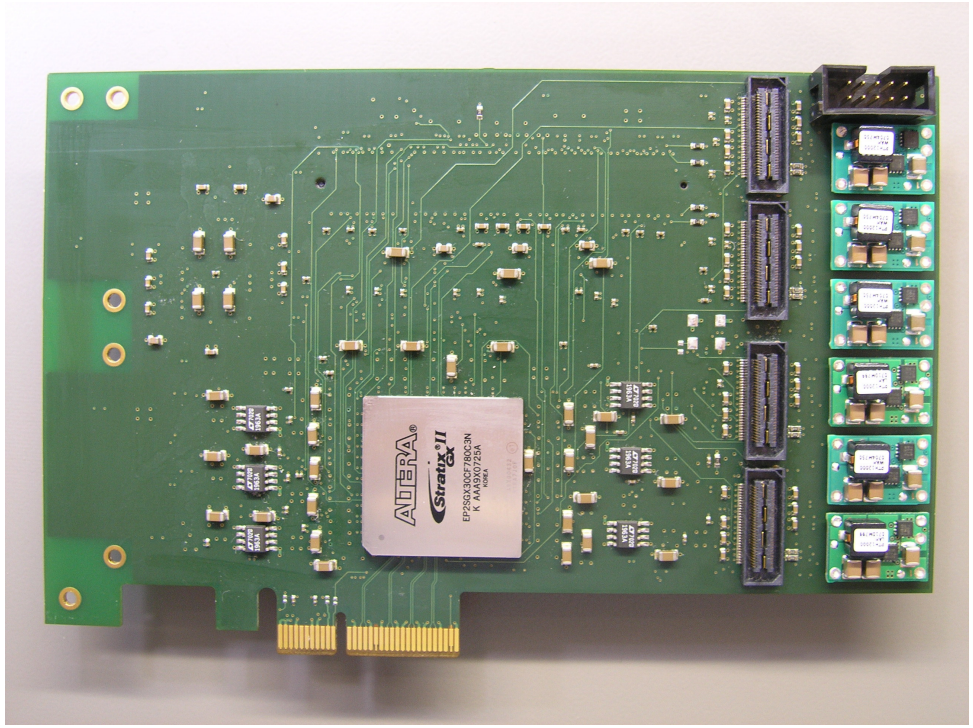
- 3 scales (channels) per PM, properly limited to avoid charge excess in NINO: x3 NINO channels x1.5 readout channels (no FADC)
- TELL1 selects the scale to be sent to PCs
- Other possible solution based on time multiplexing (1 channel/PM)
- Need a front-end splitter/attenuator card, and possibly re-engineer the NINO preamp board (prototype 8 to 24 ch. being built in Frascati now), which can also implement fast trigger/monitoring logic
- Cost is anyway not driven by the number of channels for the LAV
- L0 trigger from LAV: use same approach as RICH (daisy-chain)

Quite less expensive and bandwidth demanding than FADC solution (still open as a possibility)

Smart PCI receiver (Roma 2)

12 layers board with 4x 2.5 Gbps links, DDR2 memory, FPGA, PCI 4x
Can be used for:
- LKr readout?
- Central L0 processor?
- TELL1 data receiver?

Prototype mounted, to be tested



Optical IN: 4 x 16 bit @ 75-156 MHz (1.2-2.5 gbit/s)
Copper IN: 2-4 x 48 bit @ 66-133 MHz (3.1-6.3 gbit/s) depending on cable length o
OUT: PCI-E 4 x 16 bit @ 125 MHz (2.0 Gbit/s)

L0 trigger for LKr (Roma 2)

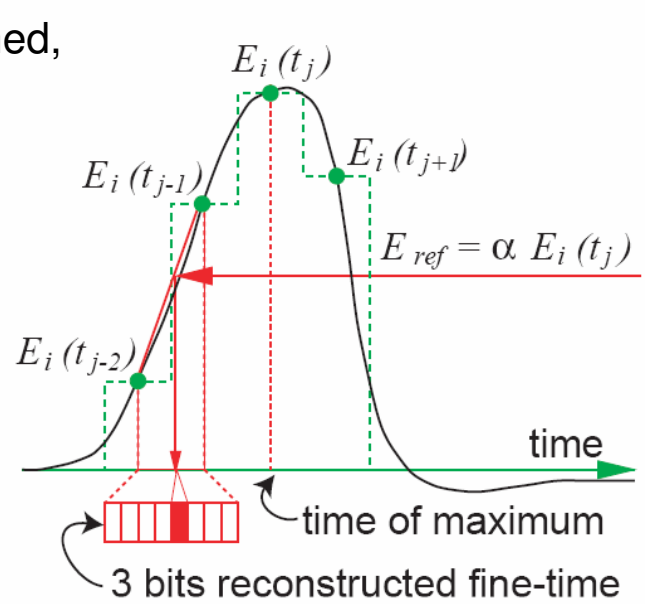
Cluster counting with 1-2 ns resolution
Baseline solution: use existing NA48 analog sums (2x8 cells) and cables, re-build following electronics (Vienna, Pisa, CERN) with: ADC mezzanines on TELL1 boards

Studied implementation in TELL1 FPGAs:

- Peak search in space, time + threshold: 1 ch = 150 LEs @ 200 MHz
- Parabolic fit around maximum: 1 ch = 1200 LEs @ 66 MHz
- Time interpolator: 1 ch = 850 LEs @ 180 MHz

A preliminary version of the firmware is ready, fully pipelined,
8 bit (256 bins) time interpolator (**100 ps/bin**)
(Preliminary) time resolution, simulated data: **RMS < 1 ns**
Non-zero suppressed readout of 2x8 analog sums:
also consistency check for main LKr readout

2 mezzanine boards: ADC and concentrator



Conclusions:

Steady progress in TDC/TELL1 pilot project

We indeed succeeded to converge on a uniform project (RICH, STRAW, CEDAR, MUV, LAV, small-detectors, partly LKr and GTK)

LKr readout: preliminary design started, some zero suppression online but allowing non-zero suppressed readout at end of burst

Central L0 processor (Pisa/Perugia): work not yet started

L1/L2 farm, algorithms, simulation: work not yet started

- *Issues: the delay in the approval is starting to raise problems for the use of LHC-based solutions:*
- *Need to secure the chips (HPTDC, TTC, TELL1), otherwise need to restart from scratch*