Silicon Pixel Detector

Special meeting

“Hits vs FatsOr mismatch”

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Hits Vs FastOr mismatch

① Offline analysis
② Hardware configuration checks
- Timing configuration of the detector
- Verify the half-stave configuration procedure
- Collect informations on the configuration of the problematic HSs
- Collect informations on the trigger behaviour of the chips in the problematic HSs
- Match the two strobe lengths for the pixel hits and the Fast-Or

③ List of features of the runs taken

https://alice.its.cern.ch/jira/browse/SPD-27

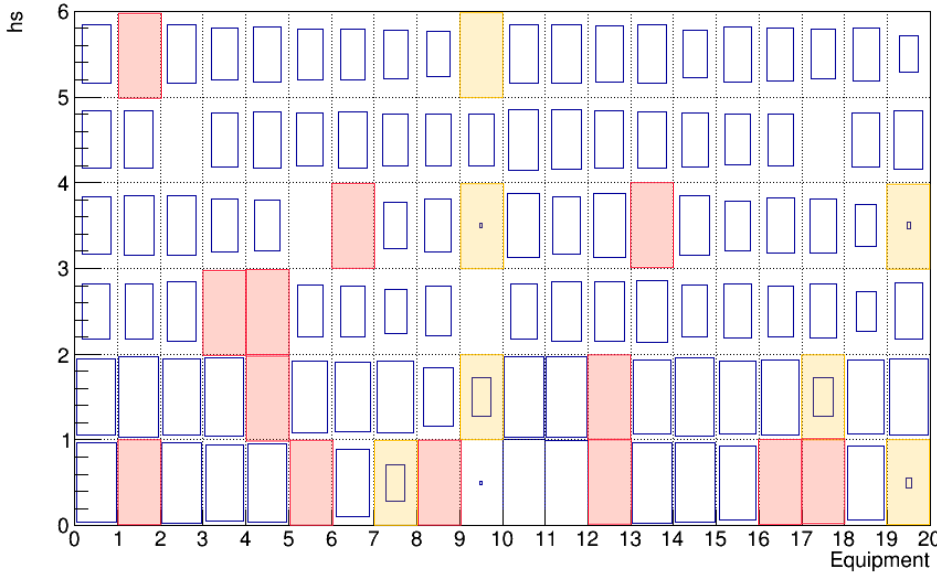
Hits Vs FastOr mismatch

① Offline analysis

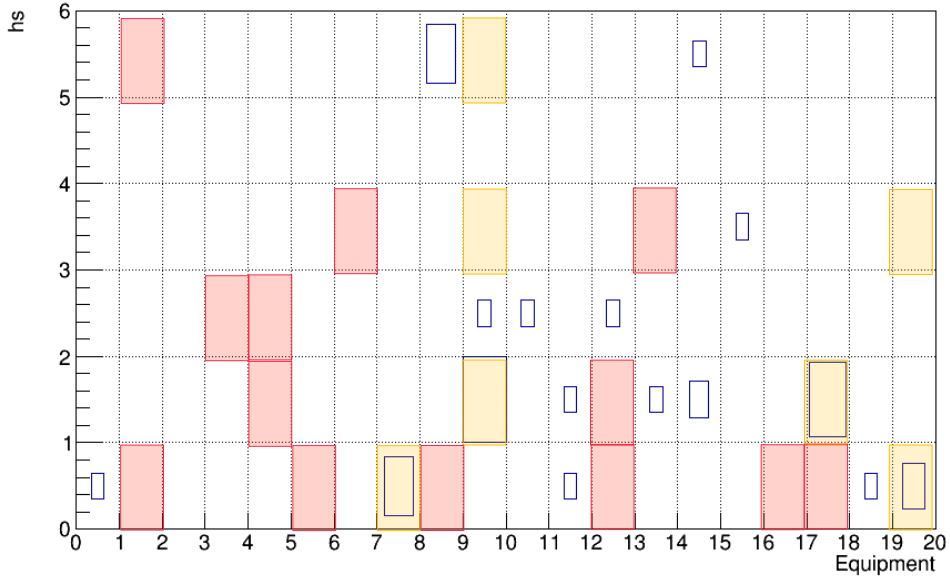
- [19 June 2015]
  - First 1000 events of the first chunk coming from each GDC have been ordered according to Period-Orbit-BC for un 226472
  - Event by event the chip-fired vs FO-fired matching was checked (Chip-fired = at least one pixel hit)

RUN: 226472 (affected by the problem)
HSs flagged in "MEB problem" plot:7C1, 7A0, 9C0, 9A1, 9A3, 9C3, 9A5
HSs out: 1A0, 1A5, 2C0, 2C1, 3A2, 3C3, 4A1, 4A2, 5A0, 6A3, 6C0, 7C0, 8A0

matching in same event



matching in previous event

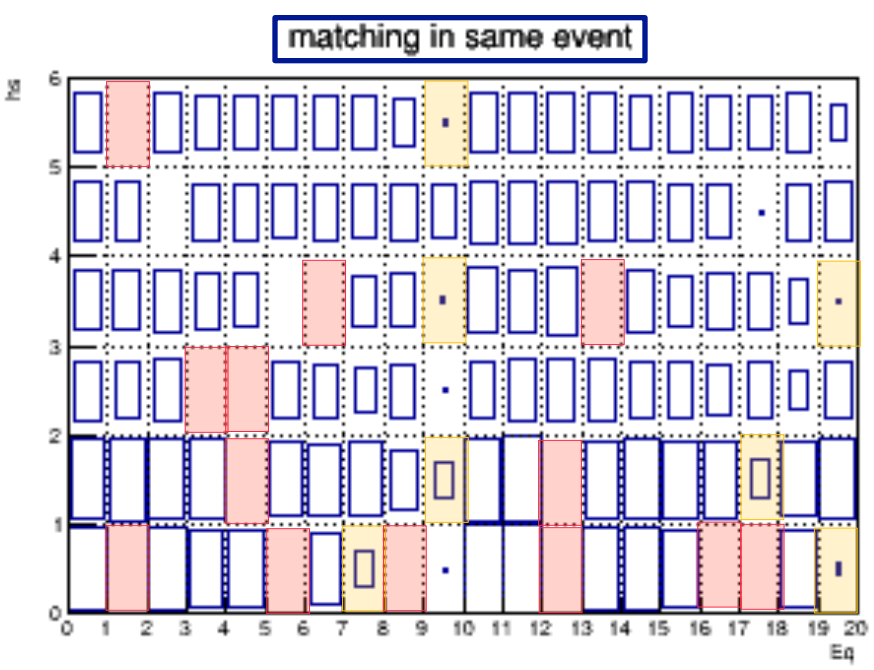


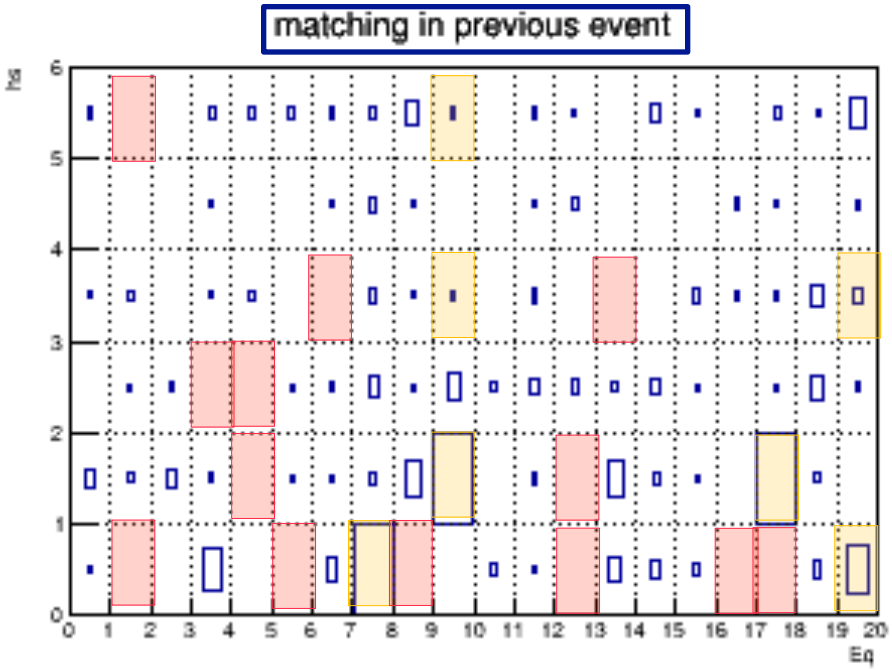
Hits Vs FastOr mismatch

① Offline analysis

- [23 June 2015]
  - First 50000 events from the run 226472 ordered in time
  - The matching in the same event is present for half-staves in sectors 9 and 19
  - Clear matching with the previous event for the half-staves 7A0, 7C1, 9A1 and 9C0
  - Matching with the previous events not always clear: e.g. 9A3

RUN: 226472 (affected by the problem)
HSs flagged in "MEB problem" plot:7C1, 7A0, 9C0, 9A1, 9A3, 9C3, 9A5
HSs out: 1A0, 1A5, 2C0, 2C1, 3A2, 3C3, 4A1, 4A2, 5A0, 6A3, 6C0, 7C0, 8A0



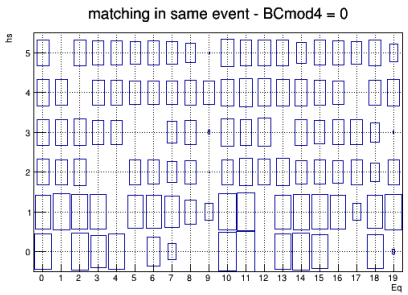


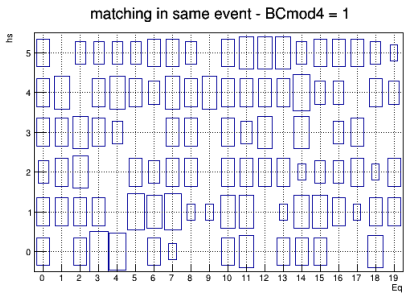
Hits Vs FastOr mismatch

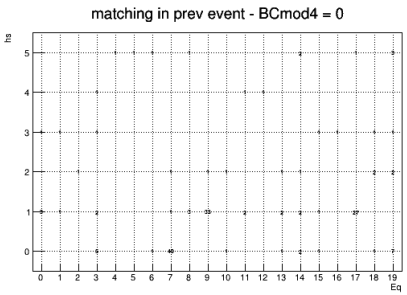
① Offline analysis

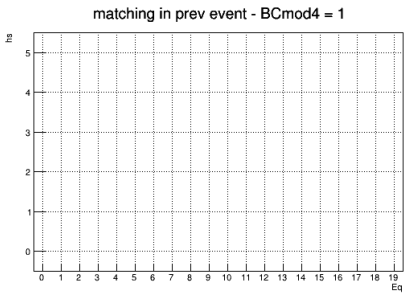
- [23 June 2015]
  - First 50000 events from the run 226472 ordered in time
  - The matching in the same event is present for half-staves in sectors 9 and 19.
  - Clear matching with the previous event for the half-staves 7A0, 7C1, 9A1 and 9C0.
  - Matching with the previous events not always clear: e.g. 9A3.
  - Different behaviour for the BCmod4=1

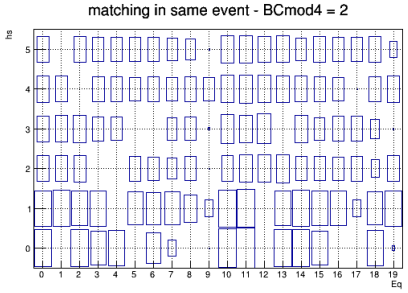
RUN: 226472 (affected by the problem)
HSs flagged in "MEB problem" plot:7C1, 7A0, 9C0, 9A1, 9A3, 9C3, 9A5
HSs out: 1A0, 1A5, 2C0, 2C1, 3A2, 3C3, 4A1, 4A2, 5A0, 6A3, 6C0, 7C0, 8A0

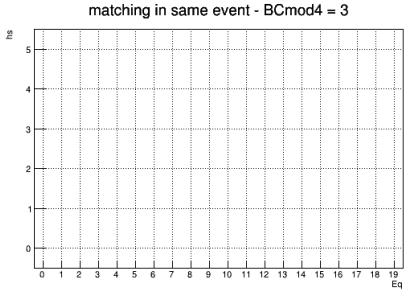


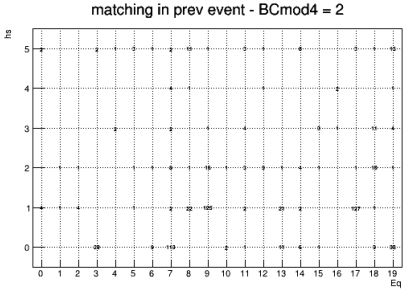


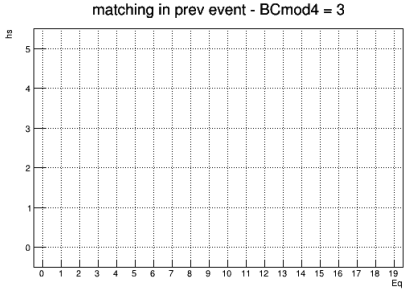












Hits Vs FastOr mismatch

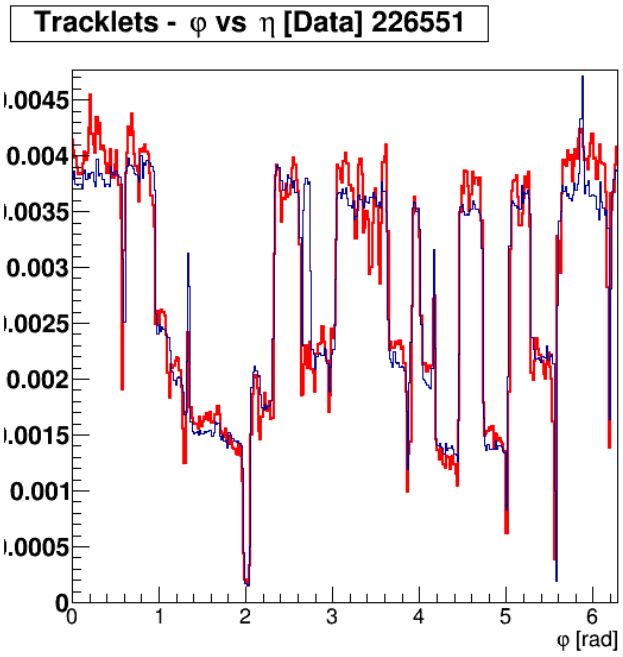
① Offline analysis

- [10 July 2015] – GEO-PAG (LF-PWG) presentation

Good Run

Checks were performed on data/mc on a "good" run:

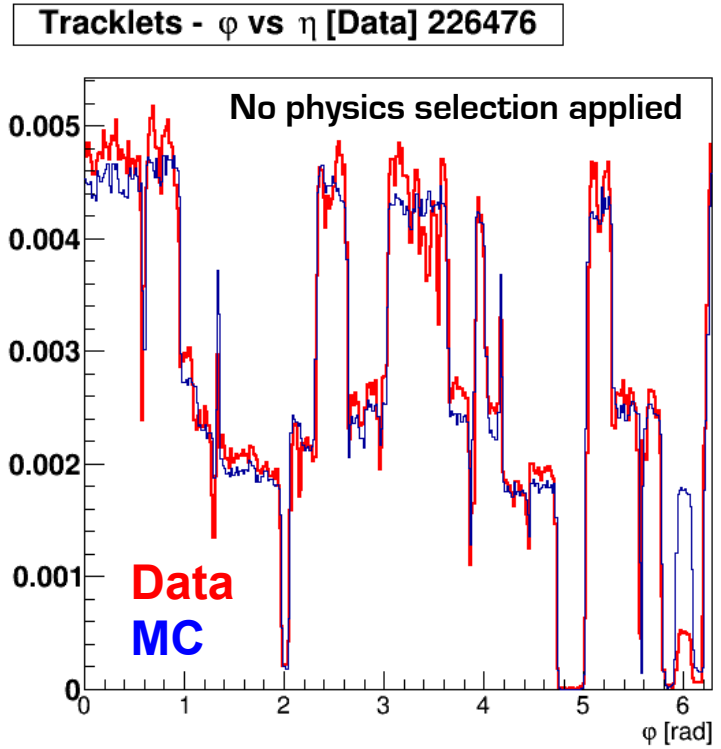
- ✓ No depletion visible



Masking the 7 HSs

Checks were performed on data/mc when masking the 7 HSs:

- ✓ $4 < \phi < 5$ → recovered
- ✓ $5.4 < \phi < 6$ → need one more HS masking (depletion at phi=6)



Hits Vs FastOr mismatch

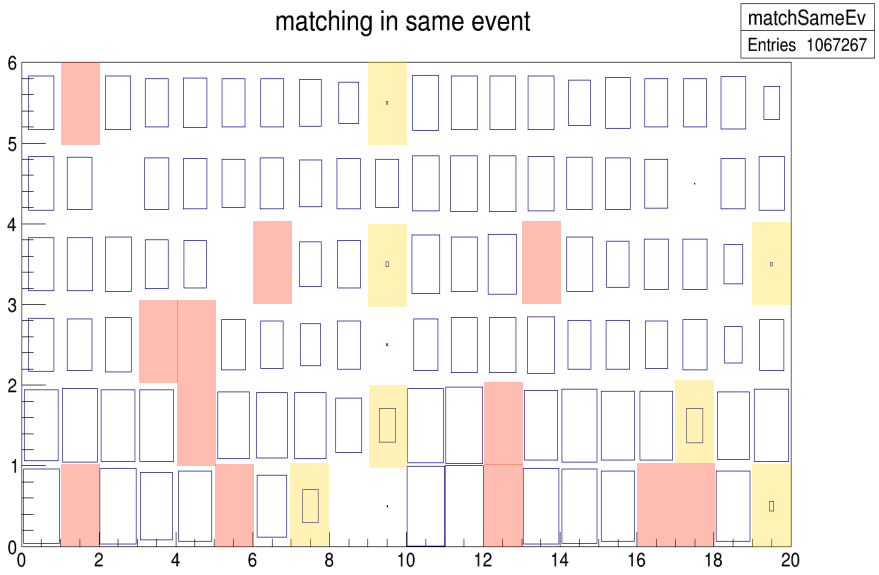
① Offline analysis

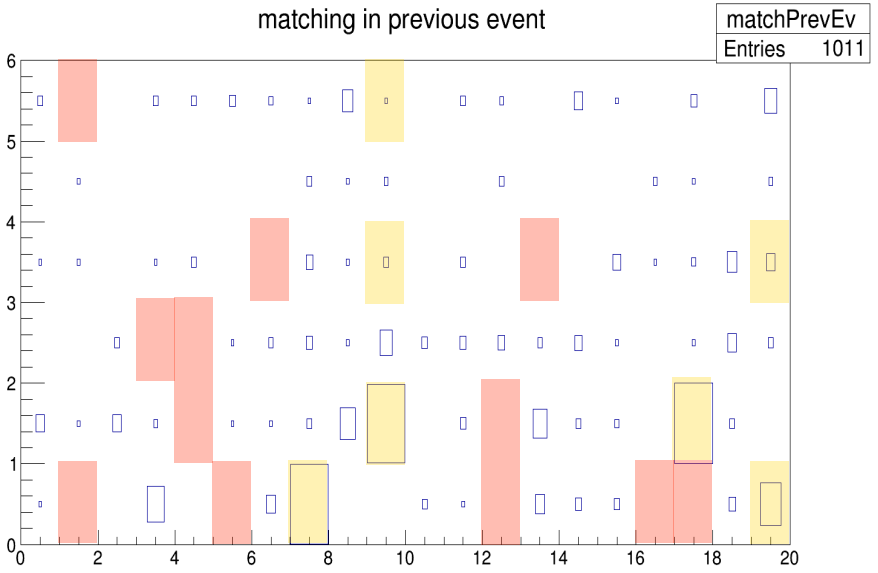
- [28 August 2015] – News from Fabio
  - Analysis tool improvement: running time over 50k events
    - ✓ reduced from time > 1d to < 3h using TTeee

Hits Vs FastOr mismatch

① Offline analysis

- [28 August 2015] – News from Fabio
  - ***Mismatch N → N-1***
  - Run 226472. Analysis of first 50000 events (from the first chunks of each GDC)
  - Events are temporally ordered (using period_orbit_BC) and then fastOr/pixel hit corrispondences are searched
    - ✓ Save event match: fastOr in >1 chip in event N and pixel hit in the SAME chip(s) in event N
    - ✓ Previous event match: fastOr in >1 chip in event N and pixel hit in the SAME chip(s) in event N-1, with no pixel hit corrispondence in event N
  - **7A0, 9A1, 7C1, 9C0**: sensibly lower matches in same event, maximum number of matches with previous event
  - **9A3, 9A5, 9C3**: very few matches both in same event and in previous event

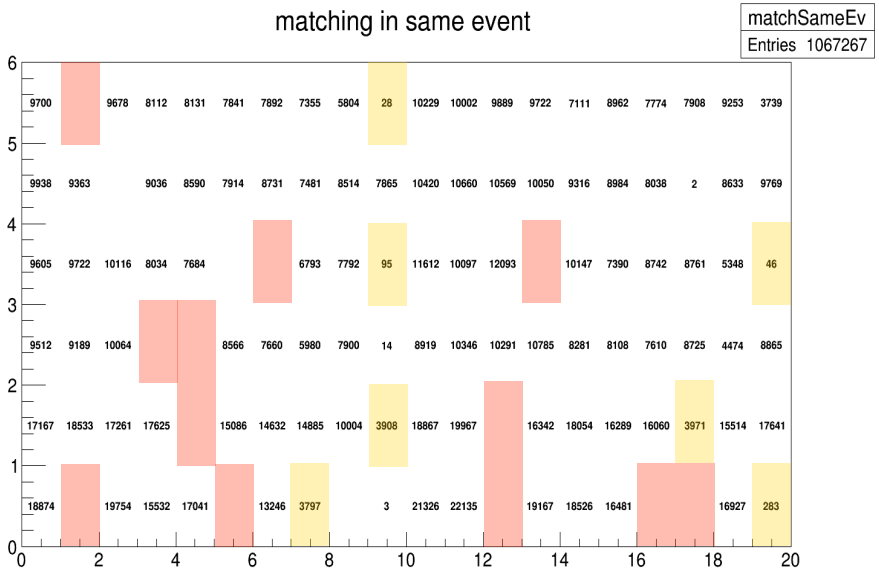


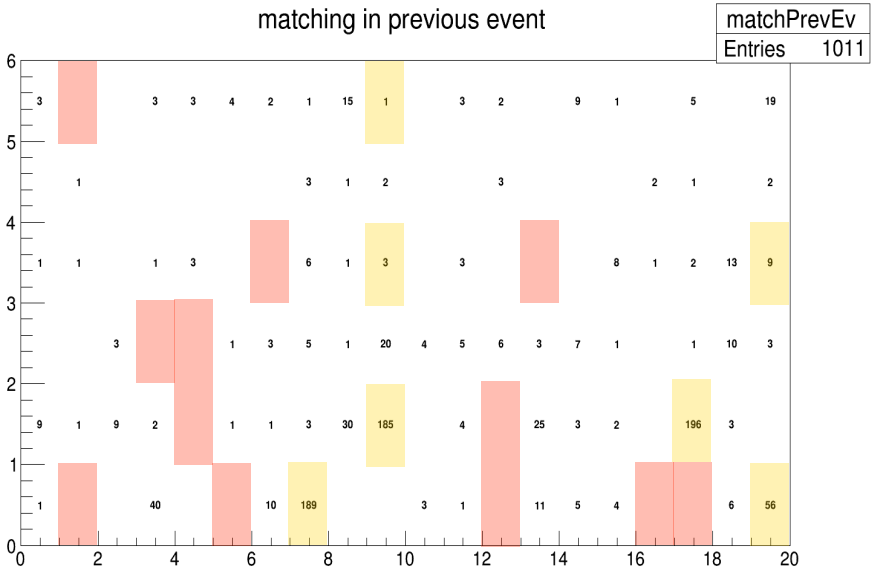


Hits Vs FastOr mismatch

① Offline analysis

- [28 August 2015] – News from Fabio
  - Here the same plots, but with numbers (more details)
  - **7A0, 9A1, 7C1, 9C0**:
    - ✓ 1/5 (at most) of matches in the same event, w.r.t. HS with no MEB problem
    - ✓ Even if there are more matches with N-1 event, their number is drastically low w.r.t. same event matches for regular HS
  - **9A3, 9A5, 9C3**: very few matches both in same event and in previous event
  - For the HS with MEB problem, hence, the total number of fastOr/pixel hits is not conserved
    - ✓ Maybe there are matches between N and N-2, N-3, or N+1, N+2, N+3? See later the check for N-2



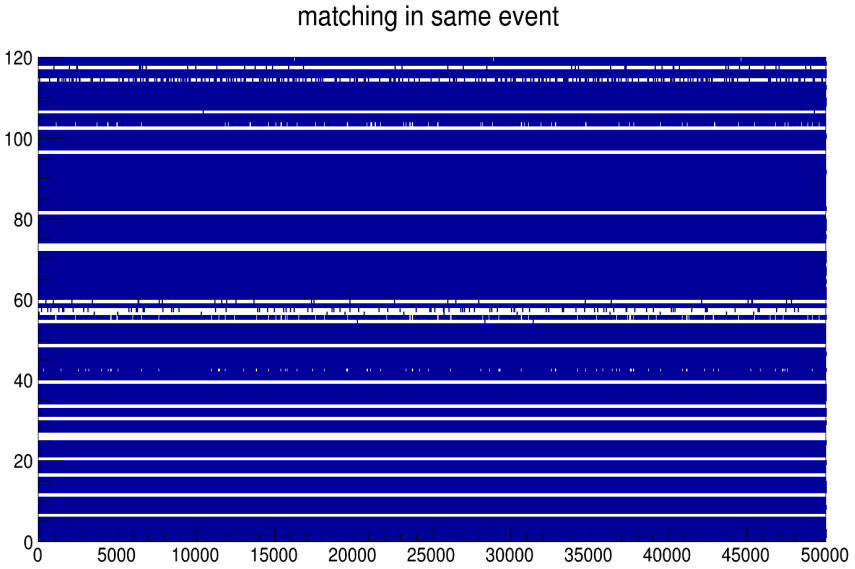


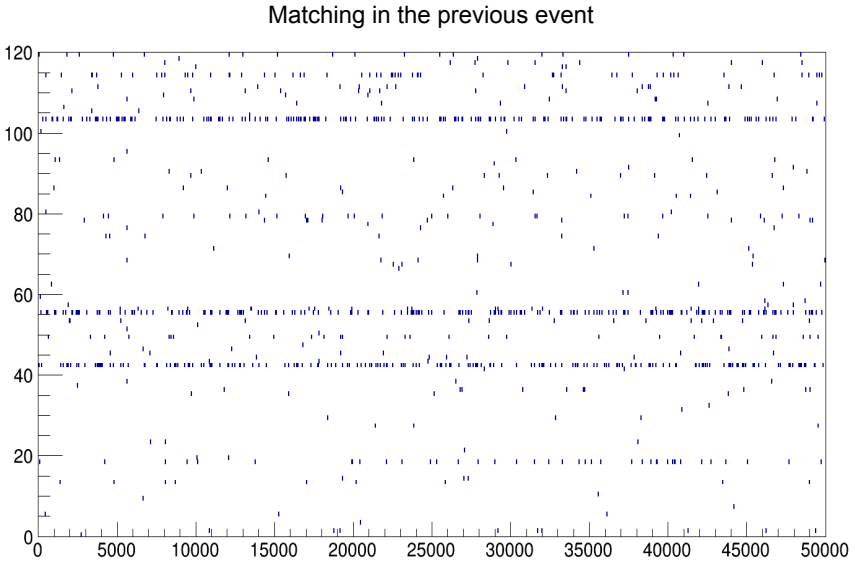
Hits Vs FastOr mismatch

① Offline analysis

➢ [28 August 2015] – News from Fabio

- More details about the ***temporal distribution*** of fastOr/pixel hit in same event and previous event
  - ✓ x axis: number of the event, in temporal order
  - ✓ y axis: number of HS (#equipment*10 + #HS)
  - ✓ If fastOr/pixel hit *match* is found for a given HS in a given event, an entry is added, otherwise the bin is empty
- In **'Same event'** plot, a match is often found, except for off HS and HS with MEB problem
- In **'Previous event'** plot
  - ✓ Very rare entries for regular HS
  - ✓ **7A0, 9A1, 7C1, 9C0**:
    - Much more entries, but RANDOMLY PLACED
    - No 'burst' or structures found
    - Independent among the four HS
  - ✓ **9A3, 9A5, 9C3**: very few entries



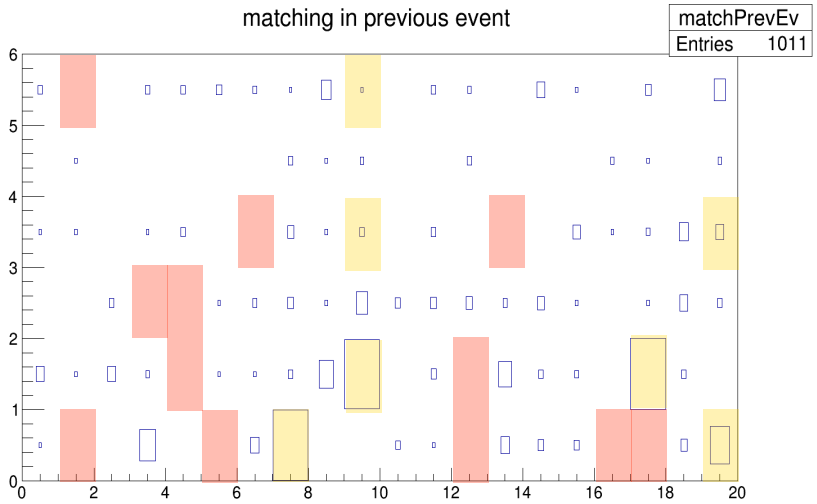


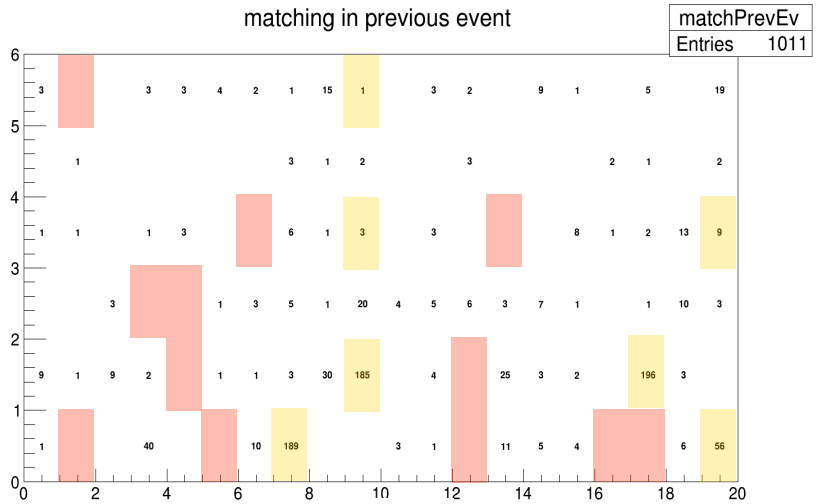
Hits Vs FastOr mismatch

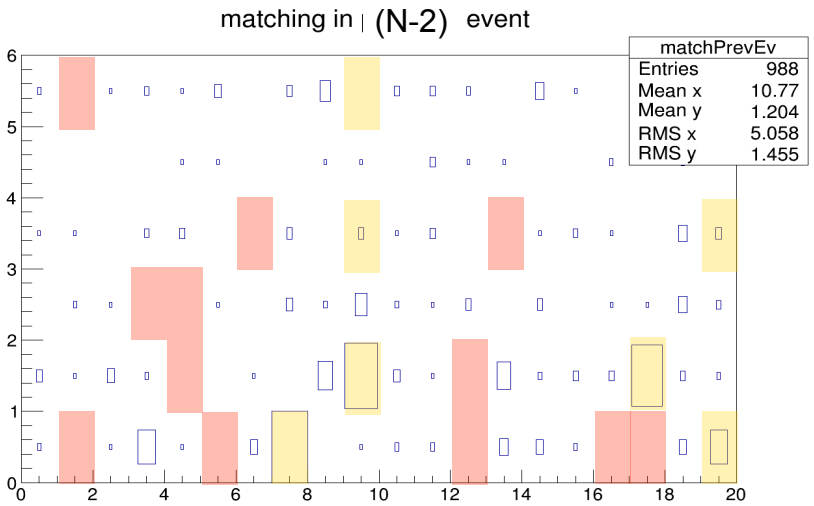
① Offline analysis

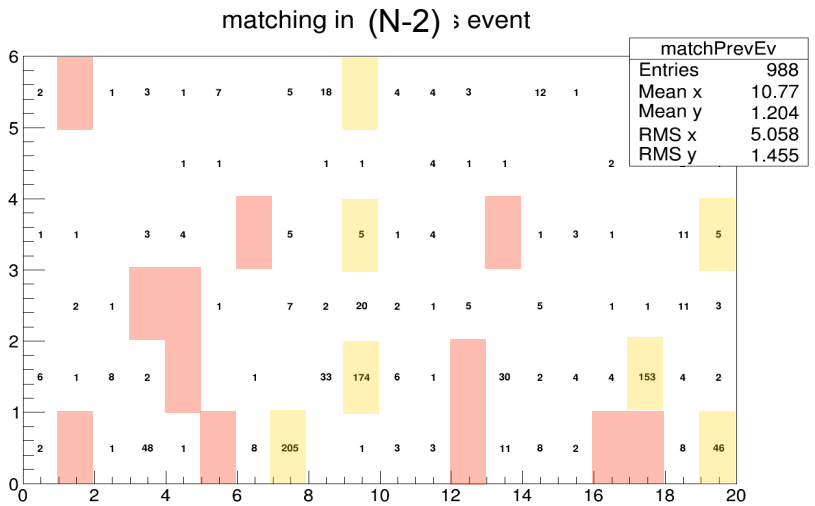
➤ [28 August 2015] – News from Fabio

- Let's check matches between fastOr in event N and pixel hits in N-2
  - ✓ The mismatch is similarly present with N-1 and N-2 events (will try other possibilities as a cross-check)





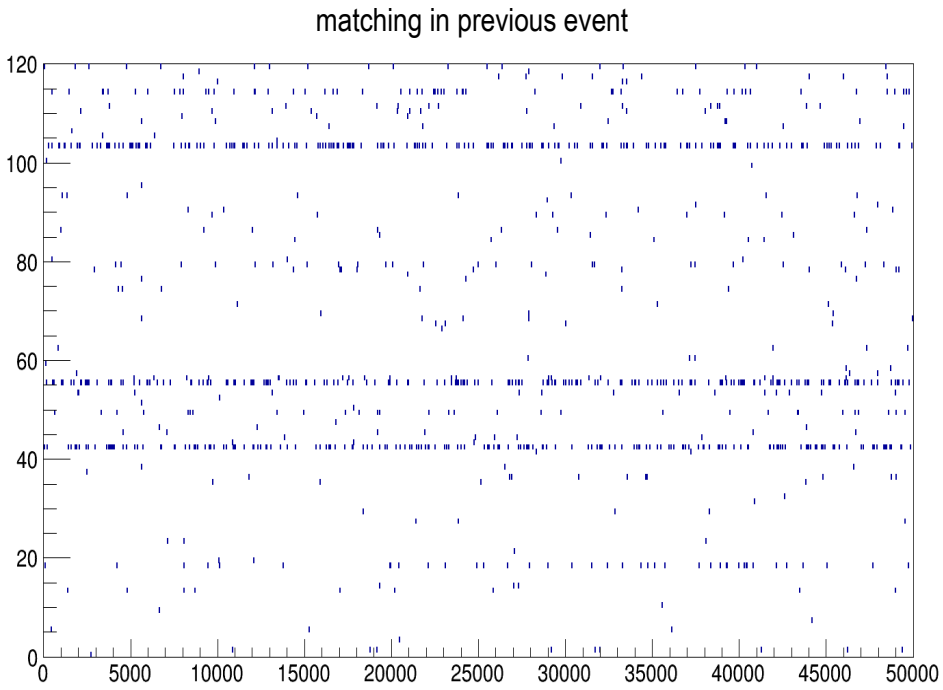


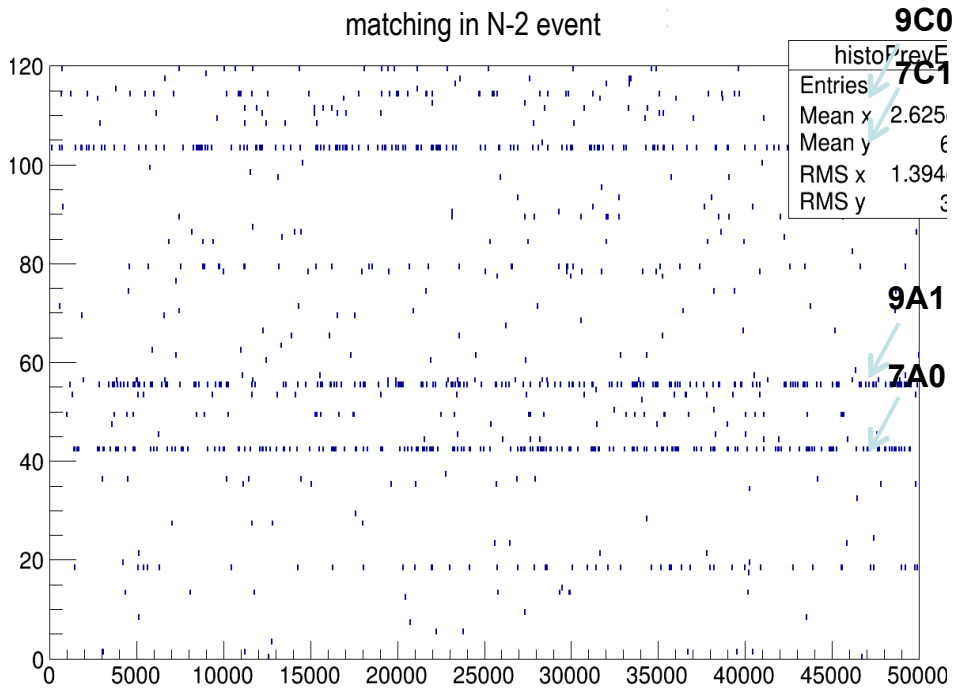


Hits Vs FastOr mismatch

① Offline analysis

- [28 August 2015] – News from Fabio
  - For N-2 matching (fastOr in event N, pixel hit in N-2), the situation is again very similar w.r.t. N-1 case, also in the temporal distribution of matches



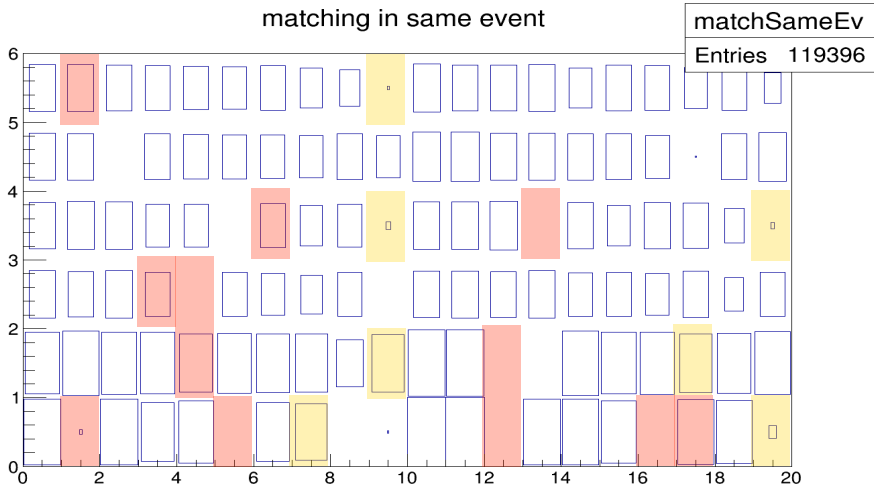


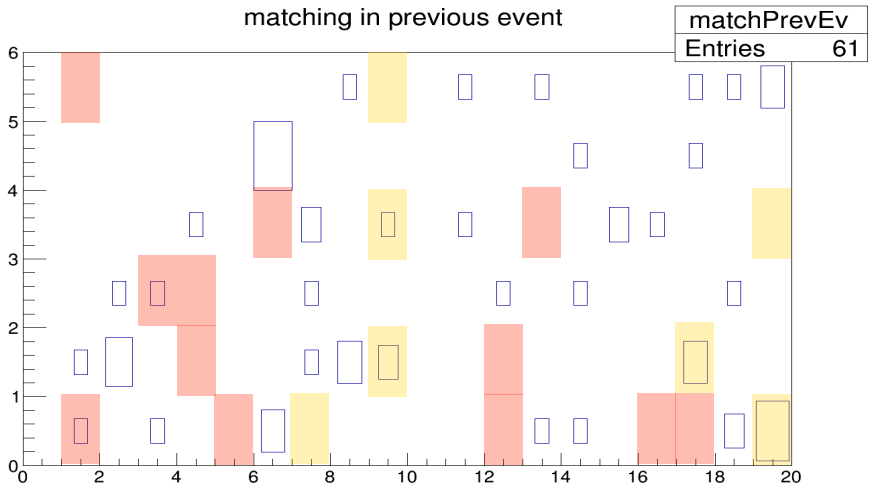
Hits Vs FastOr mismatch

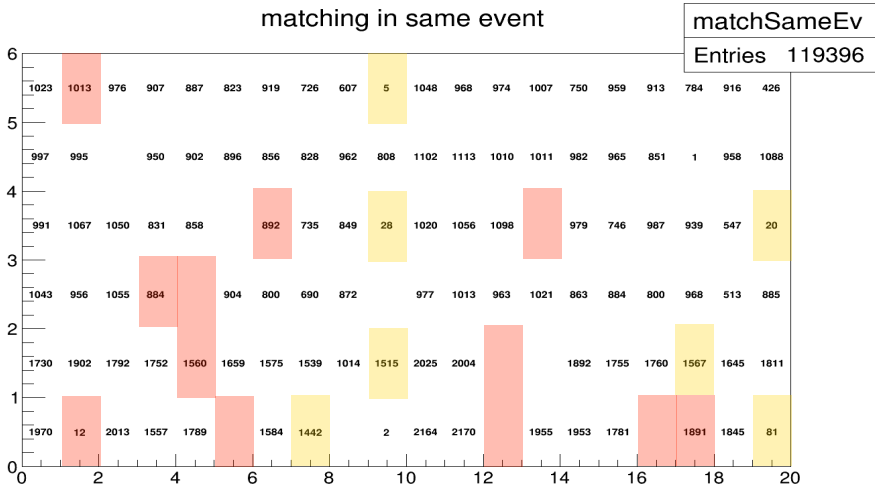
① Offline analysis

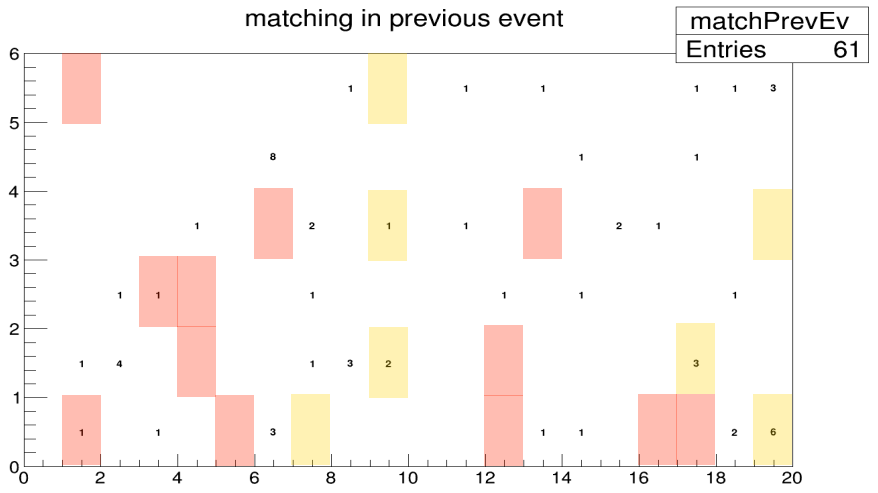
➢ [28 August 2015] – News from Fabio

- Check a more recent run 233091 → Note: only first 5000 events (1/10 of the statistics analyzed w.r.t 226472)
- Same event matches: 1/10 w.r.t 226472, as expected;
- Prev event matchs: much less than 1/10 for 7A0, 9A1, 7C1, 9C0 + equally distributed among all the HS (outlier in 6A3)









Hits Vs FastOr mismatch

② Hardware configuration check

- Timing configuration of the detector
  - Timing configuration self-consistency
    - Read-out efficiency check changing the relative delay between the Fast-Or signal and the LHC clock (given by the CTP) by BC unit (25 ns)
  - Timing alignment wrt the other L0 inputs
    - Needed to be sure that, whenever a global trigger comes in the four BC present within the 100 ns strobe of the PIT, the trigger signal from the PIT is asserted with the same efficiency
    - Two different checks: discrete delay (per BC unit) and fine delay tuning

→ **Conclusions**

1) SPD readout efficient in all the four BC lock

2) SPD needs adelay of 1 BC to be aligned to the other L0 inputs (as concluded in Run1)

Hits Vs FastOr mismatch

② Hardware configuration check

- Verify the half-stave configuration procedure
  - Few questions have been answered concerning the configuration of the HSs after the clock transition
    - The clock transition happen at the beginning of each run at the INJECTION phase
    - The HSs are not configured after each clock transition unless needed (operator intevention)
    - It was the same also during Run1

  → **Conclusion**: the configuration of the HSs cannot be perfomed at the SOR, but could be implemented in the ACT and request to be performed after the clock transition

- Start Of Run (SOR) procedure revision
  - Discovered that a request (DIM) to the CTP to execute "FEEreset" command included also the the "TTCrx reset" after the configuration of the routers
  - Solved asking to Anton to create a new command that execute only the "FEEreset"
  - Minor remaining point: the FEEreset should be executed before the resetDPI and DataReset (just after the AutoConfigRouter) → In this way the resetDPI fails → The FEEreset is executed as last operation during the SOR (and probably this was during Run1)

Hits Vs FastOr mismatch

② Hardware configuration check

- Collect informations on the configuration of the problematic HSs
  - Checked all the main parameters (COMPREF, CONVPOL, FOPOL, PreVTH, DACRefHi, DACRefMid, delay_control and delay_misc)
  - Comparing to HS that didn't show the problem in the "MEB problem" DQM plot, we observe few differences for parameters (FOPOL, CONVPOL and COMPREF) that do not affect the pixel hits and readout

  → **Conclusion**: (Gianluca) "*It can have an impact on operations if the FO vs hits correlation plots are used to detect issues*"

- Collect informations on the trigger behaviour of the chips in the problematic HSs
  - Few questions have been answered concerning the trigger behaviour
    - Practically all the chips for these 7 HSs are included in the trigger mask
    - No noisy pixels are present in these chips
    - DAC configuration checked → conclusion in the previous point
  - [*To be done*] Measure the trigger rate in each chip out of a run and during a run (always with beam).
  - [*To be done*] Measure the counts for that half-stave during acquisition

Hits Vs FastOr mismatch

② Hardware configuration check

- Match the two strobe lengths for the pixel hits and the Fast-Or
  - Discuss the possibility to match the two strobe lengths for the pixel hits and the Fast-Or.
  - At the moment (actually since Run1) the strobe length for the pixel hits is equal to 300 ns, while the one for the Fast-Or is equal to 100 ns, to allow the collection of the slowest hits signals. This configuration would for sure induce the presence of "missing Fast-Or".
  - The possibility to match the two strobe lengths require some test to check the efficiency in different strobe length configuration.
  - This need has been expressed during the ITS operations meeting during 9th July https://indico.cern.ch/event/407121/

Hits Vs FastOr mismatch

③ List of features of the run taken

- A table with the following informations is continuosly updated:
  - Run: date, duration, HLT status, #LDC, #GDC:
  - Fill: fill number, magnets status, beam mode, filling scheme
  - Detector: half-stave included in data taking, presence of cdh error, status of the FastOr missing efficiency, presence of MEB problem, presence of events flagged as 'High Multiplicity'

  → Look at the table

Backup

Backup

Collect informations on the configuration of the problematic HSs

COMPREF	Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 7	Chip 8	Chip 9
HS 1A0	128	128	128	128	128	128	128	128	128	128
HS 2A3	70	70	70	70	70	70	70	70	70	70
HS 3C2	30	30	30	20	30	20	30	30	20	30
HS 5C3	30	30	30	30	30	30	30	30	30	30
HS 7A0	30	30	30	30	40	60	60	60	60	60
HS 7C1	80	80	80	80	80	80	50	80	80	80
HS 9A1	40	20	80	40	40	40	40	40	40	40
HS 9C0	100	100	100	100	100	100	100	100	100	100
HS 9A3	100	100	100	100	100	100	100	100	100	100
HS 9C3	100	100	100	100	100	100	100	100	100	100
HS 9A5	100	100	100	100	100	100	100	100	100	100

CONVPOL	Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 7	Chip 8	Chip 9
HS 1A0	128	128	128	128	128	128	128	128	128	128
HS 2A3	140	140	140	140	140	140	140	140	140	140
HS 3C2	160	160	160	160	160	160	160	160	140	160
HS 5C3	150	150	150	150	150	150	150	150	150	150
HS 7A0	160	160	160	160	160	140	140	140	140	140
HS 7C1	140	140	140	140	140	140	140	140	140	140
HS 9A1	160	160	160	160	160	140	140	140	140	140
HS 9C0	255	255	255	255	255	255	255	255	255	255
HS 9A3	255	255	255	255	255	255	255	255	255	255
HS 9C3	255	255	255	255	255	255	255	255	255	255
HS 9A5	255	255	255	255	255	255	255	255	255	255

Backup

Collect informations on the configuration of the problematic HSs

FOPOL	Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 7	Chip 8	Chip 9
HS 1A0	128	128	128	128	128	128	128	128	128	128
HS 2A3	70	70	70	70	70	70	70	70	70	70
HS 3C2	60	60	60	50	60	50	60	60	50	60
HS 5C3	70	70	70	70	70	70	70	70	70	70
HS 7A0	40	40	40	40	40	60	60	60	60	60
HS 7C1	80	80	80	80	80	80	80	80	80	80
HS 9A1	50	50	50	50	50	50	50	50	50	50
HS 9C0	0	0	0	0	0	0	0	0	0	0
HS 9A3	0	0	0	0	0	0	0	0	0	0
HS 9C3	0	0	0	0	0	0	0	0	0	0
HS 9A5	0	0	0	0	0	0	0	0	0	0

PreVTH	Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 7	Chip 8	Chip 9
HS 1A0	190	190	190	190	190	190	190	190	190	190
HS 2A3	200	190	195	200	200	200	200	200	200	200
HS 3C2	200	195	190	190	190	190	195	190	190	185
HS 5C3	190	180	180	180	180	180	180	200	200	180
HS 7A0	170	170	170	170	170	180	180	180	180	180
HS 7C1	200	200	200	200	200	200	180	200	195	200
HS 9A1	190	190	200	200	195	200	200	190	190	190
HS 9C0	200	200	200	200	200	200	200	200	200	200
HS 9A3	200	200	200	200	200	200	200	200	200	200
HS 9C3	200	200	200	200	200	200	200	200	200	200
HS 9A5	200	200	200	200	200	200	200	200	200	200

Backup

Collect informations on the configuration of the problematic HSs

delay_control	Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 7	Chip 8	Chip 9
HS 1A0	55	55	55	55	55	55	55	55	55	55
HS 2A3	55	55	55	55	55	55	55	55	55	55
HS 3C2	55	55	55	55	55	55	55	55	55	55
HS 5C3	55	55	55	55	55	55	55	55	55	55
HS 7A0	55	55	55	55	55	55	55	55	55	55
HS 7C1	55	55	55	55	55	55	55	55	55	55
HS 9A1	55	55	55	55	55	55	55	55	55	55
HS 9C0	55	55	55	55	55	55	55	55	55	55
HS 9A3	55	55	55	55	55	55	55	55	55	55
HS 9C3	55	55	55	55	55	55	55	55	55	55
HS 9A5	55	55	55	55	55	55	55	55	55	55

delay_misc	Chip 0	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 7	Chip 8	Chip 9
HS 1A0	192	192	192	192	192	192	192	192	192	192
HS 2A3	192	192	192	192	192	192	192	192	192	192
HS 3C2	192	192	192	192	192	192	192	192	192	192
HS 5C3	192	192	192	192	192	192	192	192	192	192
HS 7A0	192	192	192	192	192	192	192	192	192	192
HS 7C1	192	192	192	192	192	192	192	192	192	192
HS 9A1	192	192	192	192	192	192	192	192	192	192
HS 9C0	192	192	192	192	192	192	192	192	192	192
HS 9A3	192	192	192	192	192	192	192	192	192	192
HS 9C3	192	192	192	192	192	192	192	192	192	192
HS 9A5	192	192	192	192	192	192	192	192	192	192

Backup

Collect informations on the configuration of the problematic HSs

DACRefHi	All Chips
HS 1A0	84
HS 2A3	107
HS 3C2	93
HS 5C3	83
HS 7A0	90
HS 7C1	81
HS 9A1	100
HS 9C0	98
HS 9A3	116
HS 9C3	116
HS 9A5	78

DACRefMId	All Chips
HS 1A0	94
HS 2A3	101
HS 3C2	111
HS 5C3	113
HS 7A0	108
HS 7C1	86
HS 9A1	112
HS 9C0	100
HS 9A3	109
HS 9C3	109
HS 9A5	111

Backup

Check of timing configuration

- Timing configuration self-consistency
  - Study performed in the days 28-29th June and 1th July
  - Read-out efficiency check changing the relative delay between the Fast-Or signal and the LHC clock (given by the CTP) by BC unit (25 ns) → *SPD parameter 'PIT Link Delay'*
    - ✓ Run in global partition with PIT as only input for the CTP
    - ✓ Looking at the events flagged by BC and changing the relative Fast-OR/LHC clock delay by more 5 BC (125 ns) we expect strong inefficiency in one of the five cases
    - ✓ In run 228448 the mean number of hits per event is strongly suppressed wrt the other runs
  - Further consistency check: delay the hits read-out strobe wrt the L1 signal → *SPD parameter 'L1 Fine Delay'*
    - ✓ In runs 228437 and 228434 → no data foreseen in the two configurations tested
  - Details on the operations done and the final good configuration to run with a data acquisition strobe equal to 100 ns (needed to run with higher rate) con be consulted at the following link:
    https://alice-logbook.cern.ch/logbook/date_online.php?p_cont=comd&p_cid=509702
    https://alice-logbook.cern.ch/logbook/date_online.php?p_cont=threadd&p_tid=509793&p_cidh=510005#le510005

Run	L1 Fine Delay	PIT Link Delay	BCmod4	Hits/events
228440	2	0	3	26
228450	2	1	0	26.5
228452	2	2	1	26.3
228446	2	3	2	25.3
228448	2	4	3	**0.99**
228437	3	3	2	1
228434	1	0	3	0.12

Backup

Check of timing configuration

- Timing configuration self-consistency
  - Study performed in the days 28-29th June and 1th July
  - Read-out efficiency check changing the relative delay between the Fast-Or signal and the LHC clock (given by the CTP) by BC unit (25 ns) → *SPD parameter 'PIT Link Delay'*
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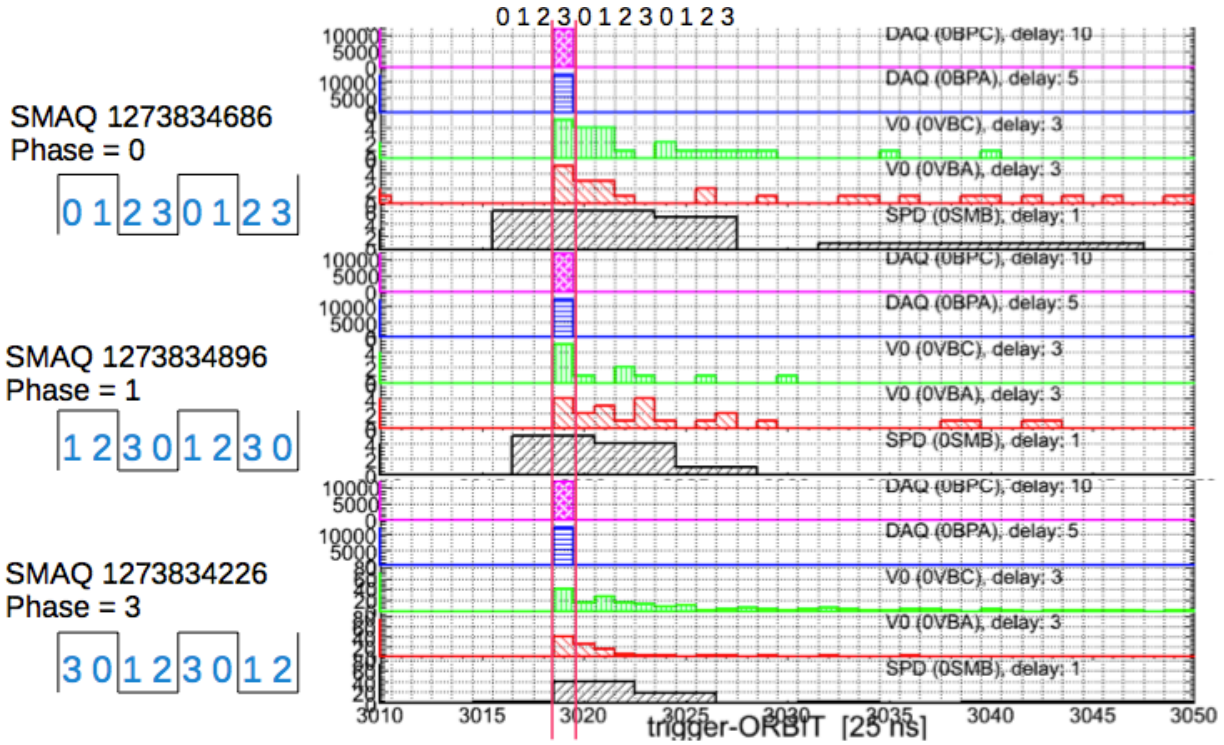
    https://alice-logbook.cern.ch/logbook/date_online.php?p_cont=threadd&p_tid=509793&p_cidh=510005#le510005

- Side note: during these tests we discovered that the PIT output OSCO (signature 29) is not aligned to the other PIT outputs
  - Output used for self-triggering in standalone runs → connected trough the LTU (3th February)
    https://alice-logbook.cern.ch/logbook/date_online.php?p_cont=threadd&p_tid=497254&p_cidh=509883#le509883
  - Details on the operations:
    https://alice-logbook.cern.ch/logbook/date_online.php?p_cont=threadd&p_tid=509792&p_cidh=509884#le509884

Backup

Check of timing configuration

- Timing alignment wrt the other L0 inputs
  - Needed to be sure that, whenever a global trigger comes in the four BC present within the 100 ns strobe of the PIT, the trigger signal from the PIT is asserted with the same efficiency
  - Study already performed in 2010 → Conclusion: need to the delay all the PIT inputs by 1 BC
    https://alice-logbook.cern.ch/logbook/date_online.php?p_cont=threadd&p_tid=398766&p_cidh=398766#le398766



Backup

Check of timing configuration

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  - Needed to be sure that, whenever a global trigger comes in the four BC present within the 100 ns strobe of the PIT, the trigger signal from the PIT is asserted with the same efficiency
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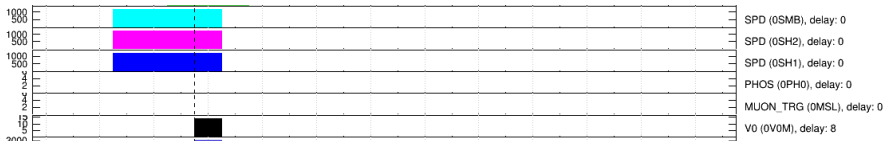
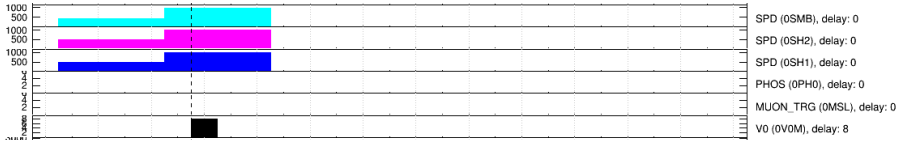
  - Details on the operations:
    https://alice-logbook.cern.ch/logbook/date_online.php?p_cont=threadd&p_tid=509793&p_cidh=510290#le510290
  - Two different checks:
    - Discrete delay (per BC unit)
      → Conclusion: need to delay all the PIT inputs by 1 BC (as concluded in Run1)

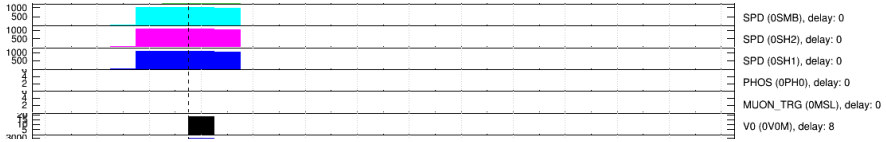
BClock0



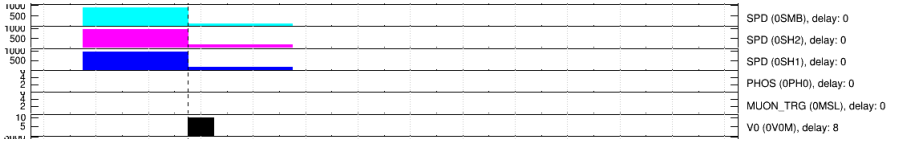
BClock2



BClock1



BClock3 → Not in coincidence



Backup

Check of timing configuration

- Timing alignment wrt the other L0 inputs
  - Needed to be sure that, whenever a global trigger comes in the four BC present within the 100 ns strobe of the PIT, the trigger signal from the PIT is asserted with the same efficiency
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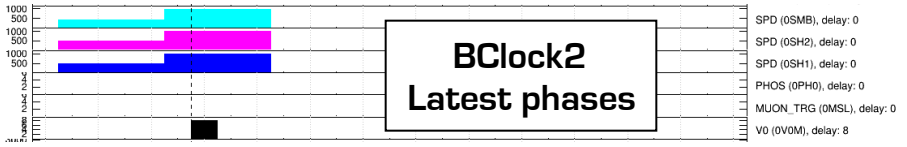
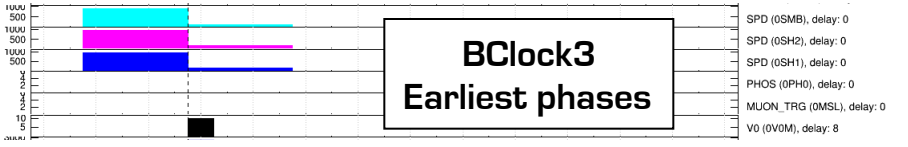
  - Two different checks:
    - Discrete delay (per BC unit)
      → Conclusion: need to delay all the PIT inputs by 1 BC (as concluded in Run1)
    - Fine delay tuning





Backup

Check of timing configuration

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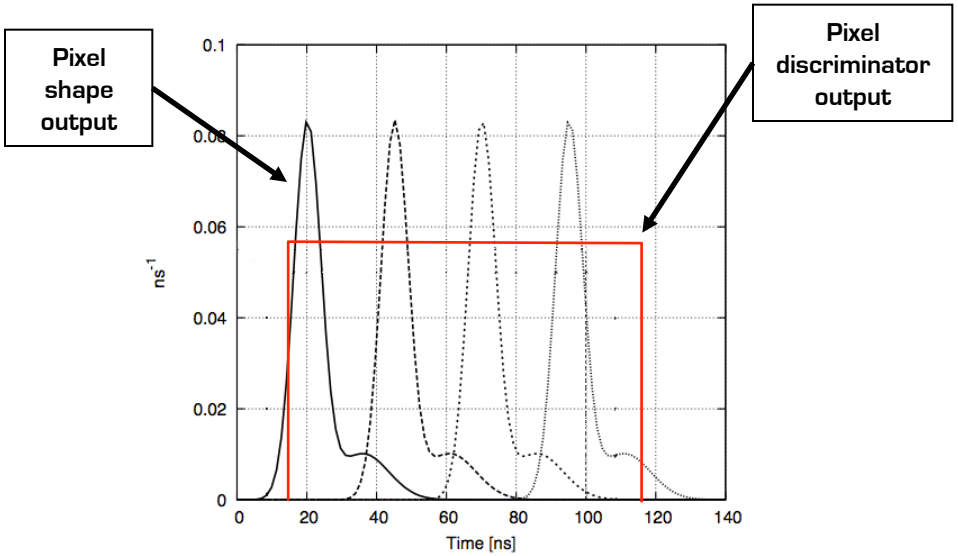
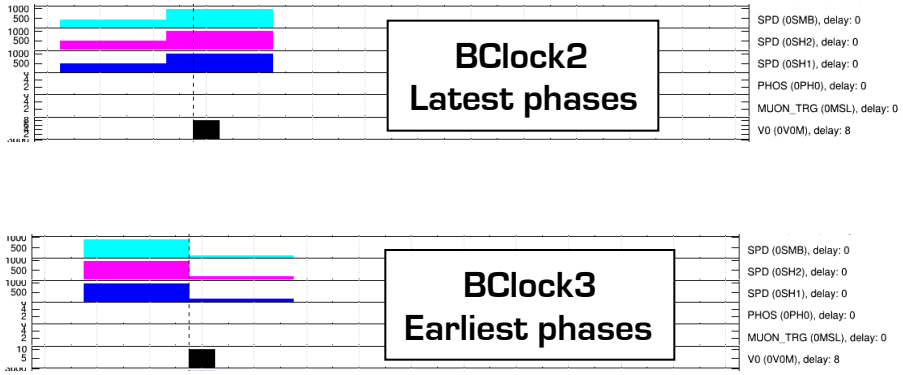
    - Fine delay tuning





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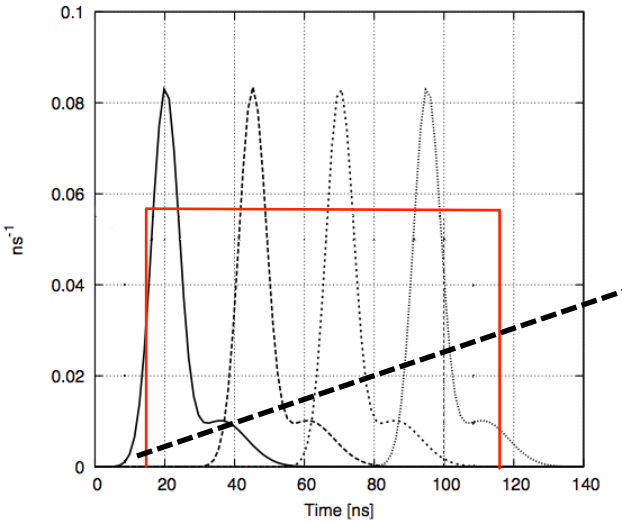

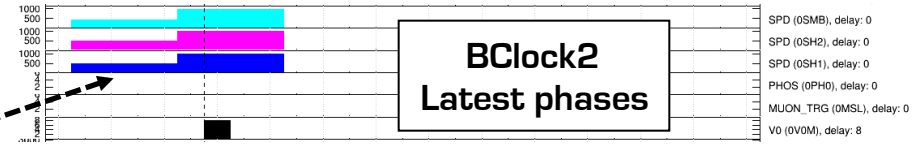

Backup

Check of timing configuration

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  - Two different checks:
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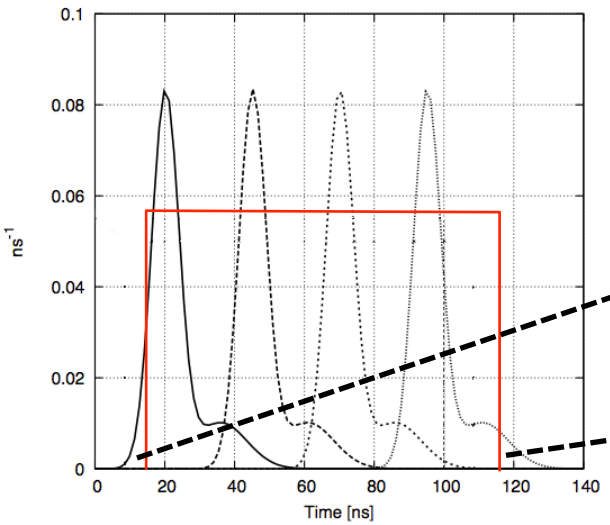
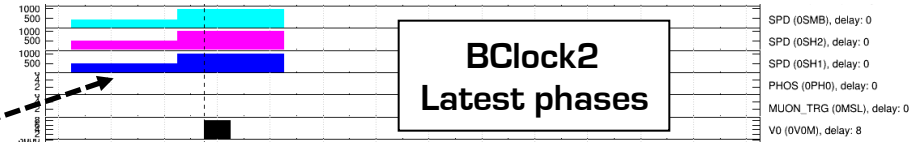
    - Fine delay tuning





Backup

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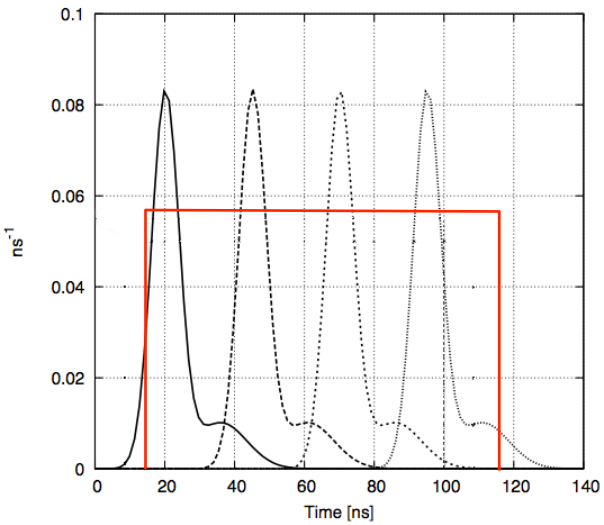
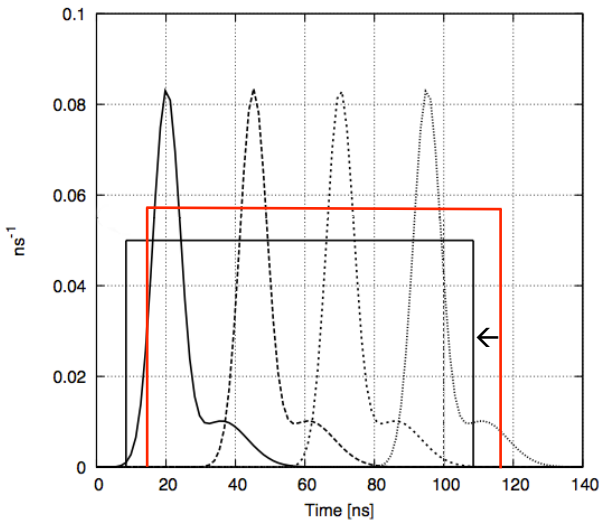
  - Two different checks:
    - Discrete delay (per BC unit)
      → Conclusion: need to delay all the PIT inputs by 1 BC (as concluded in Run1)
    - Fine delay tuning



Fine shift



Backup

Check of timing configuration

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  - Study already performed in 2010 → Conclusion: need to the delay all the PIT inputs by 1 BC
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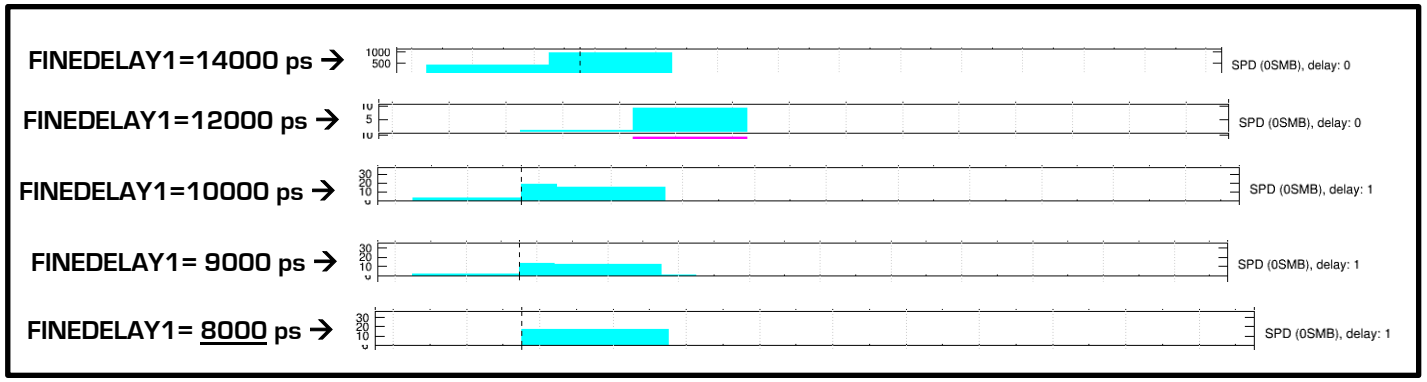
  - Details on the operations:
    https://alice-logbook.cern.ch/logbook/date_online.php?p_cont=threadd&p_tid=509793&p_cidh=510290#le510290
  - Two different checks:
    - Discrete delay (per BC unit)
      → Conclusion: need to delay all the PIT inputs by 1 BC (as concluded in Run1)
    - Fine delay tuning
      - ✓ FINEDELAY1 parameter in LTU configuration
      - ✓ Standard value 14000 ps (measured in Run1)



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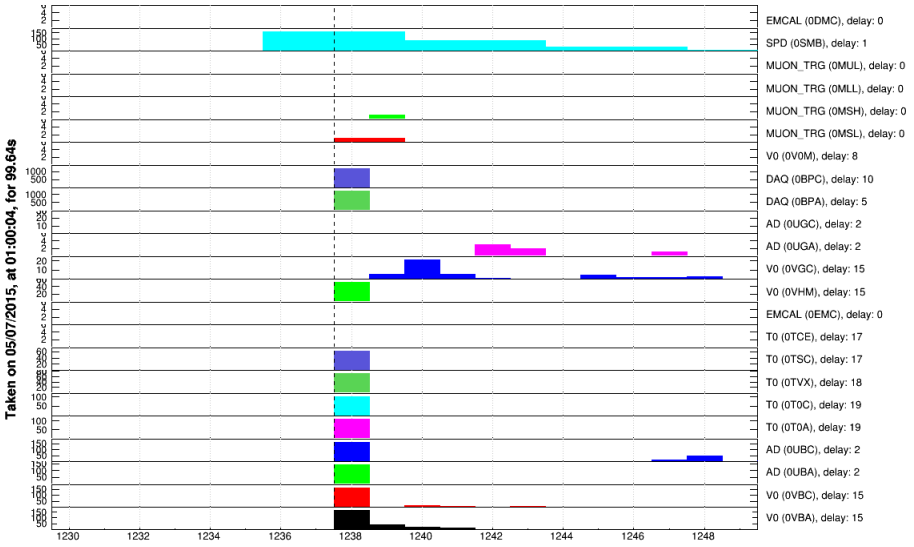
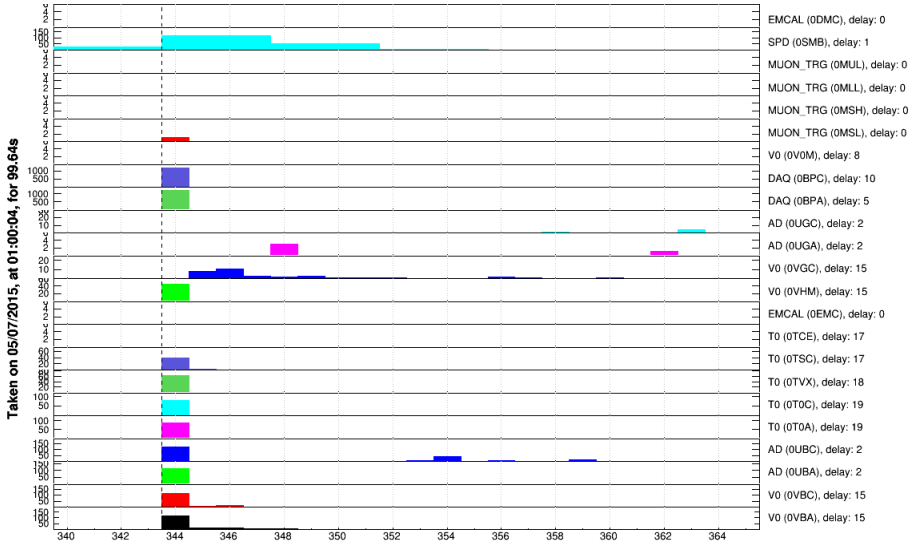
  - Two different checks:
    - Discrete delay (per BC unit)
      → Conclusion: need to delay all the PIT inputs by 1 BC (as concluded in Run1)
    - Fine delay tuning
      - ✓ FINEDELAY1 parameter in LTU configuration
      - ✓ Standard value 14000 ps (measured in Run1)
      - ✓ Best value 8000 ps

Backup

Check of timing configuration

- Timing alignment wrt the other L0 inputs
  - SMAQ plots taken during the runs show 'strange' structure
  - Already present during Run1
  - This is due to the possibility that some chips gives Fats-Or signals for more then 100 ns or to the noise
  - Actually OSMB (TT=1, IT=0, OT=0) is noisy → the long tails are cut away when OSMB is in coincidence with other primitives





Backup

Problem reading registers in the Router

- Issue in readback from LinkRx registers
  - potentially also from other memory devices as DPM and SPM (Error Handler!)
- Analysis of the VME Address Modifier signals treatment
- A non conformity of the firmware with respect to the VME specification
  1) The present VME slave interface implementation can clearly violate the RULE 2.56: "During read cycles, once the responding SLAVE has driven DTACK* lw, it MUST NOT change D00-D31 until DSA* goes high". The driving on the data bus actually changes after a fixed latency from the pulse marking the start of the transaction, i.e. not waiting for the acknowledgement from the MASTER (bus controller).
  2) The read back of the LinkRx version register is actually failing in simulation as well, without any change of the simulated VME timing. The reason is that the DTACK* is asserted when data are not yet stable on the data bus, and it is another non-conformity to the VME protocol! This was probably introduced by a re-timing of the LinkRx data paths.
- Workflow
  - Firmware patches shall be coded and verified in simulation (Gianluca, by Thu 27)
  - New programming files shall be generated with Altera tools (Gianluca, by Fri 28)
  - Reprogramming and testing in DSF shall be done (Marian, Gianluca, Serhiy, by Mon 31 or Tue 1 latest).
  - Installation on P2 Routers shall be done (Domenico, Marian, Gianluca, from Tue 1 onwards, to be scheduled)

Backup

Backup

Backup

Backup