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# The design of a fast Level-1 track trigger for the High Luminosity Upgrade of ATLAS

The high-luminosity upgrade of the LHC will increase the rate of the proton-proton collisions by approximately a factor of 5 with respect to the initial LHC design. The ATLAS experiment will upgrade consequently, increasing its robustness and selectivity in the expected high radiation environment.
In particular, the earliest, hardware based, ATLAS trigger stage ("Level 1") will require higher rejection power, still maintaining efficient selection on many and various physics signatures. The key ingredient is the possibility of extracting tracking information from the brand new full-silicon detector and use it for the decision process. While fascinating, this solution poses a big challenge in the choice of the architecture, due to the reduced latency available at this trigger level (few tens of micro-seconds) and the high expected working rates (order of MHz).
In this paper, we review the design possibilities of such a system in a potential new trigger and readout architecture, and present the performance resulting from a detailed simulation of possible hardware-based algorithms, to be implemented in the context of Associative Memories and FPGA technologies, as foreseen by R&D
plans on these devices.

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