The CMS

Timing *and*
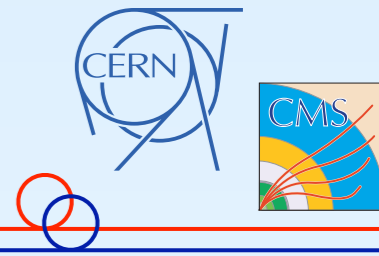# **C**ontrol
Distribution
System

J. Troska

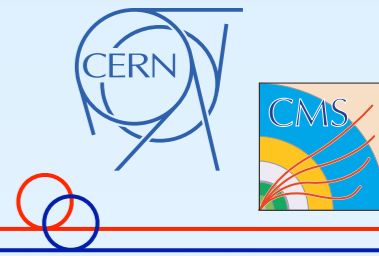*M. Hansen, J. Hegeman, F. Meijers, P. Vichoudis*
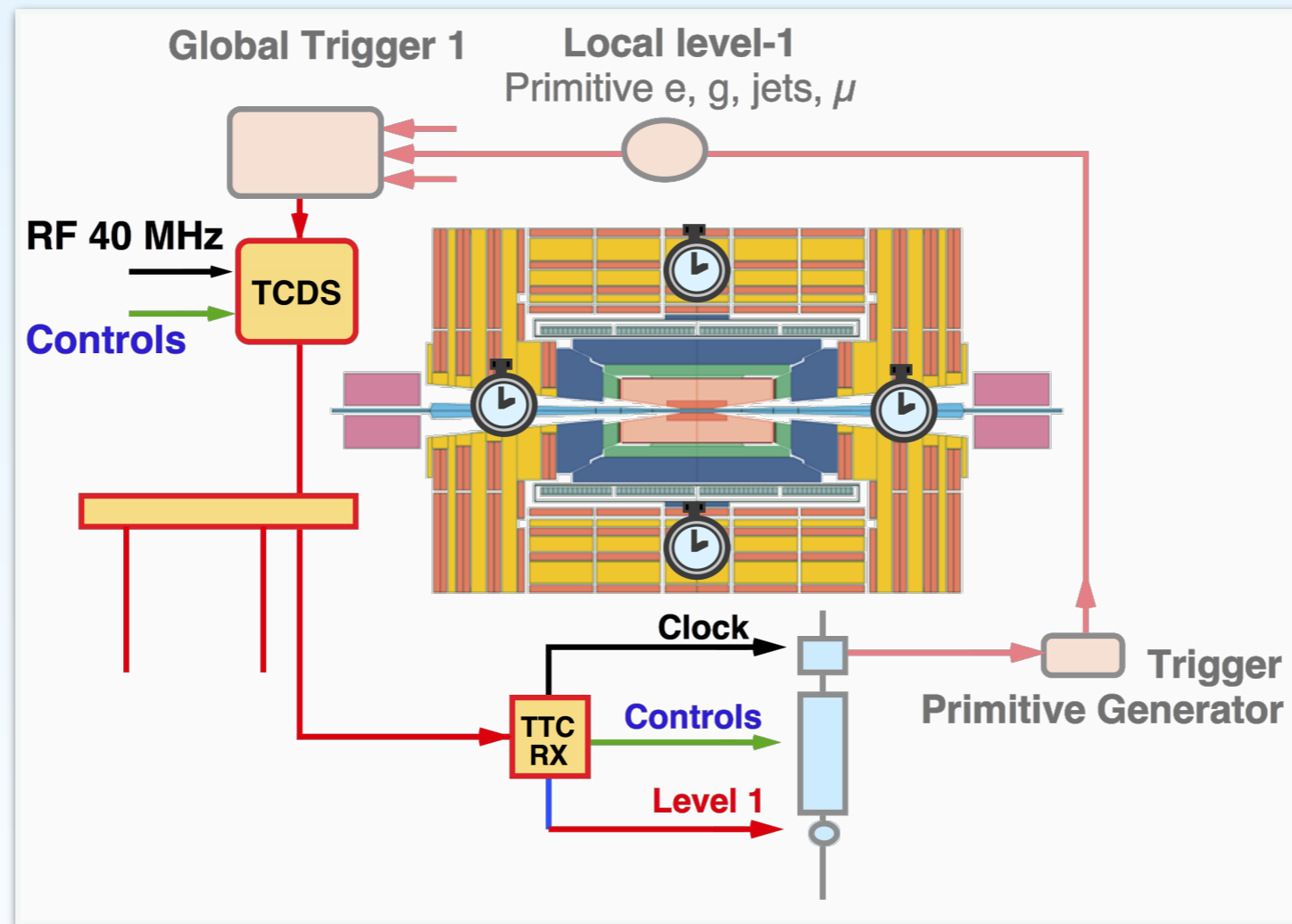*CERN-PH-ESE & CERN-PH-CMD*

Overview

- Introduction to the CMS TCDS system
- Elements of the system
- System performance
- Operational experience
- Summary

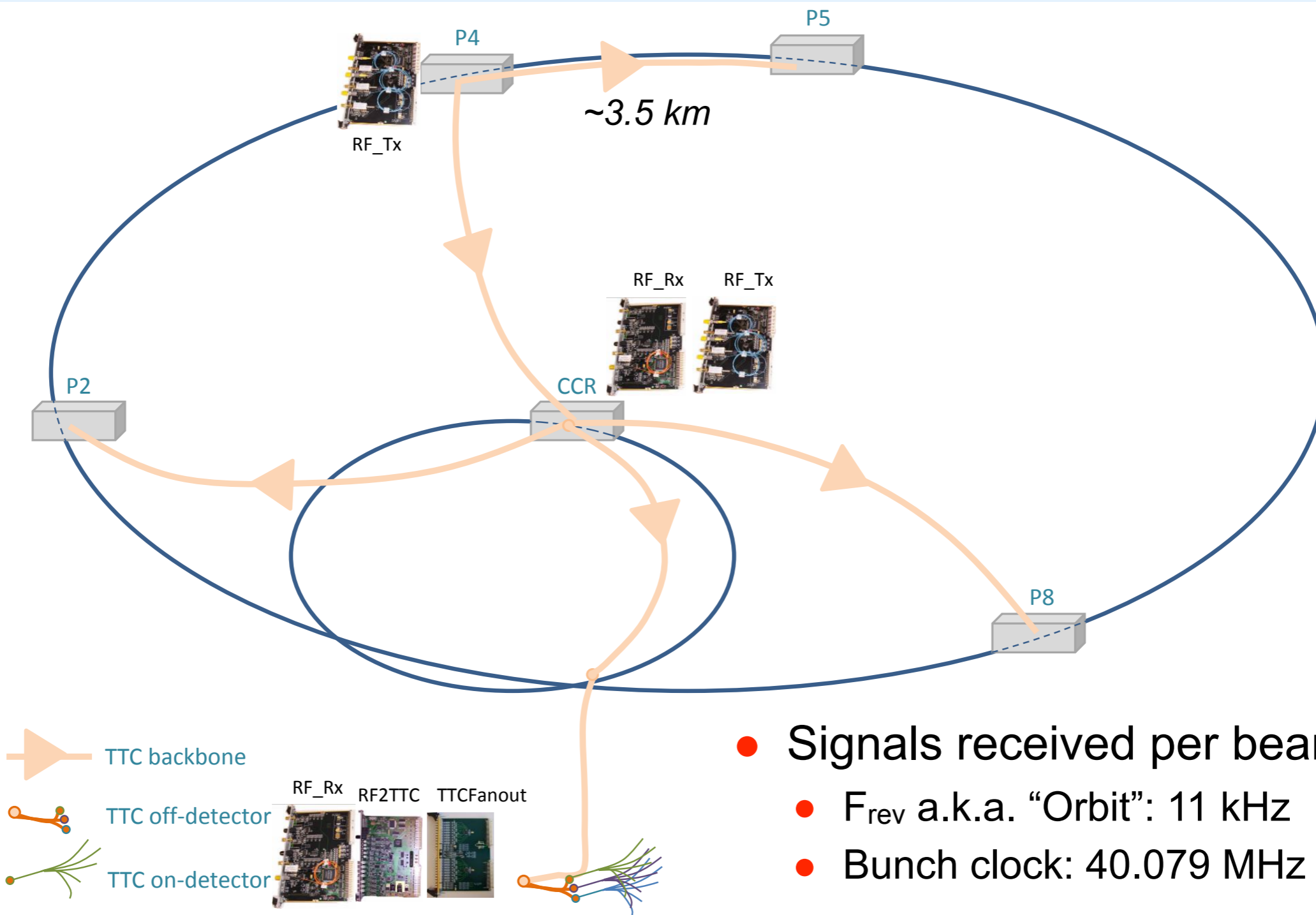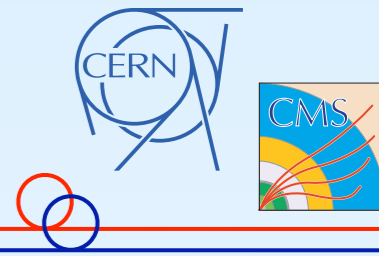# Timing distribution introduction

- ## Historical perspective:

- ## LHC collision rate: 40 MHz

- ## CMS Level 1 Trigger rate: 100kHz

- ## CMS Level 1 Latency: 3.2 µs
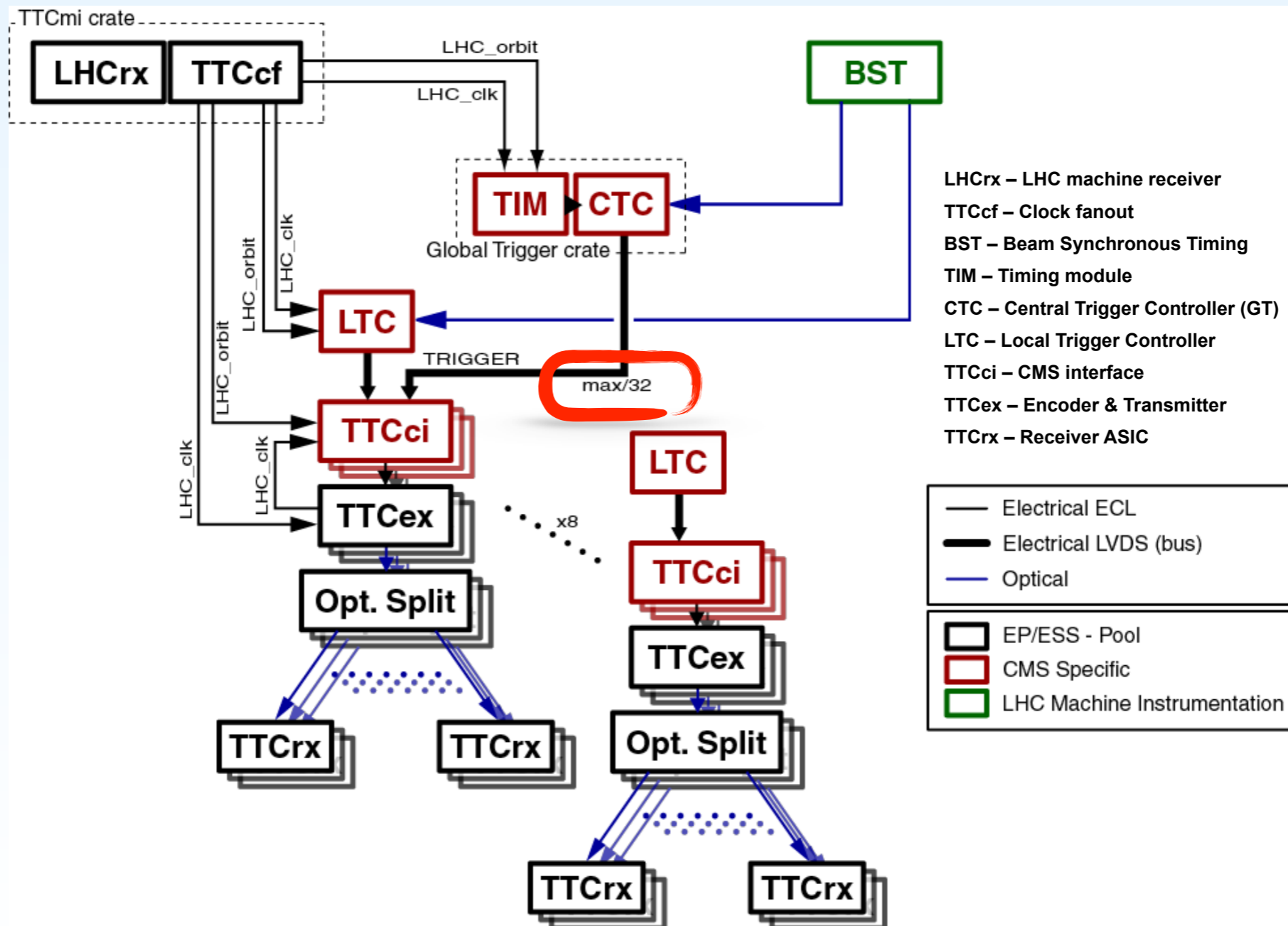
RF reference signals

~3.5 km

- Signals received per beam:
  - F_{rev} a.k.a. "Orbit": 11 kHz
  - Bunch clock: 40.079 MHz

TTC backbone
TTC off-detector
TTC on-detector

RF_Tx
RF_Rx   RF_Tx
CCR
P4
P5
P2
P8

RF_Rx   RF2TTC   TTCFanout

PH-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS

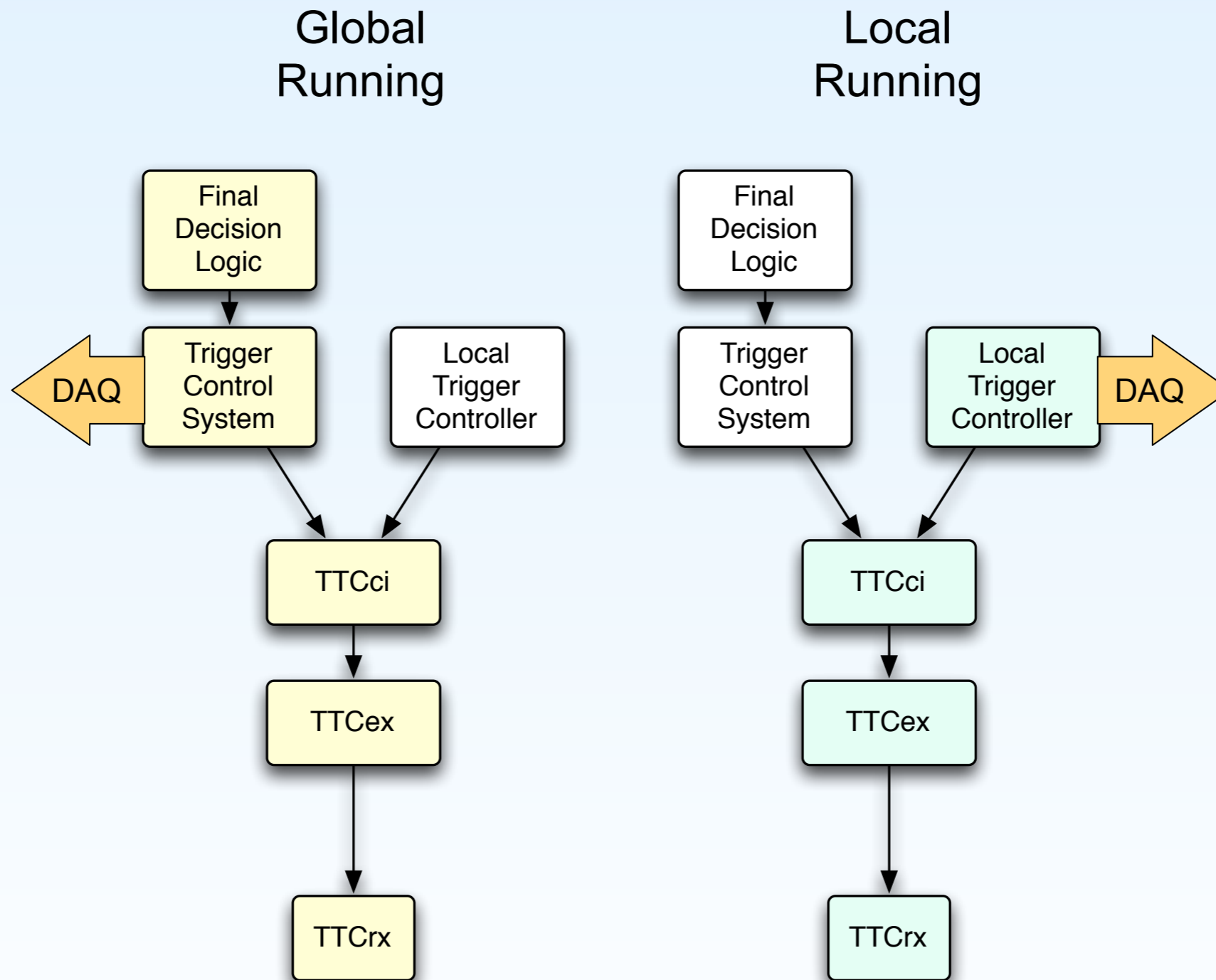*after https://indico.cern.ch/event/202454/*

4

CMS Timing system for Run 1

- ● Based upon RD12 TTC system
  - ● CMS-specific interface module (TTCci)

Signal Distribution only

LHCrx – LHC machine receiver
TTCcf – Clock fanout
BST – Beam Synchronous Timing
TIM – Timing module
CTC – Central Trigger Controller (GT)
LTC – Local Trigger Controller
TTCci – CMS interface
TTCex – Encoder & Transmitter
TTCrx – Receiver ASIC
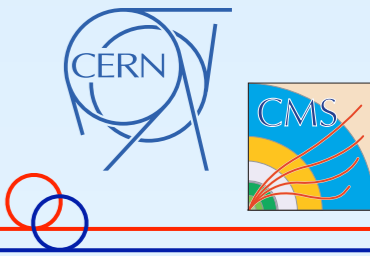
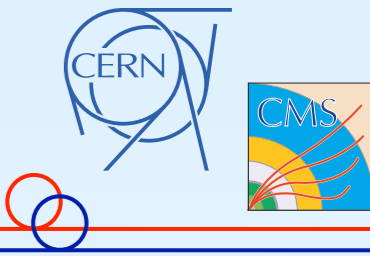# Operation of Run 1 system
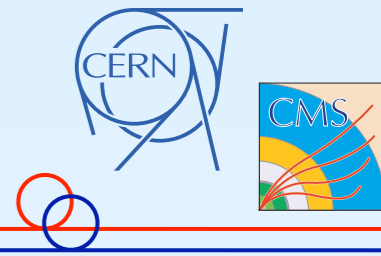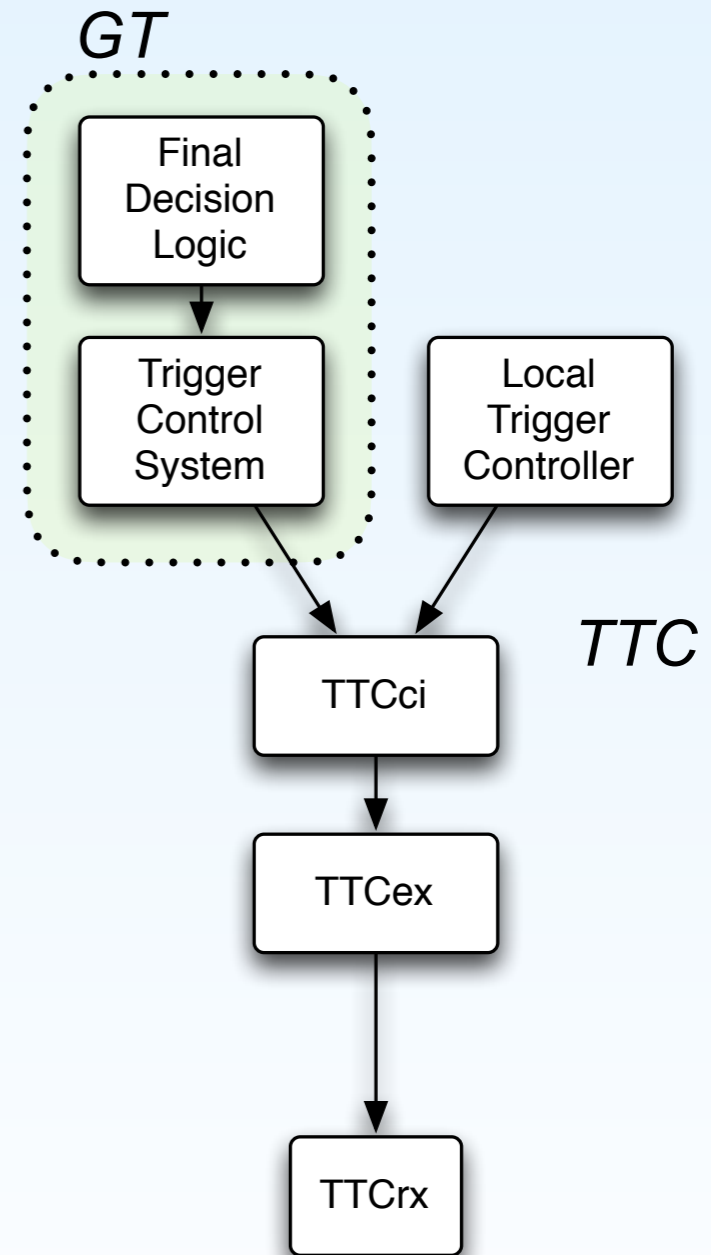
Why replace the timing distribution?

- CMS did not have enough partitions available in the existing system to service all requests coming out of LS1
    - 40 partitions requested
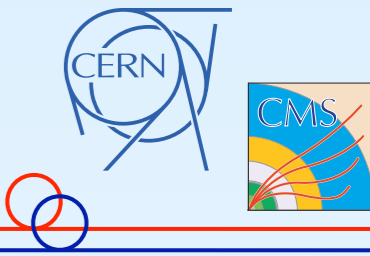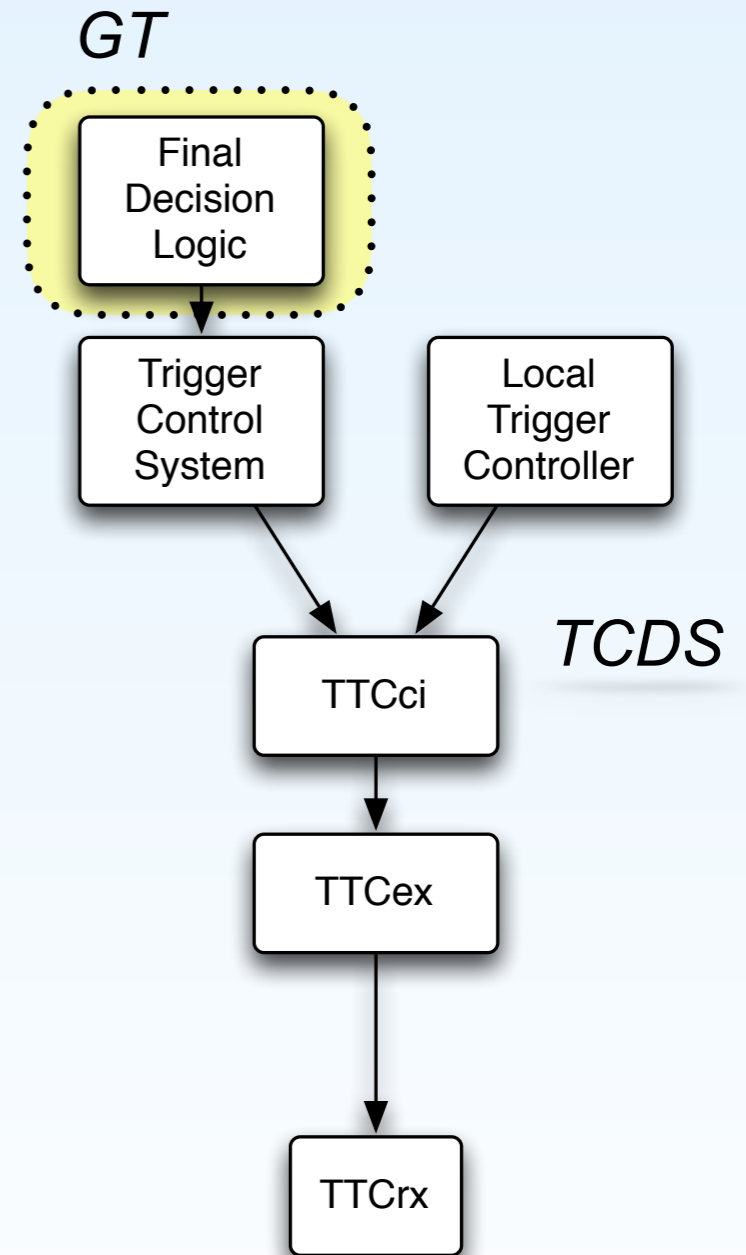
Why replace the timing distribution?

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  - 40 partitions requested

- Upgrade of CMS Global Trigger provided opportunity to revisit functional split
  - Physics Event Selection (FINOR)
  - Trigger Control System
  - Trigger and Timing Distribution

GT

Final Decision Logic

Trigger Control System

Local Trigger Controller

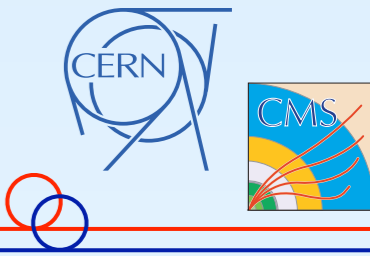TTCci

TTC

TTCex

TTCrx

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  - 40 partitions requested

- Upgrade of CMS Global Trigger provided opportunity to revisit functional split
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 - Trigger and Timing Distribution

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  - Physics Event Selection (FINOR)
  - Trigger Control System
  - Trigger and Timing Distribution

- Upgrade provided opportunity for new functionality
  - LumiDAQ synchronization
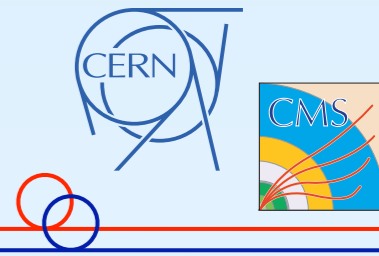 - New Trigger rules, B-Gos

GT

Final Decision Logic

Trigger Control System

Local Trigger Controller

TCDS

TTCci

TTCex

TTCrx
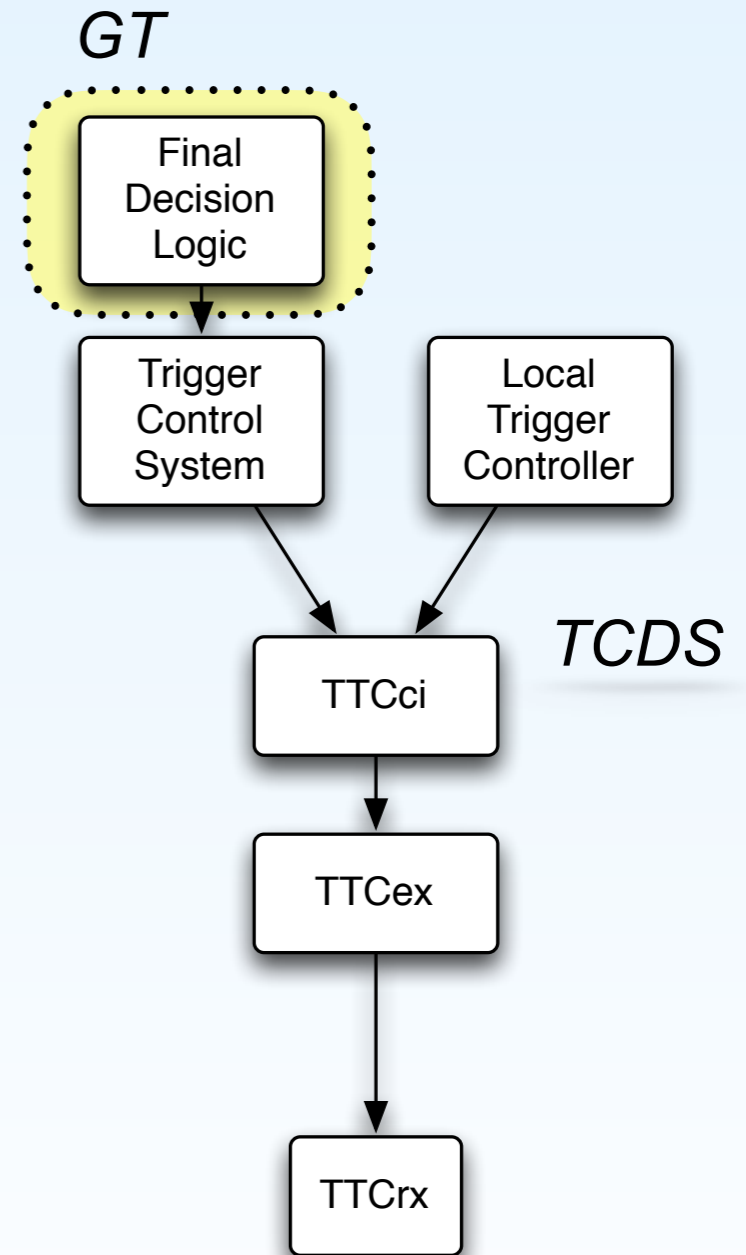
Basic ingredients for LS1 upgrade
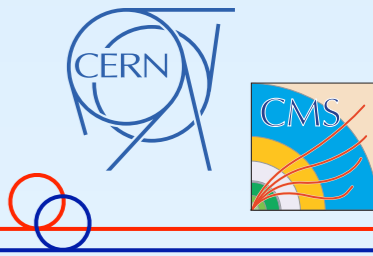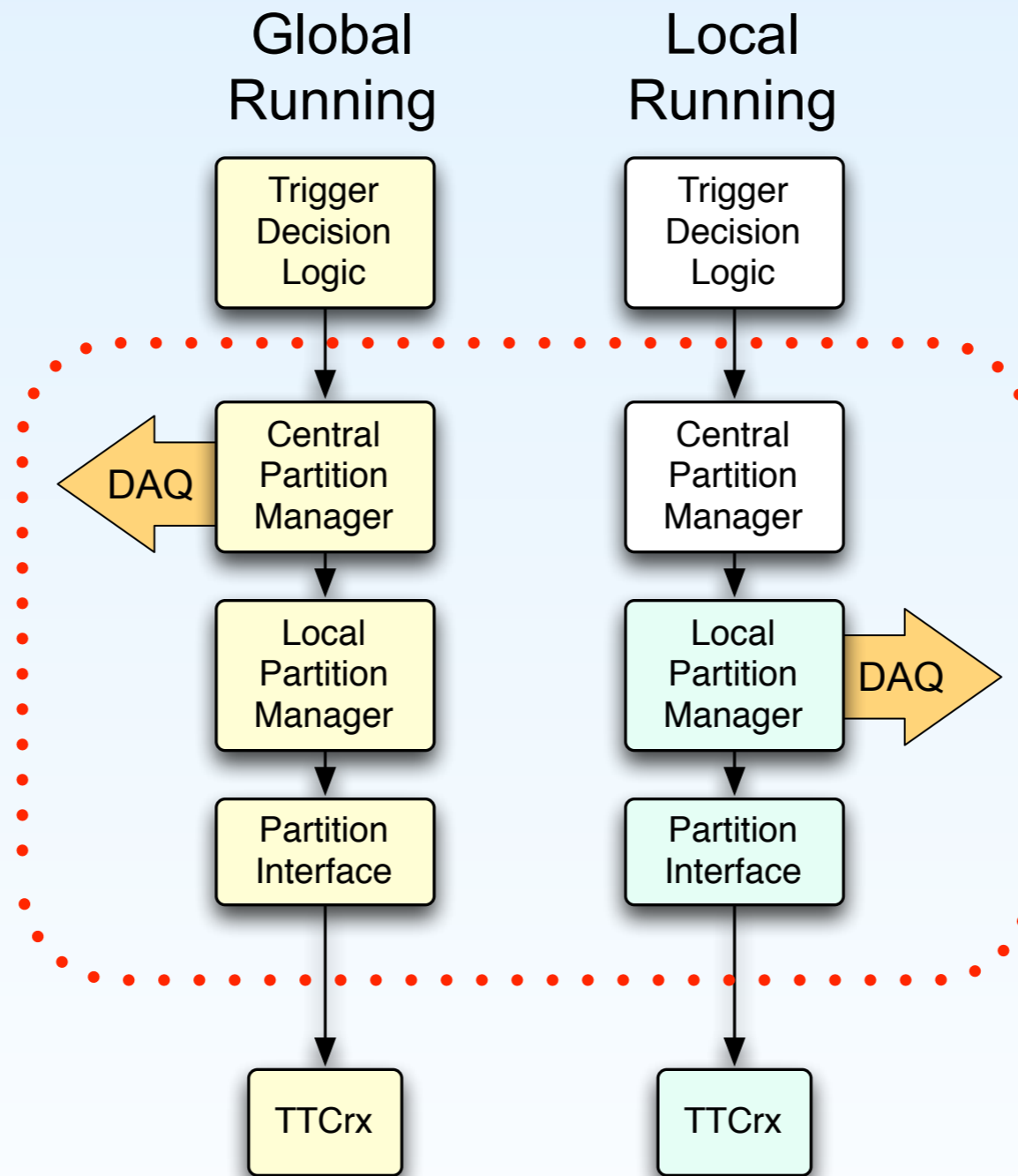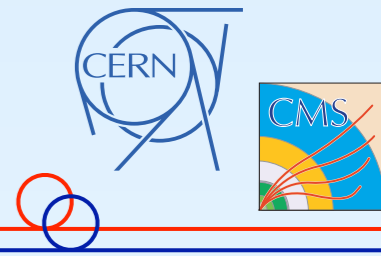
- μTCA system
  - Opportunity to exploit the use of backplane for distribution of synchronisation signals

- Larger, more modern, FPGAs
  - Kintex 7 series
  - More logic resources
  - Std i/o up to Gb/s
  - High-speed serial i/o up to 10 Gb/s

- Common AMC designs used in multiple CMS systems
  - FC7, AMC13
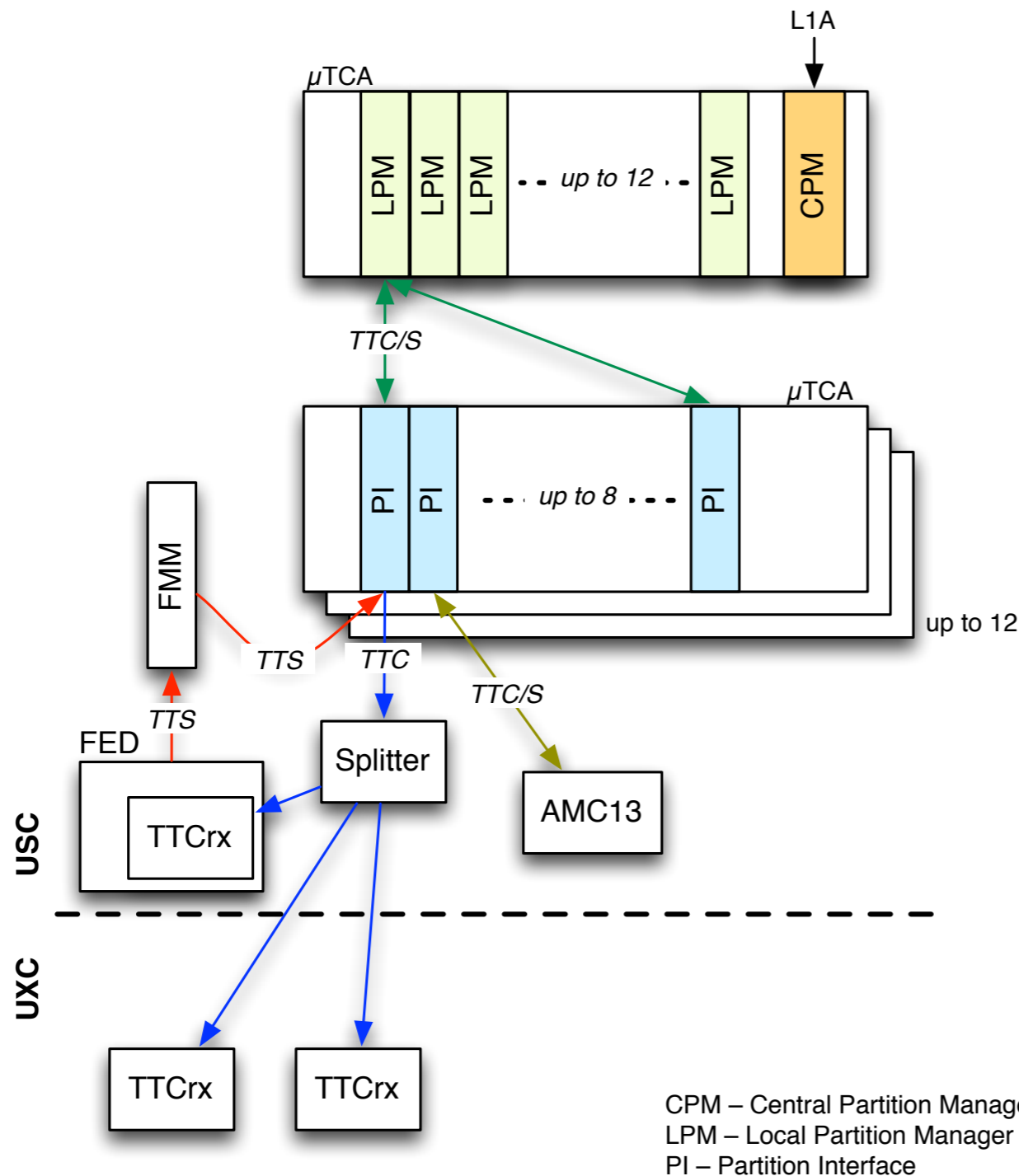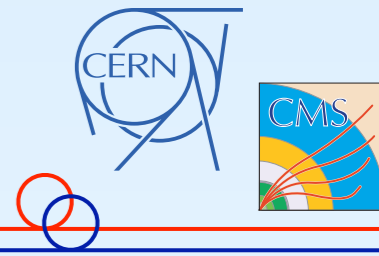 - Customized "only" i/o FMCs and firmware

TCDS system Board overview

Takes Functionality of TCS

Combines Functionality of LTC and TTCci

Bi-directional TTCex and FMM
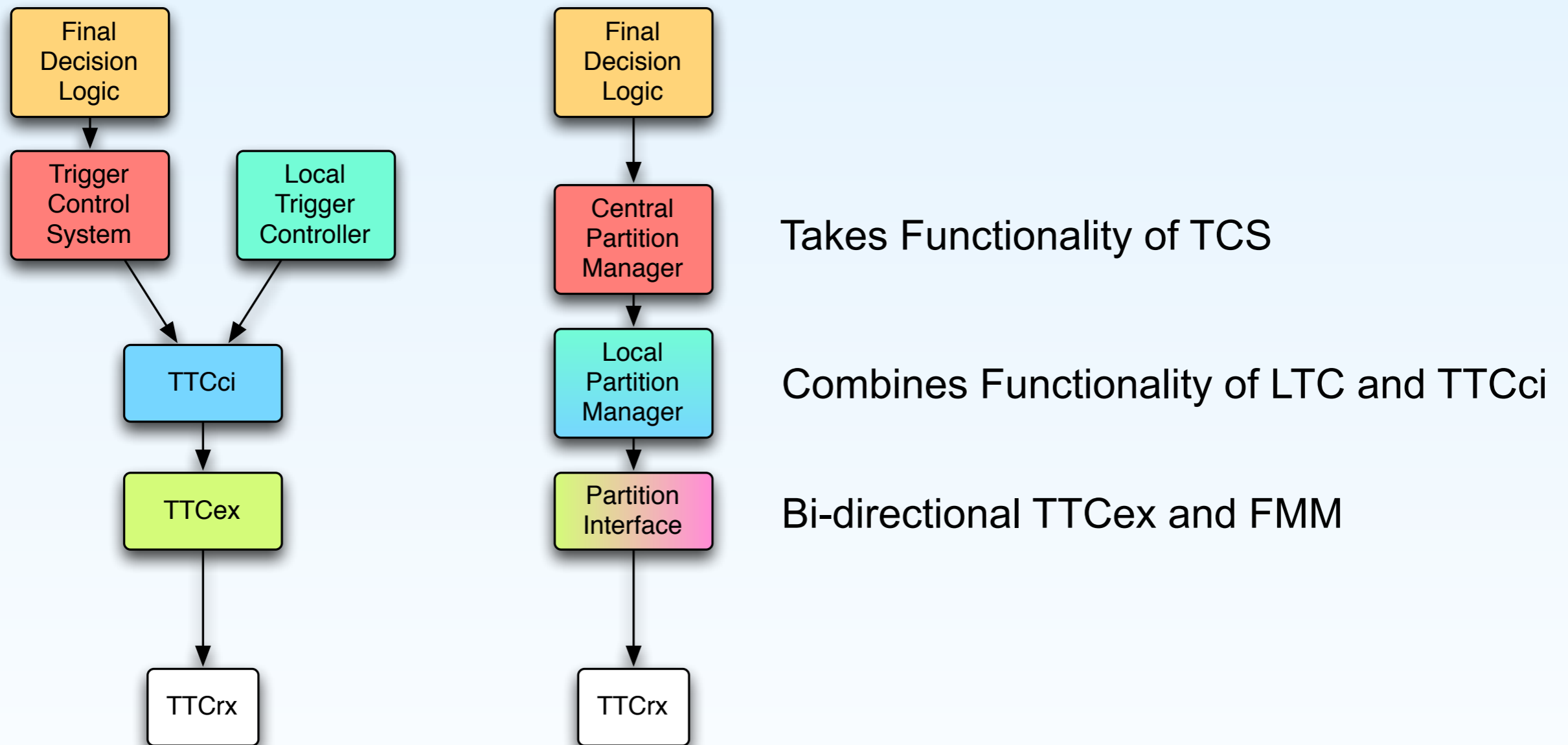
TCDS leverages µTCA backplane comms

TCDS System Operation

TCDS System Diagram

- Overall system can have
  - Up to 12x LPMs
  - Up to 8x PIs per LPM
  - Total 96 partitions
- It is possible to add a redundant PM crate
  - For debugging, (sub-) system commissioning
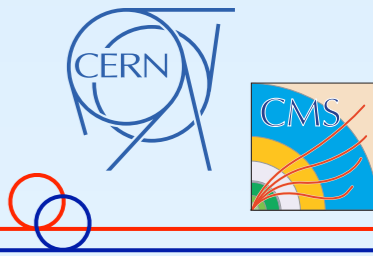
AMC13 – CMS μTCA readout board

FMM – Fast Merging Module

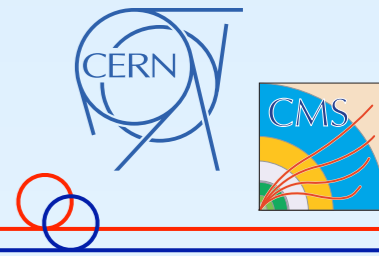|	
CPM – Central Partition Manager	TTC – Timing, Trigger & Control
LPM – Local Partition Manager	TTCrx – TTC Receiver ASIC
PI – Partition Interface	TTS – Trigger Throttling System

Overview

● Introduction to the CMS TCDS system

● **Elements of the system**

● System performance

● Operational experience

● Summary

Implementation: AMCs

- Based as far as possible on existing or already in development hardware
  - Double-width AMC: FC7
  - Single-width AMC and "crate controller": AMC13

# Implementation: mezzanine boards

- Both FC7 and AMC13 customised through the addition of mezzanine boards

- FMCs for FC7
  - 8x SFP connected to FMC std. i/o for distribution of timing signals and reception of front-end status (TTS)
  - 4x SFP & 1x RJ45 connected to FMC std. i/o for distribution of timing signals and reception of front-end status (TTS)
  - 6x Lemo for clock, orbit, and local trigger inputs; plus 2x SFP+ connected to SerDes for DAQ interface

- Tongue-3 mezzanine for AMC13
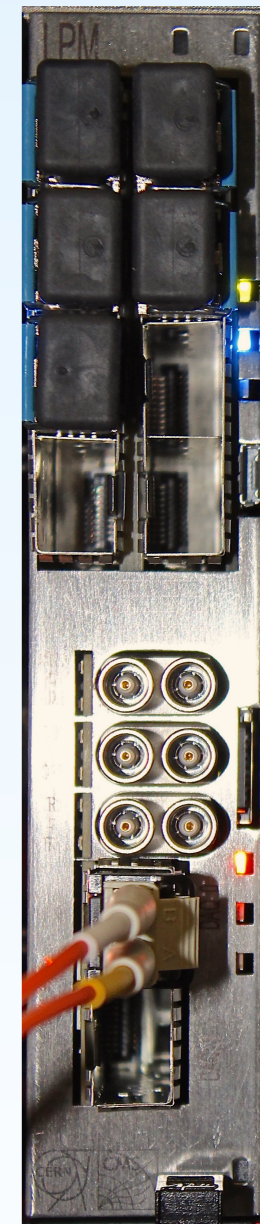 - 6x Lemo for clock, orbit, and trigger inputs, debug output

Finished AMCs

FC7 as LPM

FC7 as PI

AMC13 as CPM

Ancillary Parts
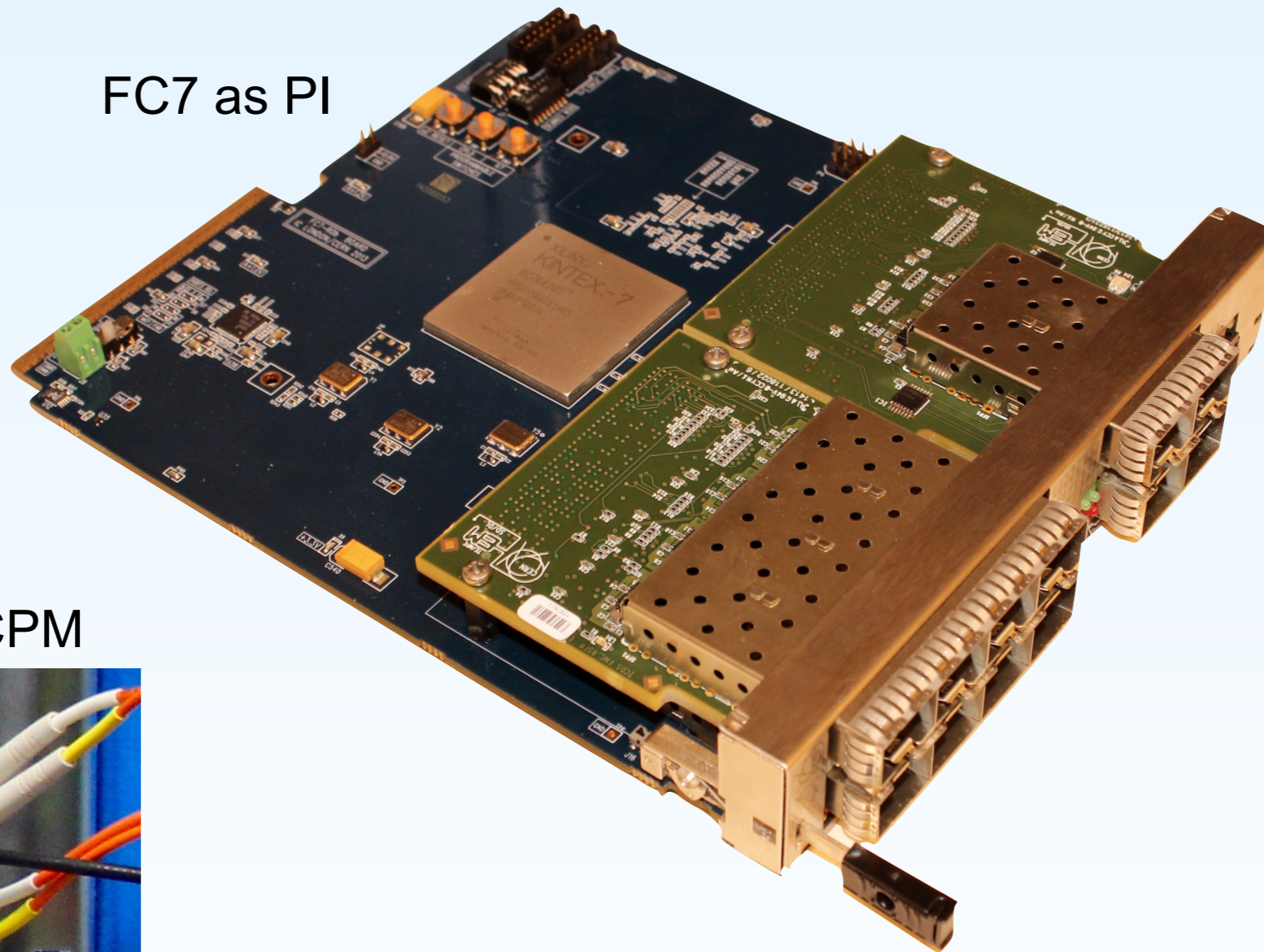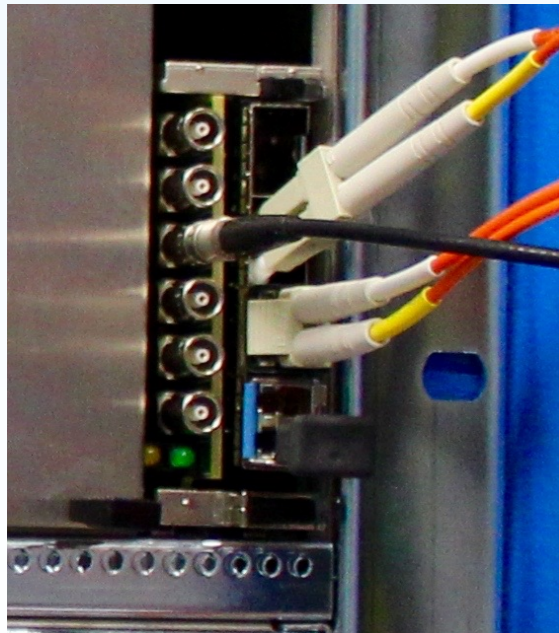
- μTCA chassis from Schroff
  - Custom development for redundant powering at full AMC power
  - 2x front-facing & 4x rear-facing Power Module (PM) slots
  - 12x full-height, double-width AMC slots
  - 2x redundant MCH slots
- μTCA PMs (NAT-DC-840)
  - 48 V DC input, 840 W per module
  - using 2 PMs per chassis
- μTCA MCH (NAT-MCH)
  - Basic version, no additional switch- or clocking modules
- AC-DC converter (PowerOne Aspiro)
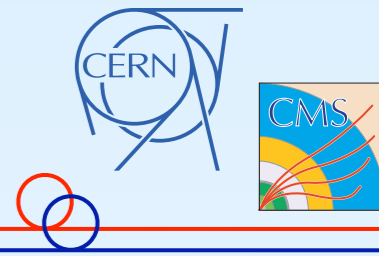 - 4x converter modules enabling 1 in 3 redundancy

Installed system
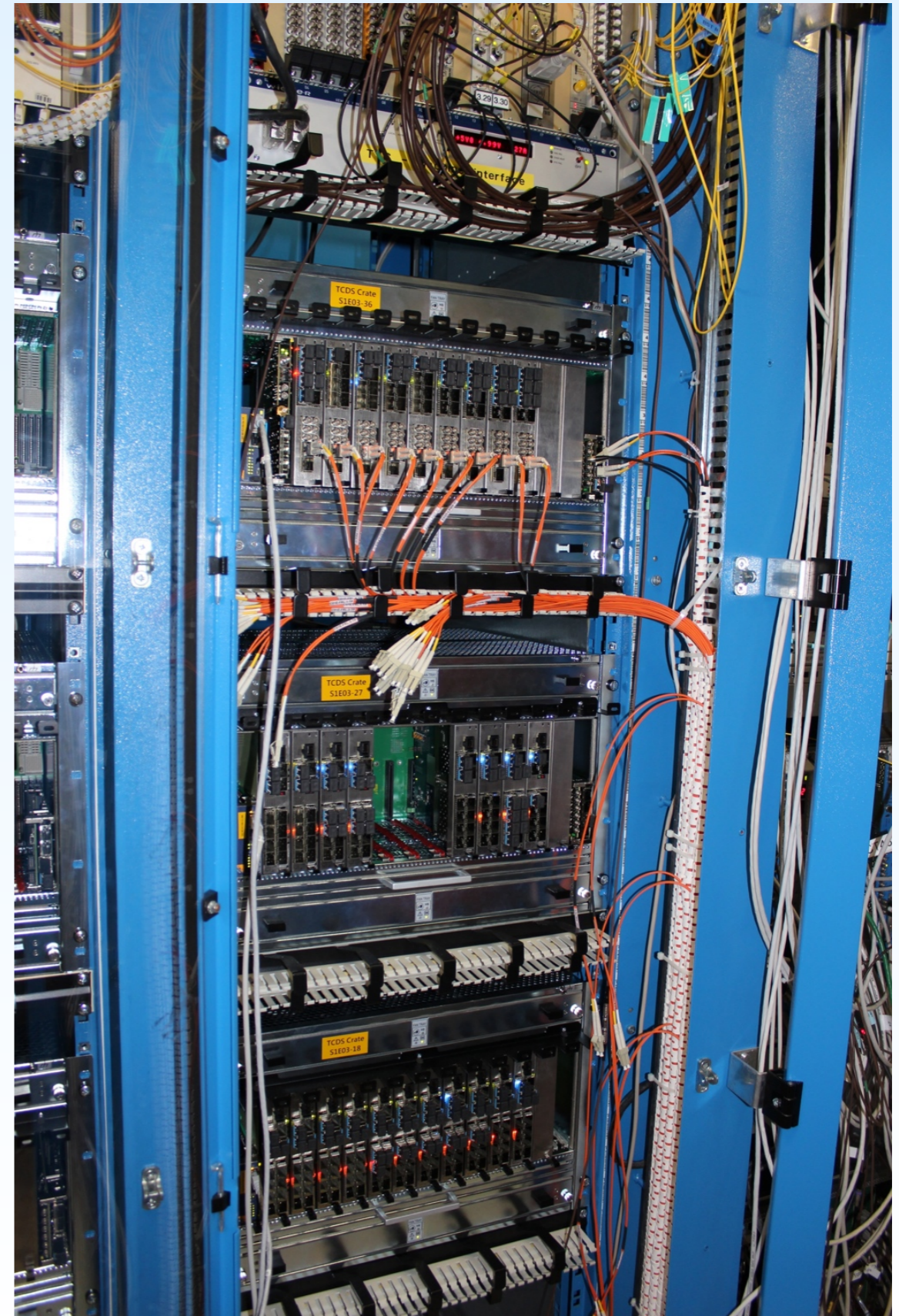
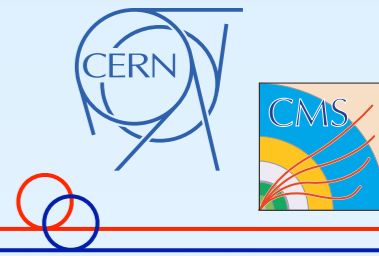# Installed system
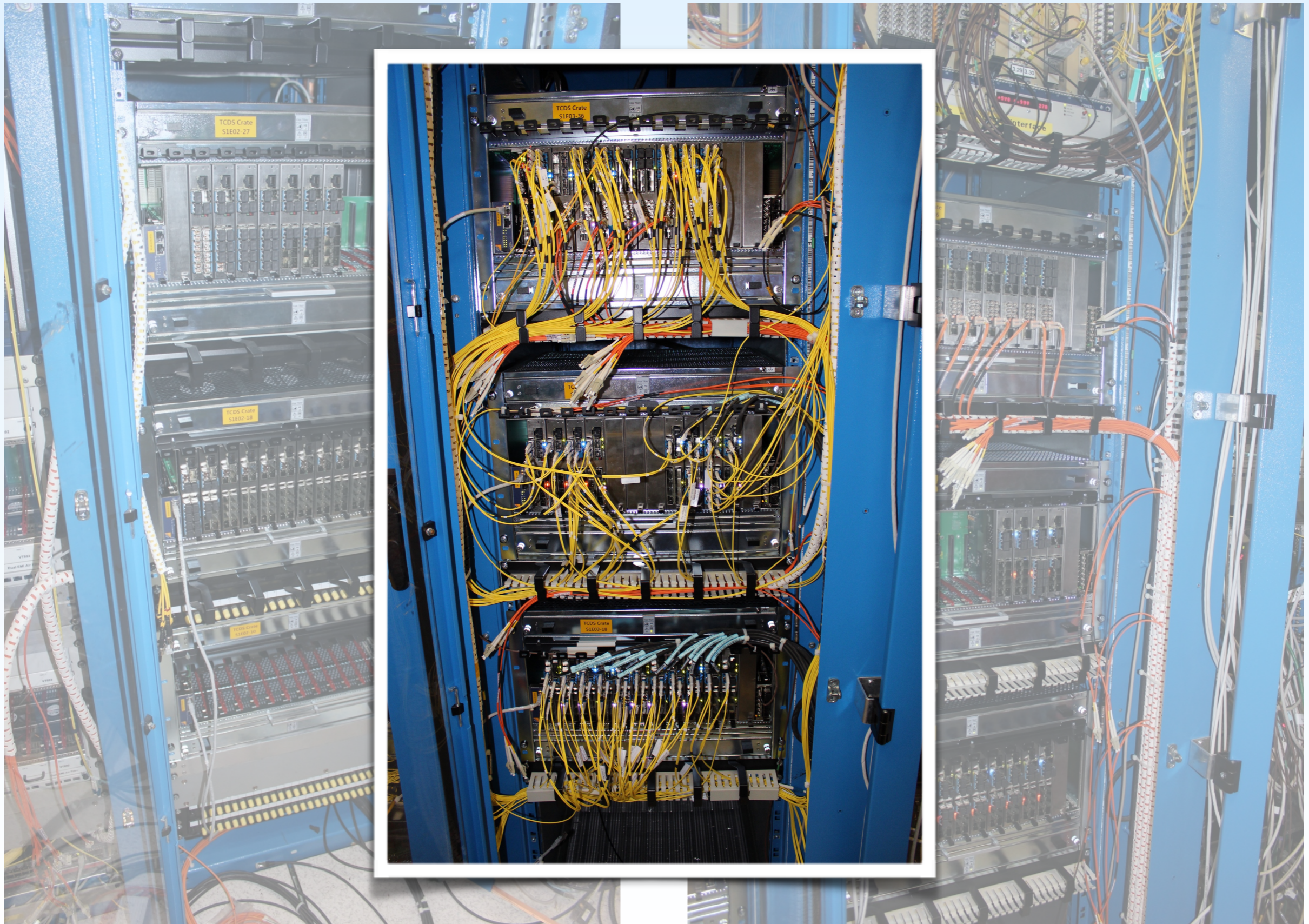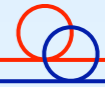
Firmware overview

- Make use of common f/w modules across whole project
  - Partition Manager (PM)
  - CMS Interface (iCi) from Run 1 TTC
  - Core library containing generators, DAQ interface, etc.
- Board-specific f/w (CPM, LPM, PI) built on top of this
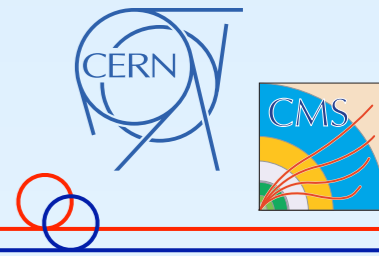- Allows similar and thus simplified mapping to control software
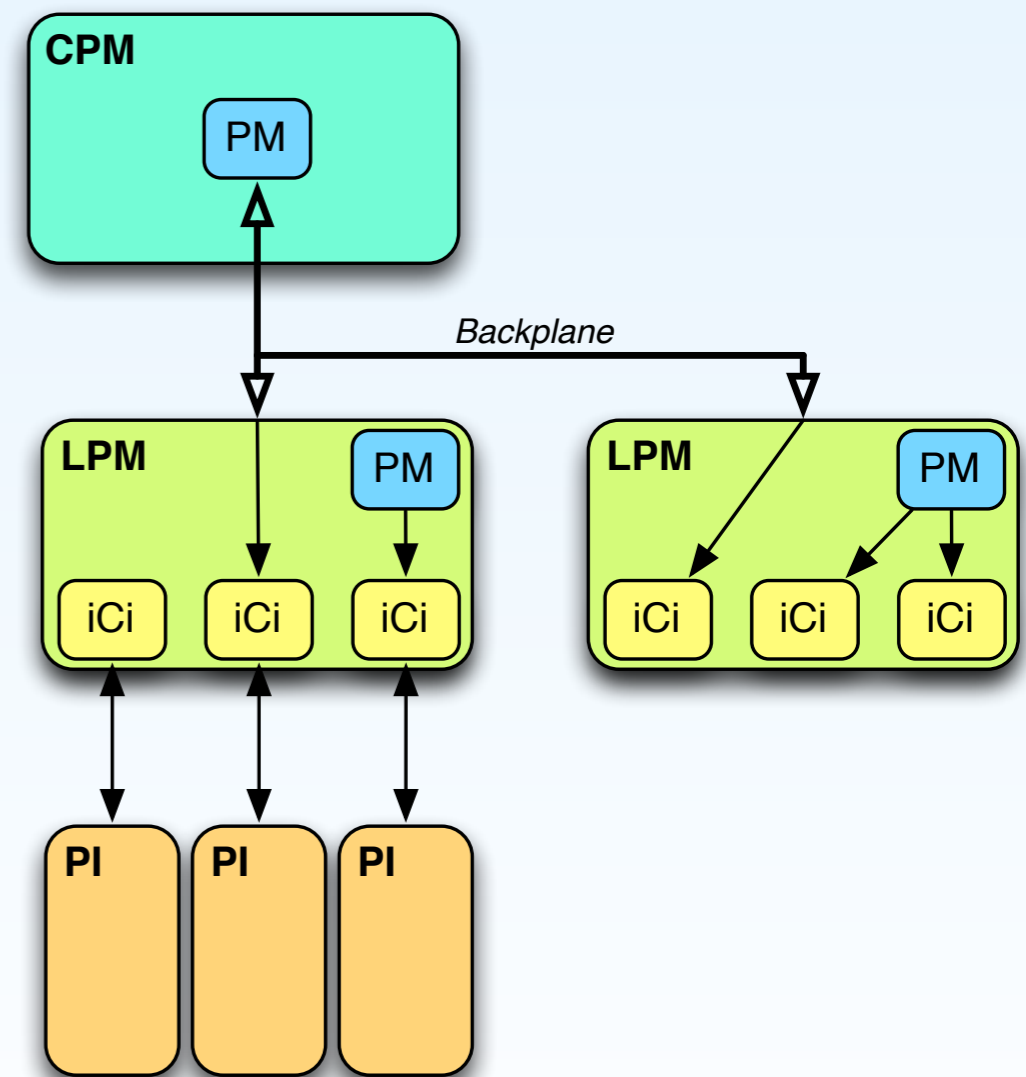
Control software

- **TCDS control software**
  - Based on the CMS XDAQ online software framework
  - TCDS 'sub-framework' developed
    - Provides uniform look and feel
    - Abstracts away hardware details from the application level

- **Division of labour**
  - Each TCDS component has a corresponding software component, implemented as a linux service
  - Service applications maintained centrally
  - CMS RunControl takes care of Partition Manager configuration
  - Subsystems maintain full control of the configuration of 'their' iCIs and PIs (via SOAP)
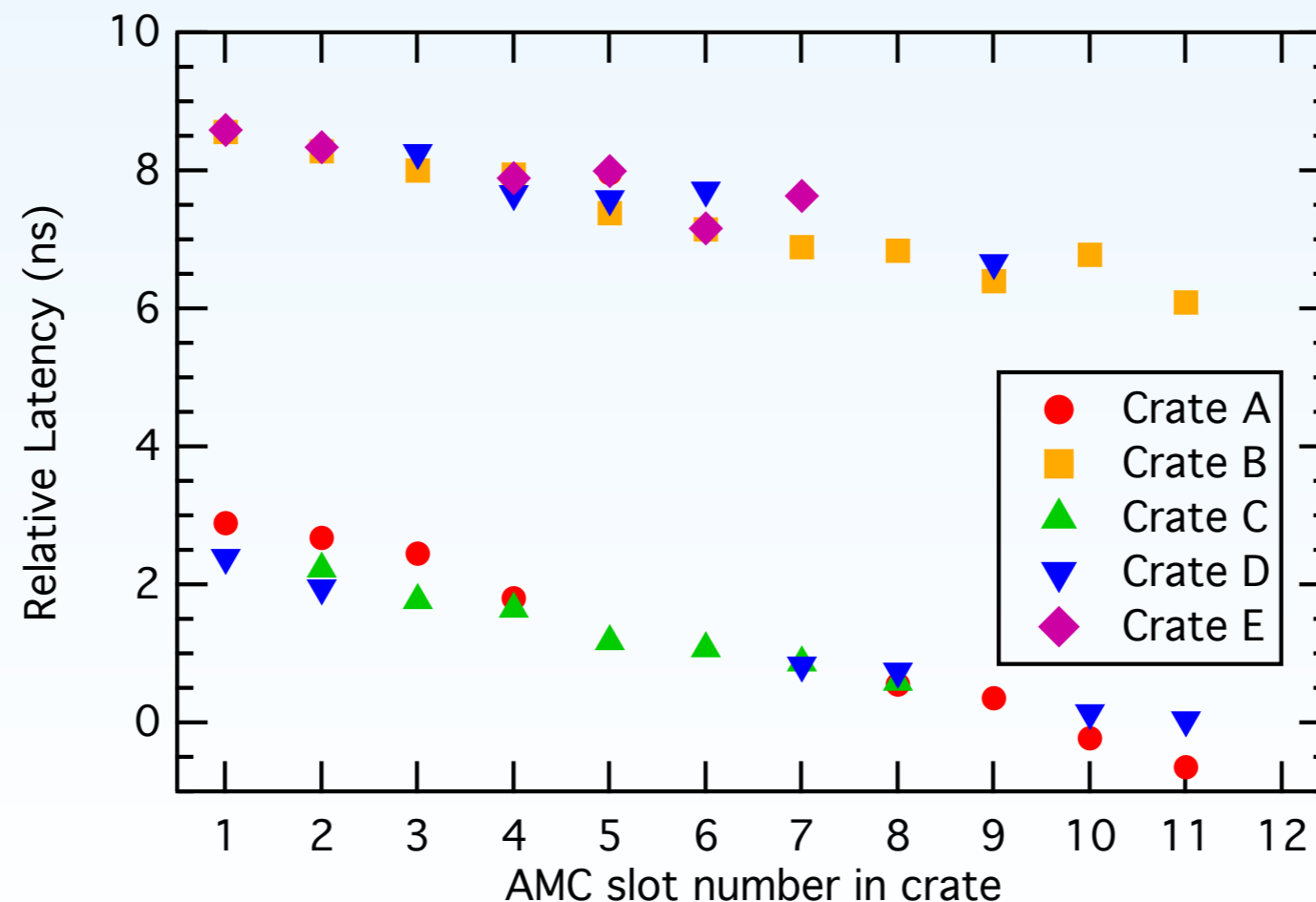
Overview

- Introduction to the CMS TCDS system

- Elements of the system

- System performance
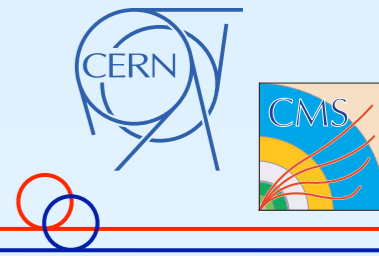
- Operational experience

- Summary

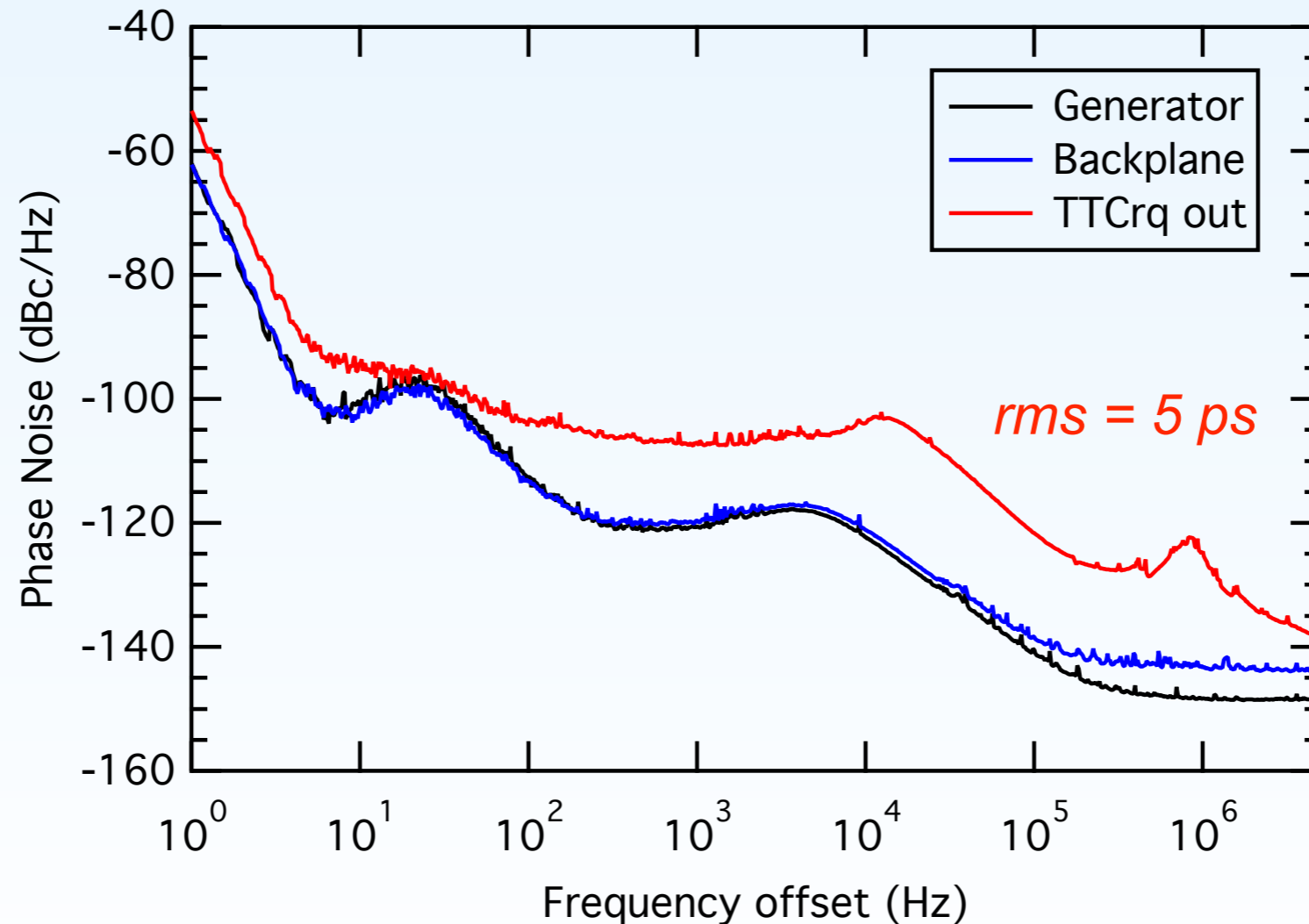# System performance: latency

- Overall CMS trigger latency after TCDS system integration increased by 2 bx
  - Extra latency required to communicate signal between GT and TCDS
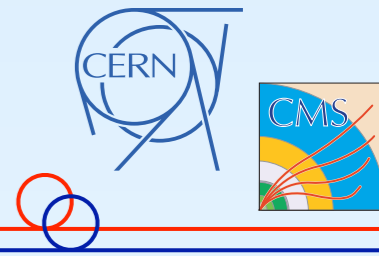- Good uniformity across all partitions
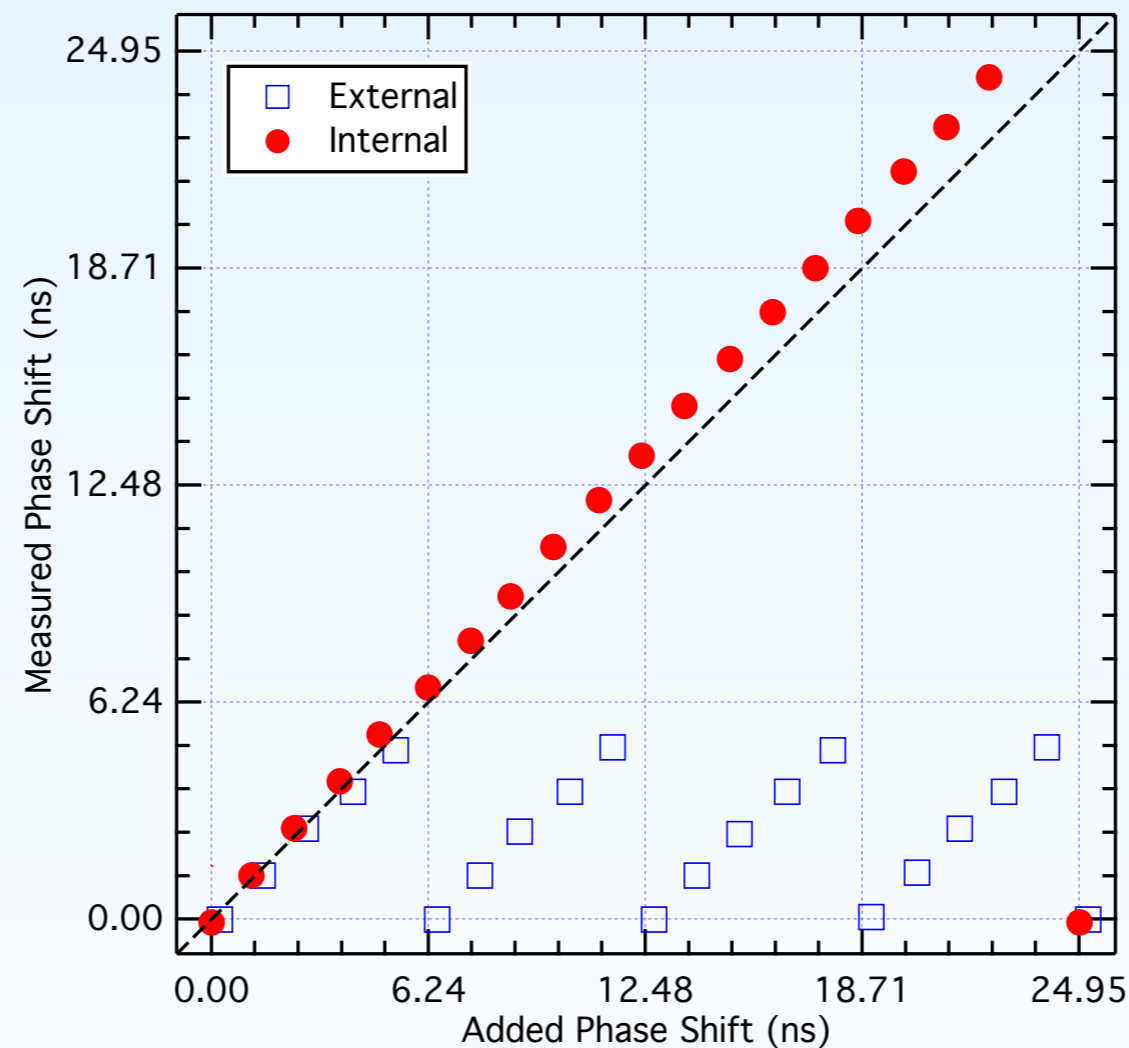
System performance: Jitter

- System jitter performance not degraded by TCDS system
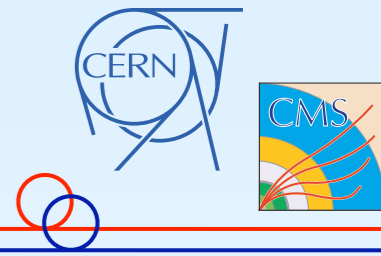 - Dominated by TTCrx/QPLL

System monitoring: Phase

- Concern over FPGA internal PLL phase stability
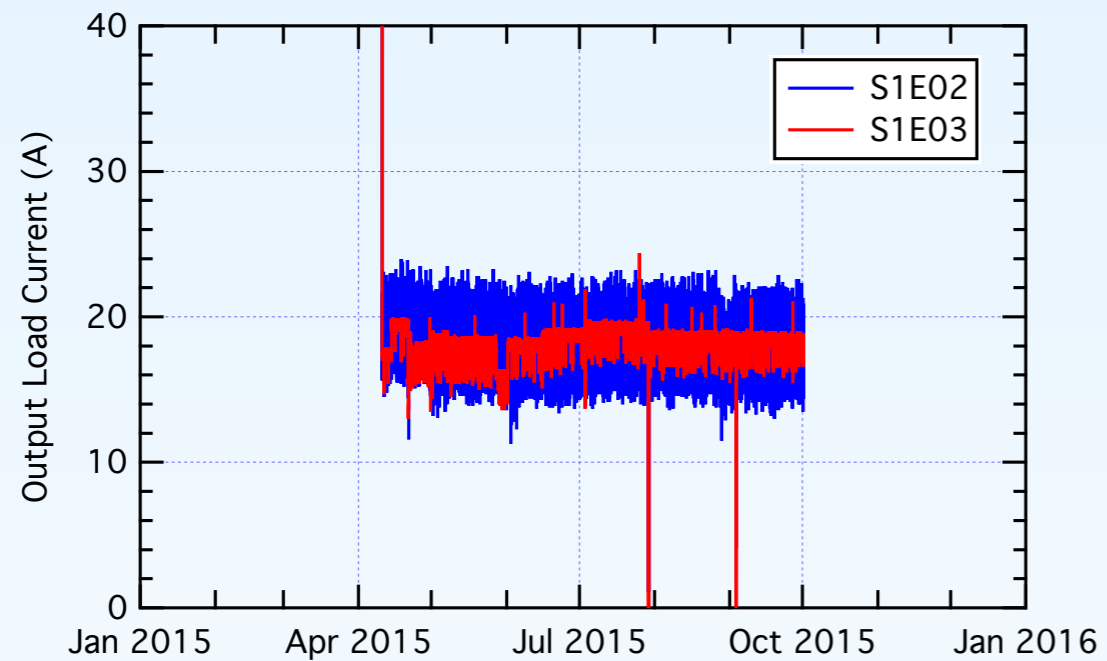 - Implemented internal phase measuring circuit

- Comparison to external measurement rather good
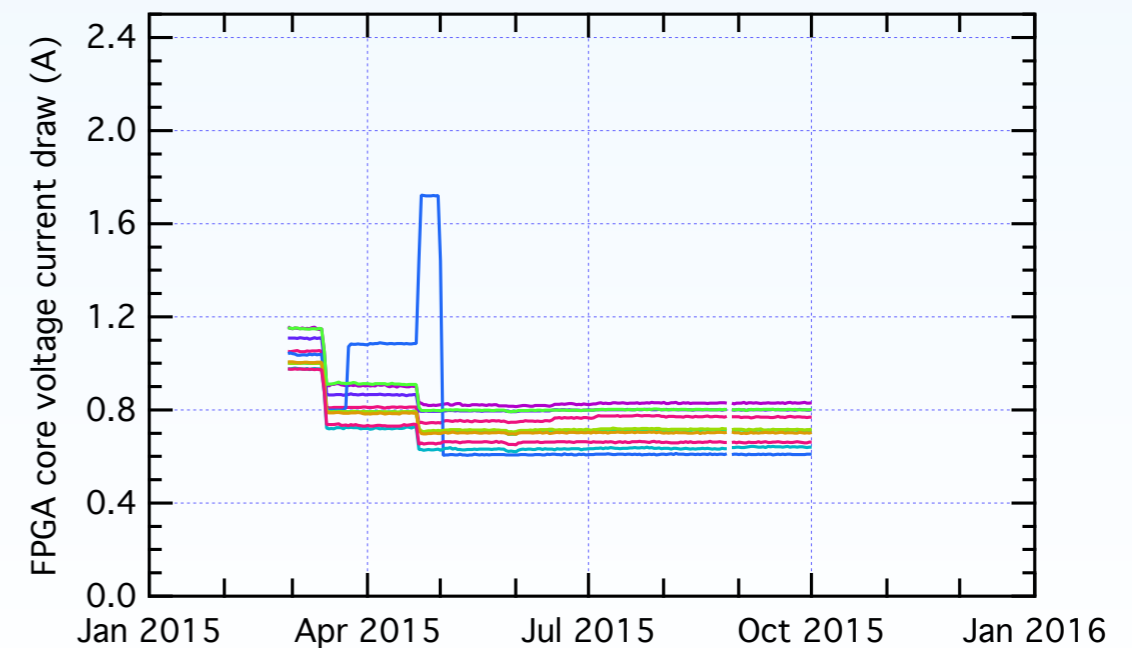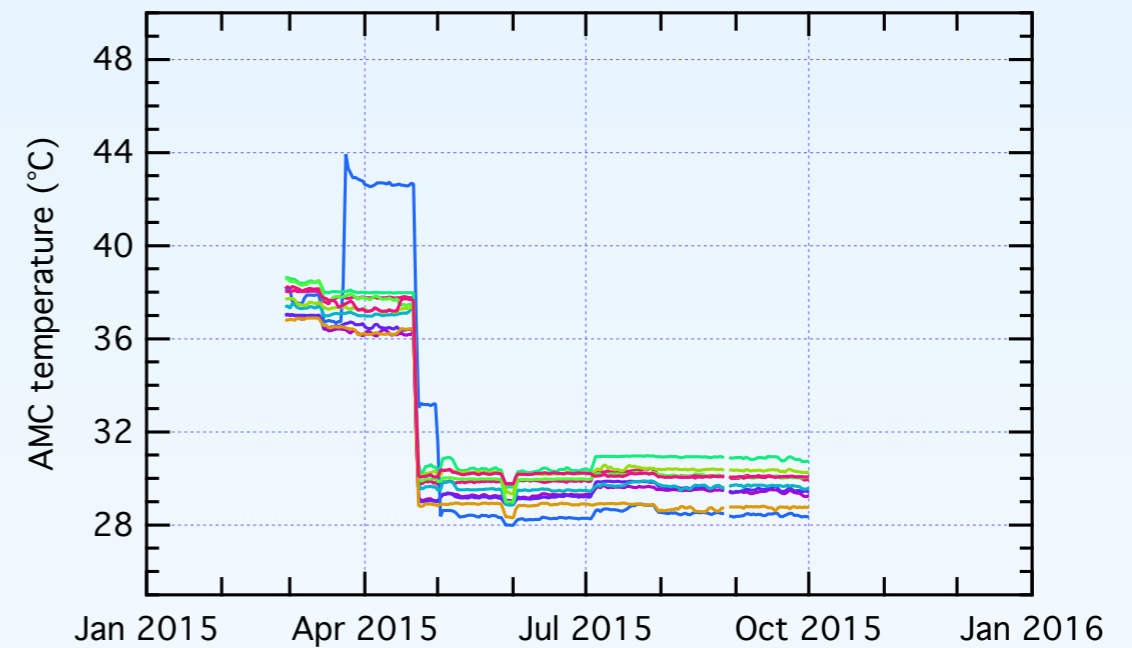 - External measurement only sees up to 1/4 period (TTC stream at 160 Mb/s)

System health monitoring

AC/DC Converters

AMC Sensors

Overview

- Introduction to the CMS TCDS system

- Elements of the system

- System performance

- Operational experience

- Summary

Operational experience

- The CMS TCDS system sustained a very high failure rate of AMCs after ~3 months of operation
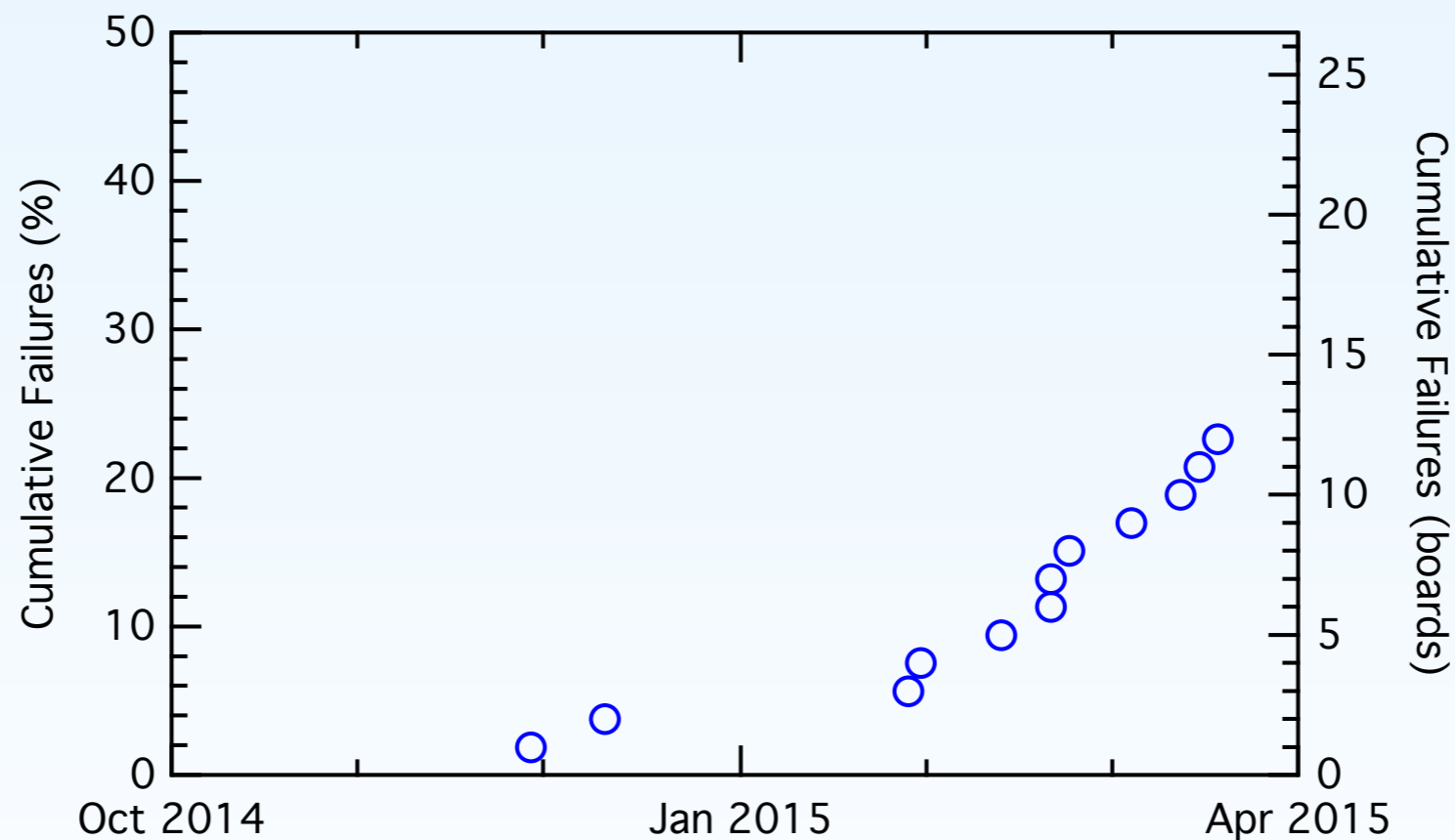
FC7 failure monitoring

- **AMC sensors provided diagnostics**
  - Board failure accompanied with increased current drawn on FPGA core voltage

- **Increased current an abrupt failure**
  - within one monitoring interval (1 minute)

Failure analysis

- Lengthy investigations inc. Failure analysis by Xilinx on failed FPGAs

  - Schematic error identified - incorrect XADC supply voltage caused EOS failure of configuration memory

4x close up image of hotspot by thermal emission.
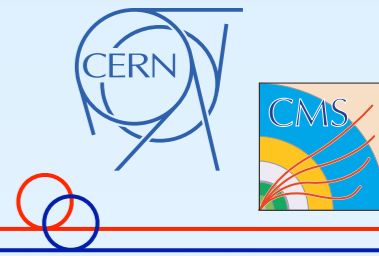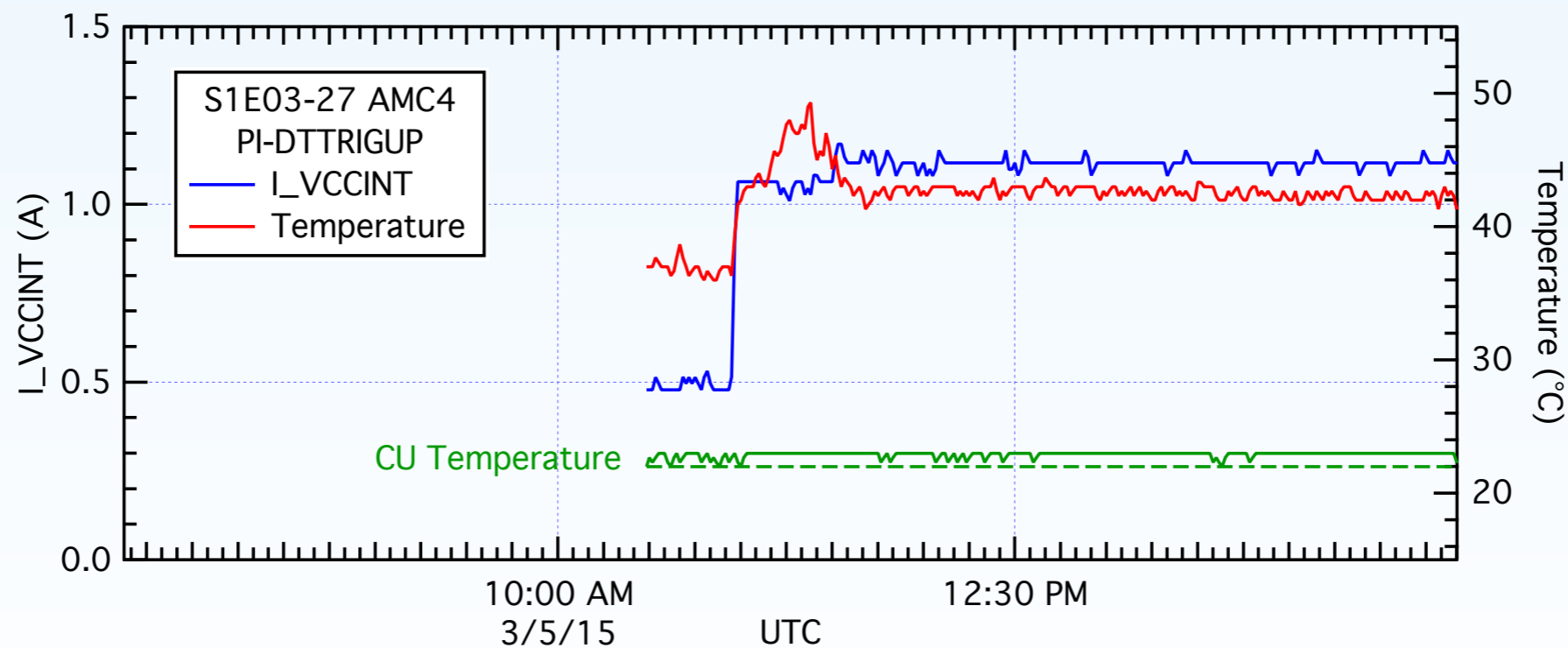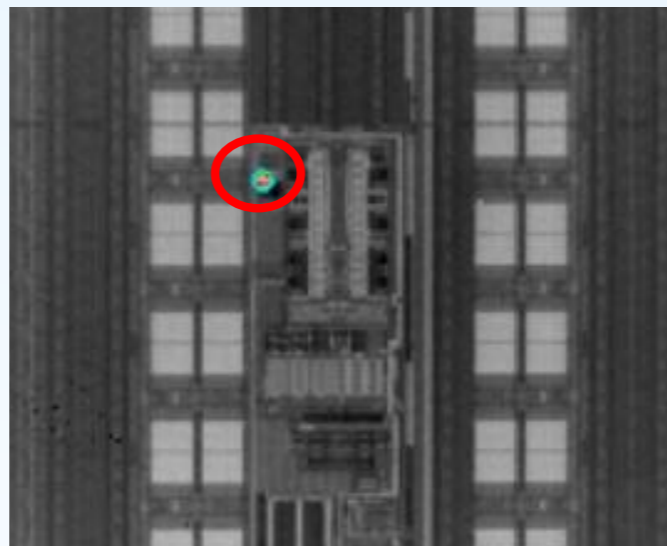

Thermal imaging - hotspot

100x close diffusion d marked in
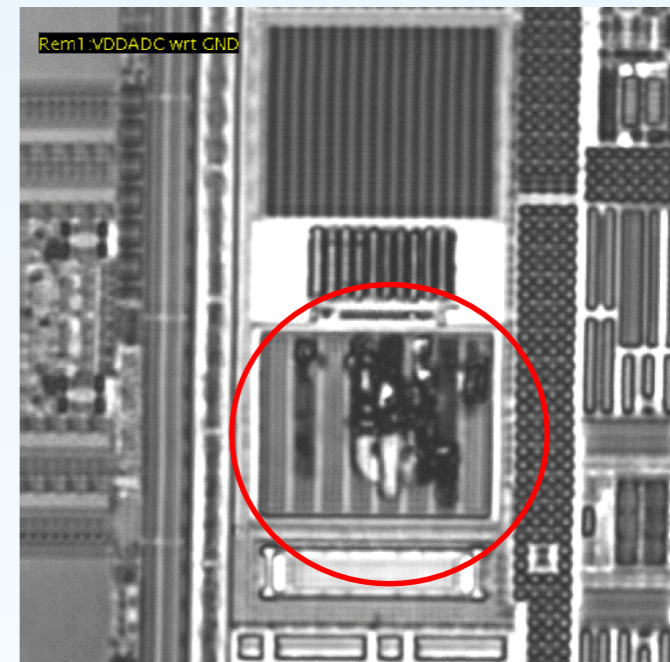
Catastrophic damage

Figure

- Simple fix possible with white wire

DAR_15022001 (v1.6) – 21-April-2015   www.xilinx.com   FRC06

  - Applied to all boards in April 2015

Failure trend cont.

- ● Problem solved
  - ● As long as firmware not updated…
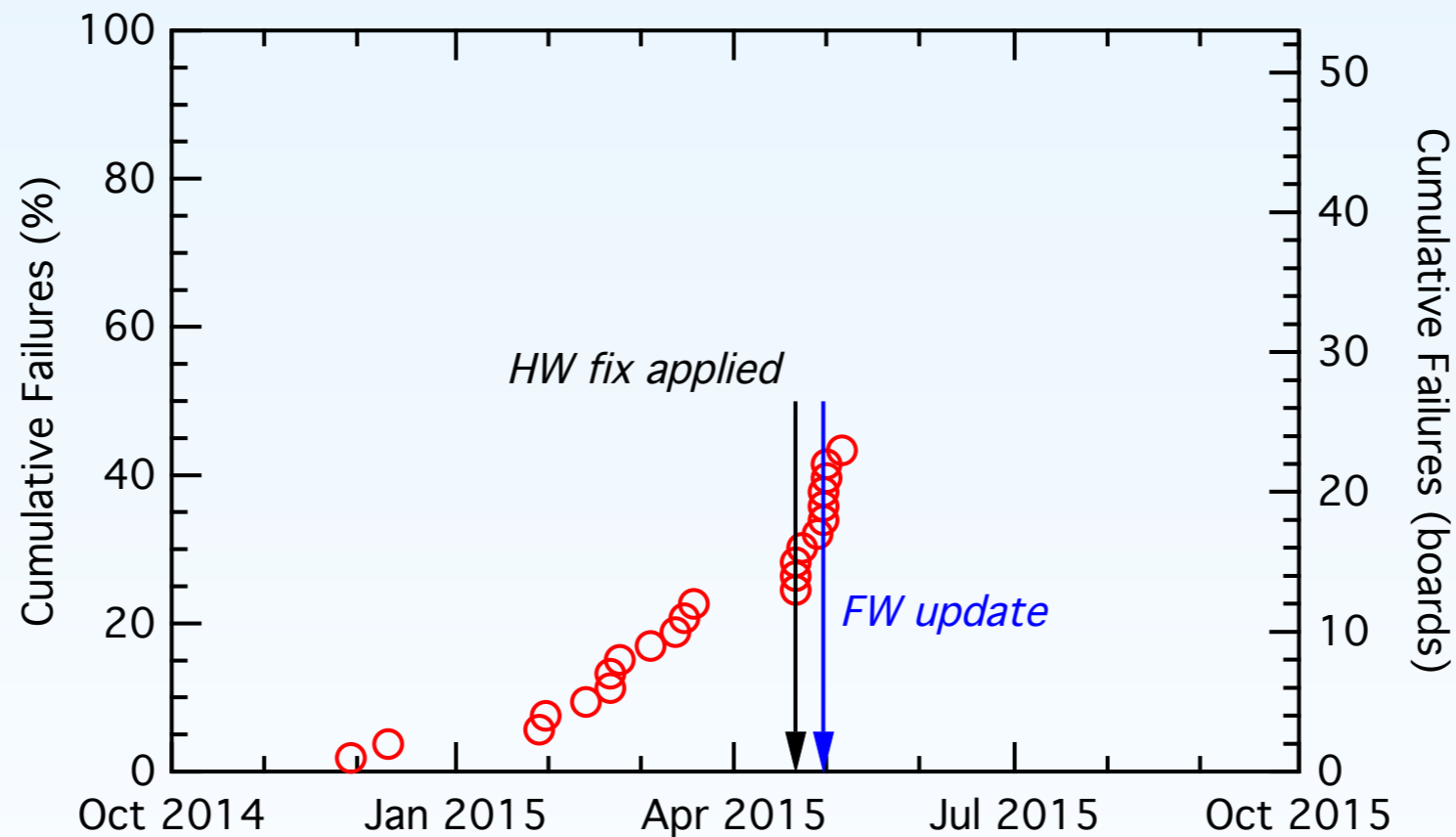
All AMCs will be replaced with new ones after end of this year's run

Summary

- CMS Timing system completely replaced during LS1
  - Project development -> deployment in 2 yrs

- Good performance achieved
  - Overall latency within limits
  - Timing jitter maintained at level of previous system

- Large effort for all CMS subsystems to integrate new system
  - Re-learned & re-visited many idiosyncrasies of the systems

- Operational difficulties due to board failures
  - Eventually solved by Xilinx failure analysis

- System now fully operational

Backup
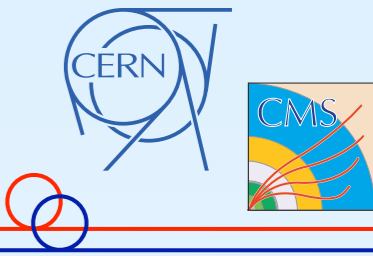
Feature summary

Feature	CMS Note 2002/033	present TCS	present LTC	LPM	CPM
Number of partitions	32	32	6	8	96
Number of partition groups	8	8	1	1	2
Number of DAQ EVM interfaces	1	1	1	1	2
LHC clock input	●	●	●	●	●
LHC orbit input	●	●	●	●	●
BST input	●	●	●		●
Number of B-Gos	10	16	16	32	32
Number of TTS States	7	7	7	16	16
B-Go and TTS sequence definition	FW	FW	SW	SW	SW
Active BX mask	●	●	●	●	●
Resonant Trigger Cancellation				●	●
External Front-end Emulator	●	●	●		
Internal Front-end Emulator				●	●
LumiDAQ sync signals				●	●
Counters active between Start & Stop					
Orbits	●	●	●	●	●
BXs with L1A inhibited	●	●		●	●
BXs with L1A inhibited L1A True	●	●		●	●
BXs with L1A inhibited L1A False	●	●		●	●
Active BXs with L1A inhibited	●	●		●	●
Active BXs with L1A inhibited L1A True	●	●		●	●
Active BXs with L1A inhibited L1A False	●	●		●	●
Active BXs with L1A inhibited, per condition	●	●		●	●
Physics Triggers	●	●	●	●	●
Physics Triggers distributed	●	●	●	●	●
Calibration or Test Triggers distributed	●	●	●	●	●
All Triggers distributed	●	●	●	●	●