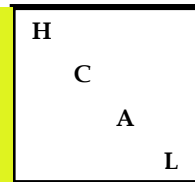




Upgrade Workshop



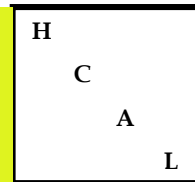
CMS HCAL Working Group FE Electronics: New QIE Nov 20, 2007

**People interested in QIE10 development: Chris Tully, Jim Freeman,
Sergey Los, Rick Vidal, Julie Whitmore**

QIE8 ASIC Engineers: Tom Zimmerman, Jim Hoff (FADC)



QIE8 Description



Current QIE8

Charge Integrator Encoder

4 stage pipelined device (25ns per stage)

charge collection

settling

readout

reset

Inverting (HPDs) and Non-inverting (PMTs) Inputs

Internal non-linear Flash ADC

Outputs

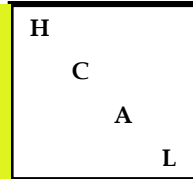
5 bit mantissa

2 bit range exponent

2 bit Cap ID



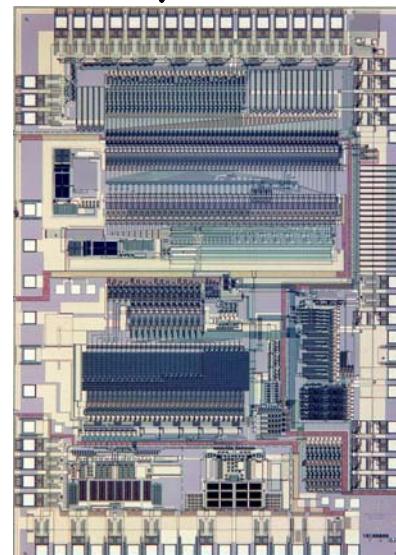
Current QIE8 Operation



QIE Design Specifications

- Clock > 40 MHz
- Must accept both polarities of charge
- Charge sensitivity of lowest range – 1fC/LSB(inverting-input)
 - In Calibration Mode 1/3 fC/LSB
- Maximum Charge – 9670 fC/25ns(inverting-input)
 - Range (1-10,297 fC)
- 4500 electrons rms noise
- FADC Differential Non-Linearity < .05 LSBs
- Package - 64 pin TQFP

QIE8 - AMS 0.8 μ m bi-CMOS process

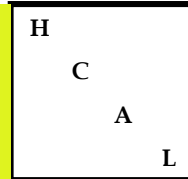


Chip Size: 3.07 mm x 4.35 mm

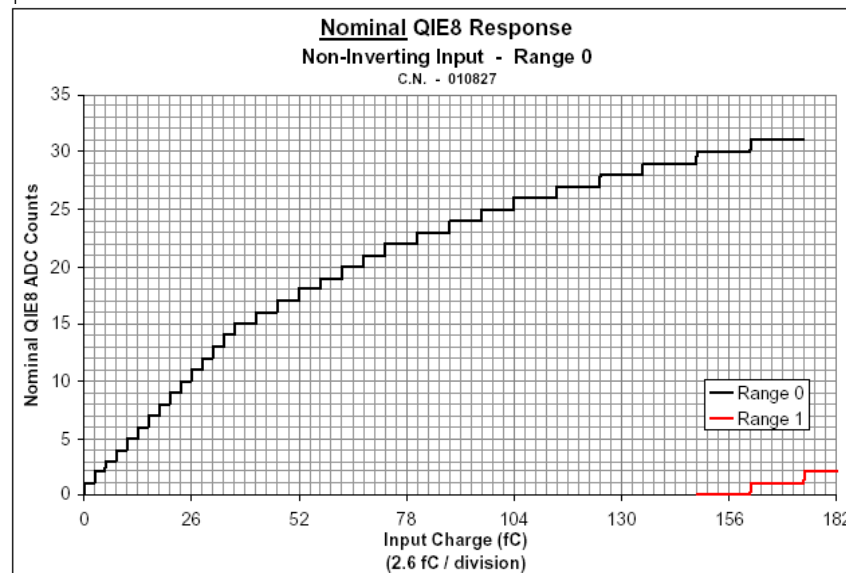
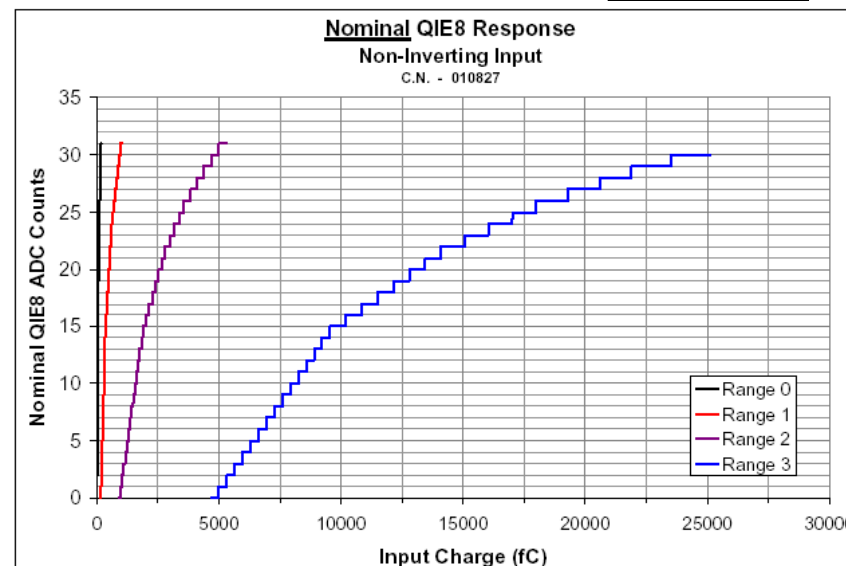
QuickTime™ and a TIFF (Uncompressed) decompressor are needed to see this picture.



QIE8 Response

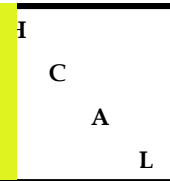


Normal Mode			
Range (Exponent)	Input Charge	FADC Codes	Gain (q/Lsb)
0	-1 fC --- 14 fC	0---14	1 fC/bin
0	14 fC --- 28 fC	15---21	2 fC/bin
0	28 fC --- 40 fC	22---25	3 fC/bin
0	40 fC --- 52 fC	26---28	4 fC/bin
0	52 fC --- 67 fC	29---31	5 fC/bin
1	57 fC --- 132 fC	0---14	5 fC/bin
1	132 fC --- 202 fC	15---21	10 fC/bin
1	202 fC --- 262 fC	22---25	15 fC/bin
1	262 fC --- 322 fC	26---28	20 fC/bin
1	322 fC --- 397 fC	29---31	25 fC/bin
2	347 fC --- 722 fC	0---14	25 fC/bin
2	722 fC --- 1072 fC	15---21	50 fC/bin
2	1072 fC --- 1372 fC	22---25	75 fC/bin
2	1372 fC --- 1672 fC	26---28	100 fC/bin
2	1672 fC --- 2047 fC	29---31	125 fC/bin
3	1797 fC --- 3672 fC	0---14	125 fC/bin
3	3672 fC --- 5422 fC	15---21	250 fC/bin
3	5422 fC --- 6922 fC	22---25	375 fC/bin
3	6922 fC --- 8422 fC	26---28	500 fC/bin
3	8422 fC --- 10297 fC	29---31	625 fC/bin
Calibration Mode			
Forced 0	-2.333 fC --- 10 fC	0---31	1/3 fC/Bin





6 Channel QIE8 FE Board



Custom ASICs

QIE (6 / board)
Fermilab

Low Voltage Regulator
(2 / board) CERN

Developed in rad hard process

AD590

Temp Sensor

P82B96

I2C Transceiver
(change to P82B715)

MC100LVELT23
LVPECL-LVTTL

MC100LVEP111
LVPECL clock
fanout chip

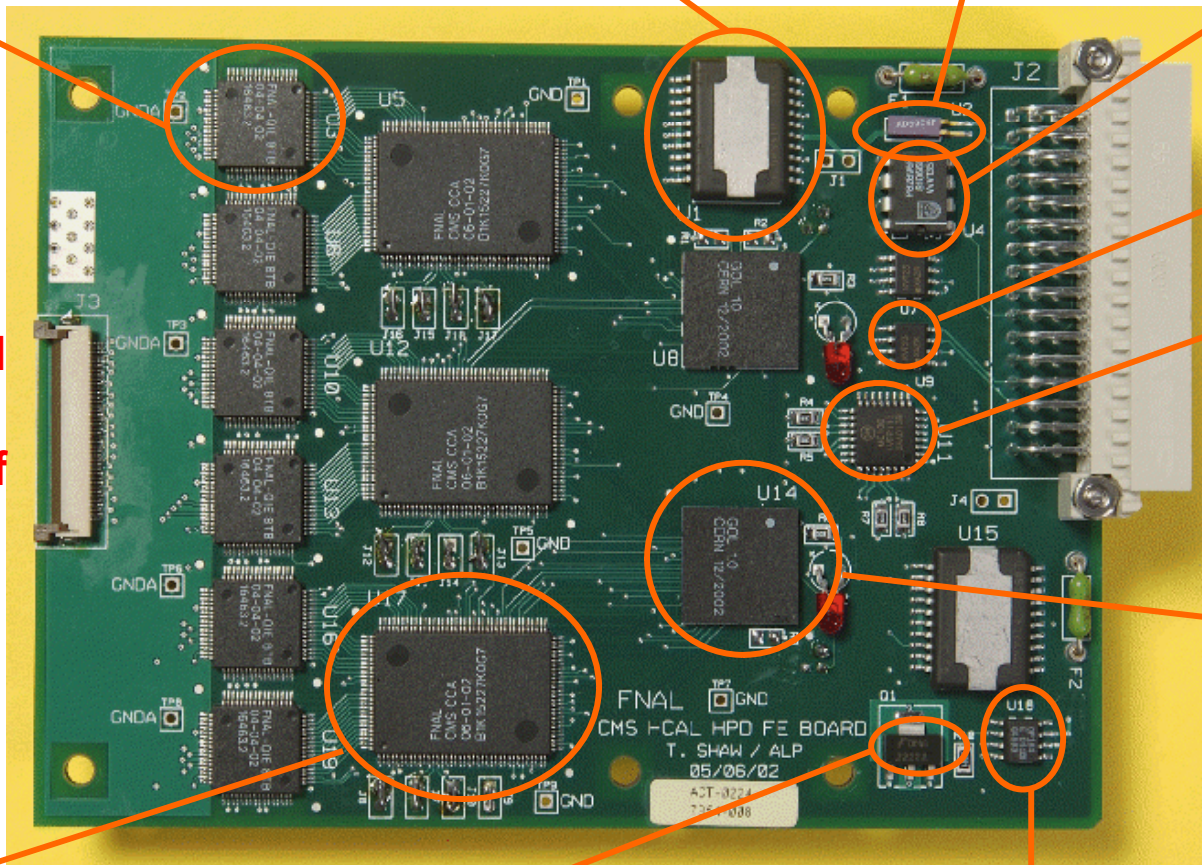
Gigabit Optical
Link [GOL]
(2 / board) CERN
Developed in
rad hard process

Honeywell
VCSEL
HFE419x-521
(2/board)
[back side of
board]

CCA
(3 / board)
Fermilab

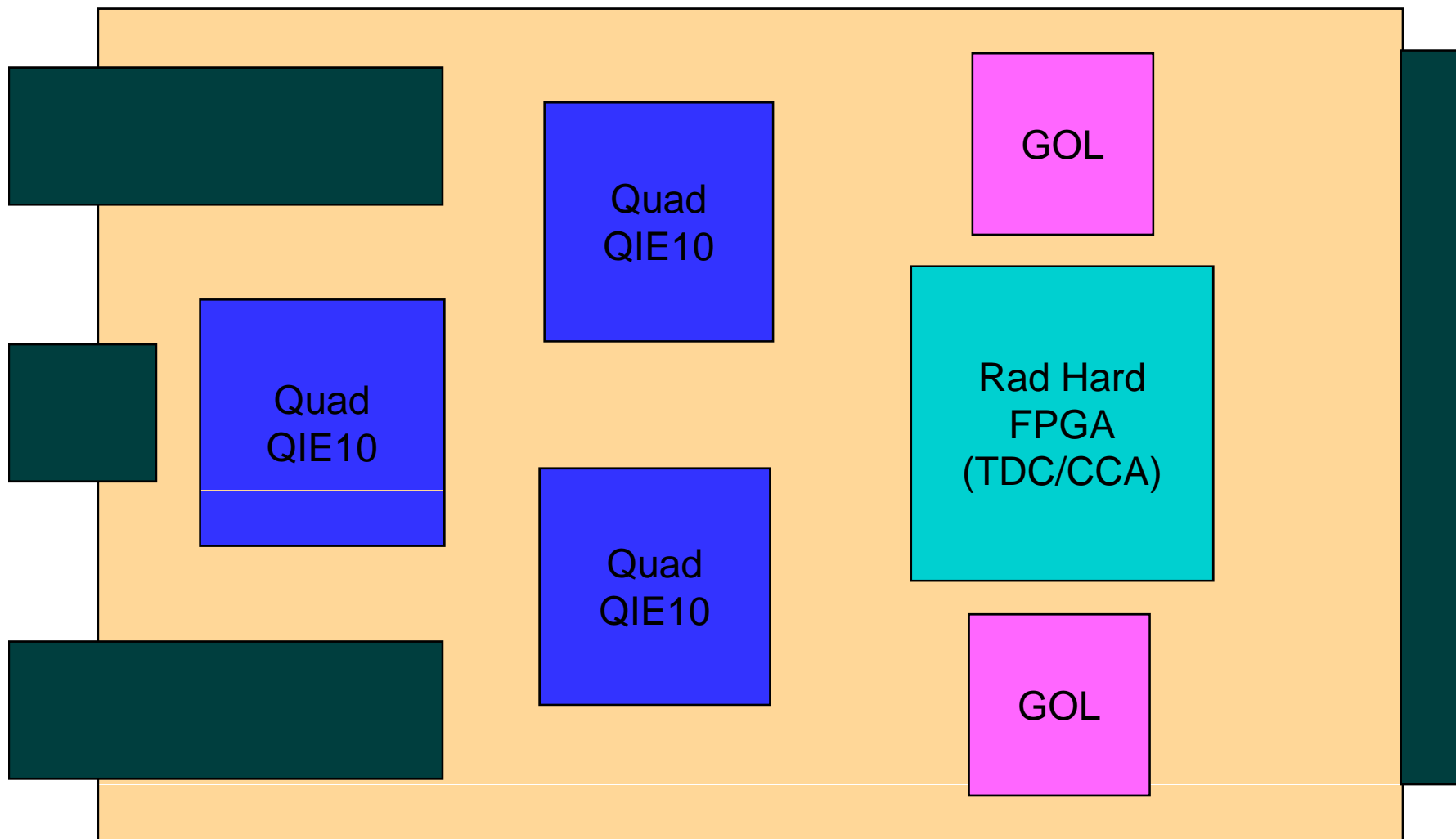
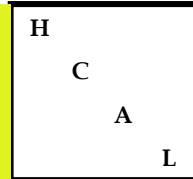
PZT222A transistor

OP184 bi-polar OpAmp



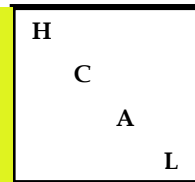


QIE10 12-Channel Cards





QIE Data



Current Configuration - 1.6 Gbps/fiber

Each RBX - 72 QIE channels/RBX (72 towers)

18 channels/RM (3 cards, 6 QIE channels, 2 fibers/card.
3 QIEs/fiber)

1 QIE = 5-bit Mantissa, 2-bit range, 2-bit CapID = 9-bits
32-bits/fiber, 1.6 Gbps (8-bit/10-bit), Gigabit Ethernet

New Configuration - 3.2 Gbps/fiber

Each RBX - 72 towers

Tower - 3 layers (1 inner, 2 inter-weaving outer)

Each Tower (3 QIEs) - Total 32-bits

1 QIE - 6-bits, 2-bit range = 8-bits (x3)

TDC - 5-bit (per tower)

CapID - 2-bit (per tower)

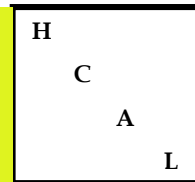
Error Bit - 1 bit (per 3 QIEs)

Each Fiber - 2 Towers (6 QIEs = 3.2 Gbps/fiber)

Use 4 cards and all 8 fibers in ribbon



Quad QIE10 Specs

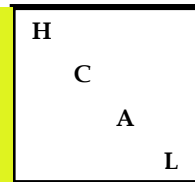


QIE10

- **Clock > 40 MHz**
- **Match to SiPM response**
 - HB - ZETEC 40,000 pixel device
 - 4X Dynamic range of QIE8
- **1 Extra bit resolution (5--> 6)**
- **Keep non-linear response as in QIE8**
- **Charge sensitivity of lowest range**
 - QIE8: Norm - 1fC/LSB, Calib - 1/3 fC/LSB
 - QIE10: 10x less sensitive
 - **Set by lowest SiPM gain (Singapore ZETEC - HB?)**
- **Need to control rate effects (DC coupling)**
- **2 or 4 QIE10 per package, either multi-channel QIE die or separate dice in single package**
- **Form a “discriminated signal” to send to the FPGA for TDCing**
 - 1 TDC signal per channel



Quad QIE10 - TomZ

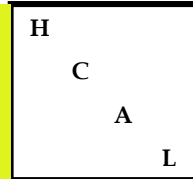


QIE10 Design Discussions w/ Tom Zimmerman (Tully/Freeman/Los)

- **Will 0.8 μm AMS Process still exist for QIE10?**
 - Tom will check with AMS
- **Prefers negative polarity for better impedance control**
 - Try for 25 Ω impedance
 - try for small dynamic impedance to avoid time slewing of inverting QIE8 input
- **Prefers DC coupling**
- **1 more bit of dynamic range seemed doable**
 - Not much more power needed ($\ll x2$)



Plans

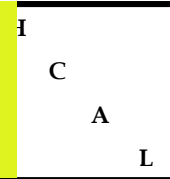


QIE10 R&D

- Need 100,000 channels (60,000 channels + spares)
- Need production run such that we have chips in hand by 2011
- Probably 2 submissions: 1)Prototype, 2)Production
- TomZ can start to work on this in March 2009
- > Need QIE10 spec from HCAL well in advance
- Issues:
 - Need to check radiation hardness of AMS process
 - CMOS registers die from TID at 200 kRad ($3.5E12$). Need to test beyond this and try accelerated annealing
 - Bipolar - Beta for npn-transistors dropped by 5-10% after equivalent of $5E11$ n/cm²
 - Have we decided on ZETEC (since this drives the dynamic range of the device)?

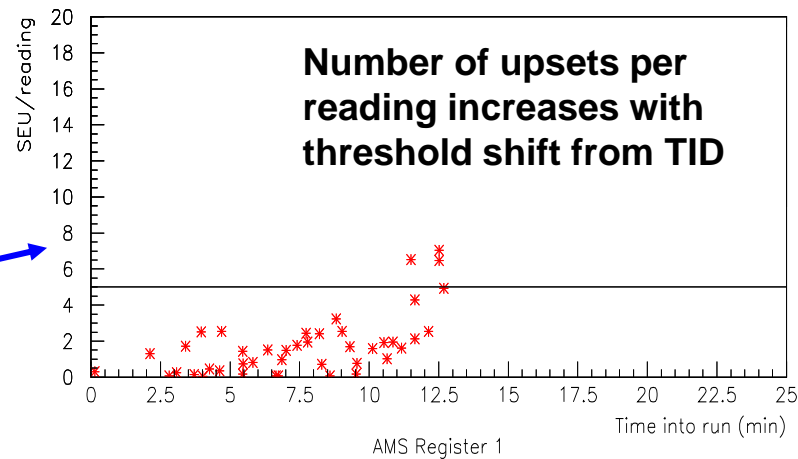
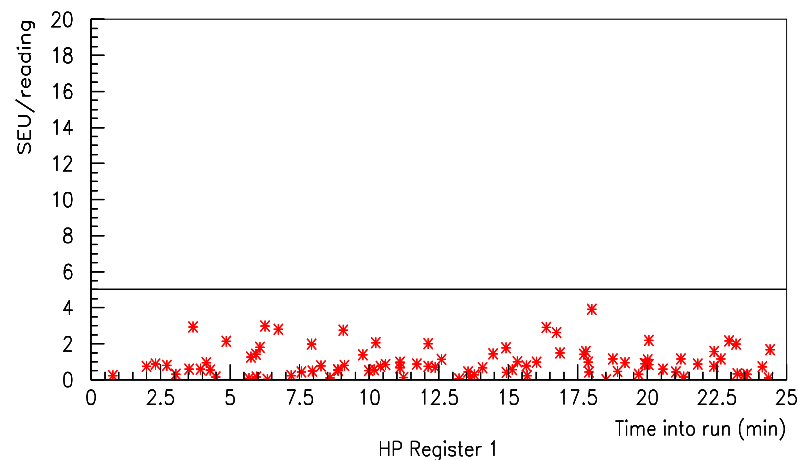
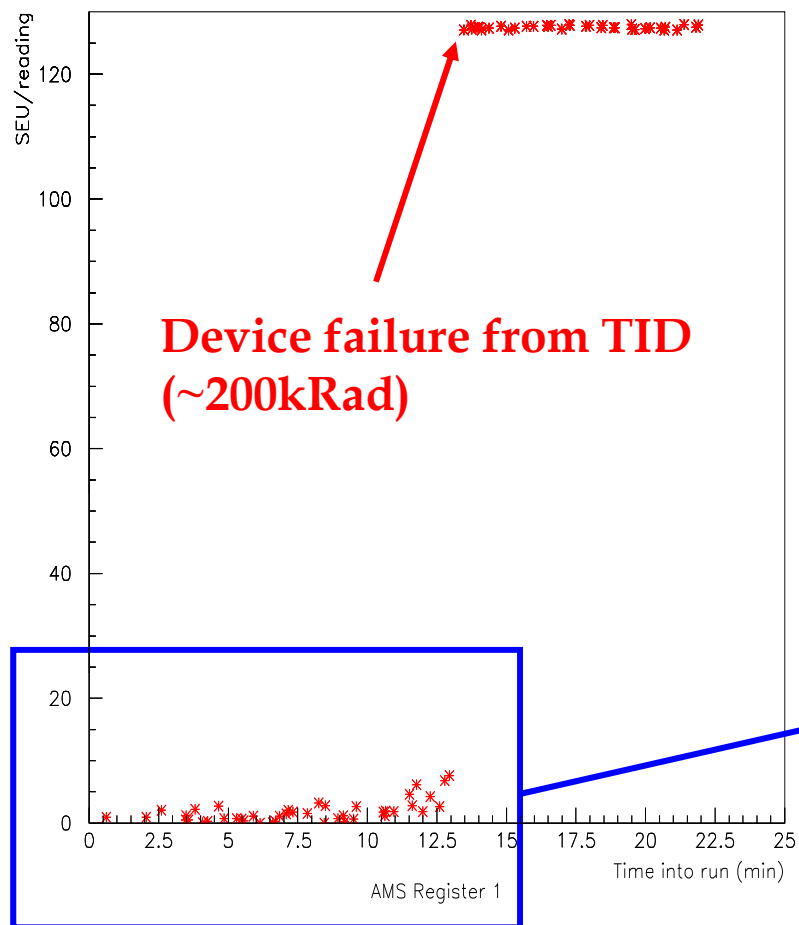


QIE Radiation Tolerance (from SEU ASIC studies)



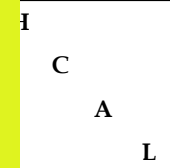
**AMS – Most sensitive register
(Minimum size + guard ring)**

**HP and AMS registers
(Minimum + guard ring)**





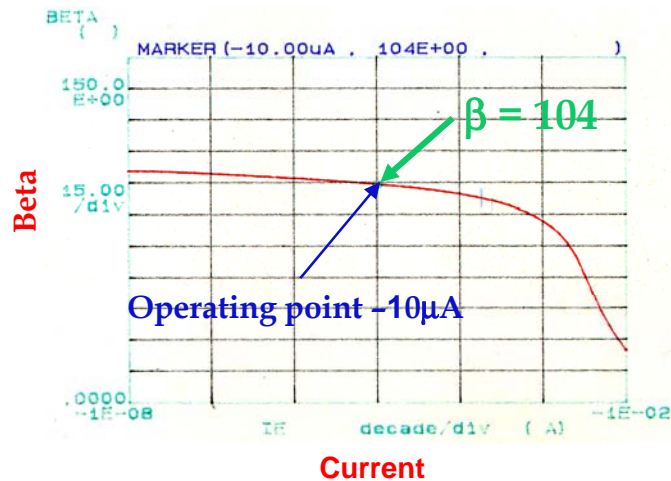
Bi-polar Radiation Studies for QIE



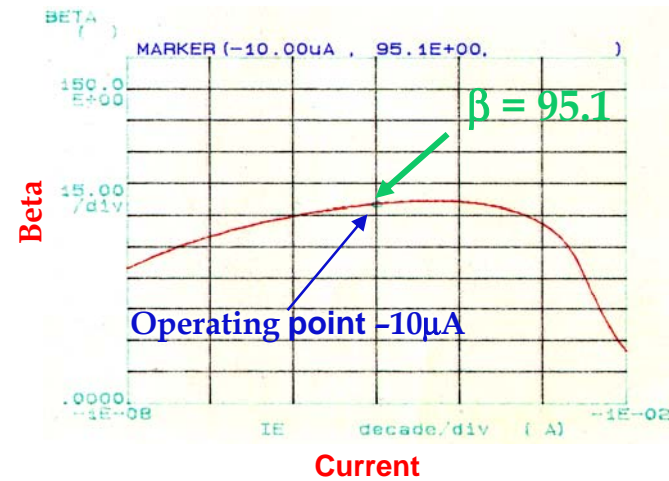
Bi-polars from AMS 0.8 μm bi-CMOS process

- Beta for npn-transistors dropped by 5-10% after equivalent of $5\text{E}11 \text{ n/cm}^2$

Pre-irradiation

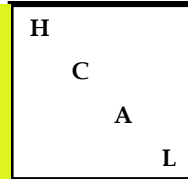


Post-irradiation (6 weeks)



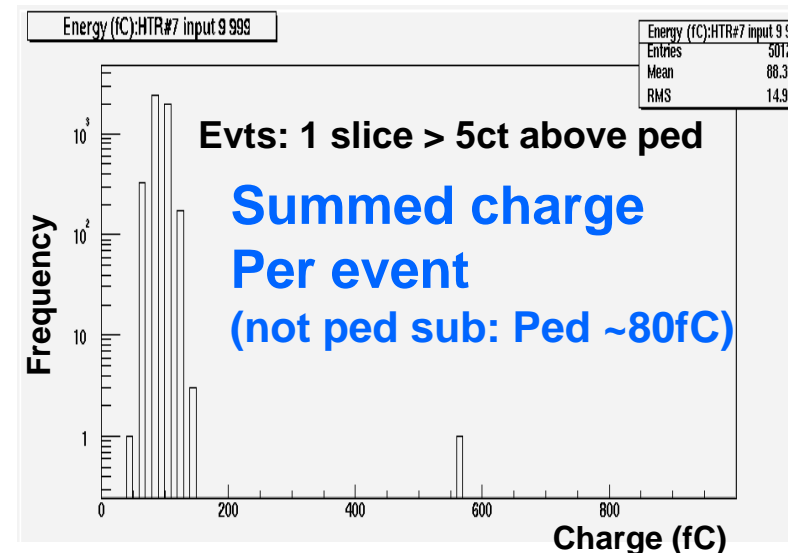
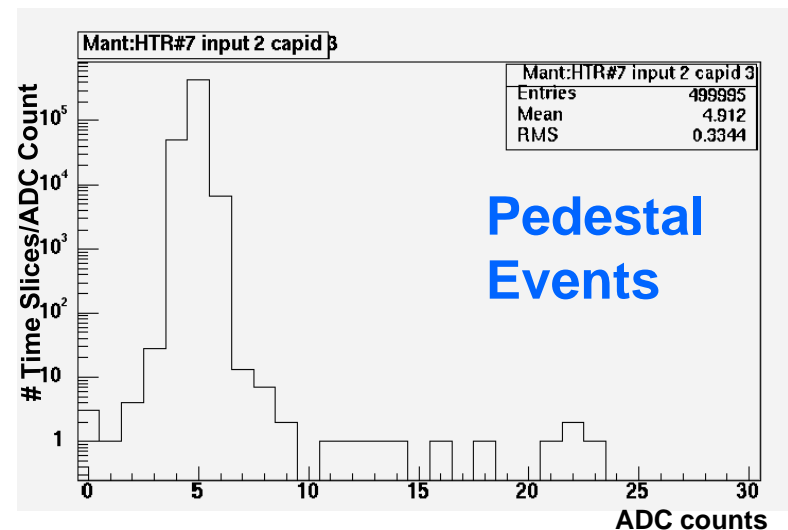


FE Board Test



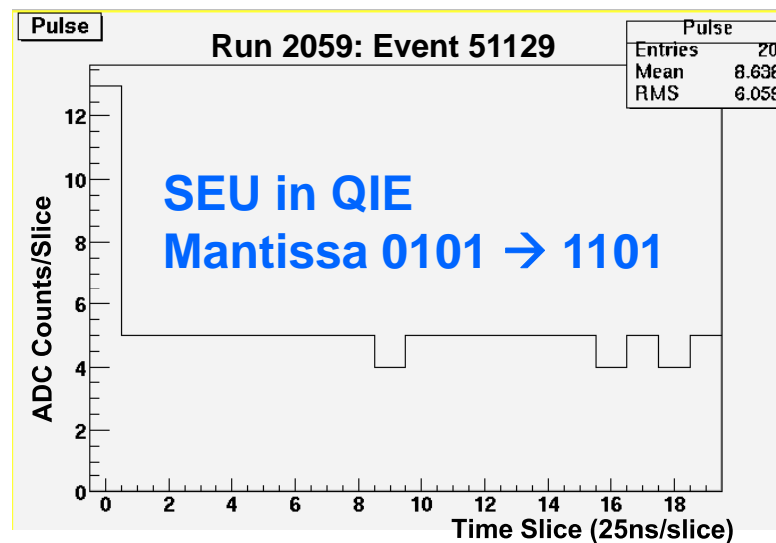
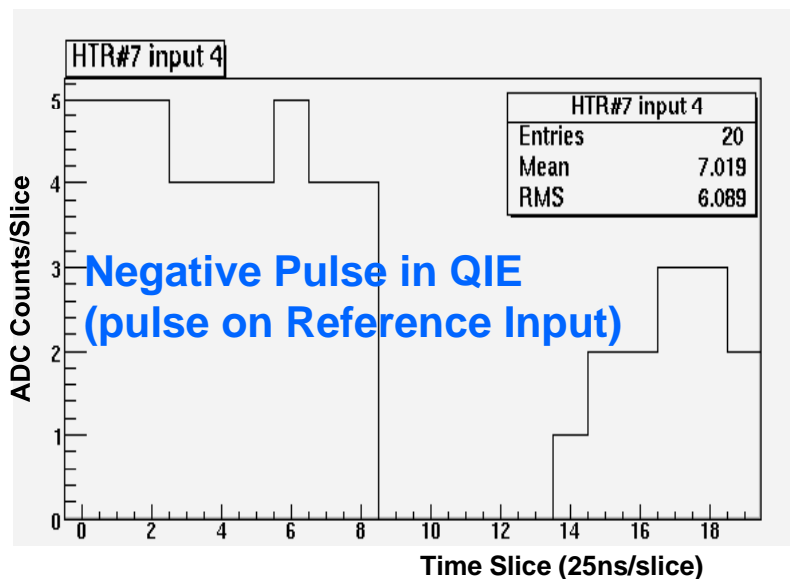
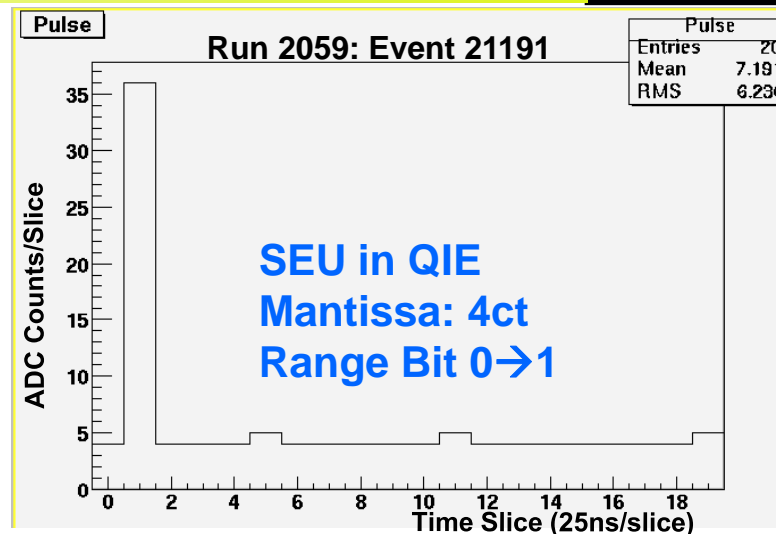
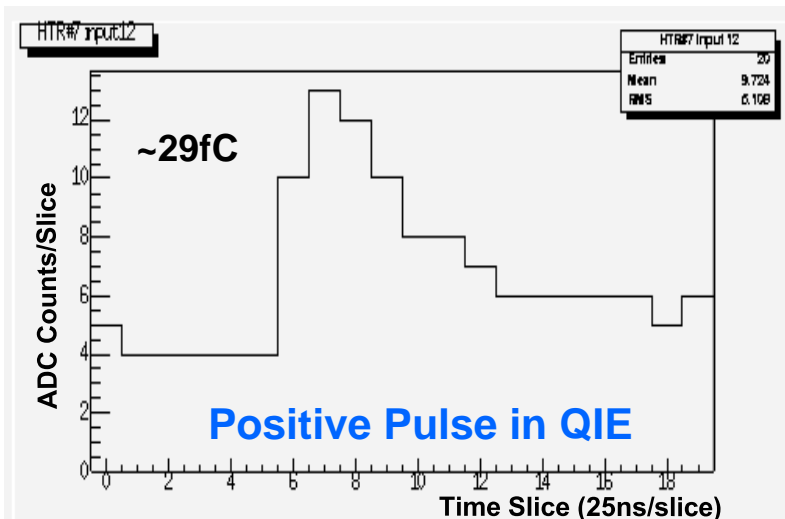
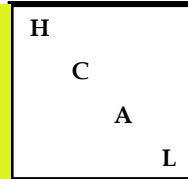
FE Board response in 200 MeV proton beam

- SEU measurement is limited by data rate
- Several pathologies
 - Signals in QIE in front of integration caps (signal & reference)
 - Signals in QIE on back of end caps (signal follows cap)
 - SEU events



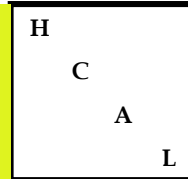


FE Rad Data Pathologies





Protons Interacting in QIE



Pulses in QIE consistent with protons interacting in QIE silicon (~10mils thick)

- MIP in Si (28k-30k e⁻) per 300 μm
- Expect maximum energy deposition (16fC-1.6pC) based on previous measurement of protons interacting in HPD silicon but also consistent with Monte Carlo simulations
- We see 60-70fC in the PEAK slice

HCAL implications

- These events (also expected in HPD silicon) will be ignored at trigger level since the energy is deposited in a single isolated channel

