CMS HCAL Working Group
FE Electronics: New GOL
Nov 20, 2007

HCAL personnel interested in GOL/GBT: Jeremy Mans, Tullio Grassi, Drew Baden, Chris Tully, Julie Whitmore

Slides borrowed from Chris Tully, Paolo Moreira, Sandro Marchioro, Jan Troska, Jorgen Christiansen,Terri Shaw

6 Channel FE Board

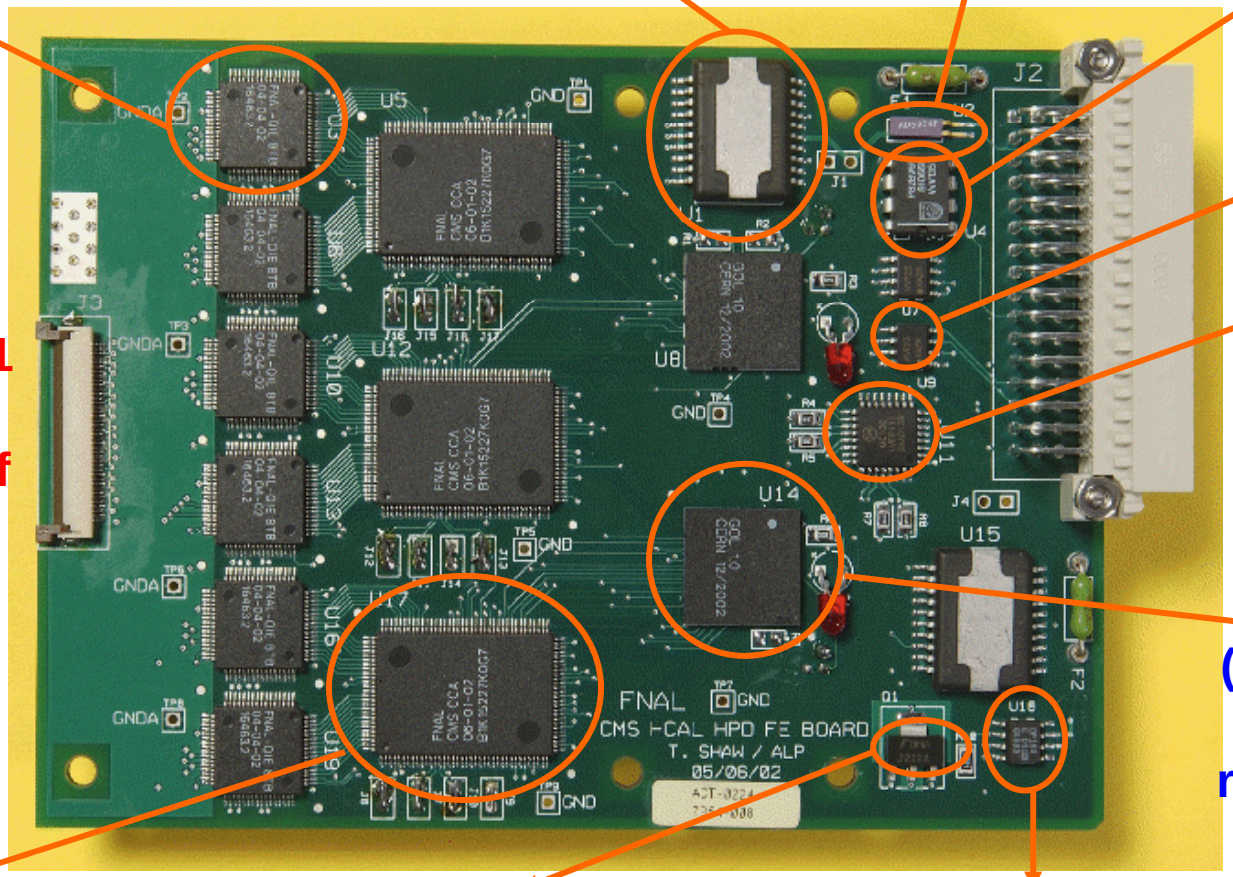
Custom ASICs

QIE (6 / board) Fermilab

Low Voltage Regulator (2 / board) CERN Developed in rad hard process

AD590 Temp Sensor

P82B96 I2C Transceiver (change to P82B715



MC100LVELT23 LVPECL-LVTTL

MC100LVEP111 LVPECL clock fanout chip

Honeywell VCSEL HFE419x-521 (2/board) [back side of board]

Gigabit Optical Link [GOL] (2 / board) CERN Developed in rad hard process

CCA (3 / board) Fermilab

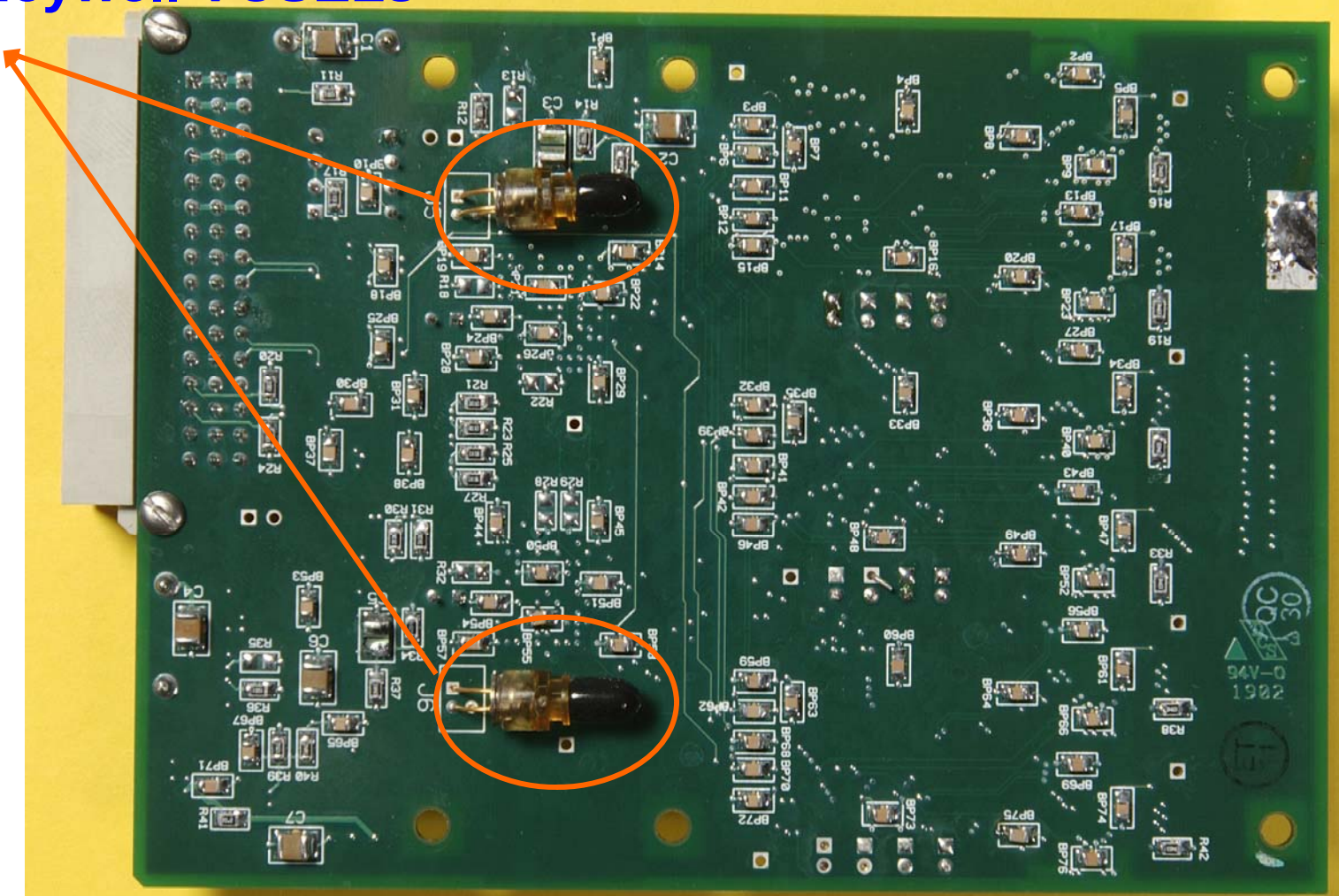
PZT222A transistor

OP184 bi-polar OpAmp

6 Channel FE Board
(Backside)

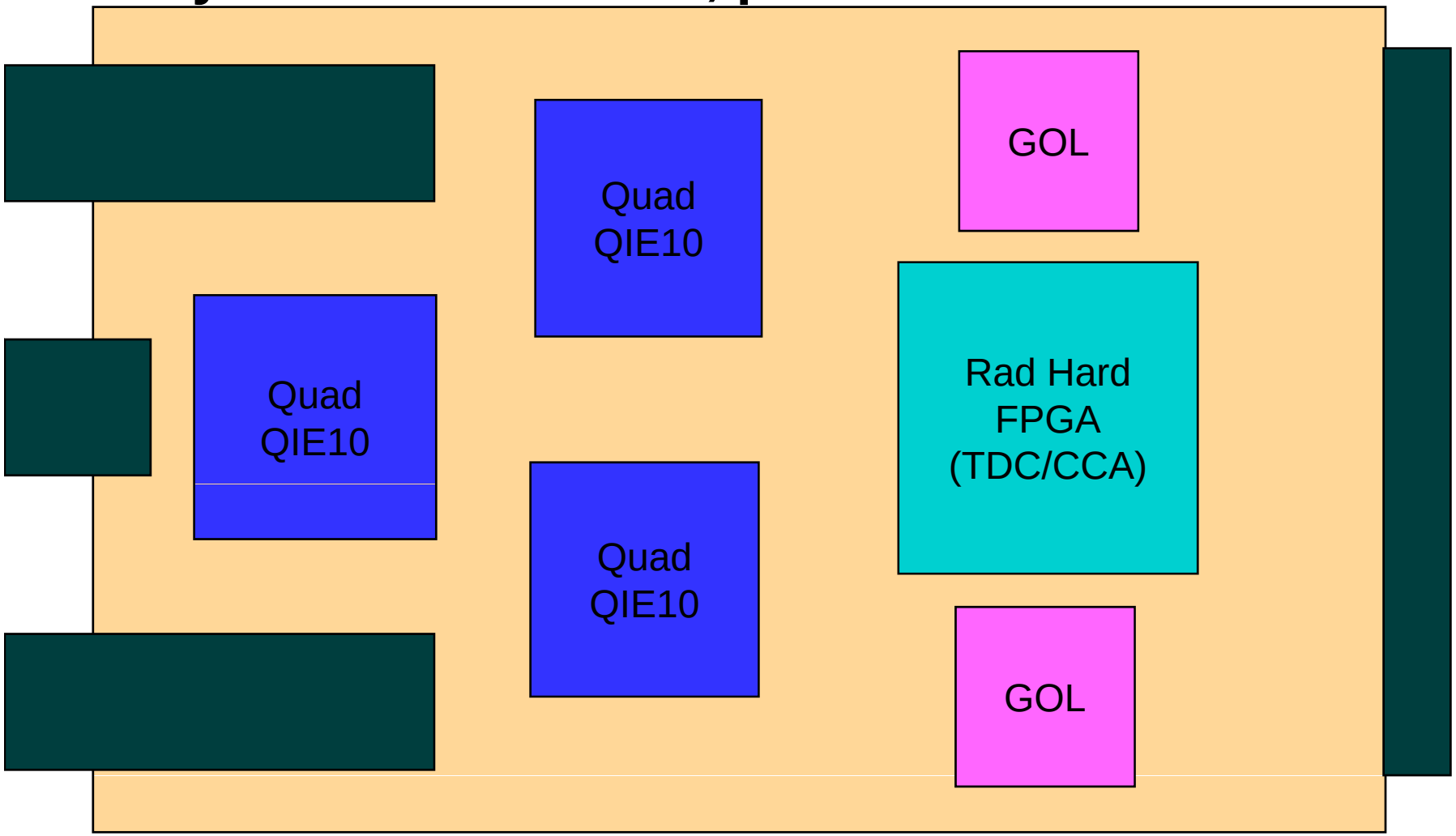
H C A L

Honeywell VCSELs



QIE10 12-Channel Cards

3 layers/tower - 1 inner, plus 2 inter-weaved outer



HB Digital Readout Bandwidth

Current Readout (1.6 GHz) Format

	D(31:30)	D(29:25)	D(24)	D(23:22)	D(21:17)	D(16)	D(15:14)	D(13:9)	D(8:7)	D(6:5)	D(4:3)	D(2)	D(1)	D(0)
Optical Cable 1	QIE 0 Exp (1:0)	QIE 0 Mant (4:0)	QIE_Reset (abort gap marker?)	QIE 1 Exp (1:0)	QIE 1 Mant (4:0)	"0"	QIE 2 Exp (1:0)	QIE 2 Mant (4:0)	QIE 0 CapID(1:0)	QIE 1 CapID(1:0)	QIE 2 CapID(1:0)	Control Flag=0	Data Flag=1	"1"
Optical Cable 2	QIE 4 Exp (1:0)	QIE 4 Mant (4:0)	QIE_Reset (abort gap marker?)	QIE 5 Exp (1:0)	QIE 5 Mant (4:0)	"0"	QIE 3 Exp (1:0)	QIE 3 Mant (4:0)	QIE 4 CapID(1:0)	QIE 5 CapID(1:0)	QIE 3 CapID(1:0)	Control Flag=0	Data Flag=1	"1"

FE DATA FORMAT

64 bits/25ns per fiber

Possible HB Readout (3.2 GHz) Format with GOL

QIE0 8-bit	QIE1 8-bit	QIE2 8-bit	QIE3 8-bit	QIE4 8-bit	QIE5 8-bit	
TDC0 5-bit	CapID(0-3) 2-bit	ErrBit 1-bit	TDC3 5-bit	CapID(4-5) 2-bit	ErrBit 1-bit	

Optical Cable 1

QIE6 8-bit	QIE7 8-bit	QIE8 8-bit	QIE9 8-bit	QIE10 8-bit	QIE11 8-bit	
TDC6 5-bit	CapID(6-7) 2-bit	ErrBit 1-bit	TDC9 5-bit	CapID(8-11) 2-bit	ErrBit 1-bit	

Optical Cable 2

Gigabit Optical Link (GOL) Configuration

- 32 bit mode; 1.6 Gb/s (8-bit/10-bit); Gigabit Ethernet Protocol
- Need to confirm max speed (3.2 Gbps?) w/ bit error rate test - UMinn
- At CERN, 30 Wafers with 1770 chips/wafer
- Packaging - (for order ~10,000, $2.5/chip, NRE already paid)
- Place order soon to avoid re-negotiating export license

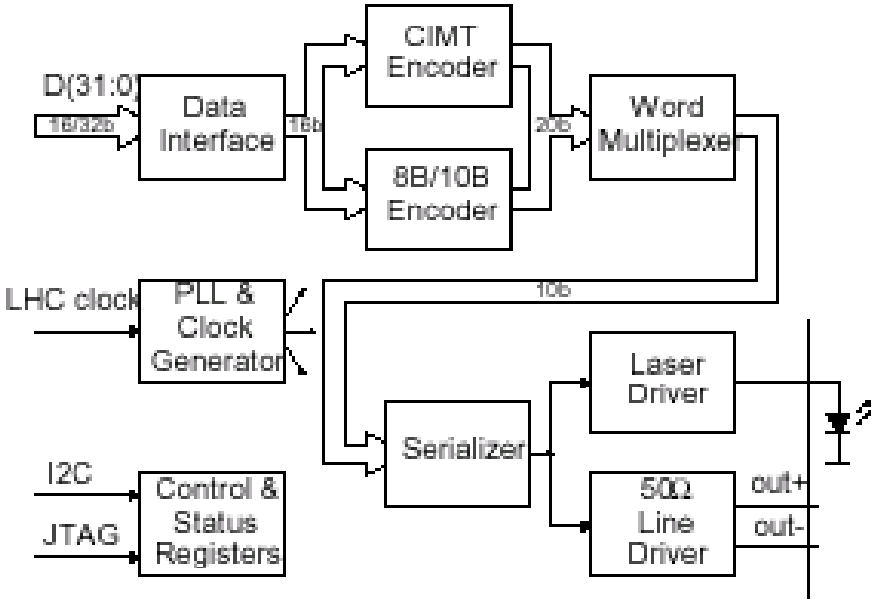
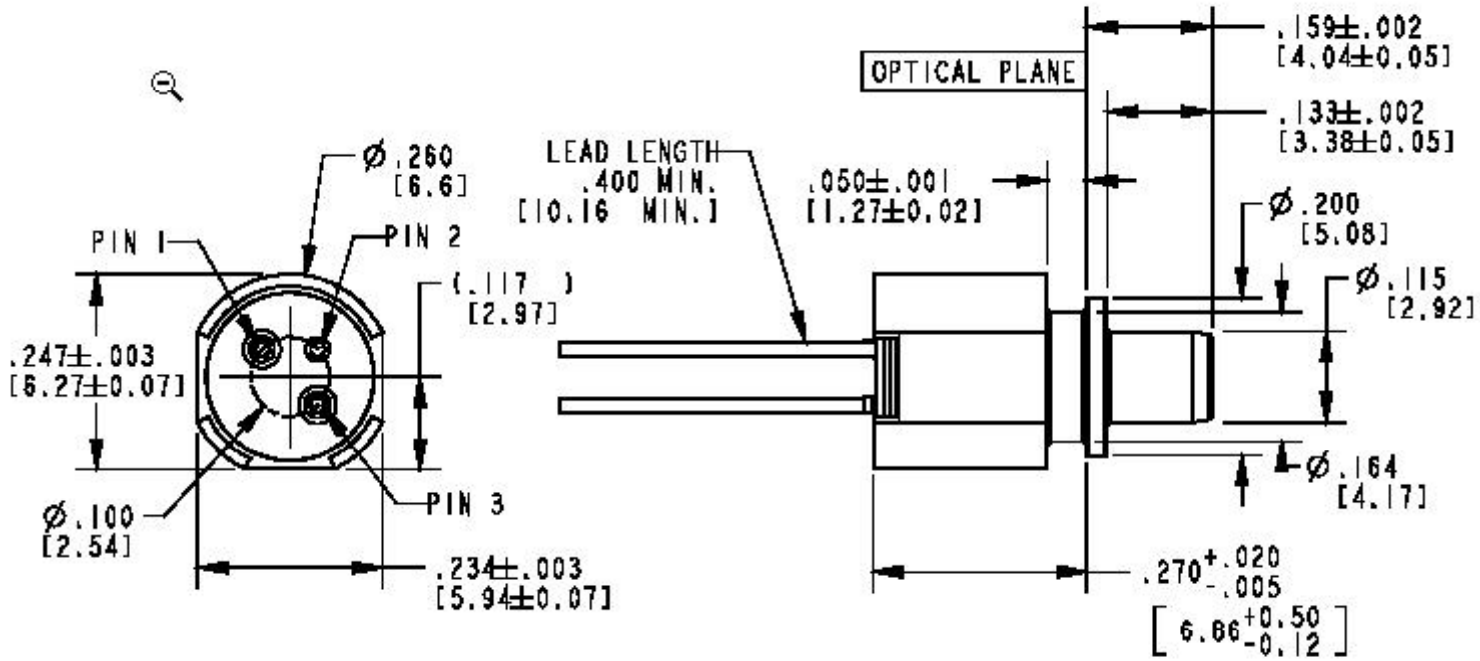


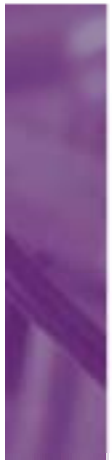
Figure 1 GOL block diagram.

Connectorized VCSEL (HPD Boards)

2.5Gbps VCSEL Connectorized - Datacom		
 NEW!	HFE419x-521  Product Sheet	LC Connectorized Components, Common Anode and Common Cathode, 2.5 Gb/s operation, attenuated



HCAL Fiber Bandwidth



Specifications Graded-Index Multimode Optical Fibre.
Type: 50 / 125 µm

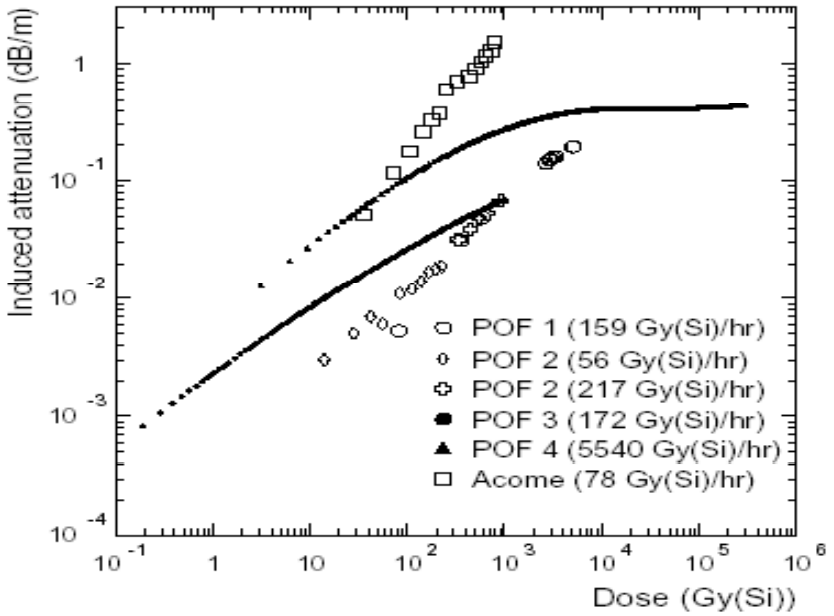
Characteristics	*Conditions*		*Specified Values*		*Units*
Optical Characteristics					
Attenuation Coefficient	850 nm	≤ 2.3	≤ 2.4	≤ 2.5	[dB/km]
	1300 nm	≤ 0.5	≤ 0.6	≤ 0.7	[dB/km]
Minumum Modal Bandwidth [1,2]	850 nm			400 to > 1000	[MHz.km]
	1300 nm			600 to > 1500	[MHz.km]
Numerical Aperture				0.200 ± 0.015	
Chromatic Dispersion				FDDI Spec	
Backscatter Characteristics [3]	1300 nm				
Step [4]				≤ 0.1	[dB]
Irregularities over fibre length				≤ 0.1	[dB]
Reflections				Not allowed	
Group Index of Refraction (Typical)	850 nm			1.482	
	1300 nm			1.477	

Fiber specifications
Modal Bandwidth - measure of signal amplitude to drop 3dB
1000 MHz-km = 700-800 Mbps
HCAL fiber - 0.1 km
850nm --> 1000 MHz-km --> 7-8 Gbps

Cable

Cable requirements

- **Able to transmit 1.6 Gbps over 90 m with low dispersion**
  - 50/125 μm rather than 62.5/125 μm
- **Very little darkening of fiber at HCAL radiation levels (3E11 n/cm2 and 1kRad TID)**
  - Plasma Optical Fiber – Graded-Index Multi-mode (Atlas)
  - CMS HCAL rad test of RM fiber – no measurable change in transmission
- **Controlled environment → No thermal or moisture issues (or rodents!)**



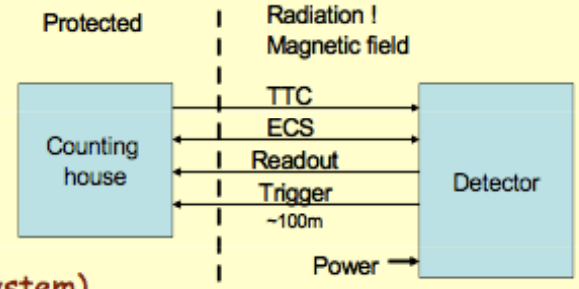
- **Fiber radiation study (Atlas)**
  - Plasma Optic Fiber 50/125μm Graded Index Multi-mode Ge-doped fiber selected
  - Rad Tolerant (~0.1 dB/m at 800 Gy(Si) and 2E13 n/cm^2)

Atlas Liquid Argon Cal (ATL-ELEC-99-001)

Link requirements
(General)

Functions needed

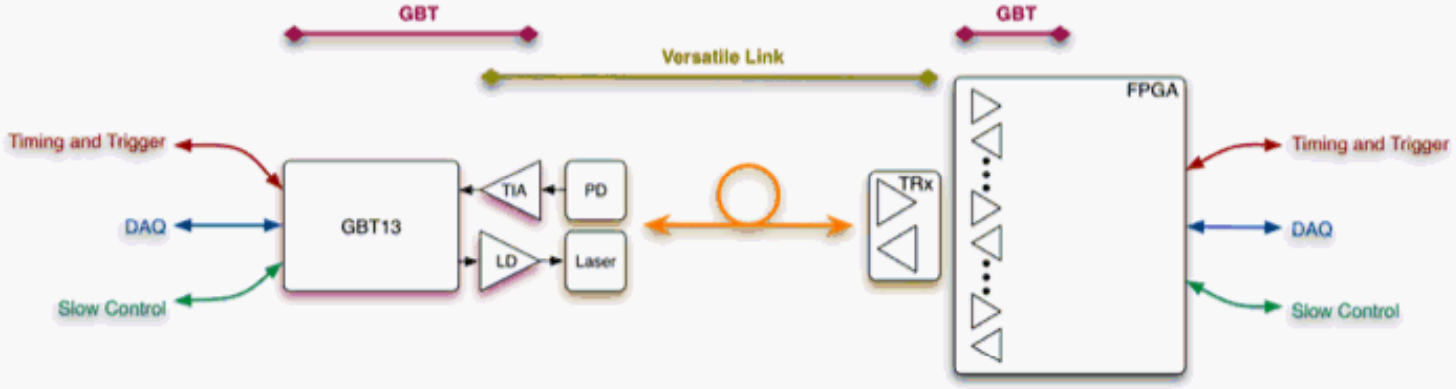
- TTC: Trigger and timing control
  - Timing reference: clock(s), timing adjust , jitter, , ?
  - Trigger signals: trigger accept(s), trigger type, , , ?
  - Sync control signals: reset, calibration pulse injection, , , ?
  - Fixed and stabilized delay and latency (as short as possible)
  - Unidirectional: down
  - Number of signals needed ?
  - Handling multiple FE chips: simple fan-out ?
  - Reliability: Very high (SEU sensitive PIN/TIA in radiation !)
- Controls/monitoring: ECS (Experiment Control System)
  - Control of parameters in front-ends (with readback)
  - Monitoring: temp, voltage, etc.
  - Also DSS related signals ? (very high reliability required, fail safe, etc.)
  - Effective data rate needed ? (normally not very high)
  - Bidirectional
  - Handling multiple FE chips: addressing, serial/parallel bus ?, other ?
  - Reliability: high
- Readout
  - Readout of event data
  - Maximum data rate possible
  - Latency not an issue
  - Unidirectional: up
  - Handling data from multiple FE chips: Merging data streams or local event building
    - Serial or parallel connections ?
  - Reliability: high (single bit flips in readout data can be accepted at low rate)
- Trigger data
  - Similar to readout but constant (and short) latency may be required.



Very expensive if developed by each expt/subsystem

Radiation Hard Optical Link: Themes

- Two Major Themes
  - The opto-electronics, its radiation and functionality testing plus packaging
    - This work is carried out in the context of the Versatile Link
    - Versatile Link project was recently approved by CMS and ATLAS
  - The ASIC design, verification and packaging
    - This work is carried out in the context of the GBT



On-Detector
Custom Electronics & Packaging
Radiation Hard

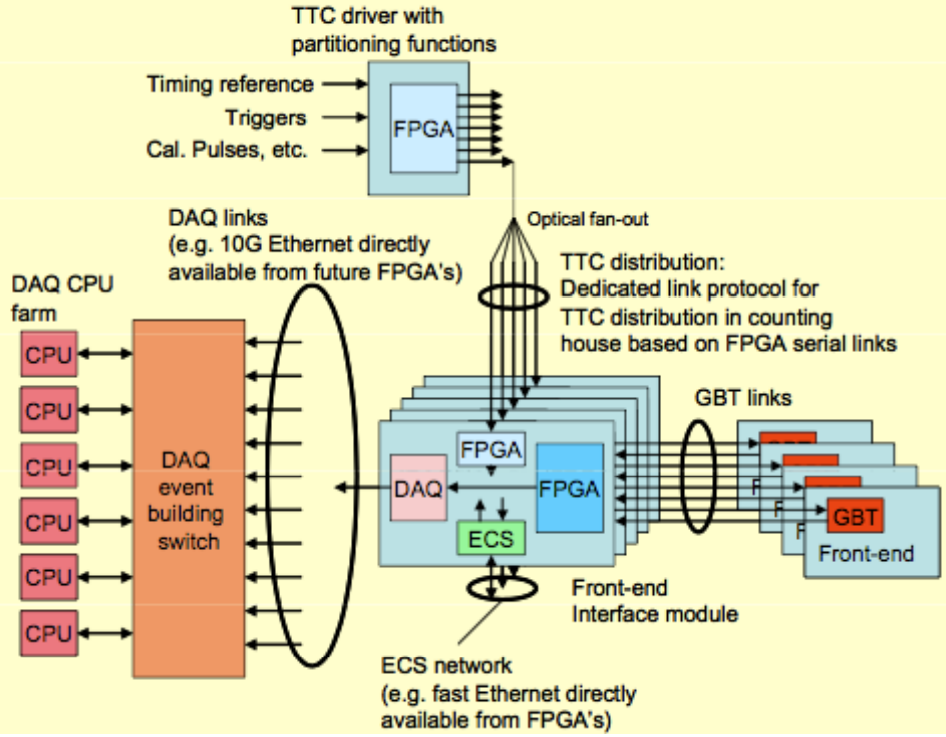
Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

NSS 2008 Paulo.Moreira@cern.ch 8

Develop Architecture

System architecture

- Decisions on the topology of the front-end link have significant effects on the global system architecture.



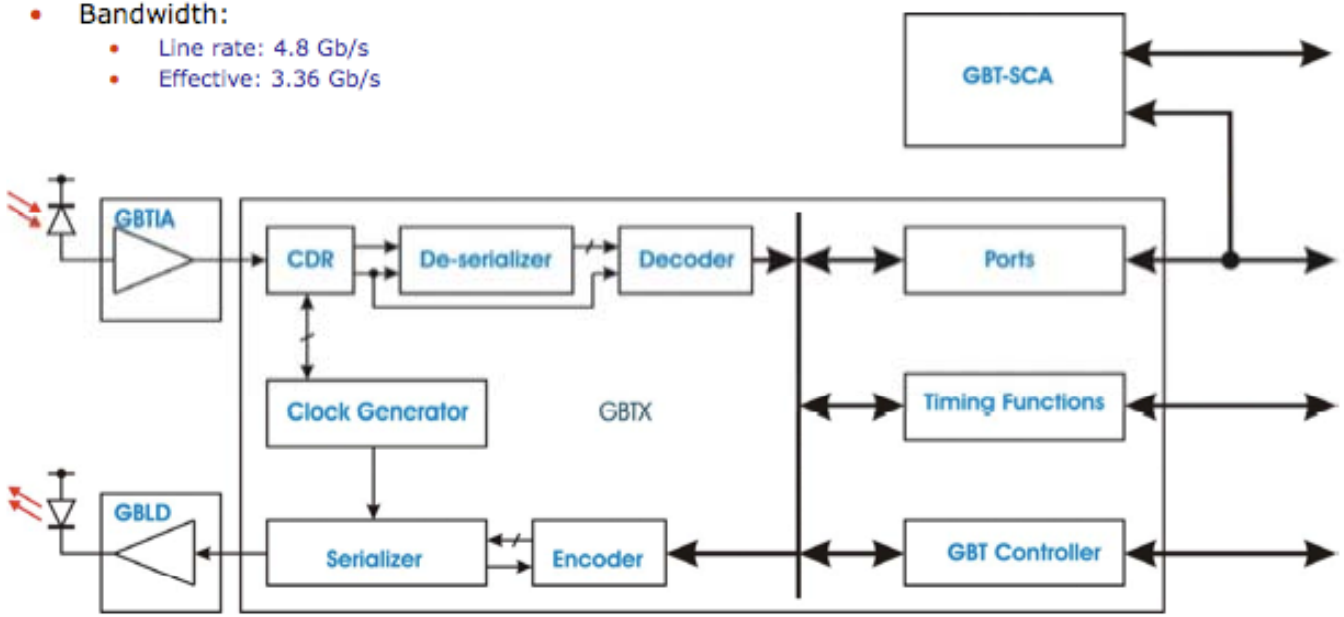
LSG Nov. 2008

slide 5

GBT chipset

GBT Chipset

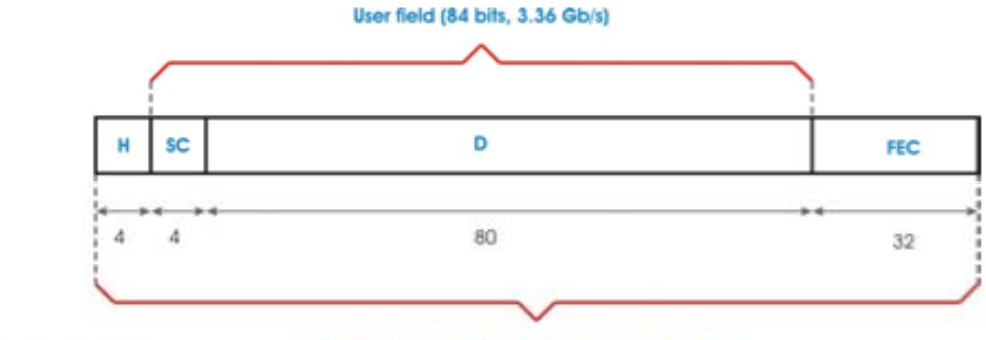
- *Radiation tolerant chipset:*
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and timing and transceiver
  - GBT-SCA: Slow control ASIC
- *Supports:*
  - Bidirectional data transmission
  - Bandwidth:
    - Line rate: 4.8 Gb/s
    - Effective: 3.36 Gb/s
- *The target applications are:*
  - Data readout
  - TTC
  - Slow control and monitoring links.
- *Radiation tolerance:*
  - Total dose
  - Single Event Upsets



GBT Link Bandwidth

User Bandwidth: 3.36 Gbps

GBT Link Bandwidth



H: Header, 4 bits
SC:
GBT control, 2 bits (80 Mb/s)
Slow control port, 2bits (80 Mb/s)
D: DATA/TTC/EC - User data, 80 bits (3.2 Gb/s)
FEC: Forward Error correction, 32 bits

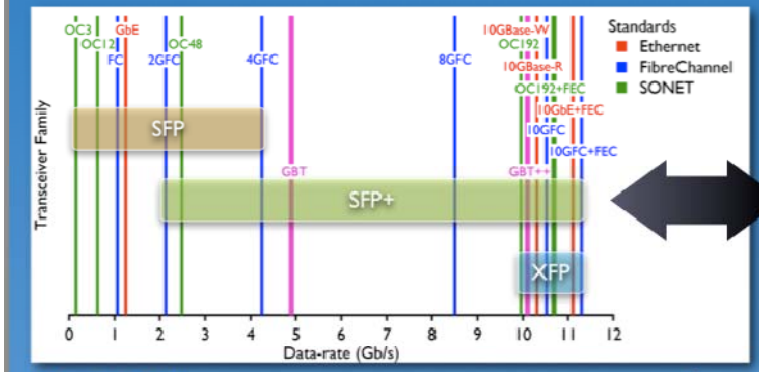
- *Bandwidth:*
  - User: 3.36 Gb/s
  - Line: 4.8 Gb/s
- *Dedicated channels:*
  - Link control: 80 Mb/s
  - Slow control channel: 80 Mb/s
- *DC balance:*
  - Scrambler
  - No bandwidth penalty
- *Forward Error Correction and Frame Synchronization*
  - Efficiency: 73%
  - To be compared with 8B/10B: 80% (no error correction capability)
- *Link is bidirectional*
- *Link is symmetrical:*
- *Down-link highly flexible:*
  (Will be clear later when discussing e-links)
  - Can convey unique data to each frontend device that it is serving
  - "Soft" architecture managed at the control room level
  - Other schemes would require dedicated topologies that will be difficult to accommodate on a generic ASIC like the GBTX
- *Now demonstrated to be compatible with FPGAs*

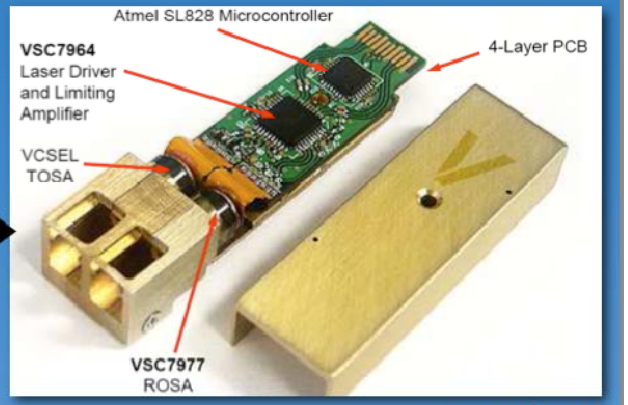
VTRx Development

VTRx_Troska.pdf (10 pages)

VTRx Customisation

- Bi-directional Module with connector interface
  - Based upon an acknowledged standard
  - Work with Industrial partner early-on
- Low Mass & Volume
  - Minimize material, avoid metals
- Non-magnetic, capable of operating in a magnetic field
  - Requires replacement of ferrite bead used in laser bias network
- MM 850nm & SM 1310nm versions

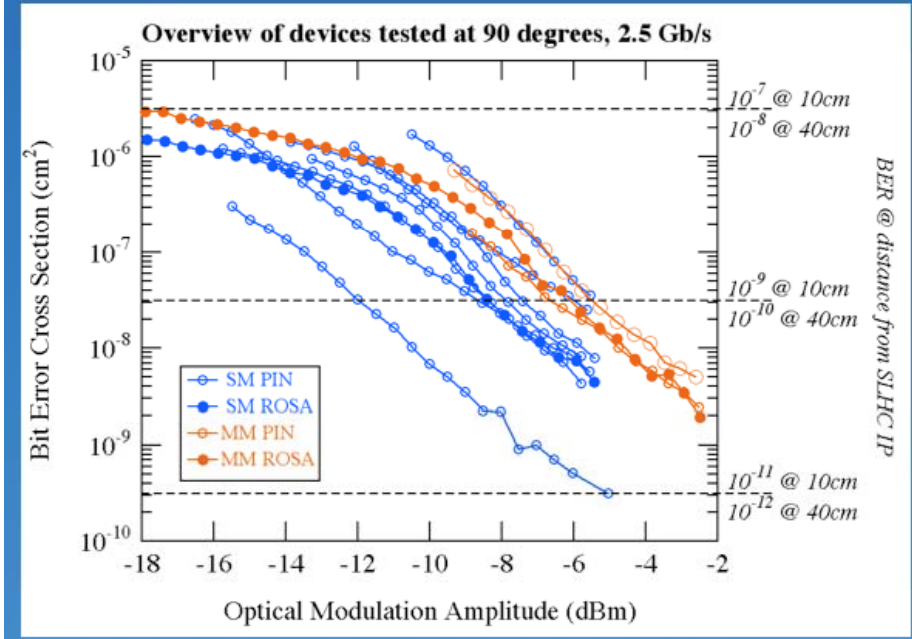




14 November 2008 2 jan.troska@cern.ch

COTS SEU studies

SEU Result Overview



- Very Similar overall trend
  - ROSA (solid symbols) not much worse than bare PINs
  - Several orders of magnitude difference in response between devices
- BER independent of Data-rate
- Burst Errors observed
  - max. 10-bits long in PINs
  - max. 00's bits long in ROSAs
  - Error correction mandatory
- Plans:
  - Total Fluence testing of Laser, PINs and possibly TIAs and Laser Drivers in early 2009

- Device Survey:

Family	Wavelength	# Device Types (# tested)
PIN MM	850nm	2 (4)
ROSA MM	850nm	1 (2)
PIN SM	1310nm	7 (14)
ROSA SM	1310nm	1 (2)
MSM MM	850nm	1 (2)

GBT Schedule

Project Schedule

- 2008
  - Design and prototyping of performance critical building blocks:
    - TIA, laser driver, PLL, serializer, de-serializer, phase shifter
  - First tests of optoelectronics components
    - (e.g. to understand SEU in PIN receivers)
  - Proceed with the link specification meetings
  - General link specification
- 2009
  - Design/prototype/test of basic serializer/de-serializer chip
  - Design/prototype/test of optoelectronics packaging
  - Detailed link specification document
- 2010
  - Prototype of "complete" link SERDES chip
  - Full prototype of optoelectronics packaging
- 2011
  - Extensive test and qualification of full link prototypes
  - System demonstrator(s) with use of full link
  - Schedule of the final production version is strongly dependent on the evolution of the LHC upgrade schedule

HCAL Needs for GBT

GBT - HCAL "requirements" (from Tullio)

- Investigate 8bit/10bit (64 bit/66 bit)
- Latency does matter
  - Max latency should not be greater than existing links
- Jitter needs to be better than QPLL
- Power dissipation should be lower than TTCrx/QPLL/GOL chipset
- Variations in latency of the GBT receiver (at detector) should be smaller than existing TTCrx receiver
- 8ns maximum over all range of operating conditions (temp, power supply, etc.)
- Estimate Latency Variations over a more limited range of operating conditions (15 - 35 C)

Issues - GOL

Concerns

- **Need to package GOLs (~$25k)**
- **Test speed of GOL link**
  - Fiber speed - OK. Test final config for BER
  - Connections - will reduce max speed
- **Need to live with TTC system**
  - Will this system be maintained when other subsystems switch to GBT in Phase II?

Issues - GBT

Concerns/Comments

- **Need to design HCAL system architecture/topology**
- **How do we establish bunch synchronizing across asynchronous links? (from Jeremy)**
  - Similar to GCT problem
- **GBT protocol - data frames are self synchronizing**
  - No need to send idle frames (abort gaps can be used for other things (Tullio comment)
- **System requirements set by large users**
  - HCAL does not have many channels
    - **HCAL needs will not get priority**
    - **Adding additional features adds "unnecessary" complexity to the chips/system**
- **GBT schedule is very tight for Phase I upgrades**
- **Tullio is starting to work on this project**
  - FPGA market survey and GBT emulator for FPGA testing