

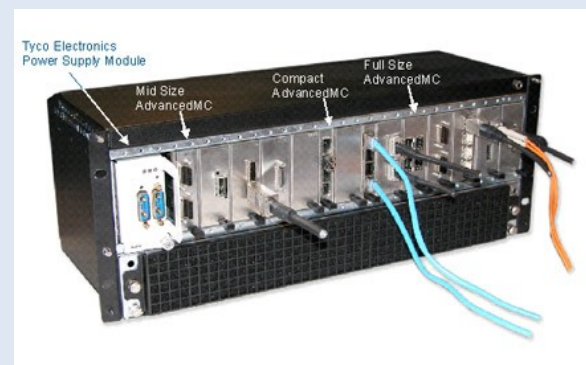
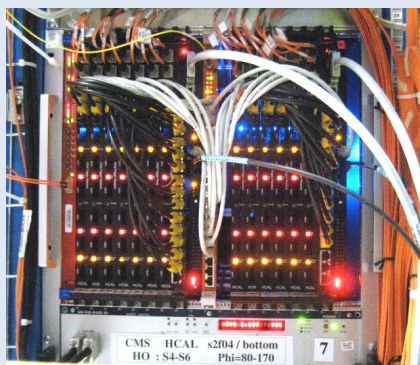
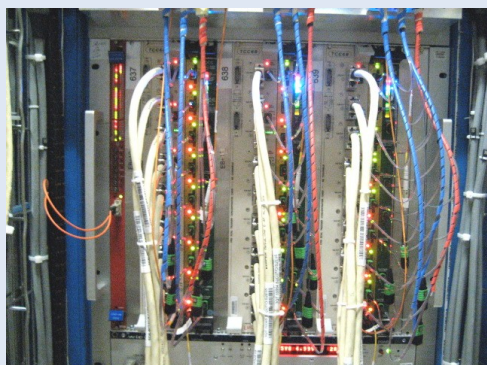


# Fermilab CMS Upgrade Workshop November 19-20, 2008

## Calorimeter (off-detector) DAQ electronics

Eric Hazen, *Boston University*

On behalf of my ECAL and HCAL colleagues





# Outline



- Calo TriDAS upgrade goals and constraints
- Review of HCAL and ECAL off-detector electronics
- Hardware Upgrade Options **Covered well by J. Mans' talk**
  - Summary of Options
  - Upgrade "Scenario I"
- Selective Readout
  - Review current ECAL scheme
  - Possible combined schemes
- DAQ Path Issues
- Staging options, compatibility with existing system
- Summary



# Calo TriDAS Upgrade Goals



- Necessary:
  - HCAL front-end changes
- Channel count, TDC data, etc
  - ECAL+HCAL: DAQ hardware changes, Lumi increase... more BW
  - ECAL+HCAL: Trigger – RCT opto inputs, architecture changes?
- Desirable:
  - DAQ: common local/global readout path
  - Combine ECAL and HCAL in common hardware (\$\$\$ savings?)
  - Provide for combined selective readout of ECAL and HCAL
  - Data compression in DAQ path
  - Provide more FPGA resources for calo trigger near detector
  - Comply with enforced or de-facto CMS standards
  - ... others?



# Calo TriDAS Upgrade Constraints



- Common

- 100kHz L1A limit stays
- L1 latency also same
- DAQ B/W likely will increase, but not necessarily by 2013
  - Must compress data if payload increases

- ECAL

- No changes in EB front-ends or links (EE not likely either)
  - L1 trigger towers stay the same in EB
  - EE could use partial sums in some clever way

- HCAL

- Use same data fibers, so speed limited to  $\sim 6\text{Mb/s}$  (guess!)
- Replace back-end, so  $\sim$  complete design freedom (limited by cost/schedule)

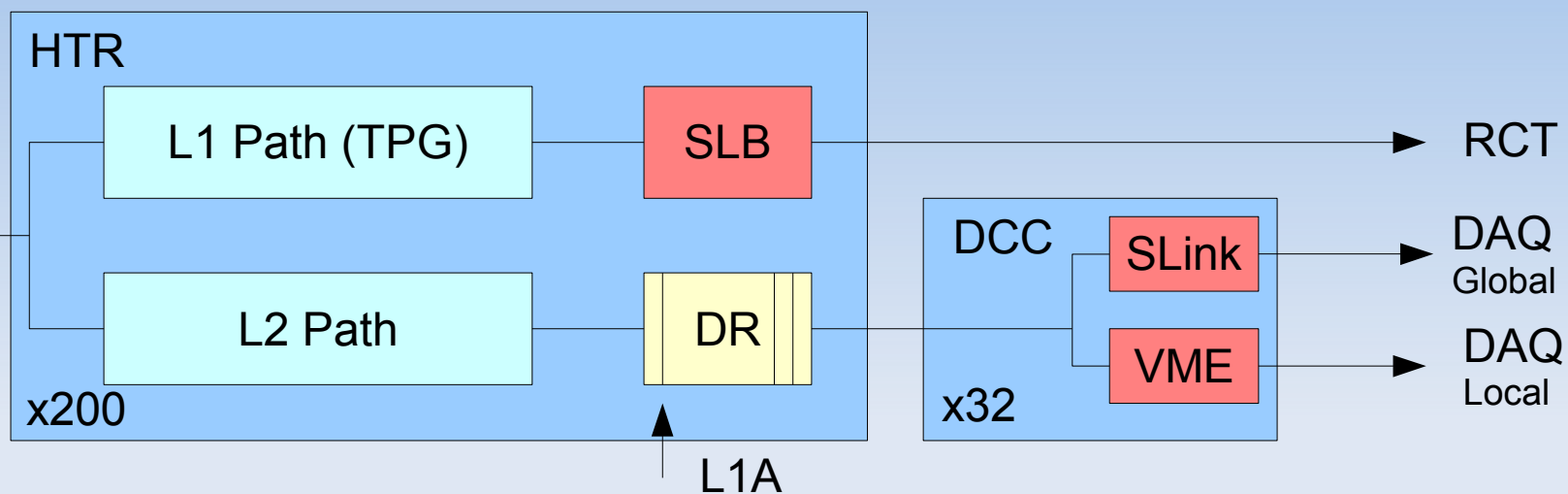


# ECAL/HCAL processing (Current system)



## HCAL

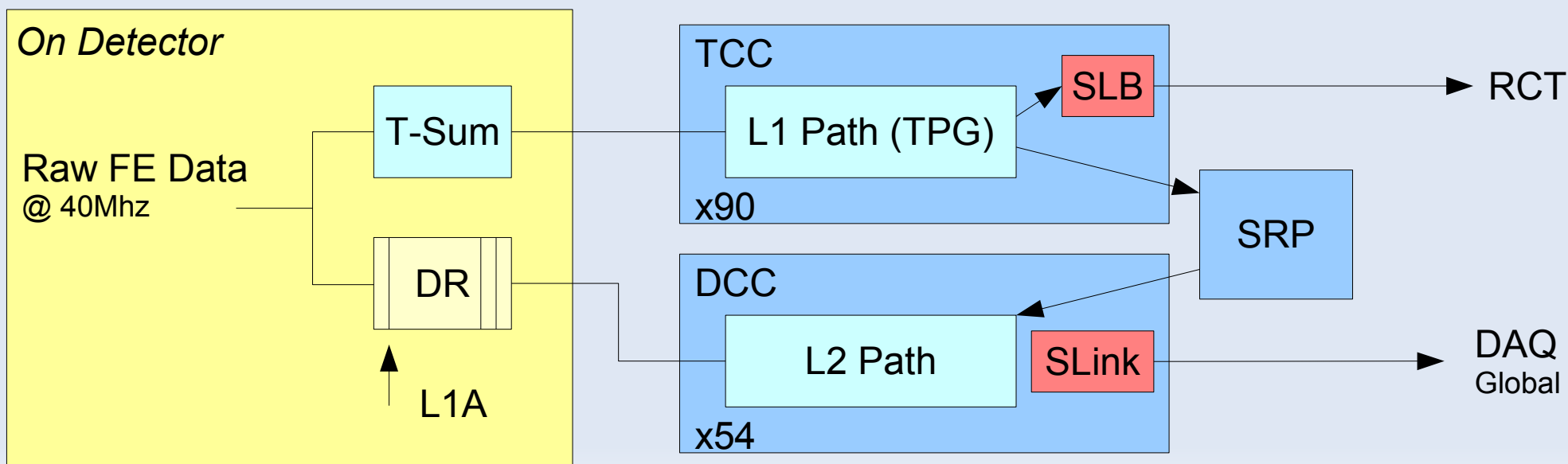
Raw FE Data  
@ 40Mhz

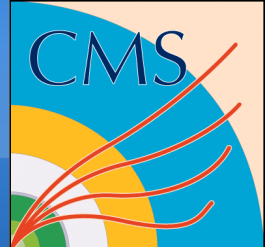


## ECAL

*On Detector*

Raw FE Data  
@ 40Mhz





# Upgrade Options

- ECAL Alone
  - New DCC
  - New TCC or optical SLB
  - Modify SRP algorithms
- HCAL Alone
  - New HTR+DCC system with SR capability
- ECAL+HCAL together (my "Scenario I")
  - New "CTR" (Calo Trigger Readout) card
    - Receive ECAL trigger, data and HCAL data
    - Generate TPs, possibly perform some RCT processing
    - Perform selective readout processing on board
  - New "DTC" (Daq / Timing Card)
    - Distribute timing/control signals to CTRs
    - Harvest DAQ data using SR flags



# Selective Readout

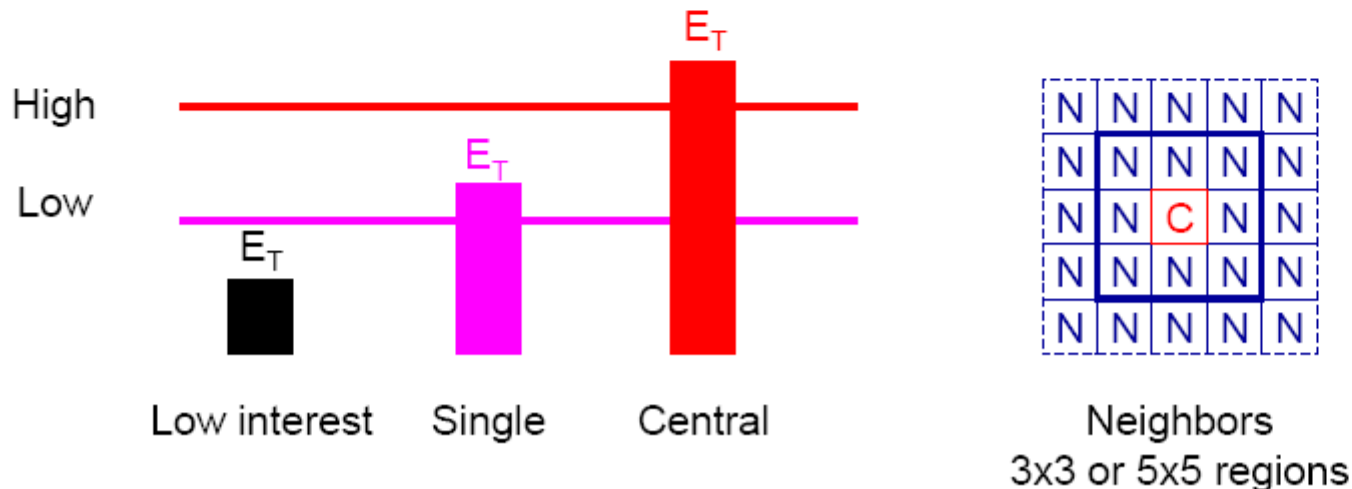


- Review of existing ECAL SR
- Implementation options

# Selective Read-out Algorithm (executed per L1A)



- Input: 3-bit flags per TT
  - 2 LSB indicate energy threshold exceeded by energy deposited in TT
    - 00:  $E_T < TH_L$
    - 01:  $TH_L < E_T < TH_H$
    - 10: Error
    - 11:  $E_T > TH_H$
  - MSB (forced flag) is set by TCC in abnormal (erroneous) situations
- SRP internally classifies TTs according to their energy and neighborhood



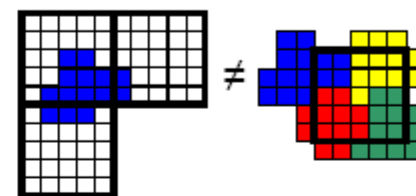
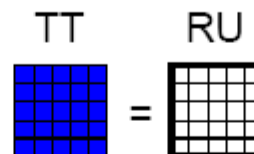


# Selective Read-out Algorithm (executed per L1A event)



- SRP derives RUs that form TTs

- straightforward in barrel
- complex in endcap



- Classifies RUs according to TTs they form

- promote RU to the highest priority flag of the TTs it participates in:
  - Central > Neighbor > Single > Low Interest

- Assigns SR actions to each RU

- Possible actions

- 00: do not read
- 01: read with ZS level 1
- 10: read with ZS level 2
- 11: read all

- Any association RU Type → SR Action is possible

- programmable:

→ standard algorithm: Low interest → ZS level 1; Central, Neighbour, Single → Read all

- Output: 3-bit flags per RU

- 2 LSBs = SR actions
- MSB (forced flag) is set by SRP in abnormal (erroneous) situations

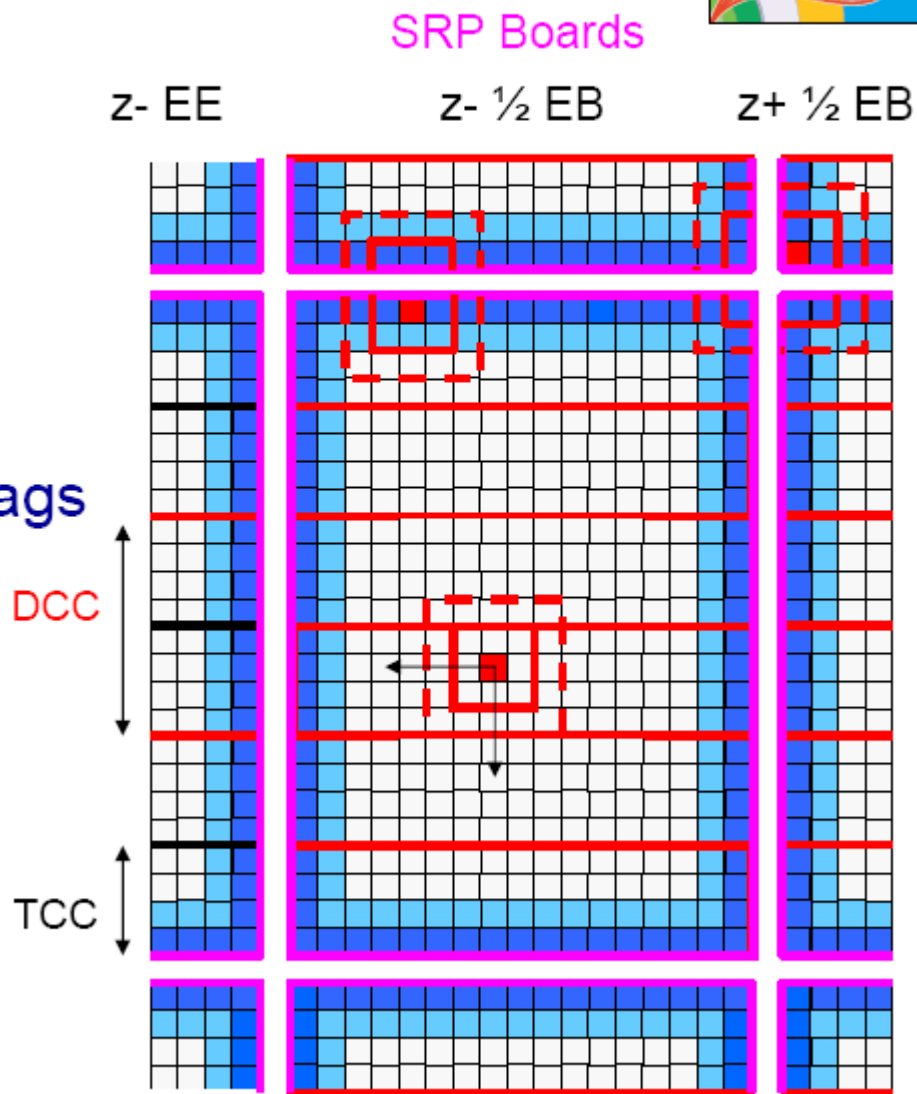


# Selective Read-out Algorithm



- $n \times n$  sliding windows
  - 3x3 and 5x5
  - programmable per SRP board
    - *i.e.* may differ in EB and EE

- SRPs exchange frontier TT flags
  - up to 9x9 windows are possible
    - *i.e.* future extensions possible





# ECAL Selective Readout Processor



dapnia

cea

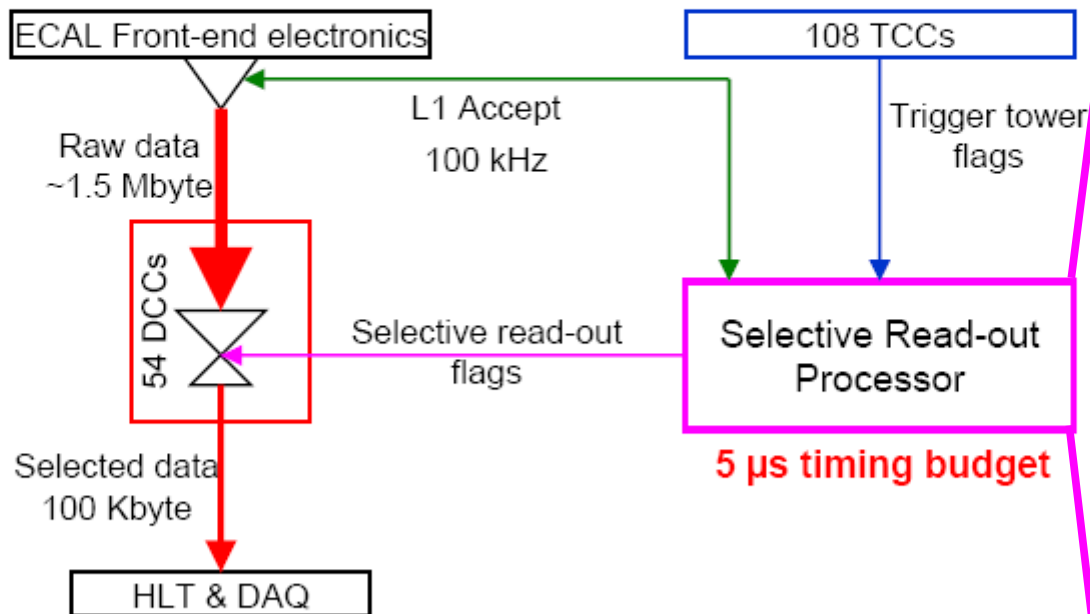
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## Selective Read-out Processor

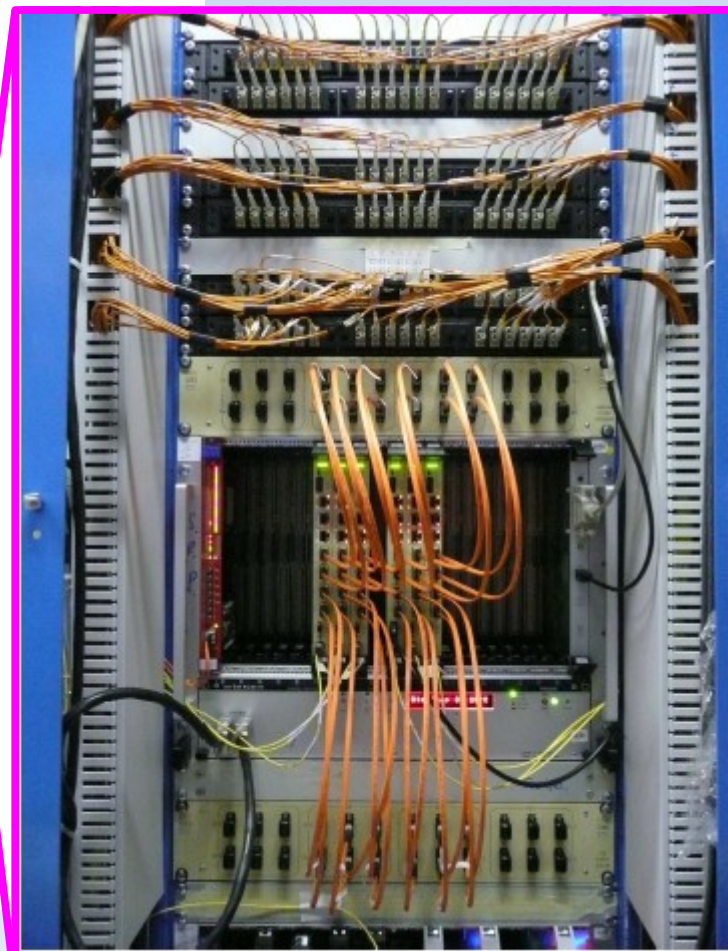


- Part of the CMS electromagnetic calorimeter read-out

→ Assists in on-line ECAL raw data reduction



Asynchronous hard real time system

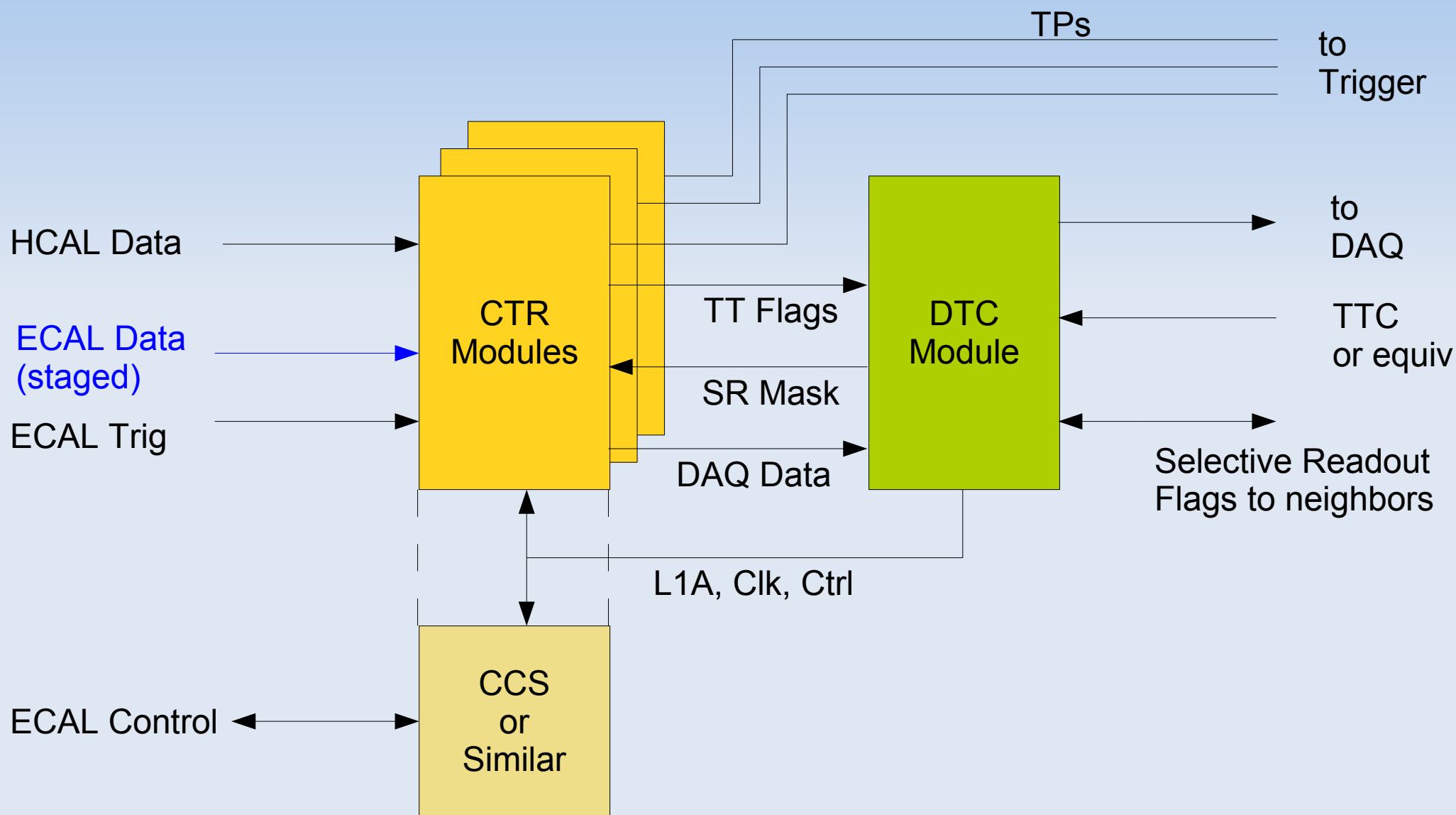


Irakli.MANDJAVIDZE@cea.fr

EE SRP meeting, CERN, 26 Mars 2008



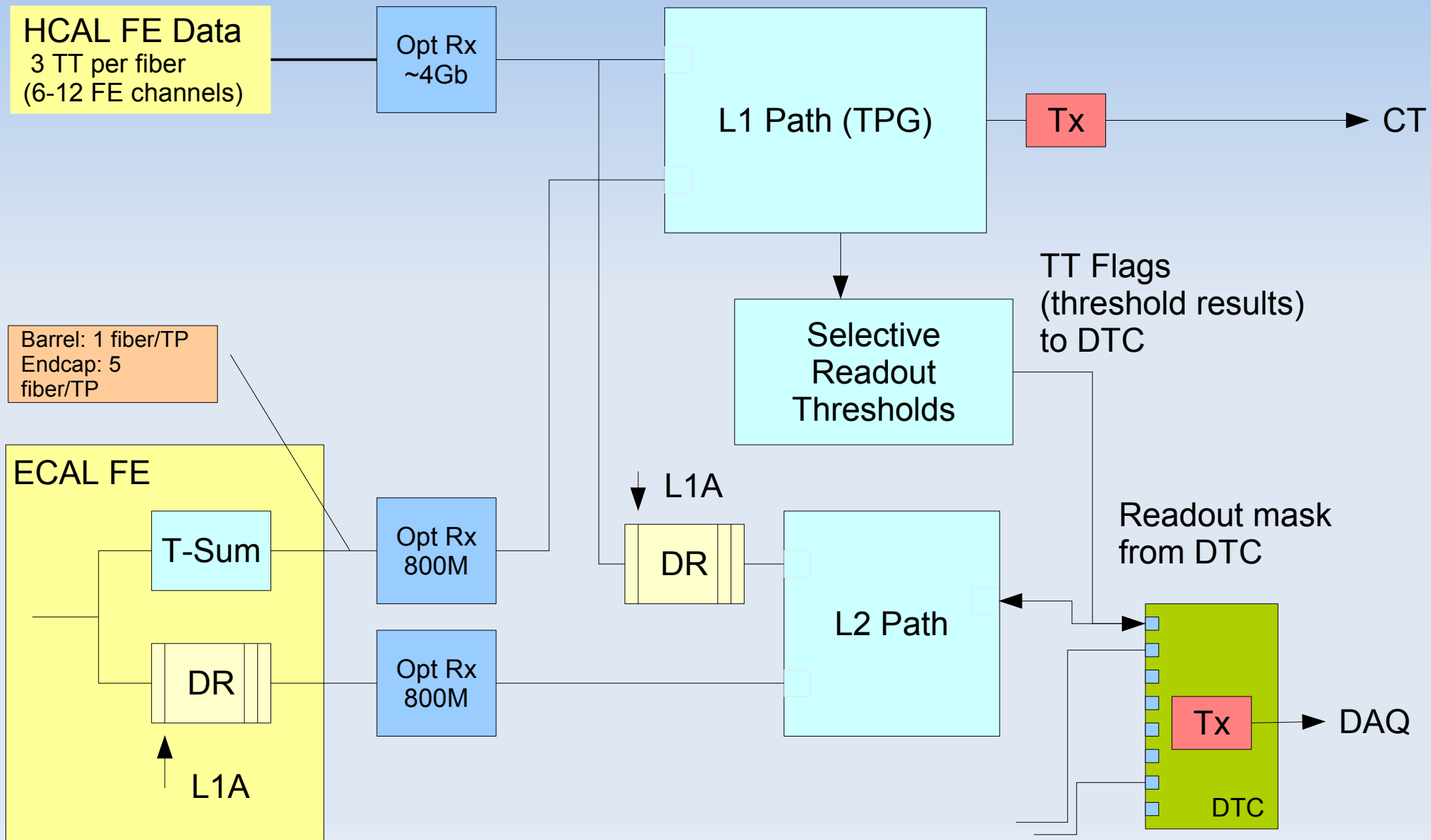
# Upgrade Scenario I





# Upgrade Scenario I

## CTR Module Details





# Cable/Fiber Counting for CTR boards



Barrel -- 25 crystals = 1 TT

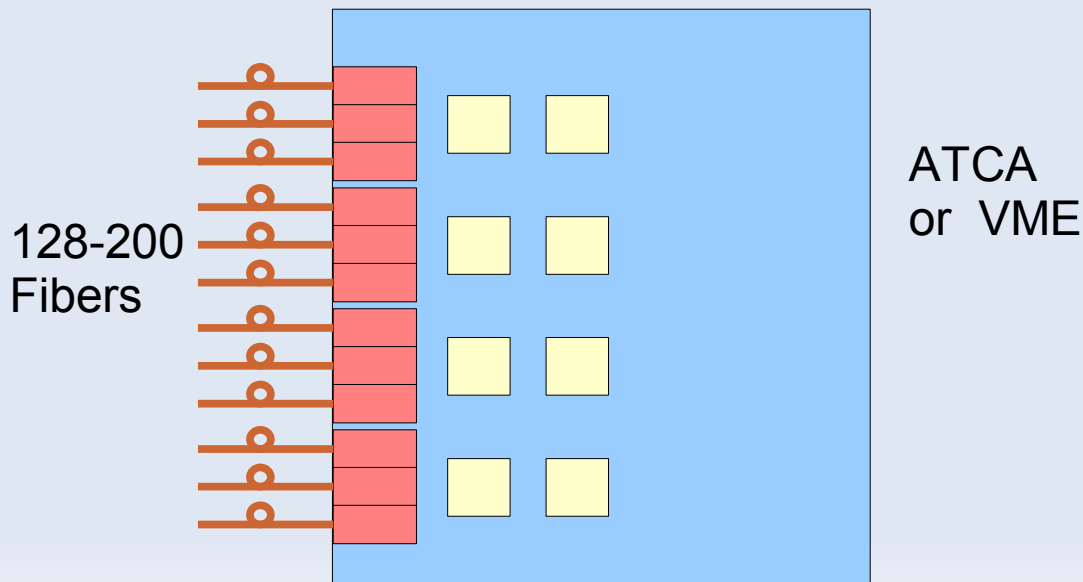
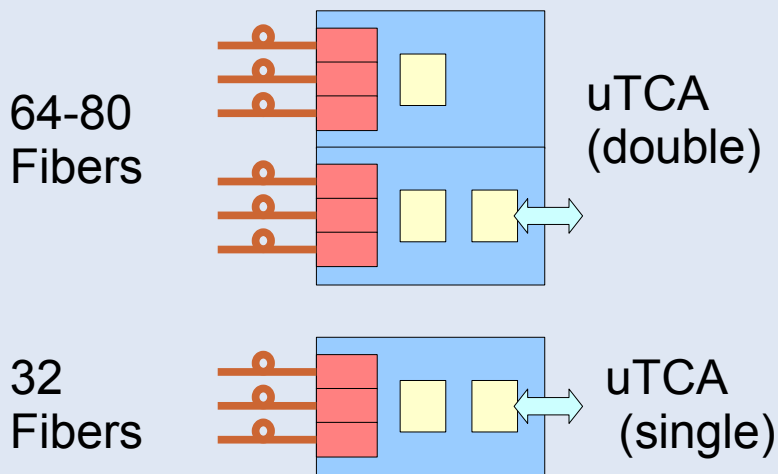
HCAL	1 fiber	for 3 TT
EB	6 fibers	for 3 TT
TP Out	<u>1 fiber</u>	
<b>Total</b>	<b>8 fibers</b>	<b>/ 3 TT</b>

2448 TTs total	Boards	Crates
uTCA board(1) - 12 TTs	~200	~16
uTCA board(2) - 24-30	80-100	8-10
ATCA/VME - 16-25 TTs	100-150	10-14

Endcap -- 25 crystals = 1 RU

HCAL	1 fiber
EE	18 fibers
TP Out	<u>1 fiber</u>
<b>Total</b>	<b>20 fibers</b>

624 RUs total	Boards	Crates
uTCA board(1) - 1 RU	624	52
uTCA board(2) - 3-4 RU	150-200	14-16
ATCA/VME - 6-10 RUs	60-100	5-10





# DAQ Path



Currently 512 FEDs possible (in theory)

Each receives  $100\text{kHz} * 2\text{kB} = 200\text{MB/sec}$

Upgrade plans (no details yet)

- Same 100kHz max L1A rate

- "Significant" additional bandwidth capability

- Use commercial standards for networking

- Common readout path for global and local DAQ

- If possible embed TTC/TTS/control path in same links

To accommodate 10x more bandwidth, we would need 2GB/sec per FED:

- Two 10GbE links in parallel per FED?

- Single 40GbE or other link per FED?



# DAQ Path Upgrades



Hard to plan without more DAQ group input, but here is a start:

- ~ 10x current throughput internally

- Build in support for full calo selective readout

- Provisions for local / global DAQ via same link

- Commercial standard (i.e. 10GbE), perhaps on daughterboard

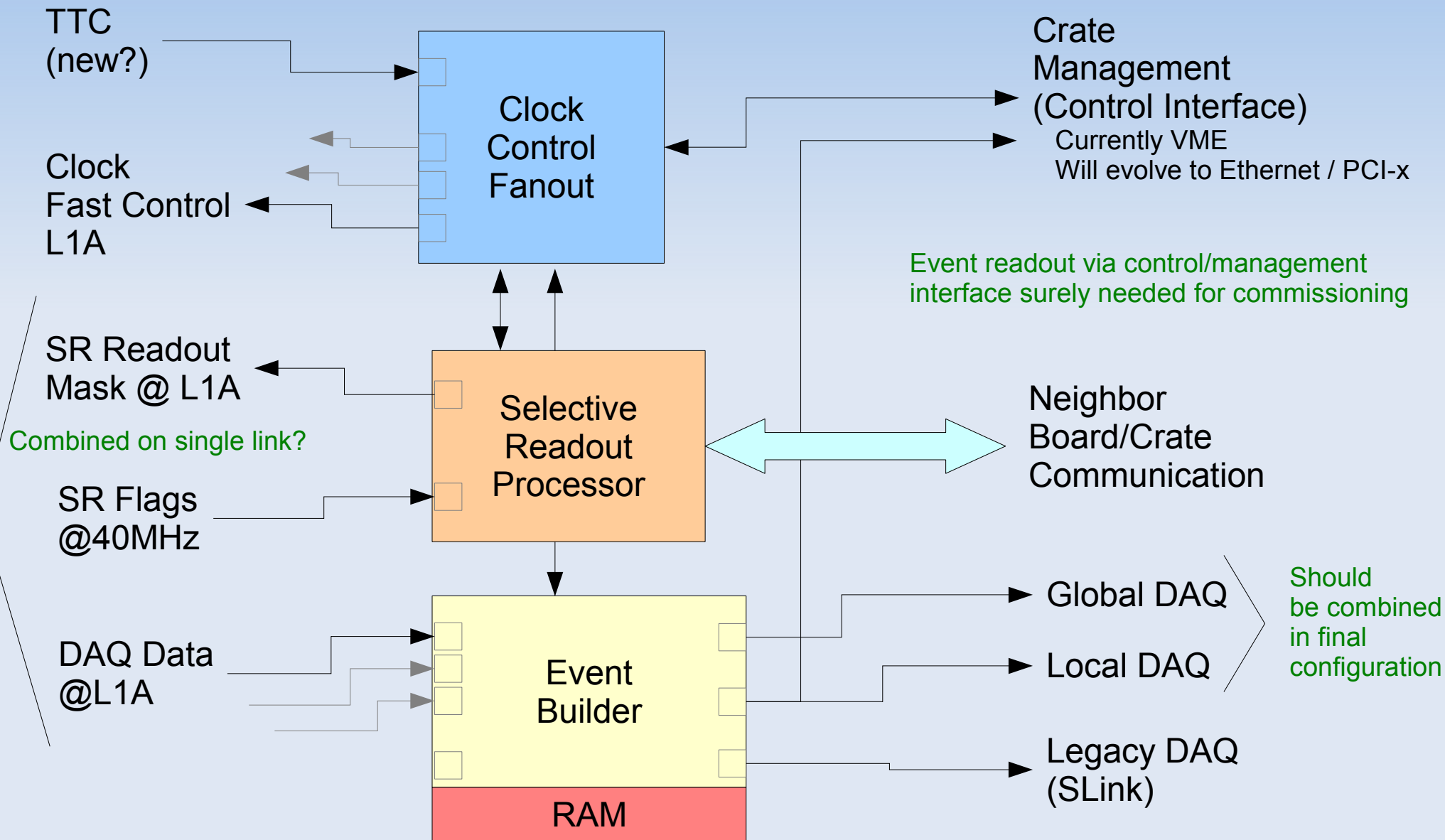
- Adapter to support current S-Link

- Provisions for TTC-like control on network link as well as current TTC





# DTC (DAQ/Timing Card)





# DAQ Bandwidth Estimate



- Per TT/RU: ~ 50 bytes *per timesample*
  - HCAL: 4 depth segments @ 16 bits each
  - ECAL: 25 crystals @ 8 bits each
  - Both: TP's and overhead, say 50%
  - $50 * 100\text{kHz} * 10 \text{ timesamples} = 50\text{MB/sec per TT}$
- Total ECAL+HCAL = 68 FEDs @ 2k bytes \* 100kHz
  - ~ 14 Gbytes/sec total / ~ 4100 TT = 3.3MB/sec per TT
  - So, we can send only about  $3.3/50 = 7\%$  of the data
  - For Jeremy's example 34 TT FPGA, this is ~ 120MB/sec per FPGA average, but must handle peak rate of  $50*34 = 1700 \text{ MB/sec}$  to RAM



# DAQ/Timing Card



- Design details depend heavily on packaging standard
  - ...which should rightly be driven by other system issues
- Current system uses cables / fibers for all inter-module links (except VME)
  - This can and should change- ATCA and uTCA both support sufficient backplane bandwidth for SR / DAQ purposes
- Must realistically support existing infrastructure (SLink, TTC)
  - Easy for larger formats (ATCA, 9U VME)
  - More challenging for uTCA
  - For DAQ output, fiber with SLink adapter may be best bet



# Summary



- Integration of many functions on DAQ card makes sense:
  - ECAL/HCAL DCC
  - ECAL SRP
  - ECAL/HCAL TTC fanout system
- Prototyping can be done with existing or planned hardware (at least in uTCA)
  - UMN "mini-CTR" board for CTR
  - Matrix card for larger scale tests
  - UW TTC/Slink-64 card for DTC
- Packaging choice should not be driven by DAQ path
  - ...and design cannot proceed very far until this is settled
- Common hardware for ECAL / HCAL CTR and even DTC is not excluded