Optimizing the Calorimeter Performance with a Depth-Segmented HCAL

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Implications for Trigger and DAQ Electronics

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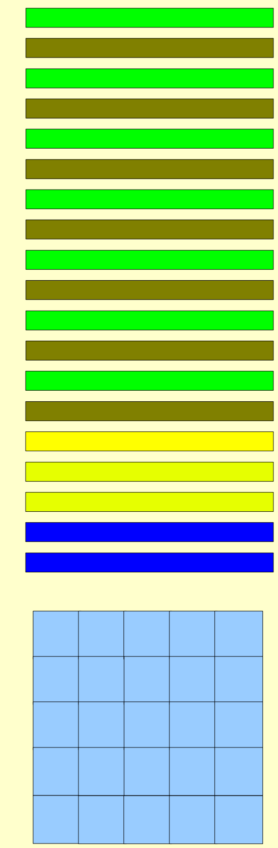
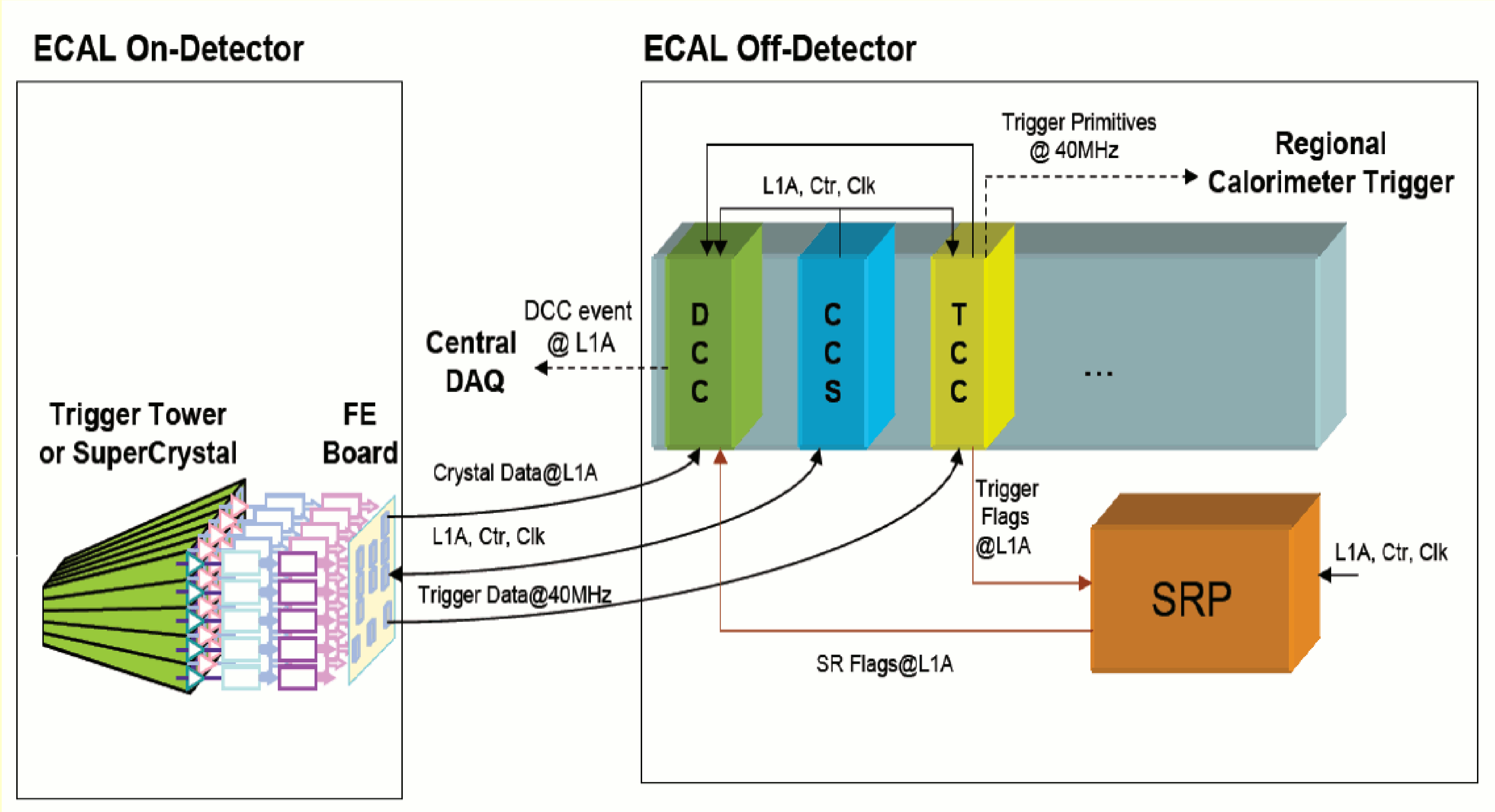
Strawman structure

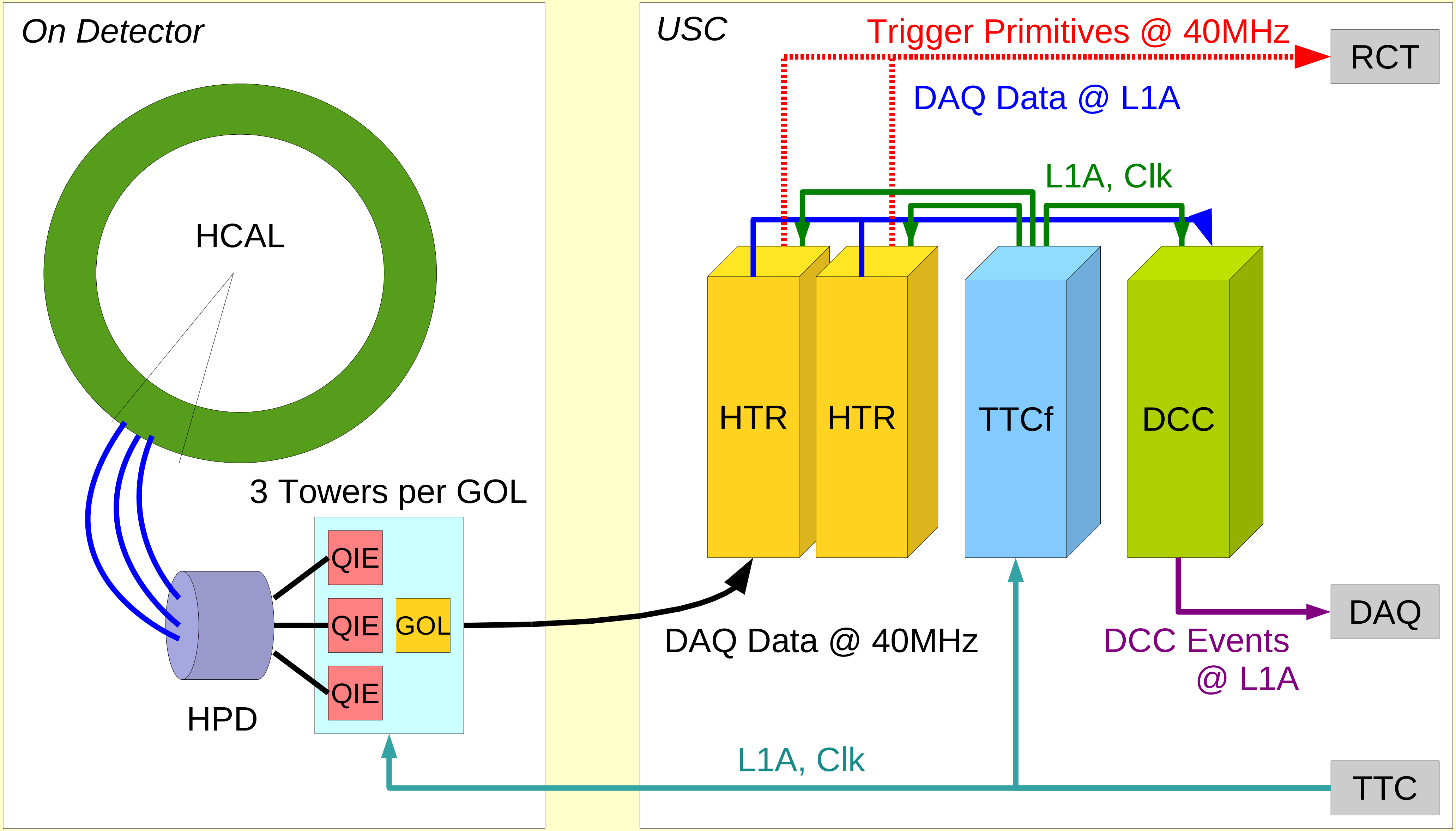
- The draft structure for an upgraded HCAL brings a significant increase in longitudinal segmentation
  - In particular, the layers nearest ECAL are grouped into separate readouts and the deeper layers are proposed to be interleaved
- In the SLHC environment, such segmentation can bring big advantages – as shown by C. Tully's group in their study of pileup effects at high luminosity
  - The layers closest to ECAL are "always occupied" at luminosities much above 10^{34}



Existing Infrastructure

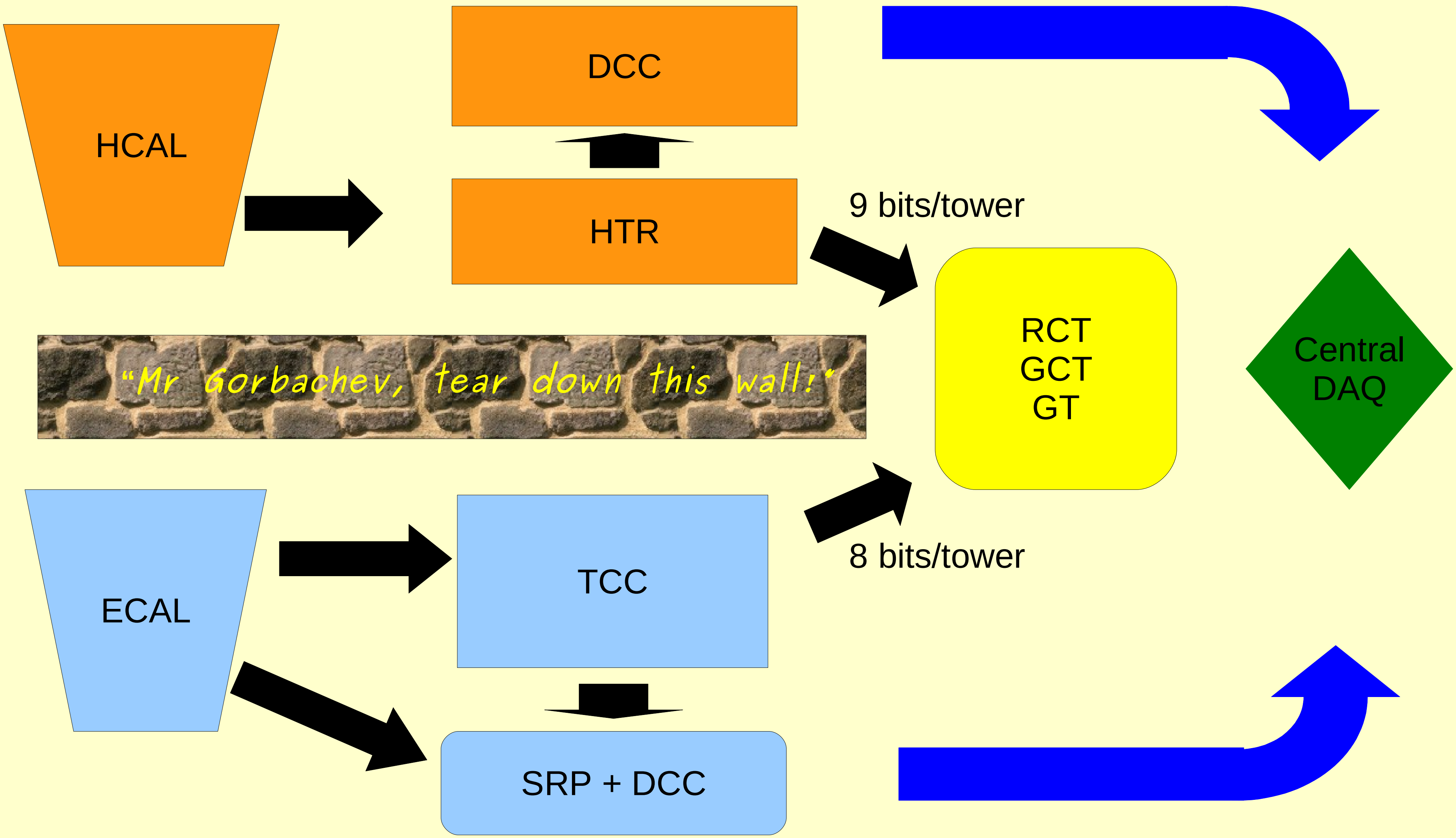


Existing Infrastructure (II)



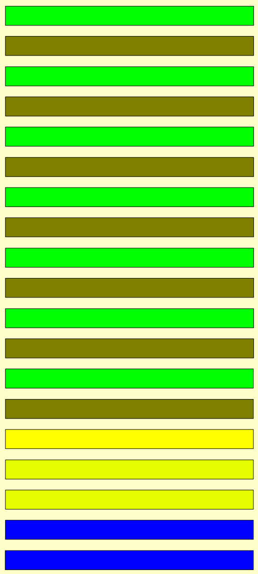
Thanks to E. Hazen

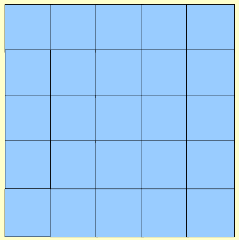
Existing Infrastructure (III)



Detector/Physics Motivations

- Trigger: E/H cut's effectiveness will be washed out by pileup contributions from first layers in a summed tower
  - If ECAL and HCAL energy are combined early (with full depth information for HCAL), we can optimize the use of the later depths for E/H requirements
- Additional considerations
  - Dynamic range in link to trigger need not be determined by requirement to support E/H cut => allows the jet and e/gamma paths to be tuned completely independently





Detector/Physics Motivations (2)

- Selective Readout: increase in HCAL channel count by a factor of four will require many more DAQ links or much harsher zero suppression exactly at the moment when it becomes harder to perform such suppression due to pileup
  - ECAL has faced this issue already: selective readout of regions of interest, but only based on ECAL seeds.
- Proper solution would allow for mutual seeding of ECAL based on HCAL and HCAL based on ECAL
  - Provides readout of necessary depths for isolation cuts on the E/Gamma path as well as fine-grain ECAL information for jets
- E. Hazen will discuss this issue in more depth in the next talk

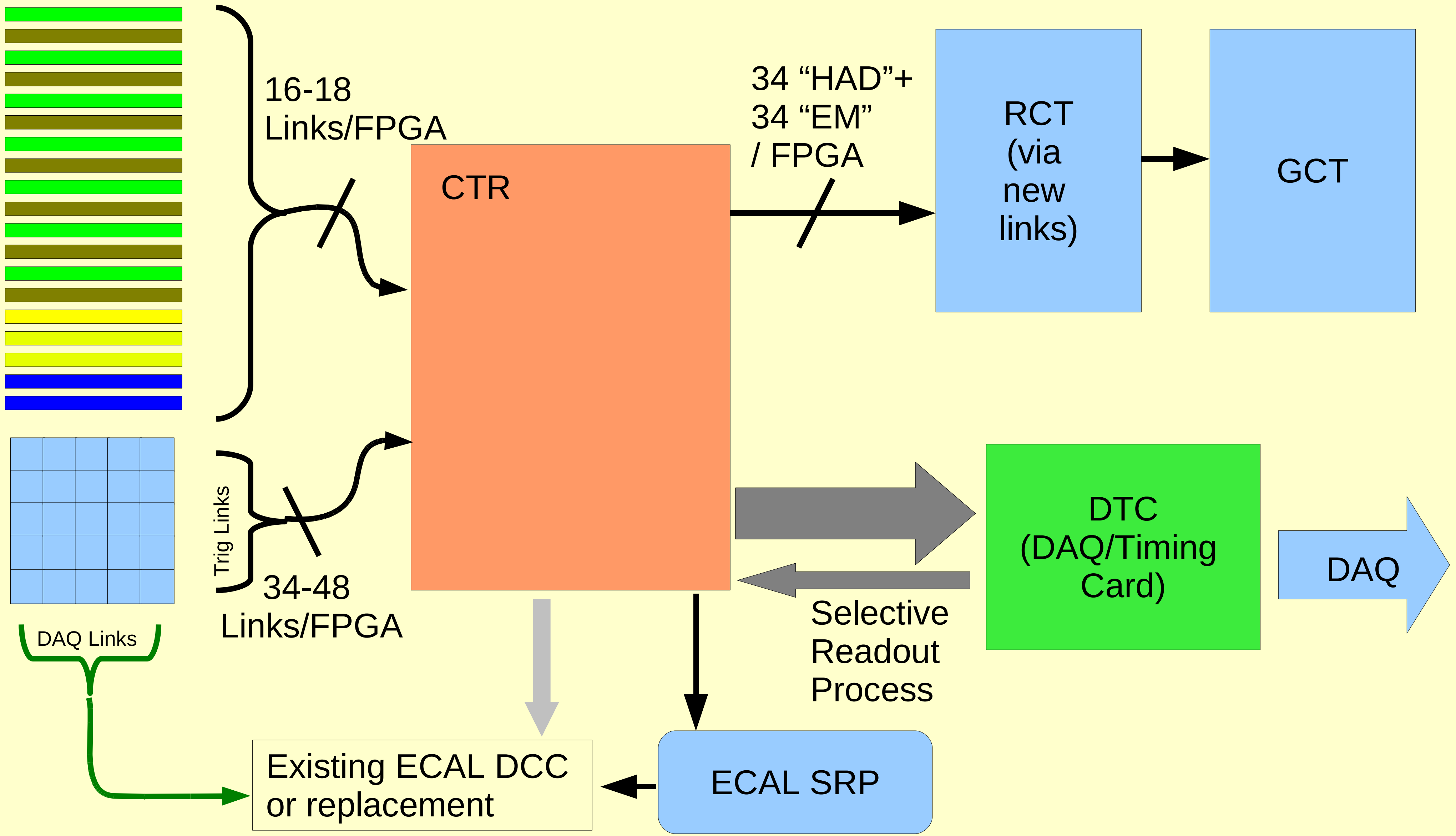
Numerology

- Barrel (EB definition) : 17 eta x 72 phi
  - Each phi requires 17 fibers of ECAL trigger data, 9 fibers of HCAL data (8 fibers from HB, 1 from HE)
  - Open question: do we need input from HO to control MET rates?
- Endcap : more complex
  - ECAL sends 1 fiber/5 crystals
  - HCAL has changing phi granularity (72 --> 36)
    - Expect that iphi 29 is completely split
  - Estimate: require 6 HCAL + 30 ECAL fibers for "1 phi"
- Forward : no ECAL, but stronger motivation for jet improvements
  - Sub-region information may improve the jet trigger performance significantly in SLHC conditions

Staged Upgrade

- Deployment of a complete system in a single short shutdown is challenging, possibly risky: staging is a useful tool for managing risk
- Stage 1: Replace TPG electronics, replace RCT receiver cards
- Stage 2: Upgrade calorimeter trigger to provide finer jet granularity, feed information to tracking system, etc
  - TPG electronics must be designed to cope with higher bandwidth requirements of Stage 2

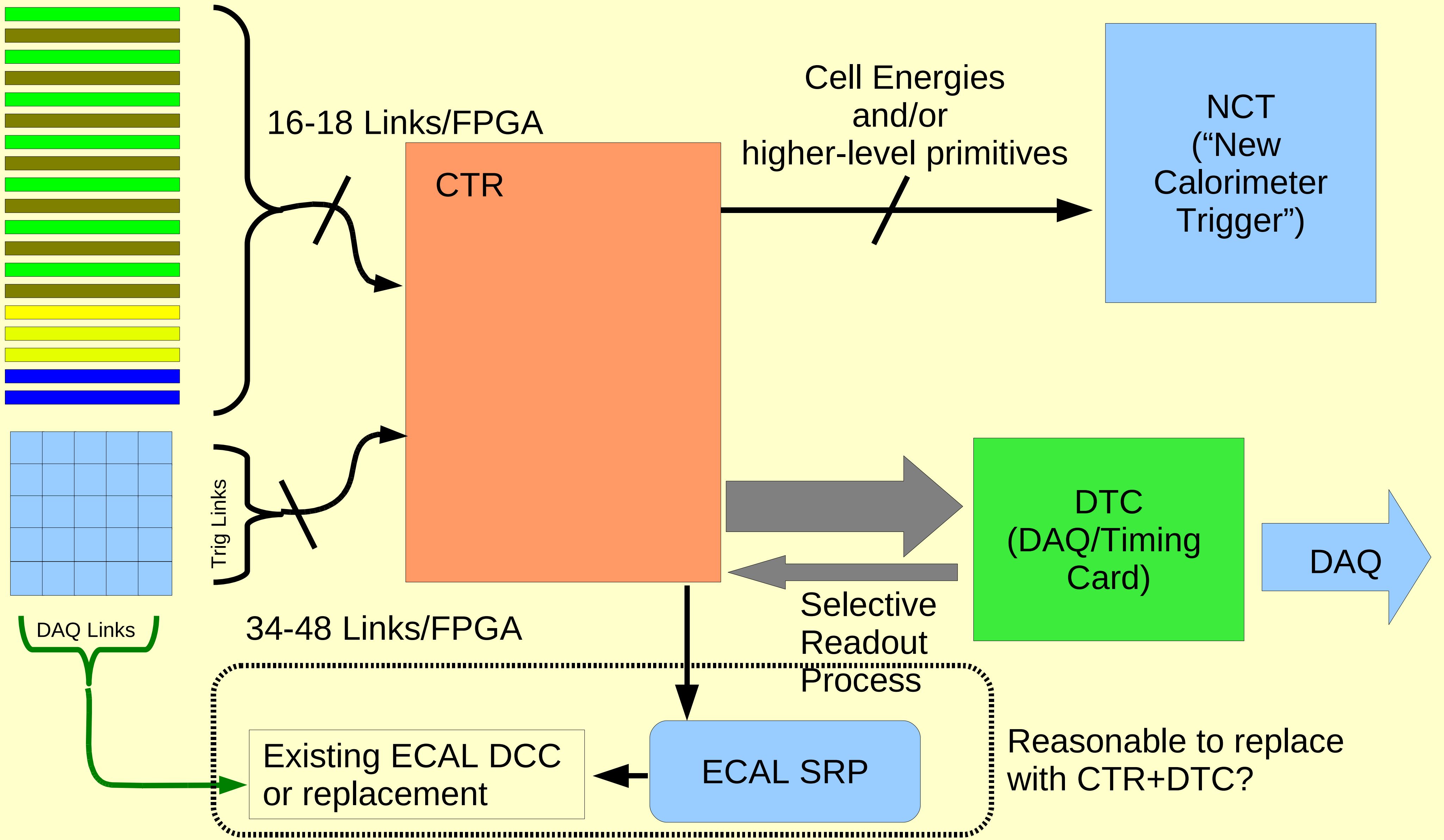
Stage 1 Architecture



A Few Thoughts about Stage 1

- With proper design, it should be possible to begin phasing in the back-end upgrade *before* HCAL front-ends are replaced – receive/process existing HCAL and ECAL data streams
- Sourcing both the "ECAL" and "HCAL" link to the RCT from a single source would allow us to consider the full 17 bits which are sent for a tower holistically
  - Possibility: use ten bits for total energy and the additional seven bits to indicate the E/H ratio and isolation quality
  - Flexibility provided by the RCT LUTs may be crucial in this case: possibility of quite sophisticated algorithms in encoding the information

Stage 2 Architecture



Key Technology Questions

- Can we receive the ECAL Trigger links with reasonable resource utilization?
  - Yes*: Xilinx Virtex 5 FPGAs contain simple deserializers on every input pair. These deserializers, coupled with FPGA logic, are capable of decoding the 800 Mbps GLINK stream from the ECAL front ends.
    - Qualification: basic functionality constructed for single channel with “miniCTR” card and GOL test card via copper (LVDS). Further development and study necessary, eventually with multiple channels.
  - Key issue: scarce resources (high-speed deserializers) are not consumed by slow links, but data can be concentrated for combined processing

Key Technology Questions (2)

- Does the link counting work out?
  - Large Virtex 5 FPGAs have 16-20 high speed tranceivers
  - If we can couple the trigger link rate and the detector link rate (e.g. if the detector link is fast), we can use transmitters of transceivers to drive to trigger electronics. If not, FPGA count will increase significantly.
- Does this strategy require uTCA?
  - No. It can be developed using traditional VME technology with the use of front-panel interconnections or possibly a custom backplane. However, it would match well with uTCA, particularly as a unifying technology in Stage 2 of the upgrade.

Project Questions

- What is the incremental cost for unifying ECAL + HCAL?
  - Remember: new electronics of much this design will be required by the new HCAL front ends in any case
  - Very small: the only direct costs are additional parallel optical receivers and a small increase in board complexity
  - Associated cost: optical receiver upgrade for RCT (to keep avoid latency increase while increasing bandwidth of the processing)

Project Questions (2)

- How can we deploy/commission this system safely in a live experiment which is taking physics data?
  - Designing the system to support the "latency" links from the HCAL front ends should allow any of several deployment strategies
    - Partial/complete upgrade of HCAL with changeover of Hadronic channels of RCT, followed by shift of ECAL to combined system and front-end upgrades
    - Starting upgrade in HF and proceeding with HCAL + ECAL
    - Partial replacement of HCAL front-ends if a single shutdown is too short (e.g. HB only or HE only)
  - Gather operational experience using optical splitters on live detector with prototype electronics

Next steps

- Hardware
  - Fully validate reception of ECAL trigger links with Virtex 5 deserializers (is a TCC development/test/transmitter board available?)
  - Resolve link questions for HCAL Front End
  - Check connectivity requirements for use of existing ECAL electronics (RCT, DCC) [Seems ok, needs to be checked]
- Simulation
  - With high-pileup simulation, study the improvements available to the trigger performance with such a structure
  - Similar work needed for selective readout (Jet/Met participation?)
- Technology decision
  - uTCA versus VME will need to be resolved in the second half 2009