FE Electronics: TDC, Clocking & Control

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20th November 2008 / SLHC Workshop, FNAL

Outline

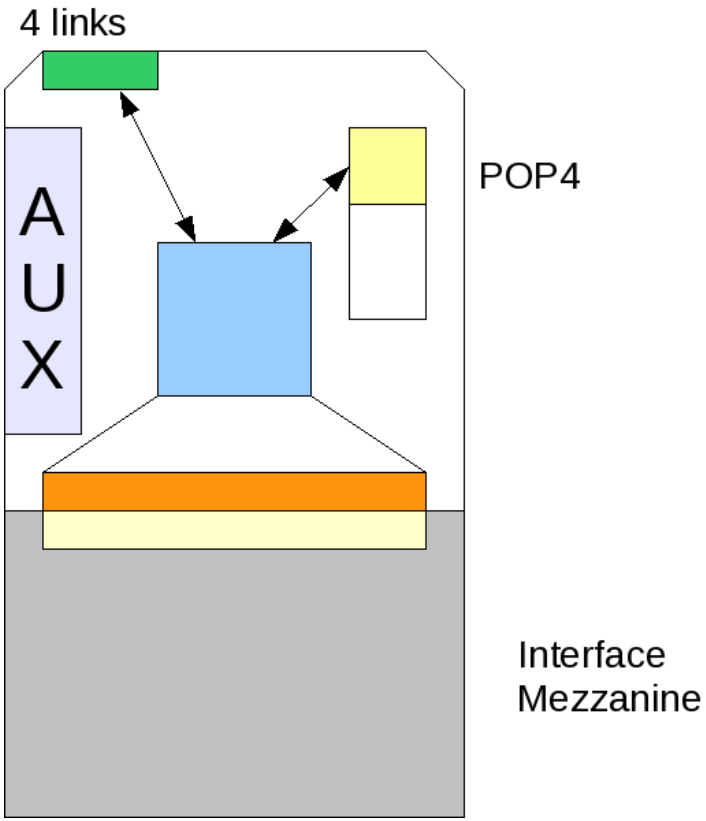
- Requirements for TDC, clocking, etc...
- μDAQ card
- 4-phase TDC + clocks in a Xilinx Virtex-5
- SEU mitigation & scrubbing

Requirements

- Phased clock per QIE
- TDC per channel
- Configuration of QIEs
- (Unforeseen) additional functionality

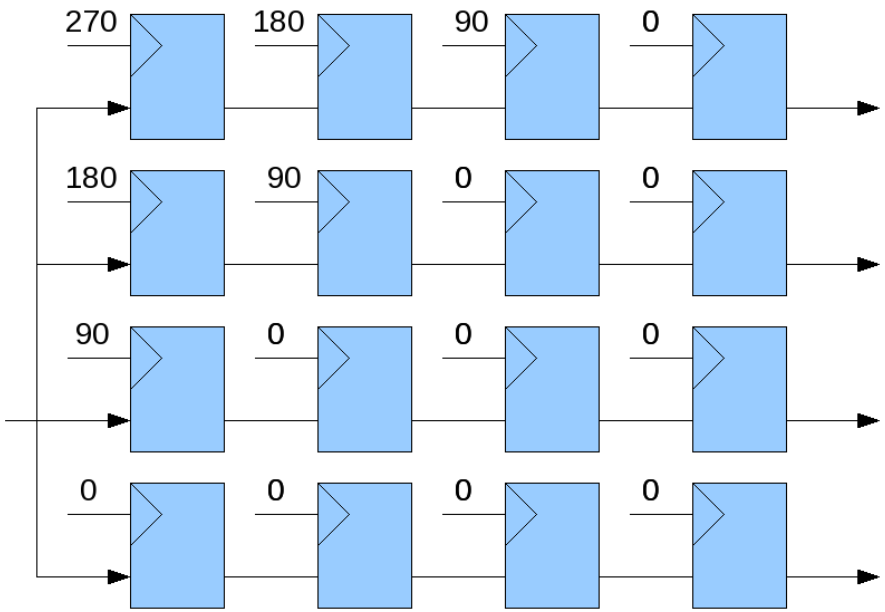
Prototyping platform for QIE/MPPC readout

- Designed to inter-operate with μTCA standard for testing
- Will also operate on a bench (or in a test-beam)
- Small Xilinx Virtex-5 for development
- Radiation tolerance taken into account (e.g. Enpirion power supplies)
- Simple configuration scrubbing via SelectMAP
- Many external I/O to connect to QIEs


4 links
AUX
POP4
Interface
Mezzanine

TDC

- Folds input signal into 4 phase-shifted registers
- A variant of this was implemented in T2K with a Xilinx Spartan-3 (2.5ns resolution)
- In a Virtex-5, this increases to 0.5ns resolution (500MHz clock, 4 phases)
- Still need discriminator input (TBD)


270
180
90
0
180
90
0
0
90
0
0
0
0
0
0
0

QIE Clocking

- Use serialised output at multiple of LHC clock
- With DDR, resolution of 0.5ns-2ns should be achievable (needs further study)
- Minimal resource usage

- V5s support readback CRC and new scrubbing features
- Firmware configuration is now Hamming coded
- Single bit & double bit detection now possible
- Software implementation of firmware checker implemented
- Other parts of design must be made triple redundant

- Prototype / test in Xilinx Virtex-5
- Finalise algorithms / readout
- Implement in antifuse or ASIC for final design