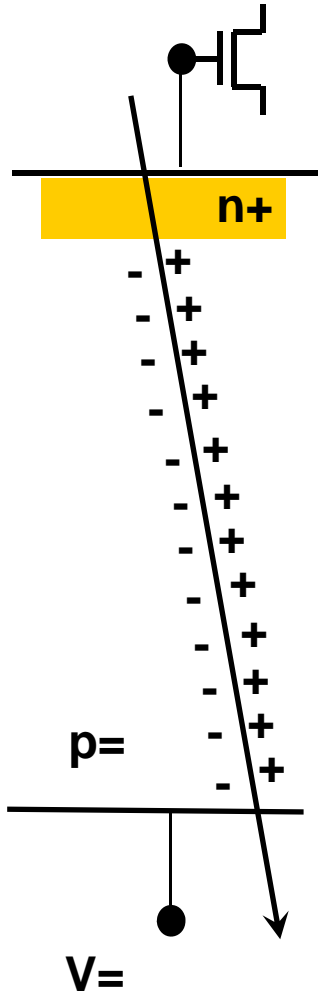# A monolithic pixel detector for a tracker upgrade ?

Charge generation by MIP in Si and MIP detection

$$\text{Signal-to-Noise} \sim \frac{Q}{C} \sim \frac{\text{Charge collection depth}}{\text{Collection electrode capacitance}}$$

$$\text{Noise} \sim \frac{1}{\sqrt{gm}} \sim \frac{1}{I^{m}} \quad \text{where } m < 1/2$$

$$\text{Signal-to-Noise} \sim \frac{Q \times I^{m}}{C}$$

Weak dependence of the noise on current !

Segmentation is good

n+

n+ **n+**

Divide one detector element into two

- Collected charge remains the same

- Capacitance divided by 2 (up to a certain point)

- Power to obtain same signal to noise gets divided by at least a factor two due to the weak dependence of the noise on the current

S/N increases up to the point when:

- Charge is shared over more electrodes

- The decrease of the electrode capacitance slows down

Conclusion : segment until increase in S/N starts to saturate

Keeping power constant: $\left[\dfrac{S}{N}\right]_{new} = \dfrac{Q(I/2)^m}{C/2} = 2^{(1-m)}\left[\dfrac{S}{N}\right]_{old} > \left[\dfrac{S}{N}\right]_{old}$ m < 1/2

Strategy for readout : power driven

- 'Minimal' cell which sends current signal out

- Detecting element + readout transistor, biasing diode or transistor, and charge injection structure for test. Use metal lines as capacitors in a current mode front end

- Gm = 25 μS, t = 25 ns, C = 1 pF, ~1μA per detecting element

- Can have 10 000 elements per square cm

  (100 x 100 μm^2 per element)

- Need fine metal pitch to create all the busses (for one cm column 100 elements to be routed in 100 microns or 1 micron metal pitch, 2 cm means 0.5 micron…, less if cell size reduces…)

- Large data processor at the edge of the chip to 'digest' the info of all these busses arriving.

- Advantage: minimal activity/power consumption within matrix

Power as a starting point

- 10 mW/cm² = 1 microW/(100x100 micron)

- Example: Basic element of 100x100 micron with 1 µA of current (so we split elements to optimize power to signal/noise ratio)

- Take transistor noise at 40 MHz BW
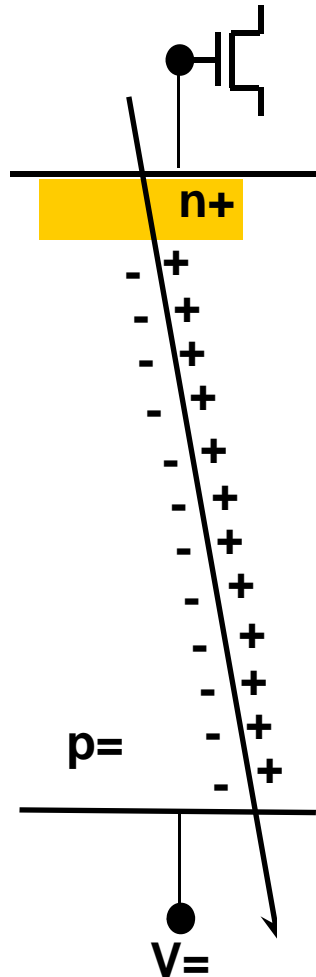
$$Veq \approx 0.16mV$$

$$\frac{S}{N}=25 \Rightarrow \frac{Q}{C}=4mV = \frac{4fC}{1pF} = \frac{0.4fC}{0.1pF} = \frac{0.04fC}{10fF}$$

Collection depth   **300 µm**   **30 µm**   **3 µm**

Radiation tolerance of silicon detectors at very high fluences can no longer really exploit the 300 microns thickness

**Could fit both integrated and non-integrated approach !**

Front end

Simulations started:

~ 900 nA for integrated amplifier – shaper

Already found a few questions related to very deep submicron technology (cfr Sandro's presentation)

Note: compared to current pixel detectors important savings in power, but less S/N (maybe some of this can be recovered, depends on Q/C finally achieved)

Iout

Comp in

Comp out

After inverter
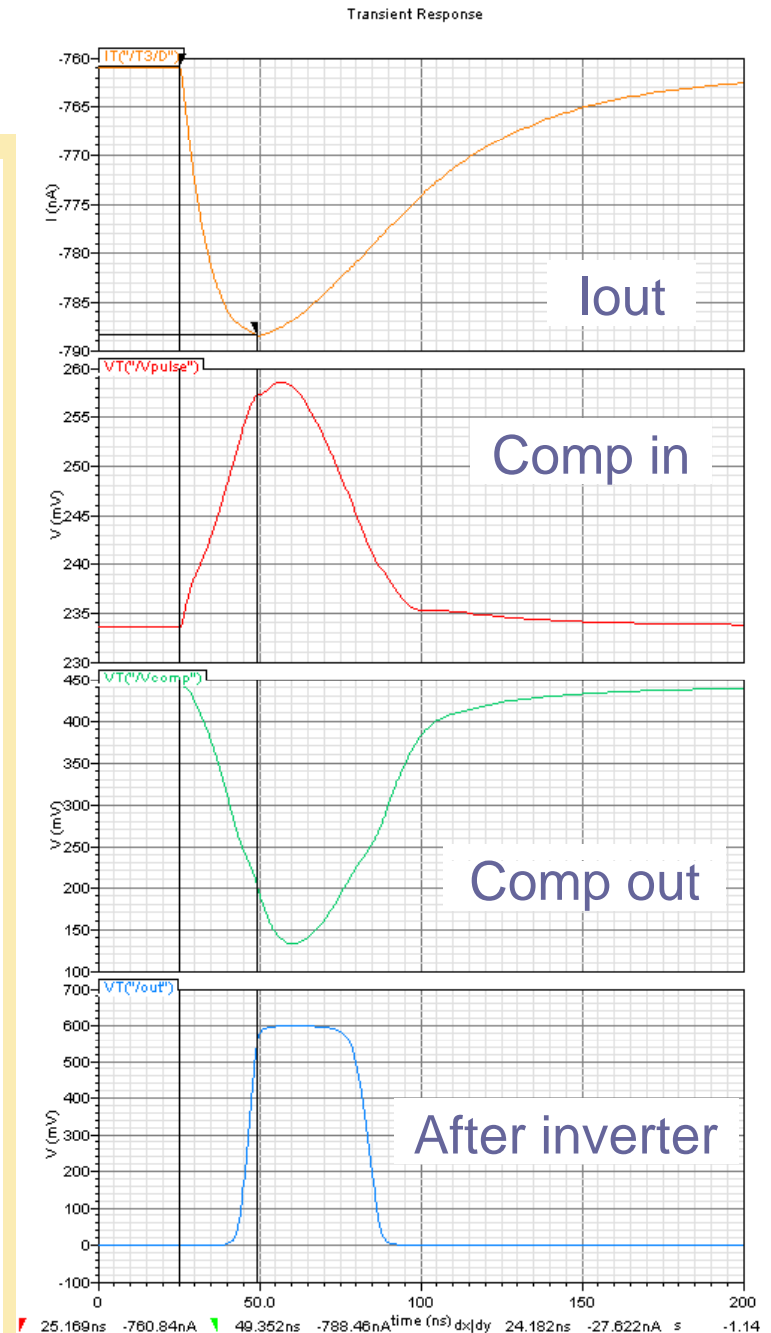
Clocking ??

- ~256x256 detecting elements 20 fF per element for the clock line = 1.28 nF

- Power to switch this around at 1 V at 40 MHz = 25.6 mW for ~ 4 square cm, eat about full power budget…

- Conclusion: if we optimize power vs signal to noise we have large number of elements, and cannot distribute the clock to every element

Strategy

Matrix

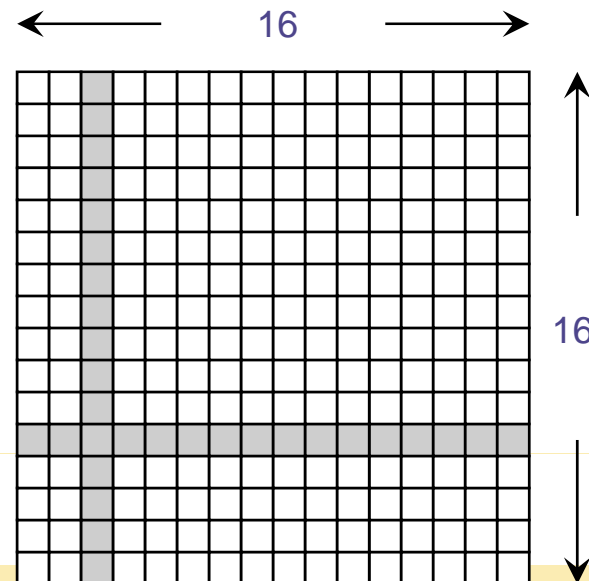Line up and down for **every** cell

Data processor

Chip

- Challenge is efficient processing in the data processor at the edge of the chip and communication to the outside for trigger signals

- Thinking about how to reduce the information to be sent off-detector for the trigger, depends on hit occupancy, not fully clear yet

- Example: group elements, for instance in 16 x 16 arrays, means 32 bits/event for the group

16

16
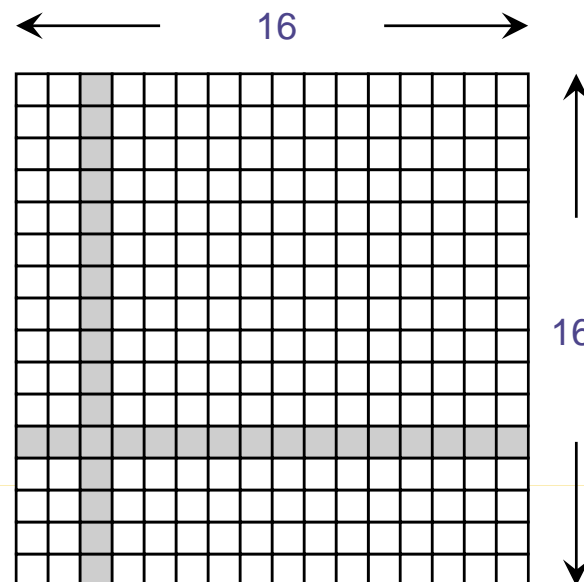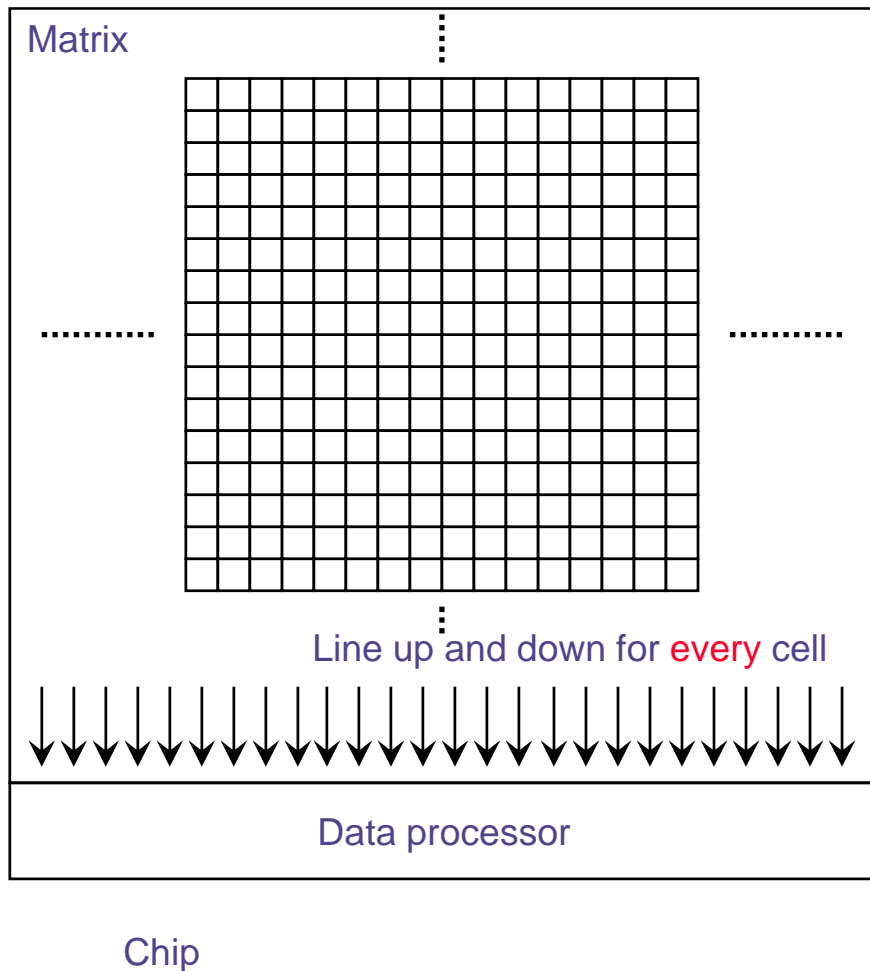
Strategy: compression of data, example, needs more work

Occupancy	Element 100x100 micron	Superelement 256x100x100 micron
PXB Layer 1	5.56E-03	1.42E+00
PXB Layer 2	2.41E-03	6.16E-01
PXB Layer 3	1.39E-03	3.55E-01
TIB Layer 1 int	3.39E-04	8.69E-02
TIB Layer 1 ext	2.82E-04	7.23E-02
TIB Layer 2 int	2.18E-04	5.58E-02
TIB Layer 2 ext	1.88E-04	4.82E-02
TIB Layer 3 int	1.28E-04	3.29E-02
TIB Layer 3 ext	1.14E-04	2.91E-02
TIB Layer 4 int	9.32E-05	2.39E-02
TIB Layer 4 ext	8.55E-05	2.19E-02
TOB Layer 1	5.94E-05	1.52E-02
TOB Layer 2	4.58E-05	1.17E-02
TOB Layer 3	3.54E-05	9.06E-03
TOB Layer 4	2.78E-05	7.11E-03
TOB Layer 5	2.57E-05	6.58E-03
TOB Layer 6	1.97E-05	5.05E-03

This is just example, looking into several compression schemes and ways to transfer info
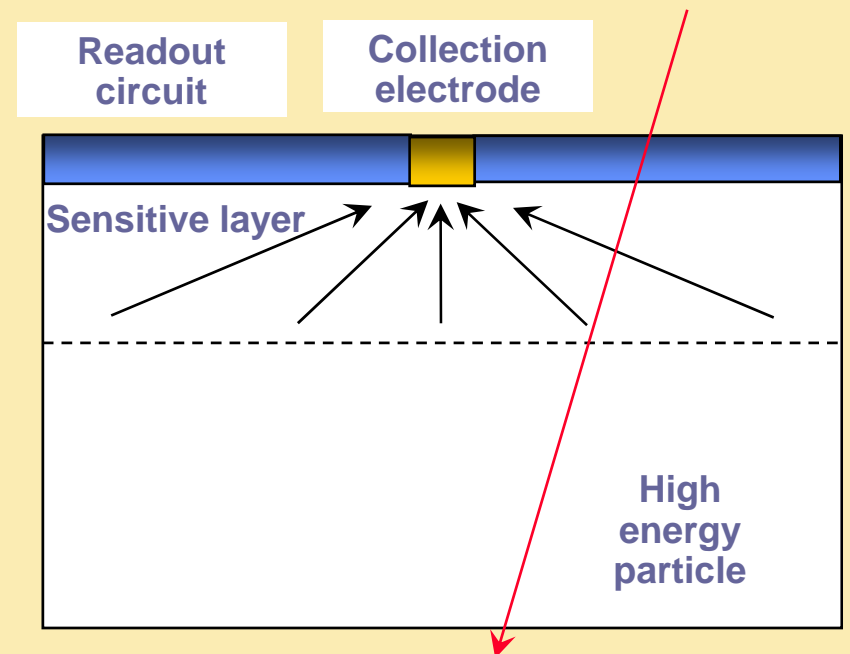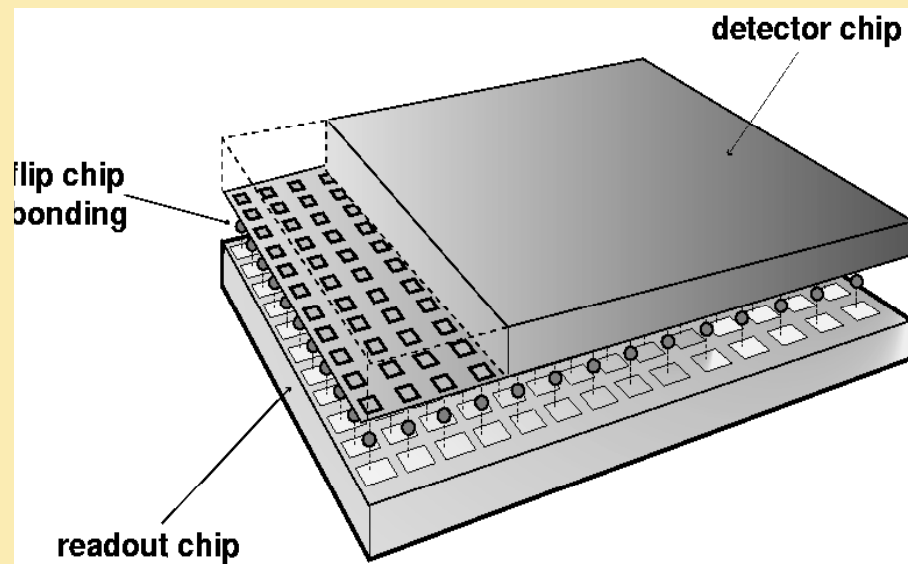Needs a lot of work

- We have super-elements of 16x16 elements, which each give strip like info -> 32 bits

- We have matrix of 16x16 elements where we could do the same.

- -> 64 bits for 256x256 array, could double this to have multiple direction to reduce ambiguity (eg diagonal…), or reduce # superelements in matrix

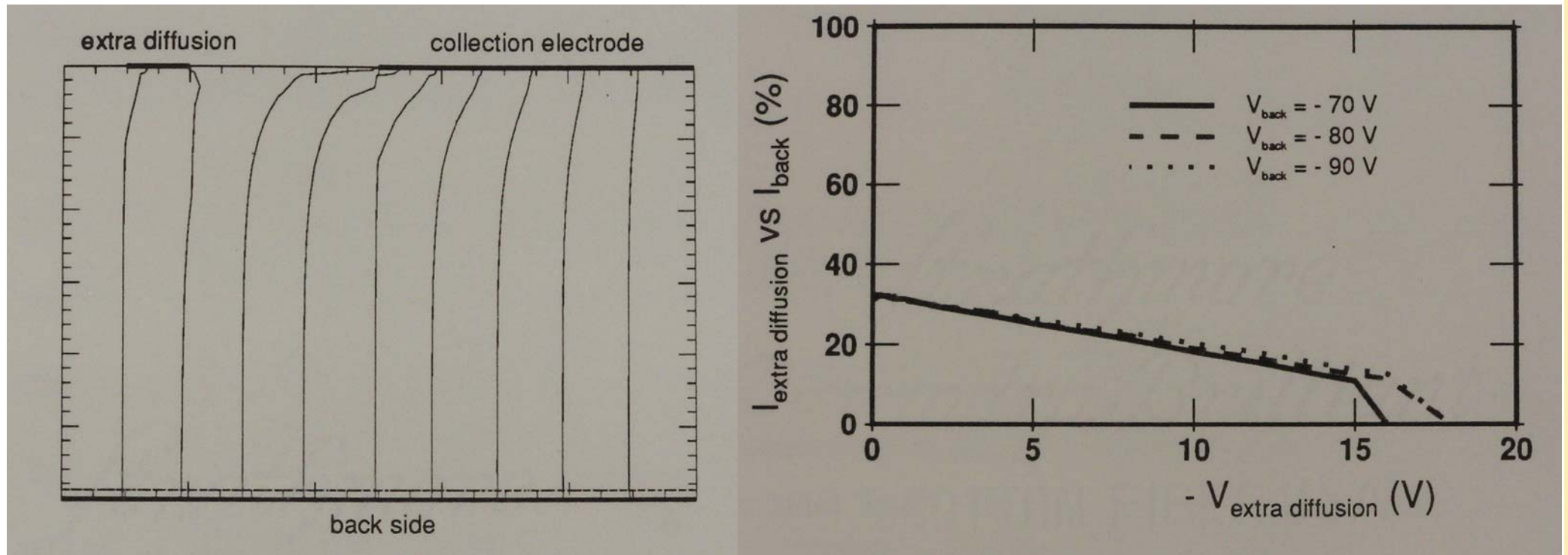- Occupancy table: cannot do second level for pixels, but will work for outer tracker layers

A monolithic detector in standard very deep submicron CMOS technology ?

- 'Traditional' monolithic detectors:
    - non-standard processing on very high resistivity substrate

    or

    - MAPS based with serial readout not necessarily compatible with future colliders, and with collection by diffusion very much affected by radiation damage

- Feedback from foundry that substrate sufficiently lowly doped is available in very deep submicron technologies (130 nm and beyond)

- 10 micron depletion no problem, strong perspectives to obtain more

detector chip

flip chip bonding

readout chip

Readout circuit

Collection electrode

Sensitive layer

High energy particle

Issues

The charge should be collected by the designated collection electrode, it should not be lost 'somewhere' in the readout circuitry:

in the example extra diffusion collects charge from a considerable fraction of the substrate, on the right bias required to divert the flow lines

Use of wells: example

Readout   Biasing diode

N+   N+   N+   P+
P well   N well

D

Edge of depletion layer

P- substrate.

-V
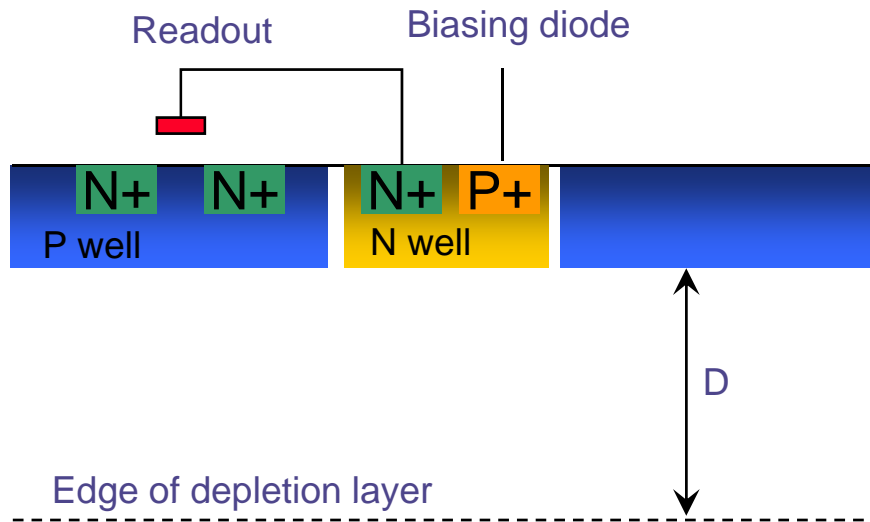
- Use well with junction at the top

- Need to be careful about fields

- AND about voltage difference between N and Pwell for full charge collection on Nwell -> will limit the area of the Pwell, might be ok for small readout circuit

- Optimize Q/C or D/C

- Can have circuit enclosed by readout electrode

- Device simulations started (IN2P3 Strasbourg)

P+ for isolation

P well

N well
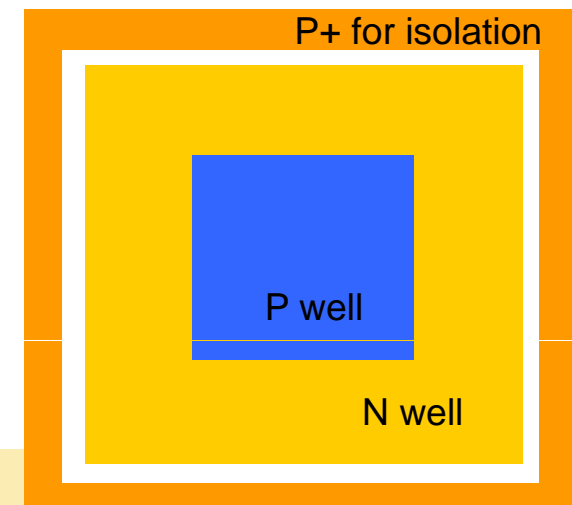
How about monolithic (integrate senor and readout on one piece of silicon) ?

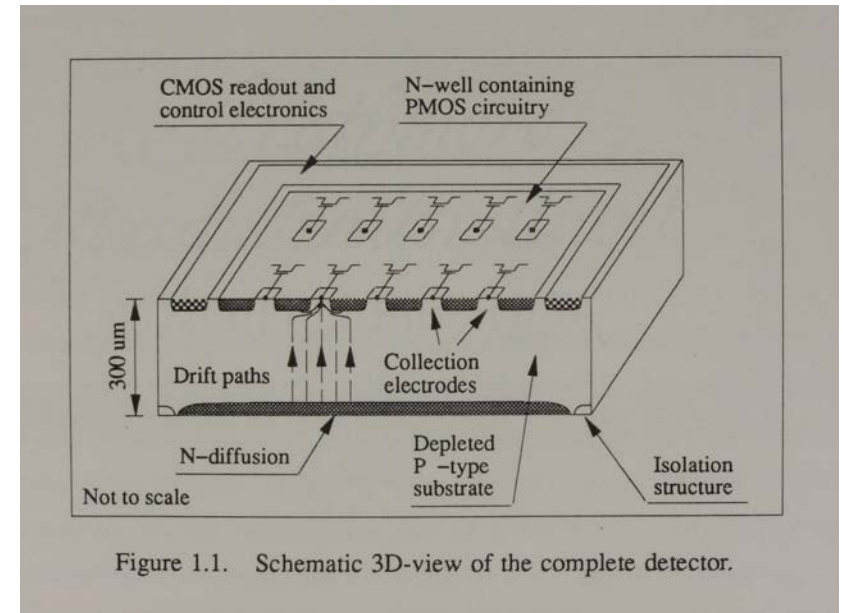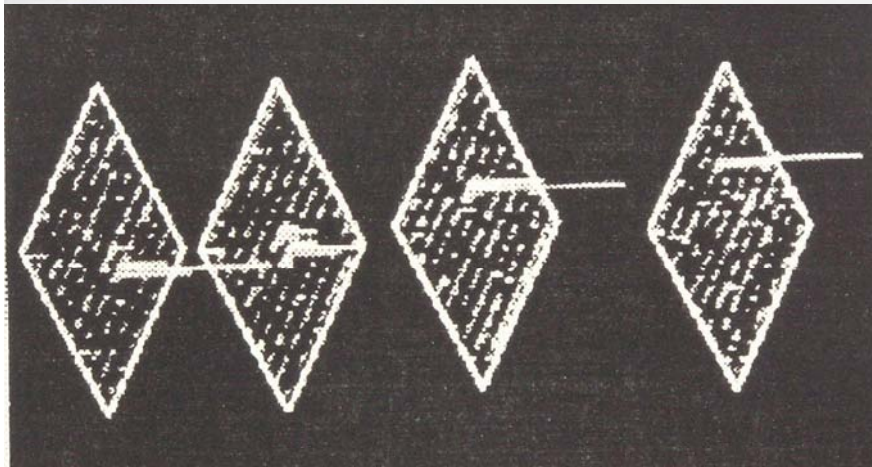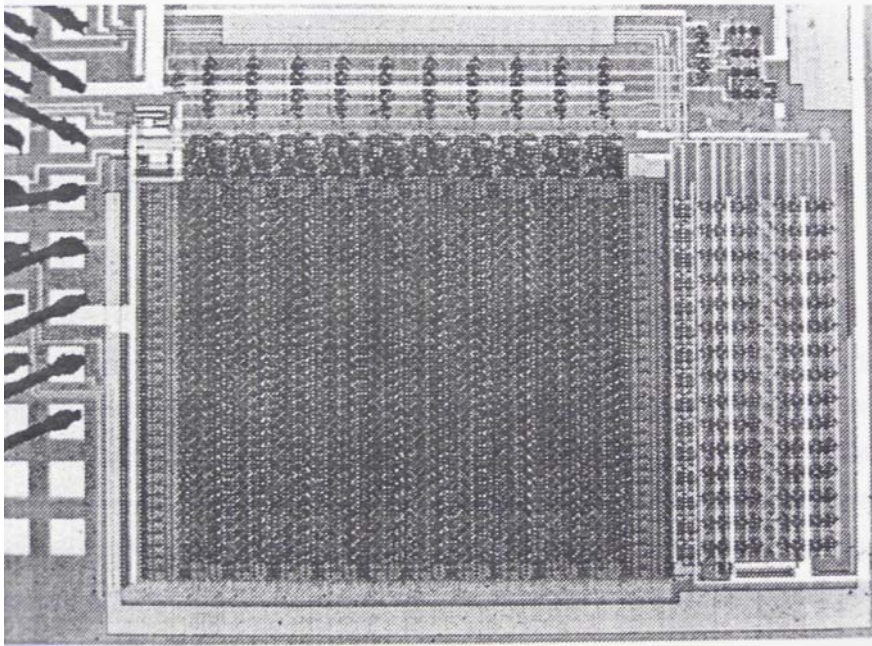Figure 1.1. Schematic 3D-view of the complete detector.

Note 300 micron thick fully depleted substrate

N=1E12cm^{-3} Ccoll=26fF

Worked nicely in non-standard technology

C. Kenney, S. Parker, W. Snoeys, J. Plummer et al.

(1992)

Perspectives: monolithic in deep-submicron

- Fine metal pitch allows novel circuit architectures

- Need to work on Q/C: 10 micron depletion layer established, means:

$$\frac{S}{N} = 25 \Rightarrow \frac{Q}{C} = 4mV \boxed{= \frac{0.13 fC}{33 fF}}$$

- 33 fF achievable (cfr CMOS imagers order of magnitude less, but smaller…)

- => Strong perspectives for more favorable Q/C ratios

- Need to pay attention to radiation tolerance – guardrings etc…

- Note: collection dominated by drift, not diffusion (!) for increased radiation tolerance

Monolithic now possible in very deep submicron standard CMOS !

- **Cost per unit area in production less than that of traditional silicon**
- **Standard volume production (~ 20 square meter a day)**
- **Detector-readout connection automatically realized**
- **Low capacitance allows very favorable power – signal-to-noise ratios**
- **Very deep submicron allows power and speed advantages**
- **Allows innovative readout circuits**
- **Collection by drift will allow increased radiation tolerance**

Very interesting for the LHC upgrades

Significant investment dominated by engineering run submissions (90 nm or beyond !)

- **Aiming for 10 mW per square cm or less with 100x100 micron elements**
- **Significant advantages beyond 130 nm (low k dielectrics in metallization)**

Conclusions

- **Architecture**

    - **Upgrade warrants to examine process options, including advanced ones.**

    - **Upgrade power driven ~10mA/cm^2. Need to optimize collected charge over capacitance ratio. Increased segmentation is advantageous up to small sizes**

    - **Thinking of a 'minimal' cell approach, requires fine metal pitches, has the advantage of minimal activity in the matrix, power savings on clock lines, buffers, etc…**

    - **Issue is limiting power for processing and off-detector communication, thinking about data compression for trigger and data signals**

- **Monolithic in standard very deep submicron CMOS**

    - **First detailed discussion with foundry very promising**

    - **Advantages: Cost per unit area, standard volume production, detector- readout connection automatically realized, very favorable power – S/N, advanced technology allows innovative readout circuits, increased radiation tolerance**

    - **Still need integration work on for production/test/mounting but for monolithic already significant step taken**

    - **Radiation tolerance: doping level higher than traditional detectors => phenomena become significant only after (much) larger dose …**

Proposal + Preliminary plan of work

Sep 2009
- Definition, simulation and verification of readout circuit + submission of test circuit in a multiproject fabrication run
- Includes a significant amount of more general work in very deep micron technologies: preparation of libraries, test structures for characterization of the technology, also with respect to radiation tolerance also needed for development of C4i.

Dec 2009
- Test setup (printed circuit boards, software…) for readout circuit test

Mar 2010
- Test of the circuit.

Mar 2010
- Definition, simulation and verification of the device structure supported by device simulations

Jun 2010
- Submission of a complete monolithic detector on a more lightly doped substrate than the standard one.

Sep 2010
- Test setup for the full demonstrator including test with particles, perhaps with reference telescope and instrumentation

Dec 2010
- Test of the demonstrator

2011
- Corrections/improvements in design and rerun + test

Conclusions

- **Perspective for monolithic in standard deep submicron with several advantages**

- **Project**

    - **2-3 years to put prototype on the table**

    - **MPW for circuit + 2 engineering runs (in 90 nm !) 2-3 MCHF**

    - **Device, circuit, architecture – also need some technology characterization and design environment development**

- **CERN committed to at least ¼ of the material cost, already activity on front end**

- **IN2P3 Strasbourg started device simulations, and would be involved heavily in testing.**

- **Very large chance for funding of engineering time from the Conseil General de la Haute Savoie**

- **Second visit to foundry next week**

- **Would like to submit proposal to CMS before the end of the year**