PAUL SCHERRER INSTITUT

# Development of an on-chip Charge Pump in CMOS Technology

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Pixel Replacement/Upgrade Discussion Meeting

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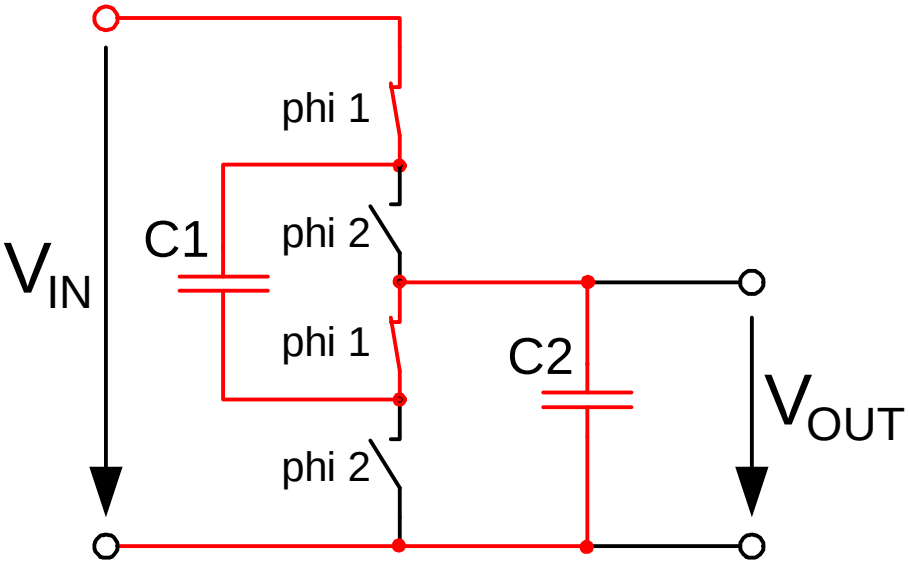
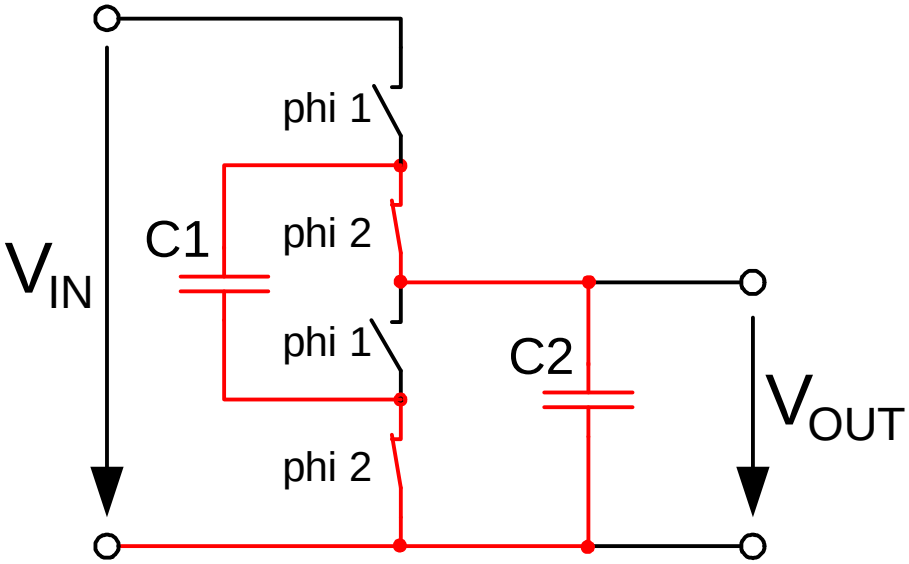
# Motivation

- CMS Pixel: two supply voltages Vdigital = 2.0 … 2.5V and Vanalog = 1.5V (or lower)
- DC-DC converter for Vanalog on the Detector Module → only one power line
- some free space on an ASIC for data link tests in April 2008
- to learn something about switched capacitor DC-DC converter (area on chip, …)
- Voltage divider by 2 (simple design)
- for only one CMS Pixel ROC (24 mA)
- switching frequency higher than sensitive frequency range of the ROC (> 10 MHz)

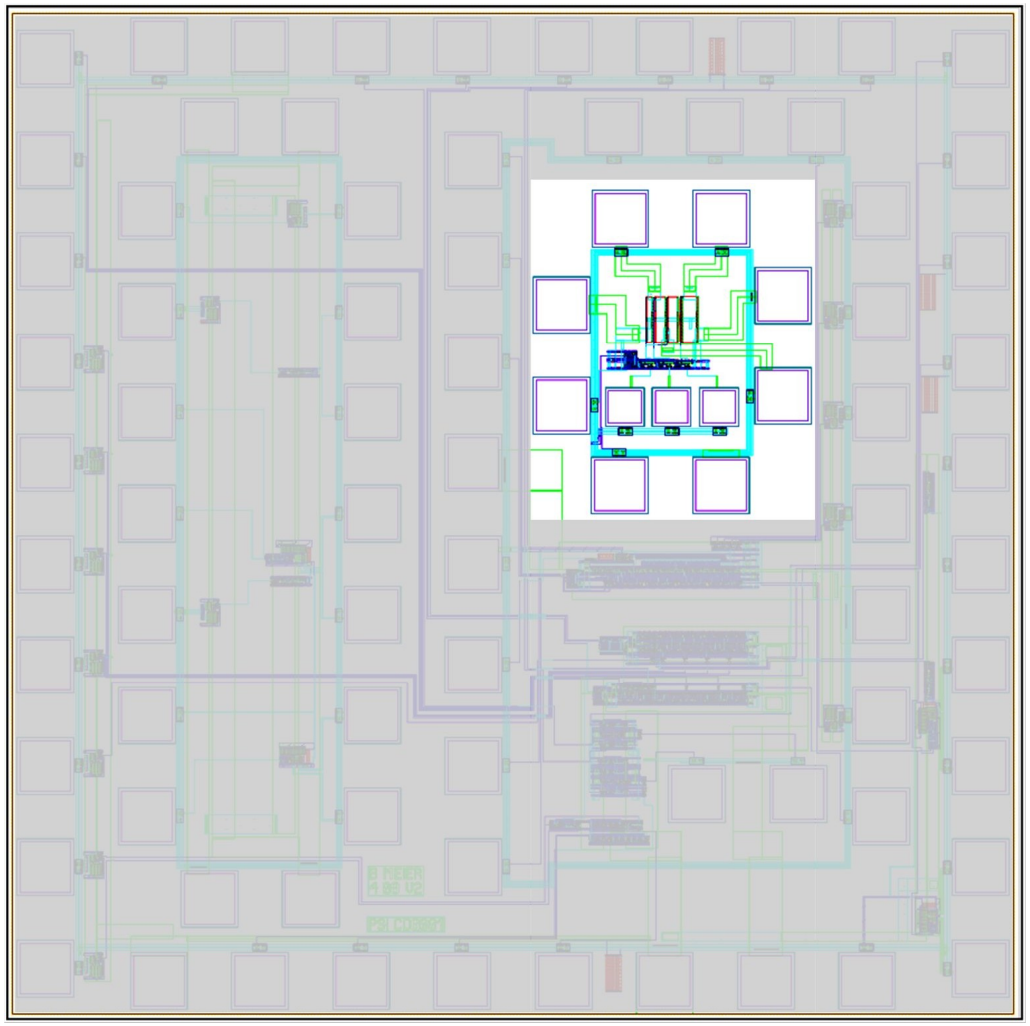
# Principle



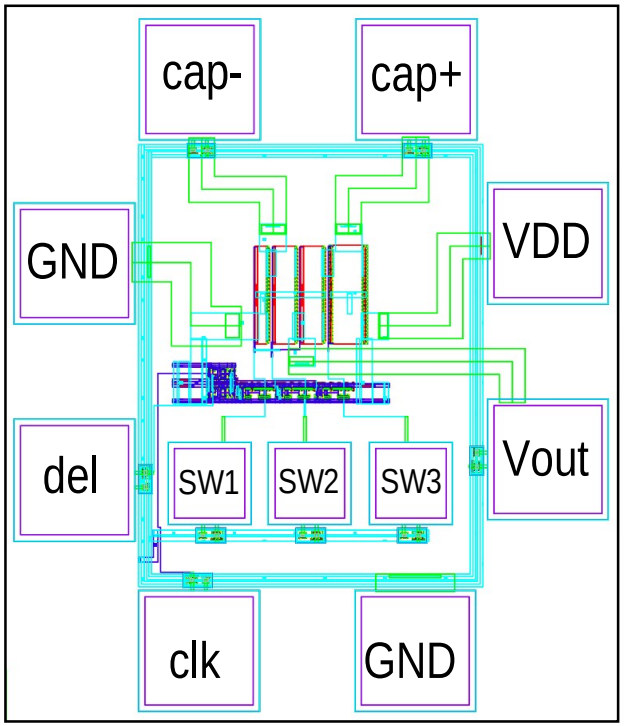

- Voltage divider by 2
- on chip: four switches, two phase generator and drivers
- external oscillator
- external capacitor C1 and C2 ( 10 … 100 nF)

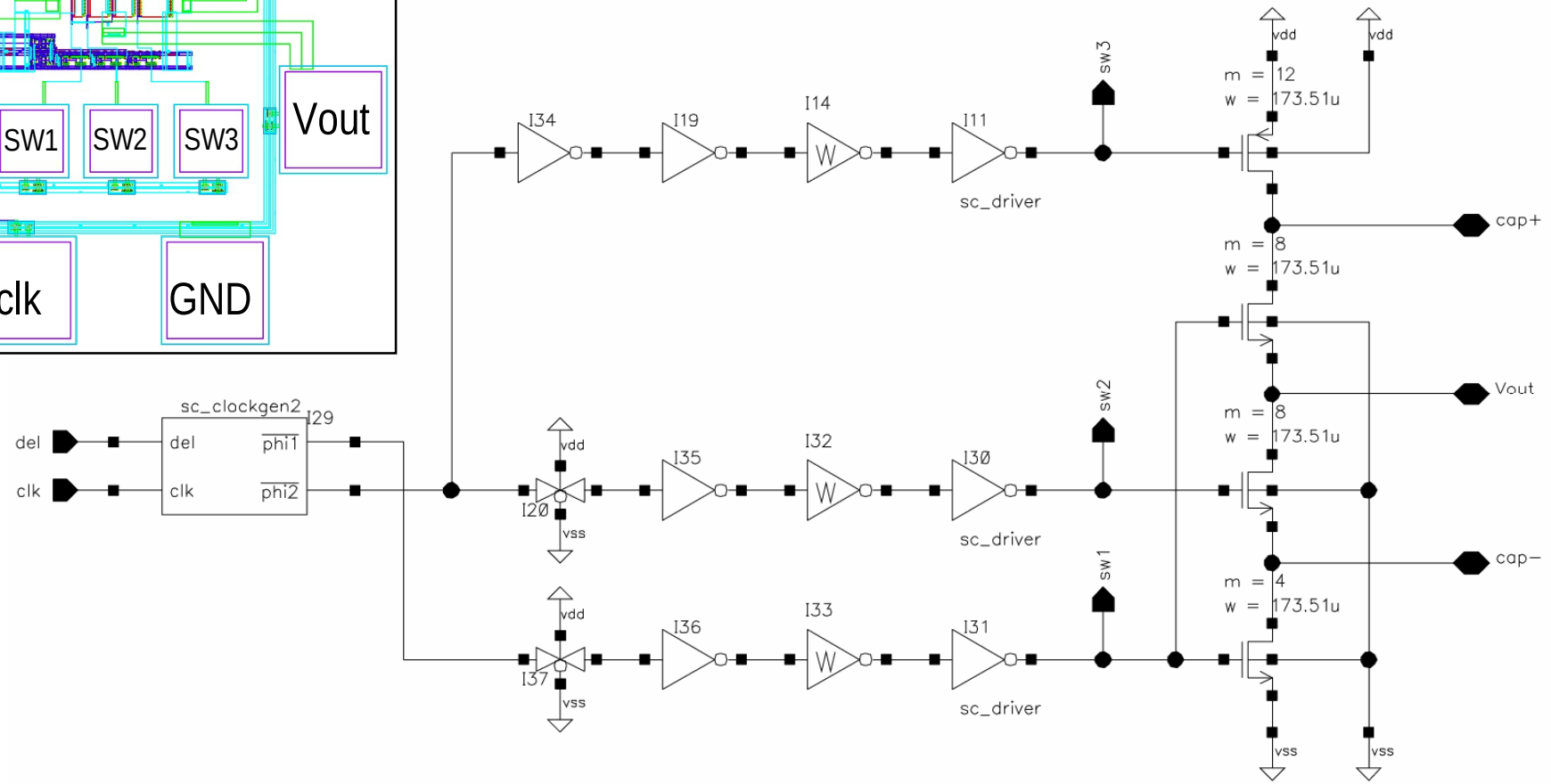
# ASIC Design



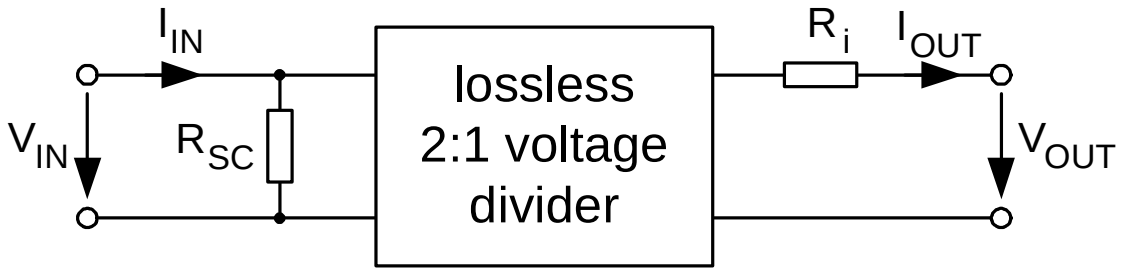
- Size 2 x 2 mm
- Technology: 250 nm CMOS IBM
- Radiation hardness design
- CERN MPW in April 2008
- Samples end of July

# Schematic and Layout



# Efficiency




Source resistance: $$R_i = \frac{1}{4} \cdot \frac{1}{f\,C} \cdot \frac{1 + \exp\left(-\frac{T}{2\,\tau}\right)}{1 - \exp\left(-\frac{T}{2\,\tau}\right)}\;; \qquad \tau = 2\,R_{ON}\;C$$

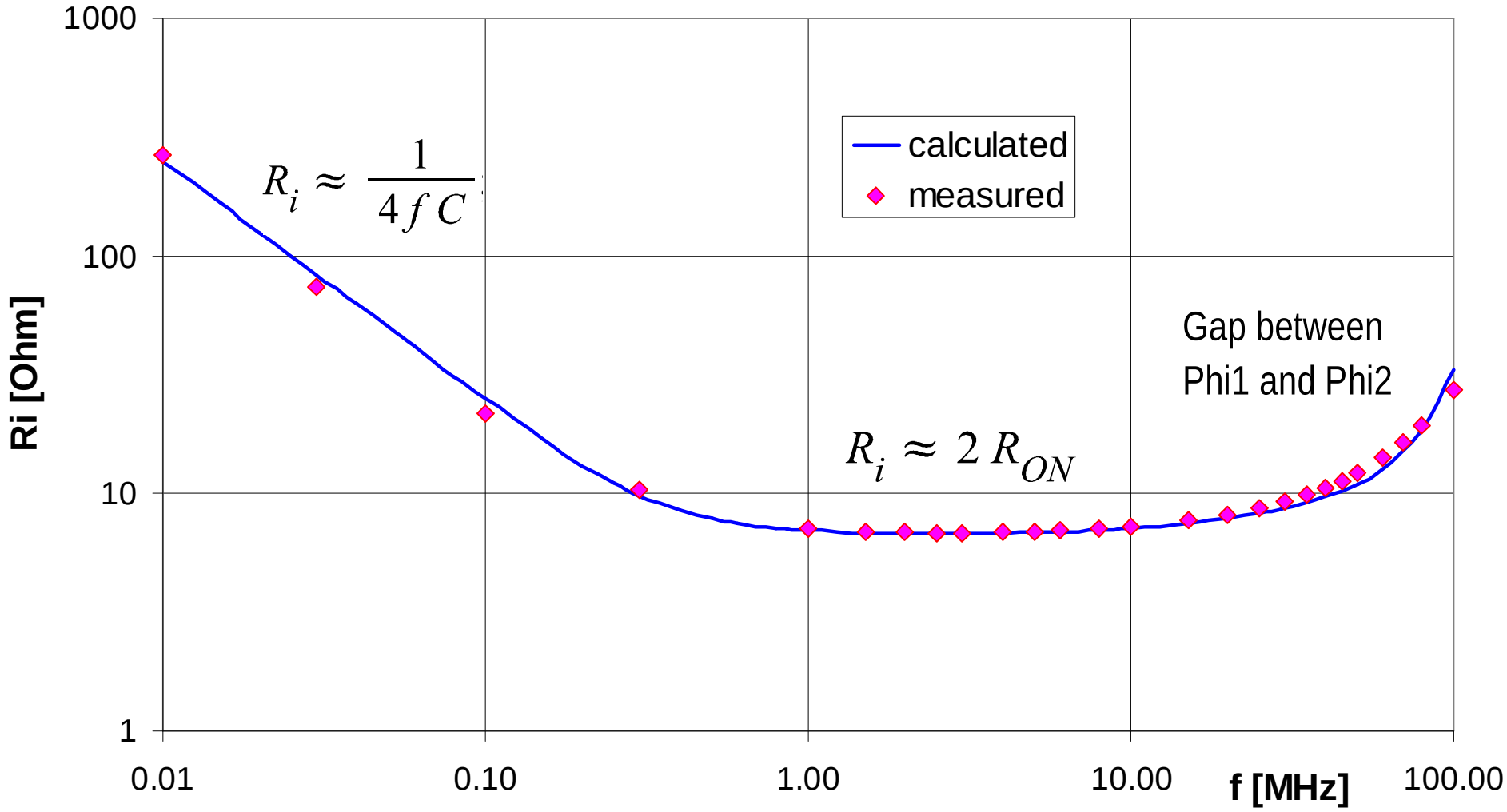
for low frequency: $$R_i \approx \frac{1}{4\,f\,C};\quad 2\,\tau << T$$

for high frequency: $$R_i \approx 2\,R_{ON};\quad 2\,\tau >> T$$

Gating Loss: $$P_{SC} = \frac{V_{IN}^2}{R_{SC}} = f\,C_{SC}\,V_{IN}^2$$ Power required to drive the switches

Efficiency: $$\eta := \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}\;I_{OUT}}{V_{IN}\;I_{IN} + P_{SC}} = \frac{\left(V_{IN} - 2\,R_i\,I_{OUT}\right)I_{OUT}}{V_{IN}\,I_{OUT} + 2\,f\,C_{SC}\,V_{IN}}$$

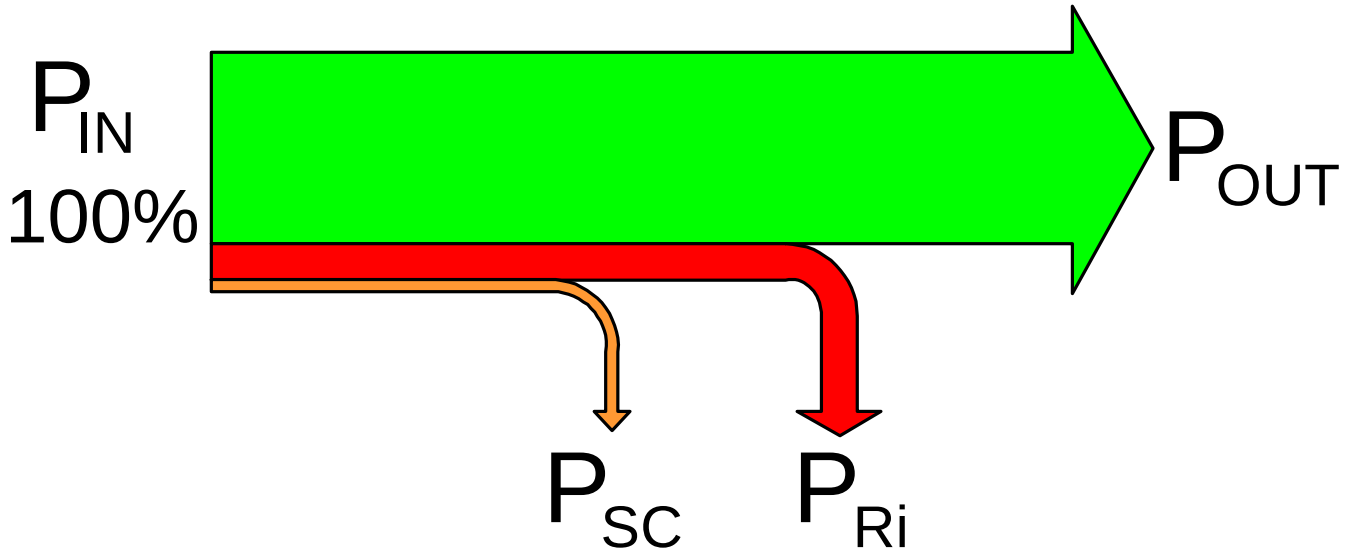
# Output Resistance




Vin = 2.5V C = 100 nF

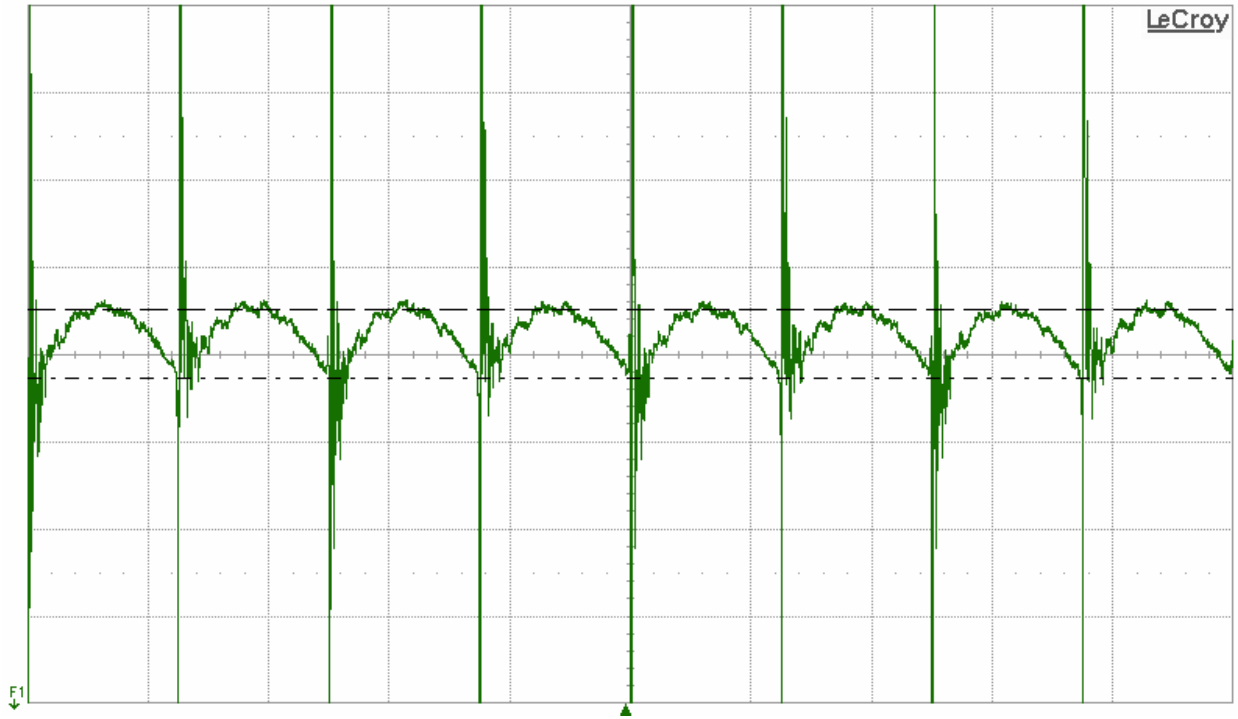
Iout = 24 mA Ron = 3.3 Ohm

# Power Budget




| f [MHz] | P_SC | P_Ri | Pout |
|---|---|---|---|
| 10 | 2 % | 14 % | 84 % |
| 20 | 4 % | 15 % | 81 % |
| 40 | 8 % | 18 % | 74 % |

# Ripple




Output Voltage

200 ns/div

5 mV/div

f = 4 MHz;  C = 10 nF;  Iout = 25 mA;  Ripple: 4 mVpp (smaller at higher freq)

→ripple is not a problem

spikes ?  frequency outside the sensitive frequency range

# Summary

- over 80% efficiency at 20 MHz switching frequency
- better efficiency with lower Ron → bigger FETs
- area on chip: 10'000 $\mu m^2$ (100 $\mu$m x 100 $\mu$m)
- output voltage to small (Vout = 1.1V @ Vin=2.5V and Iout = 24 mA)
- not adjustable, no voltage regulation

# Outlook

to do

- test of the SC-regulator together with the ROC (noise)

possible configurations

- one small (24mA) regulator per ROC → advantage: adjustable for each ROC
- or one big regulator per module (=16 ROCs) → less external capacitors

no concrete plan for future projects

- 3:2 voltage converter
- scale-up for 16 ROCs
- adjustable