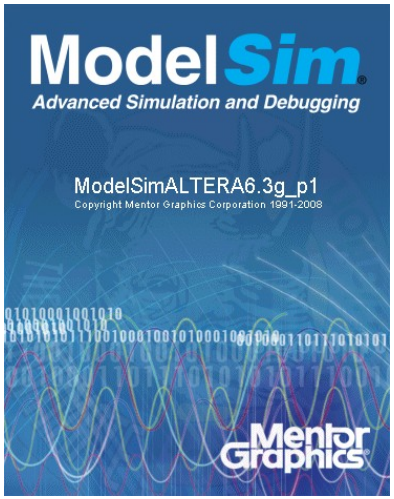
GBT protocol implementation on Altera Stratix II GX FPGA

Outline

- Hardware platform and design software used
- Implementation details
  - Embedded Ser/Des configuration
  - Manual header finding
  - Encoding/Decoding
  - Latencies and used resources
- Results and measurements
- Conclusions

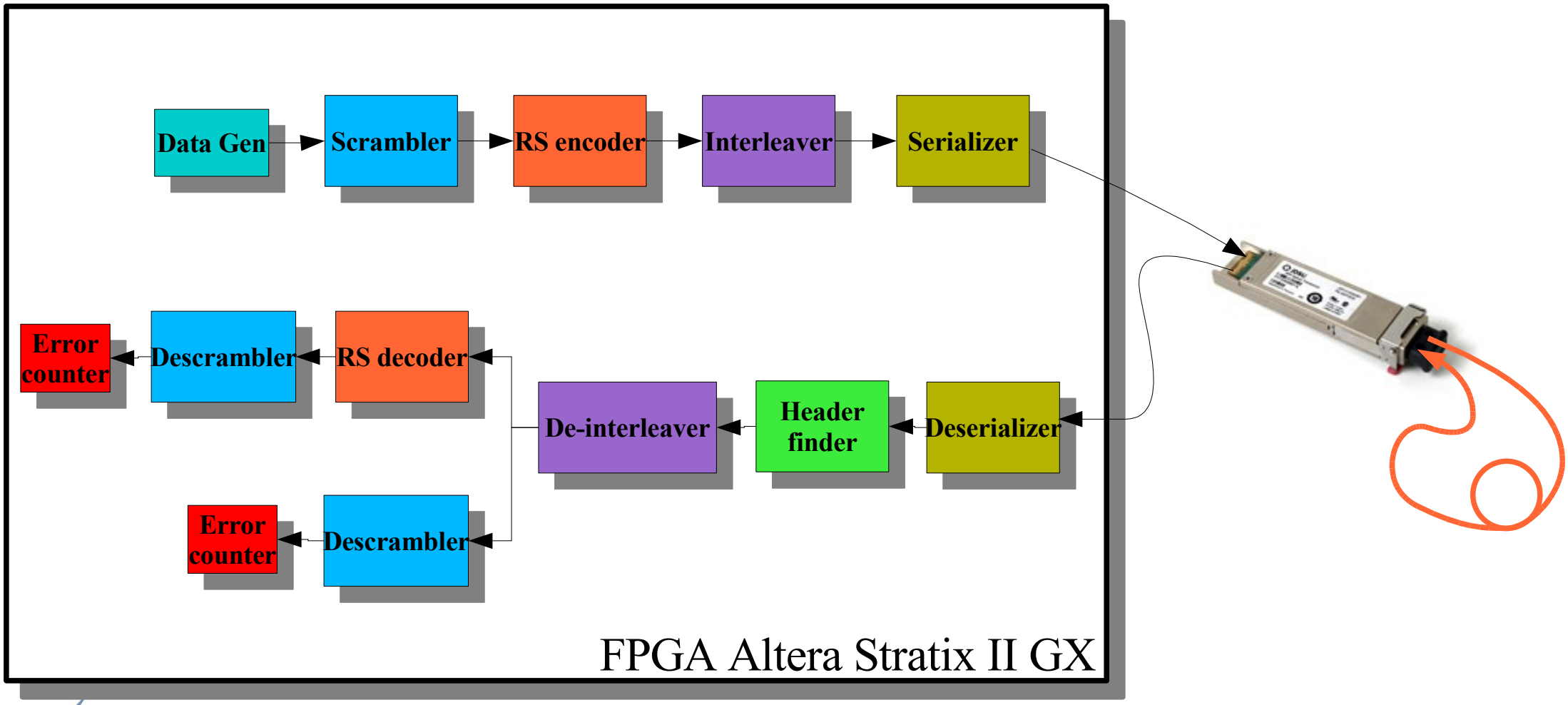
Hardware platform and design software used

- **Altera PCI Express Development Kit with Stratix II GX**
- **JDSU (ex. Picolight) SFP+ transceiver up to 8.5Gbps**

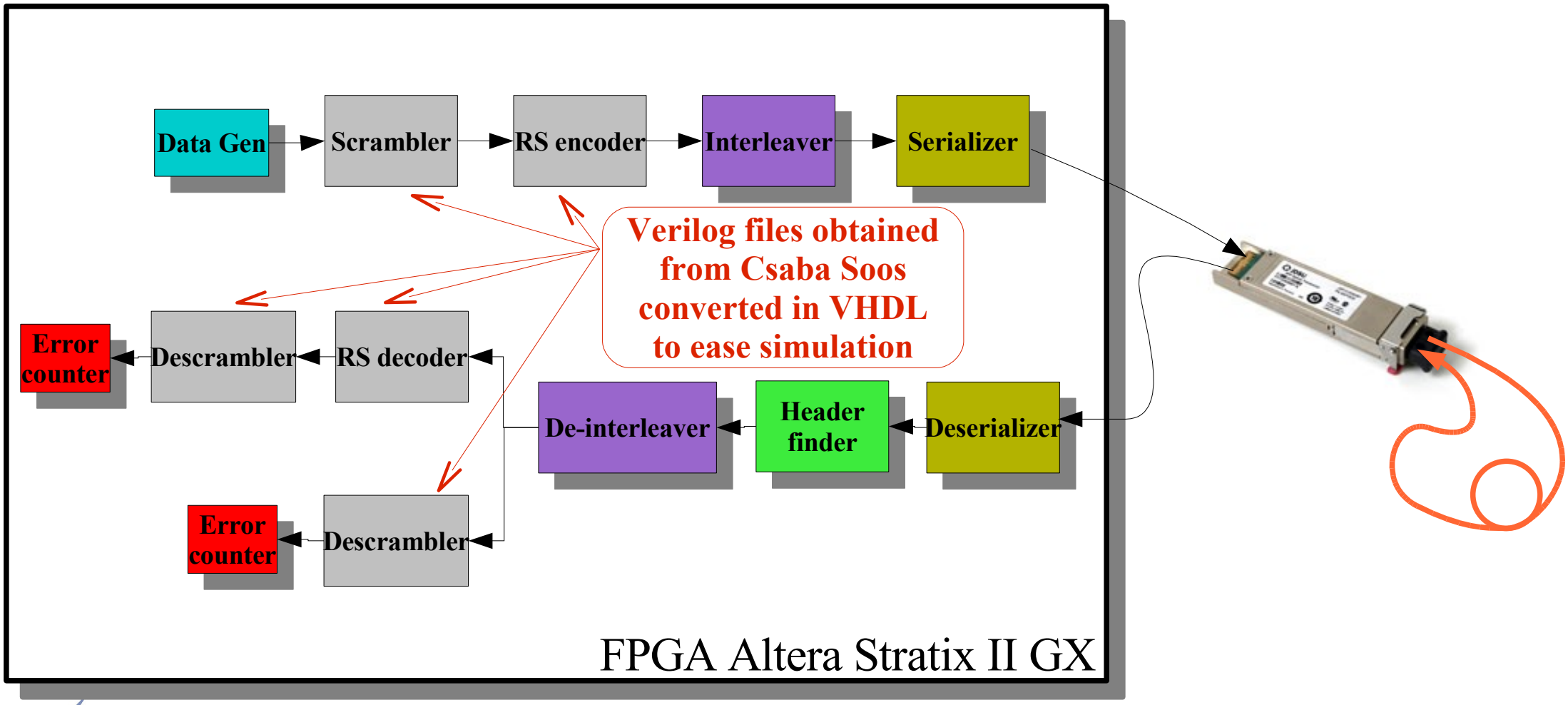


- **Altera Quartus II version 8.1 with corresponding Modelsim-Altera**

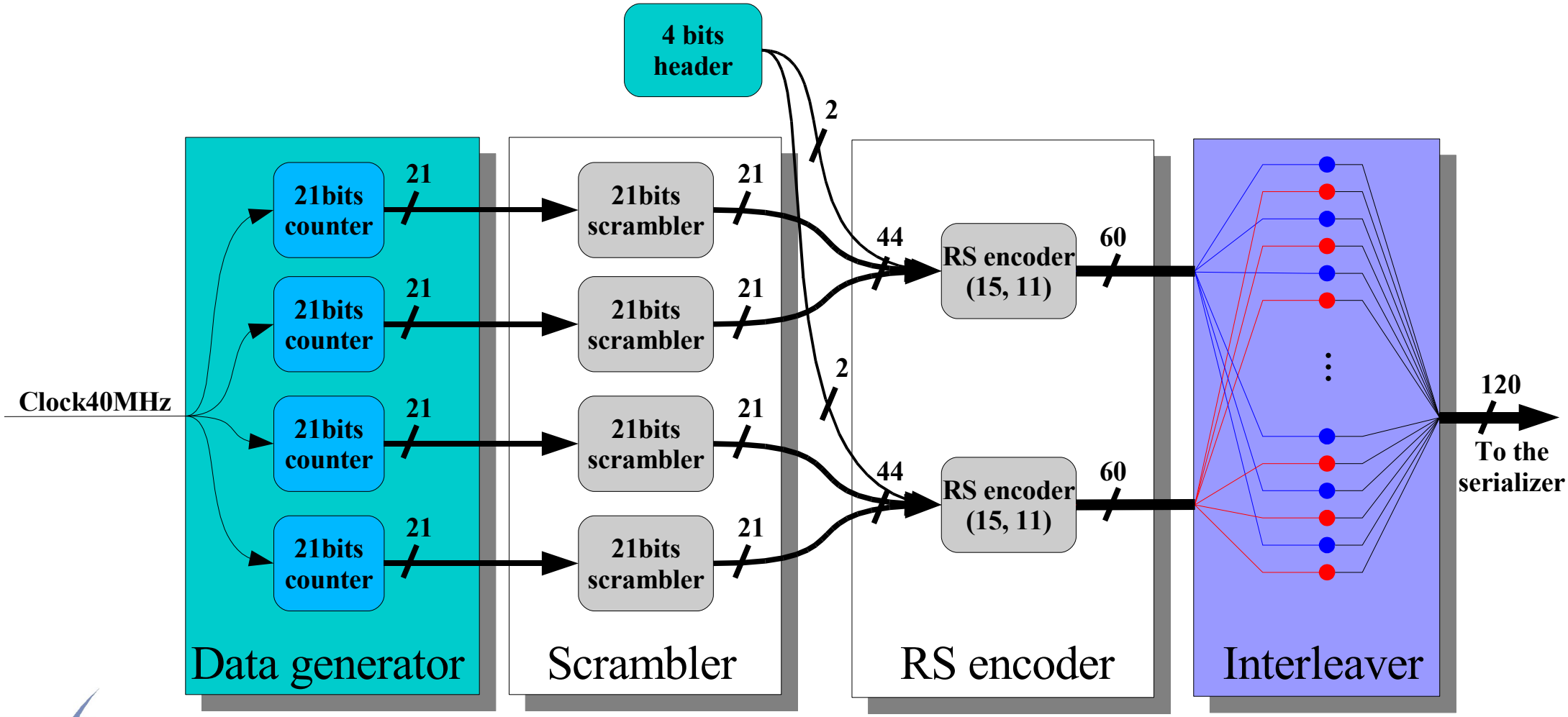
Block diagram (1)



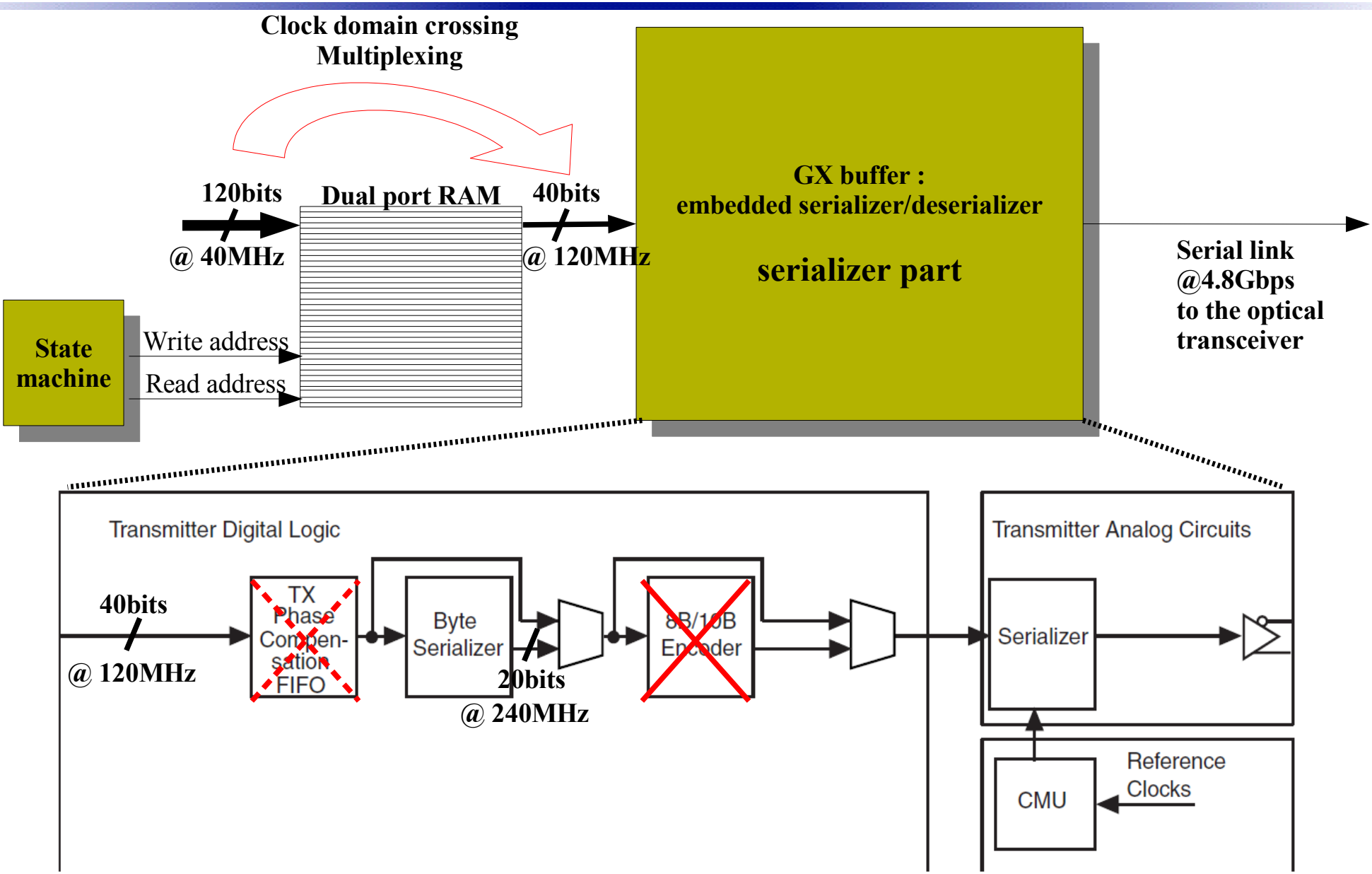
Block diagram (2)



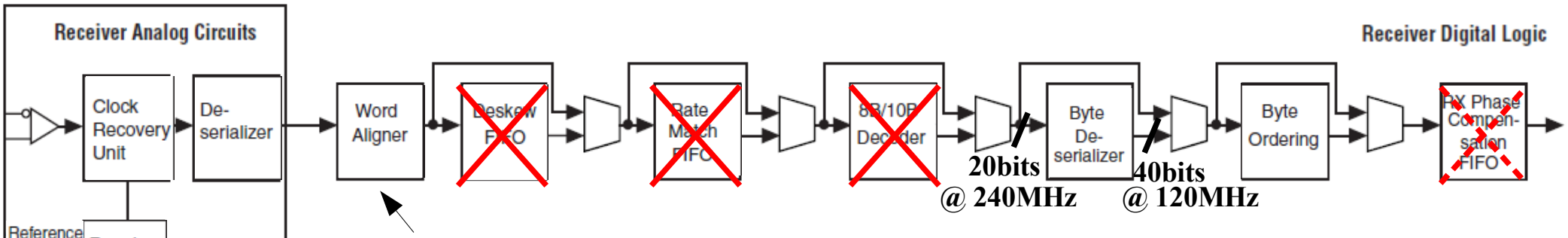
Encoding chain



Serialization



Stratix II GX receiver block diagram



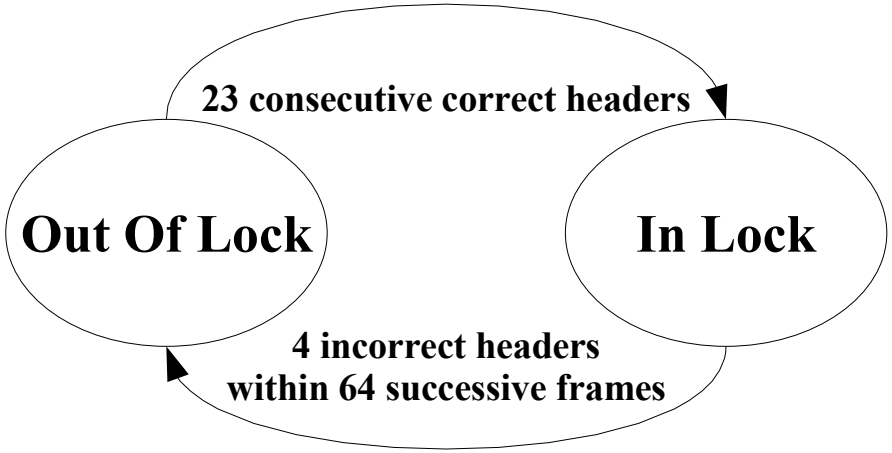
- Tries to align data on a pattern but pattern length can be:
  - 7 bits
  - 10 bits
  - or 20 bits
  - but not 4 bits

- Offers a manual bit slip mode
  - Available when using 16 or 32-bits parallel interface
  - but not available when parallel interface on 40 bits (16 and 32 bits parallel interface not usable because not a divisor of 120)

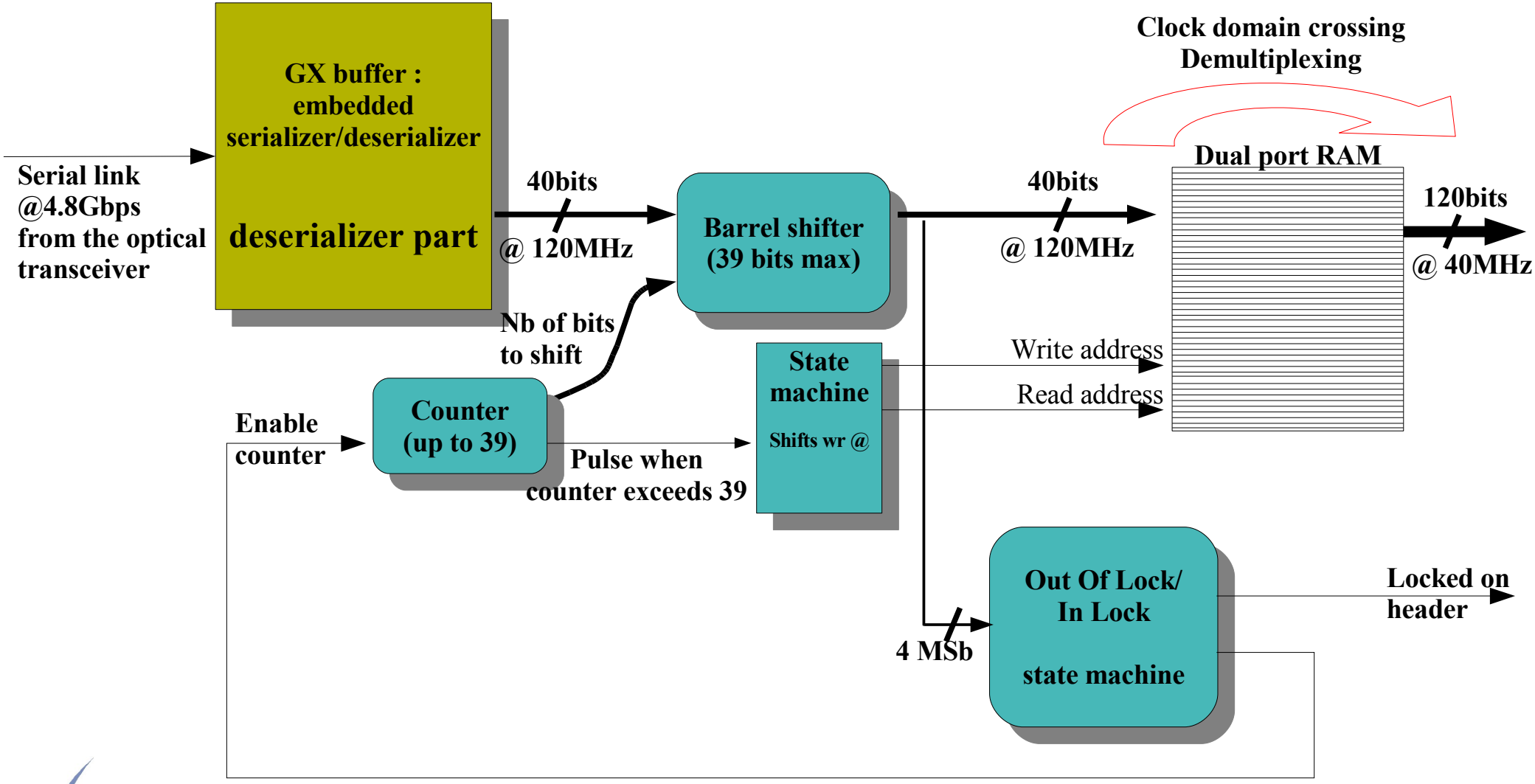
Deserialization and manual header finding (1)

- **Word boundary search fully manual:**
  - **"word aligner" module of the GX buffer allows to search for pattern of 7-bits minimum**
    - **Means that we have to search ourselves the 4-bits header**
  - **"bit slip command" is not available in the GX buffer configuration we use**
    - **Means that we have to do the bit slipping ourselves**

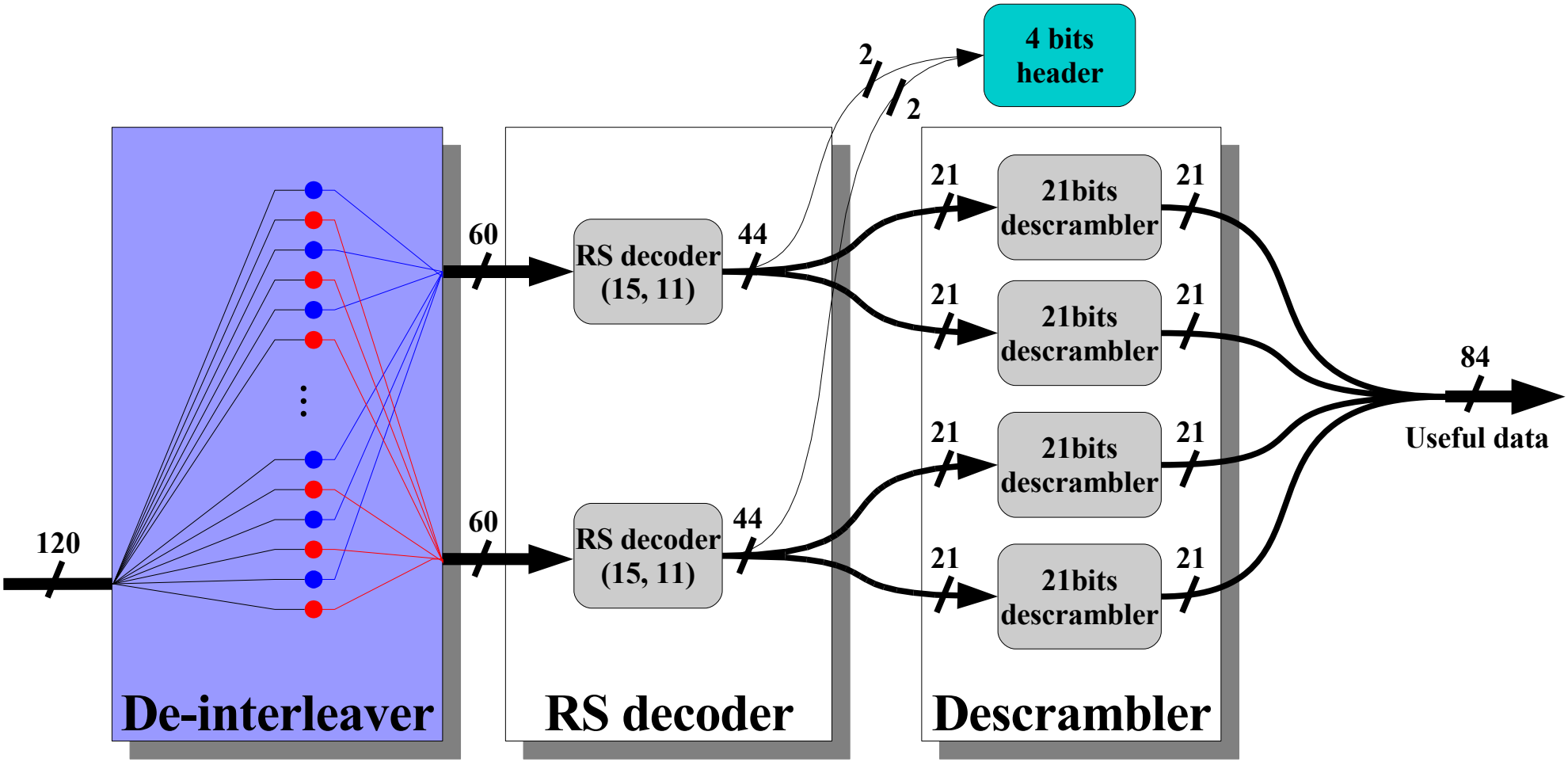
- **From the thesis of Giulia Papotti, following parameters were used:**



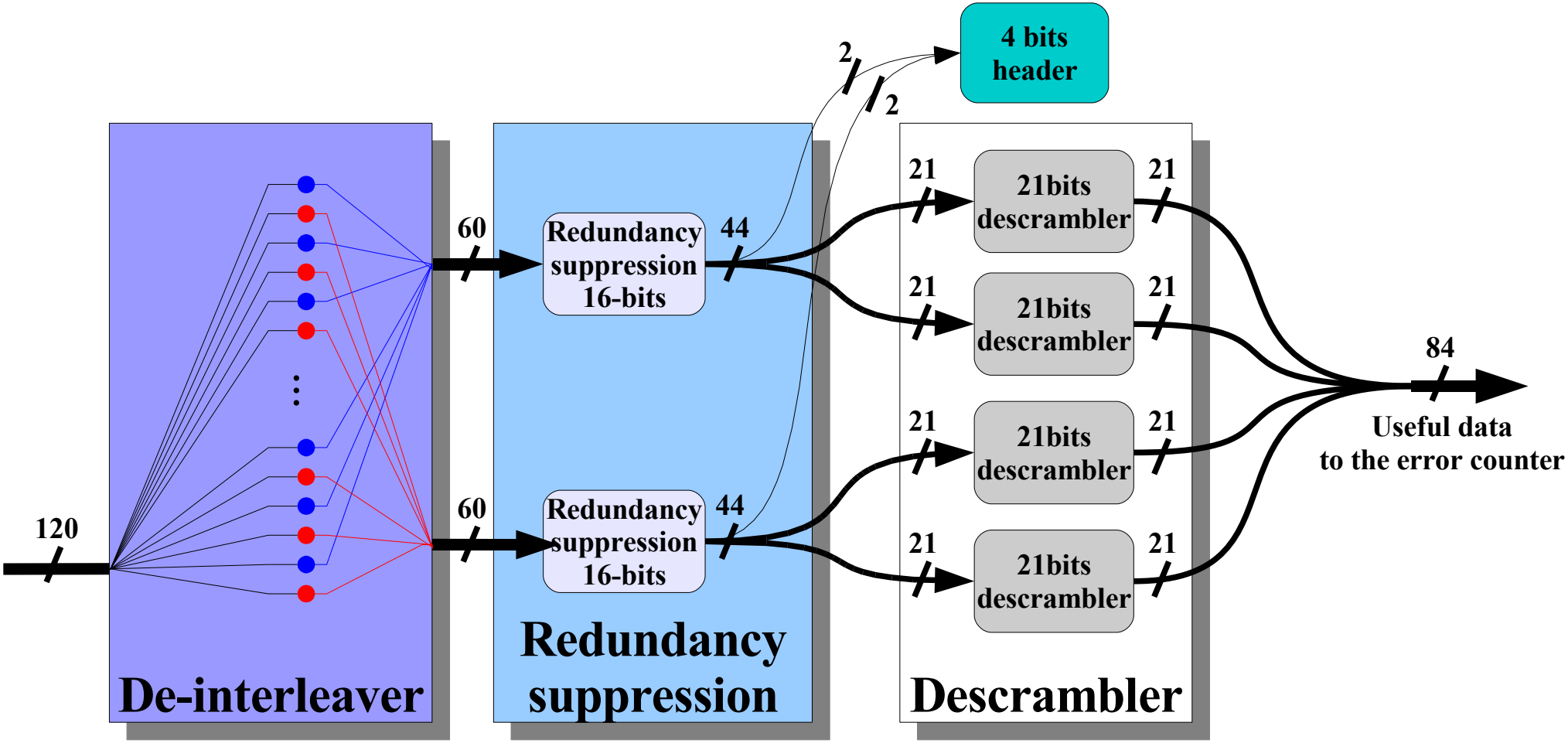
Deserialization and manual header finding (2)



Decoding chain



Decoding chain without FEC



- In such way, we really test the quality of the physical link because we do not occult errors eventually corrected by the RS decoder

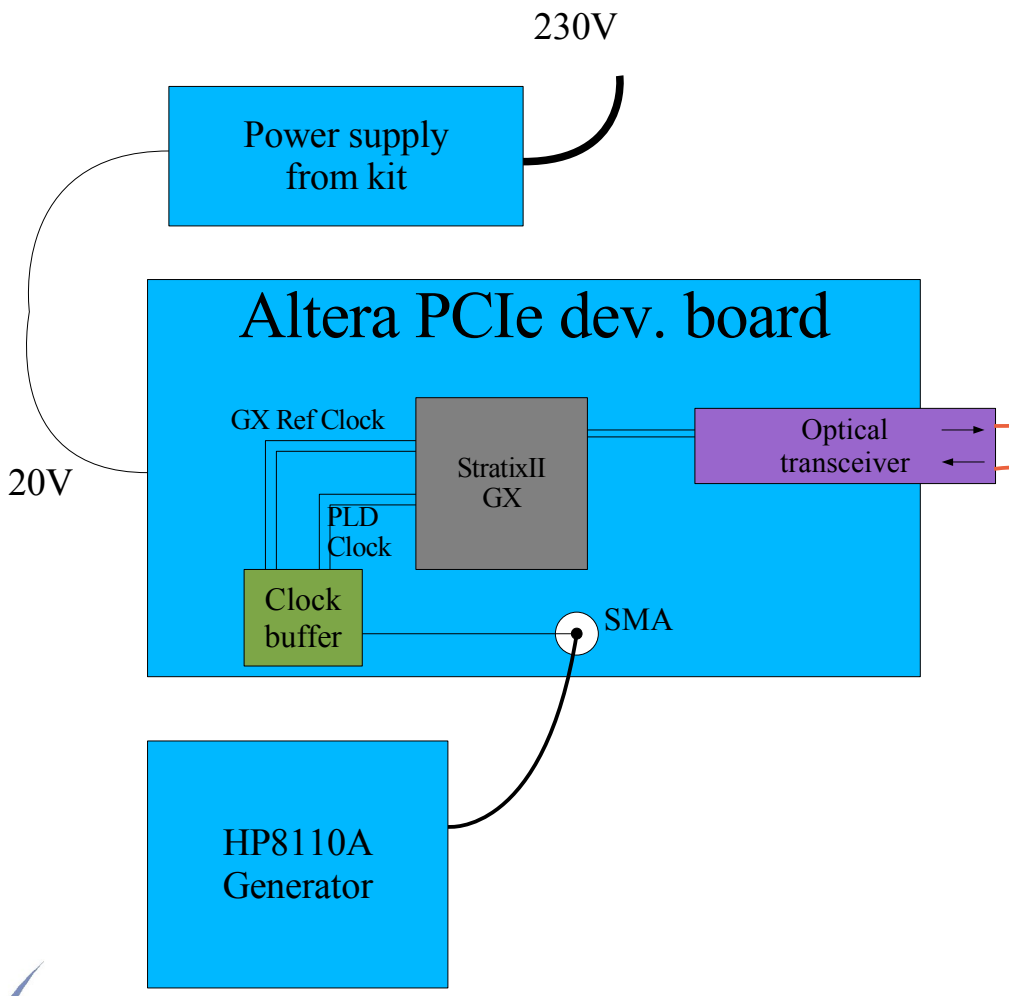
Latencies and used resources

Function	Size in Adaptative Logic Modules (ALMs) 36384 available EPS2GX90		Latency in 40MHz clock cycles
Scrambler	173	0.48%	2
RS encoder	126	0.35%	0
Interleaver	0	0.00%	0
Multiplexer	11	0.03%	2
Header finder	259	0.71%	23<N<618
Demultiplexer	10	0.03%	2
De-interleaver	0	0.00%	0
RS decoder	819	2.25%	1
Descrambler	169	0.46%	1
Total for one channel	1567	4.31%	

- **Extrapolation for more channels...**
  - **EP2SGX30 (8 channels max)**
    - **93% of logic usage**
  - **EP2SGX60 (12 channels max)**
    - **78% of logic usage**
  - **EP2SGX90 (16 channels max)**
    - **69% of logic usage**
  - **EP2SGX130 (20 channels max)**
    - **59% of logic usage**

- **To be investigated...**
  - **How can we reduce the used logic ?**

Test setup and results



First test:

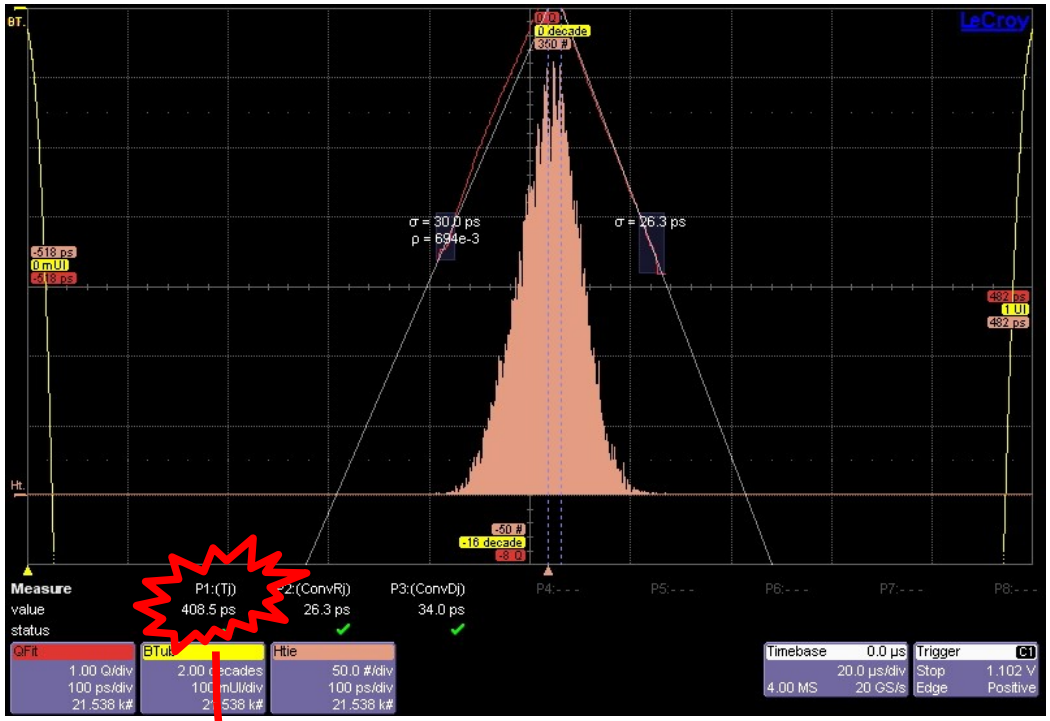
Clock input 120MHz (4.8Gbps)
Using decoding without correction
➔ Runs 48h without any error

Second test:

Clock input 160MHz (6.4Gbps)
Using decoding without correction
➔ Runs 48h without any error

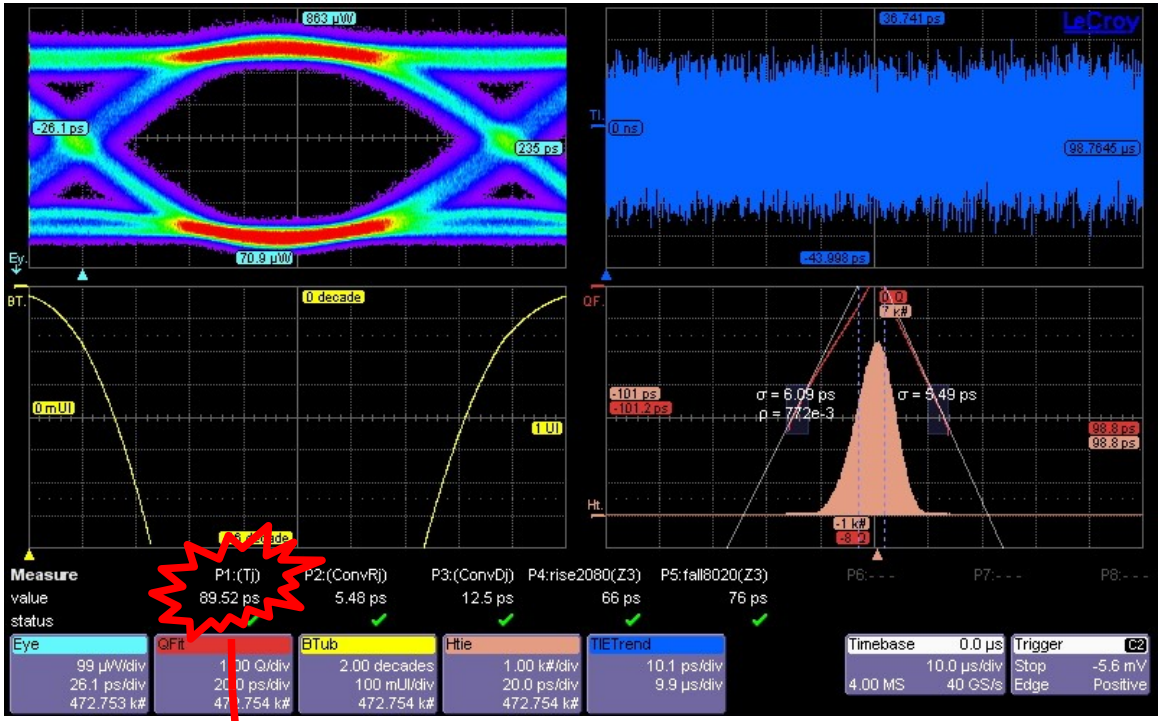
Measurements

- **120MHz clock jitter characteristics**



$Tj^{@BER=10^{-12}}=408ps$

- **Corresponding serial data jitter characteristics data rate = 4.8Gbps**



$Tj^{@BER=10^{-12}}=89ps\approx0.43UI$

Conclusions

- GBT protocol successfully implemented in an Altera Stratix II GX FPGA for up to 16 channels
  - The code will be available soon
- This custom protocol seems to need a lot of logic resources
  - Is it possible to decrease it ?
- The new Stratix IV GX will also be compatible with the GBT protocol and even better:
  - the deserializer latency will be reduced, due to the possibility to bypass the word aligner
  - it contains more logic resources

Questions, remarks ?