

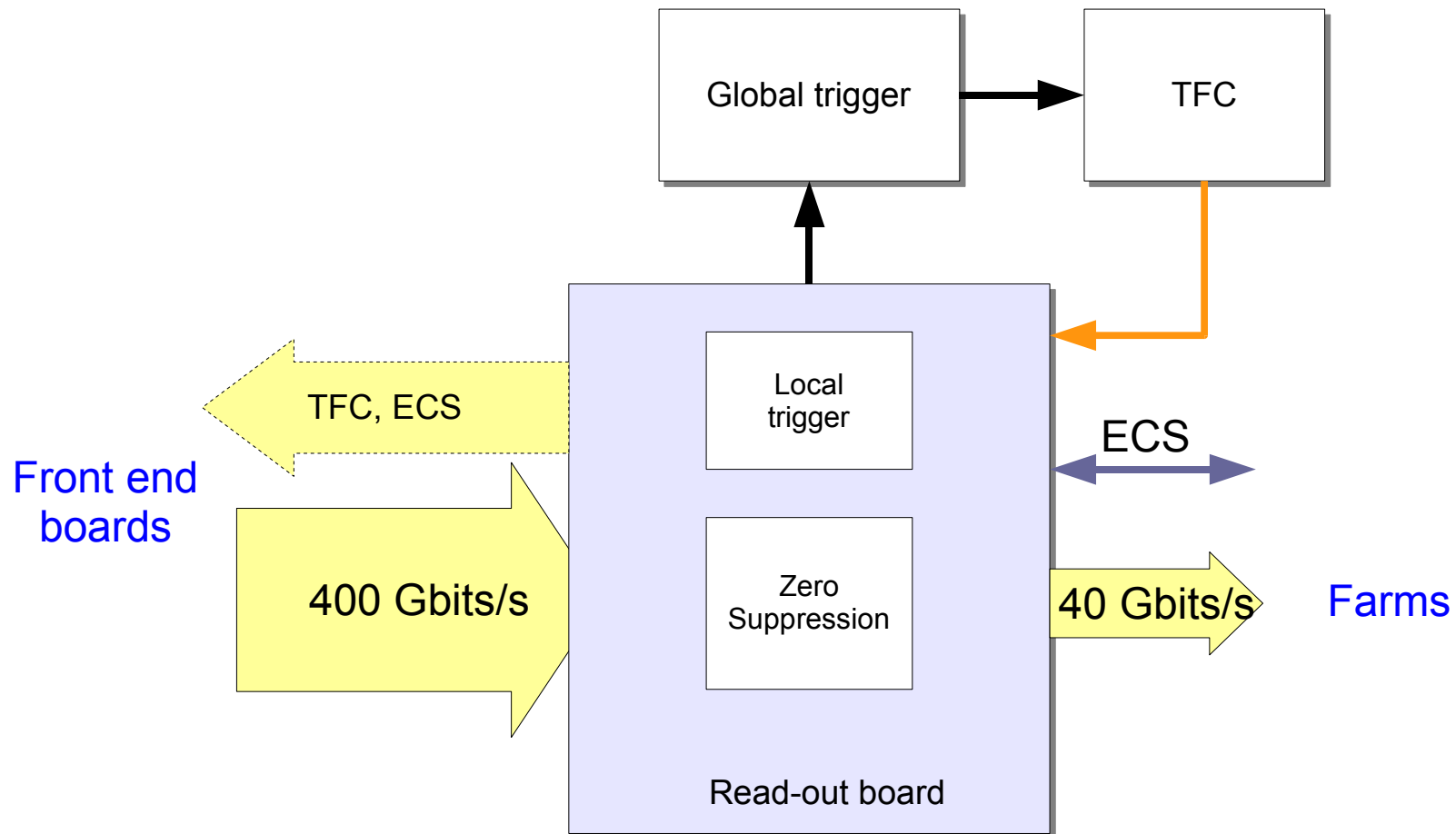
# CPPM R&D plans for LHCb upgrade in 2009

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- **Feasibility**
- **Identification of key technologies**
- **Studies to be done**
- **Conclusion**

Jean-Pierre Cachemiche on behalf of the Marseille group, CPPM

# Foreseen « New Readout » board



# Feasibility ?

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## New readout board: can we do it ?

- ◆ **Density:** 400 Gbits/s = 125 GBT links (if 80 bits are used for data acq)
  - ➔ 11 SNAP12 receivers  
4 to 6 times the density of current boards
  - ➔ + 11 SNAP12 transmitters if we follow the GBT bidirectional philosophy
  - ➔ (8 + 1) large FPGAs to collect and process the data  
2 times the density of current boards
- ◆ **Speed:** 4.8 Gbits/s in input, 10 Gbits/s in output
  - ➔ 3 to 6 times the current speed !
  - ➔ Parasitic phenomenas increase exponentially with the speed  
(skin effect, dielectric losses, sensitivity to jitter, ...)
- ◆ **Compression factor:** is a factor 10 still achievable with a higher luminosity ?
- ◆ Can we build a 40 MHz read out board at a cost equivalent to the current Tell1 boards ?

**No immediate reply: Above points need to be carefully studied**

# Other crucial points (1)

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## How do we supervise the system ?

- ◆ Can we embed the « Credit card PC » within the FPGAs ?  
Can we run Linux on it ?

## Can we comply to emerging standards ?

- ◆ New standards based on high speed links: ATCA,  $\mu$ TCA
- ◆ But ... impose severe constraints: communication topologies, board formats
- ◆ Really a lot of possible configurations !  
Manufacturers cannot provide all solutions.  
**How many will survive in a few years ?**
- ◆ Usability ?

# Other crucial points (2)

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## Can we emulate the GBT protocol in FPGAs ?

- ◆ GBT protocol and coding is custom
- ◆ No support in current FPGA serializer/deserializers  
**Implementability of the GBT protocol on the FPGA side ? Occupancy ? Latency ?**
- ◆ **Feasibility of TFC broadcast through FPGAs deserializers/serializers**
  - ➔ FPGAs **DO NOT** guarantee the phase of the extracted clock

## Can we accelerate the design and redesign ?

- ◆ Current size of FPGAs is 10 fold the size of FPGAs used in LHCb
- ◆ Time required to fill a FPGA was already around one year or more.  
Unthinkable to multiply this time by a factor 10.  
**Can we find methods and tools to accelerate designs ?**

# Other crucial points (3)

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## Can we take advantage of the huge FPGA processing power ?

- ◆ Could be used to provide additional pre-process data to help farm doing their job

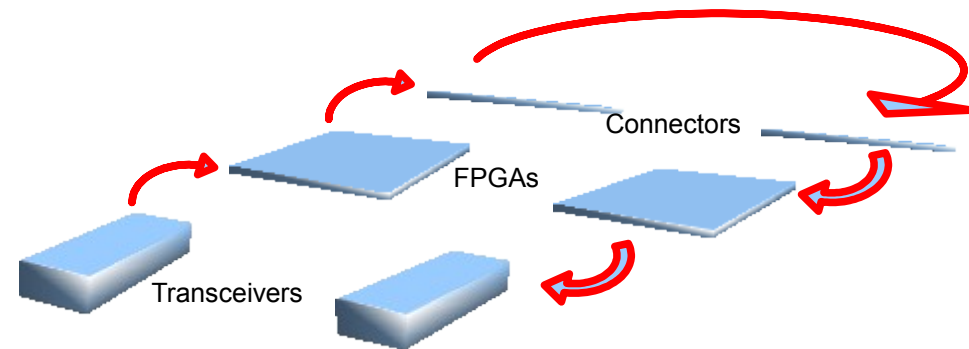
## Do we completely suppress the hardware trigger ?

- ◆ Read out boards could be used to compute the trigger or part of it
- ◆ Decreases pressure on farms and network
- ◆ But requires configurable **high speed connectivity between FPGAs and boards**

# What we propose to study

## Technology validation

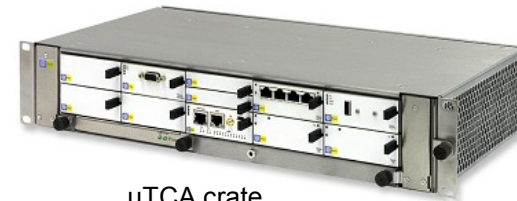
- ◆ **This is a technological survey not a final product !**
- ◆ The prototype helps us to test **typical data paths**:
  - ➔ *Optical transceiver to/from FPGA*
  - ➔ *FPGA to FPGA through backplane*
- ◆ **Limit the number of solutions to be explored**



# Electronics

## Prototype implemented on $\mu$ TCA form factor

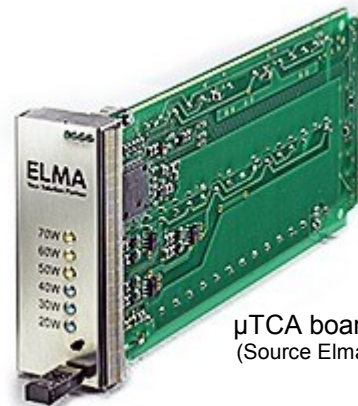
- ◆ Form factor is small:  
more appropriate for prototyping
- ◆ Cheap
- ◆ Many features off the shelf:
  - ➔ Crate
  - ➔ Power supplies
  - ➔ Standard backplane with dual star connectivity
  - ➔ Supervision entity running Linux
  - ➔ Embedded hub
  - ➔ Clock distribution



$\mu$ TCA crate  
(Source Elma)



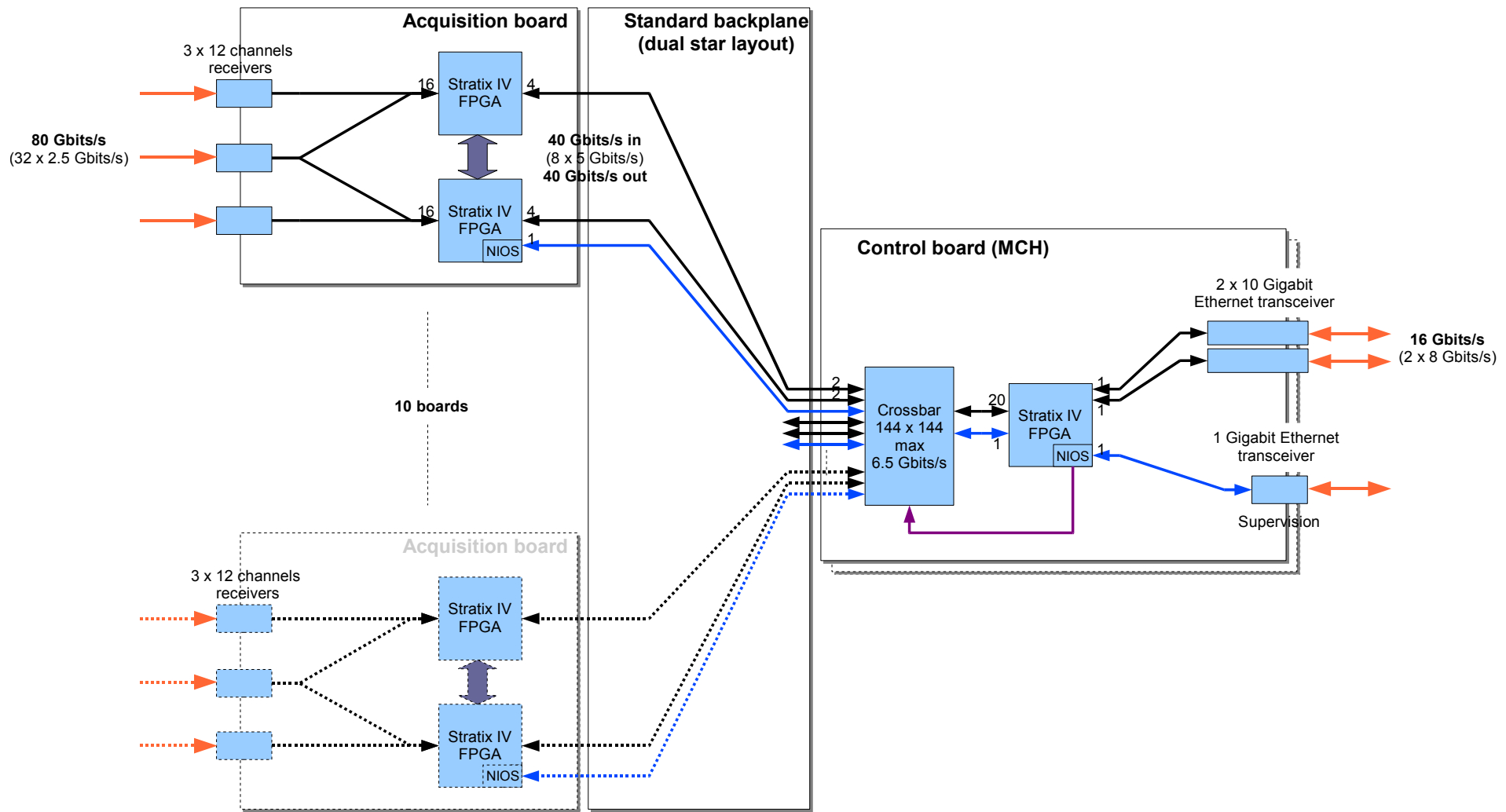
$\mu$ TCA crate  
(Source Kontron)



$\mu$ TCA board  
(Source Elma)



# Prototype architecture



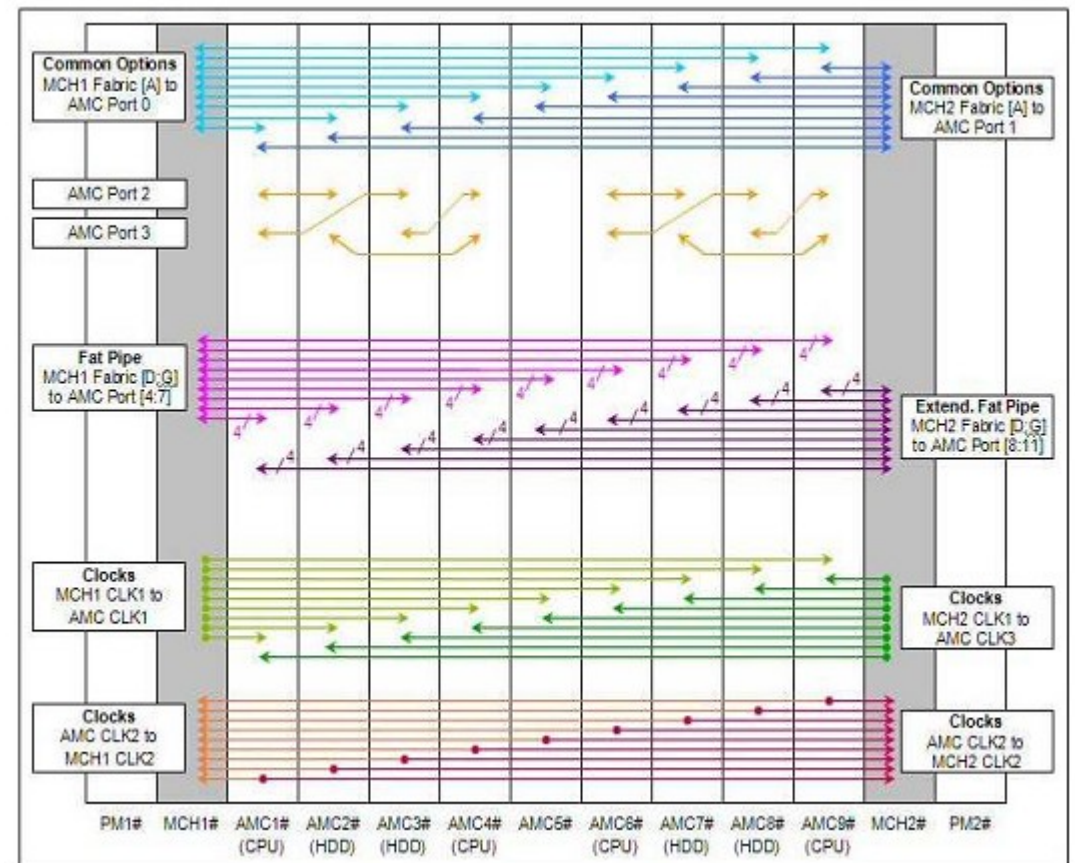
# Technological blocks we will focus on (1)

## Signal integrity

- ◆ Links at 8 Gbits/s and more
  - ➔ Connectors and backplanes
  - ➔ Domain of operation
  - ➔ Manufacturing constraints

## Connectivity between boards

- ◆ Use of a **star** or **dual star** connectivity to allow exchanges between boards



Dual star topology (source Schroff)

# Technological blocks we will focus on (2)

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## Control

- ◆ Implementation of a  $\mu$ C Linux core embedded in the FPGA
- ◆ Implementation of Dim/PVSS server on it

## Development speed

- ◆ Study tools for automatic generation of VHDL code from software
  - Automated generation of local bus interface/ registers
  - High level layer connecting precompiled pieces of design « à la L0DU »
  - Build customizable compression libraries, build or use IPs, ...
  - SystemC evaluation for codesign
  - ...

# Conclusion

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- ◆ 40 MHz read-out relies on **emerging technologies** and maybe on next generation
- ◆ Very difficult for the time being to define the better cost/technological compromise:
  - ➔ **Feasibility studies** mandatory on envisaged technologies
  - ➔ Validation elementary building blocks
  - ➔ **Key input to design final architecture and to determine its costs**
- ◆ Important to **keep open hardware solutions for the trigger**
- ◆ We are supported by our lab and by IN2P3 to evaluate these building blocks