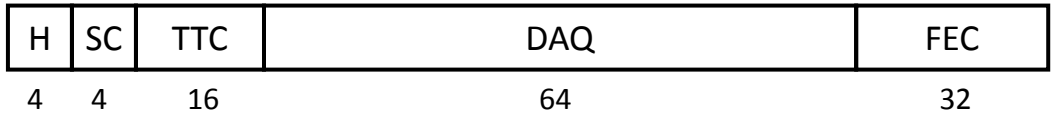
GBT protocol implementation on Xilinx FPGAs

Csaba SOOS

PH-ESE-BE-OT

GBT frame



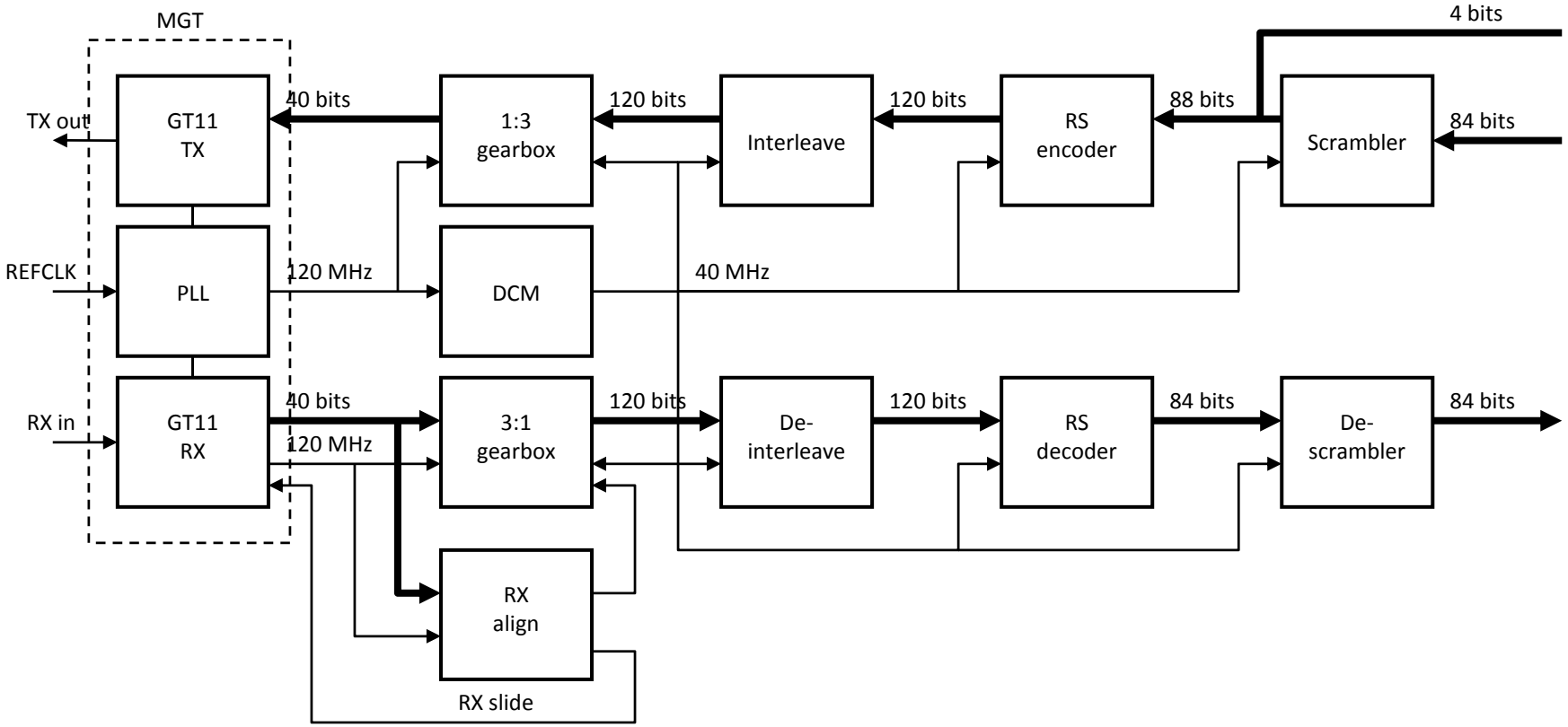
- 120 bits at 40 MHz => 4.8 Gb/s line rate
- User field of 84 bits, 3.36 Gb/s
  - 4 bits slow control (SC) => 160 Mb/s
  - 16 bits trigger, timing and control (TTC) => 640 Mb/s
  - 64 data (DAQ) => 2.56 Gb/s
- Bandwidth can be shared between front-end devices

Forward Error Correction (FEC)

- Interleaved Reed-Solomon double error correction
- RS(15,11): 4 bits per symbol, 11 data symbols + 4 parity symbols (60 bits)
- 2 encoders are used in interleaved mode
- Error correction capability: 2 x 2 symbols ≈ 16 bits
- Code efficiency: 88/120 = 73%

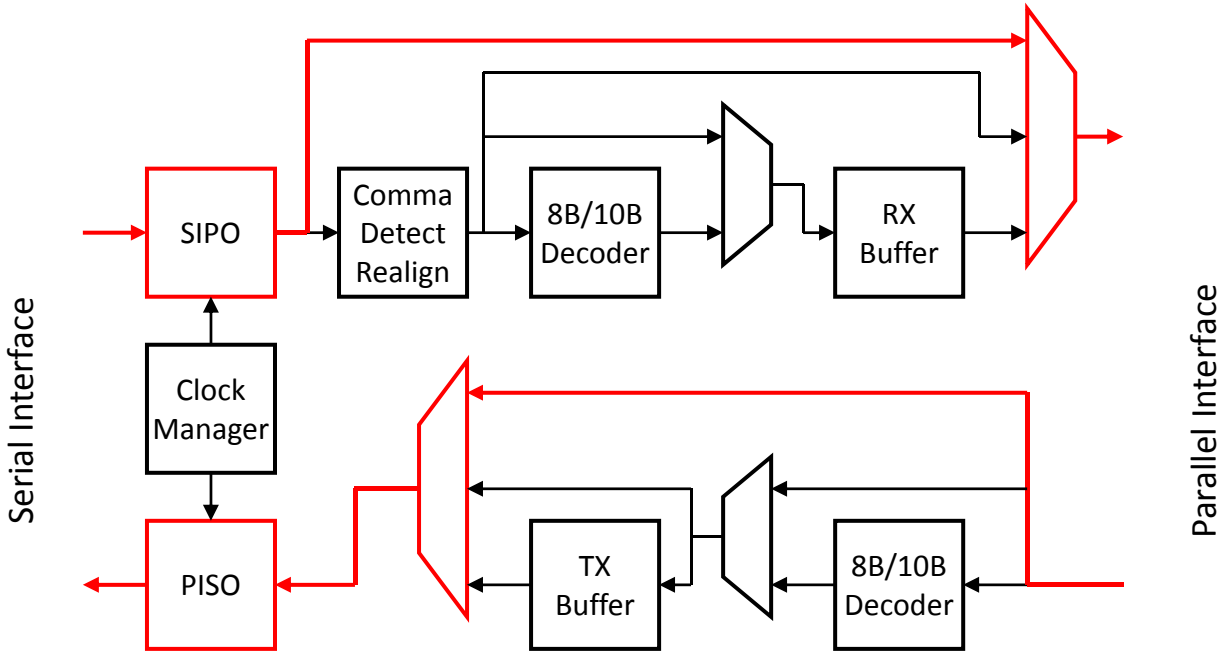
GBT channel

GBT transmit data path



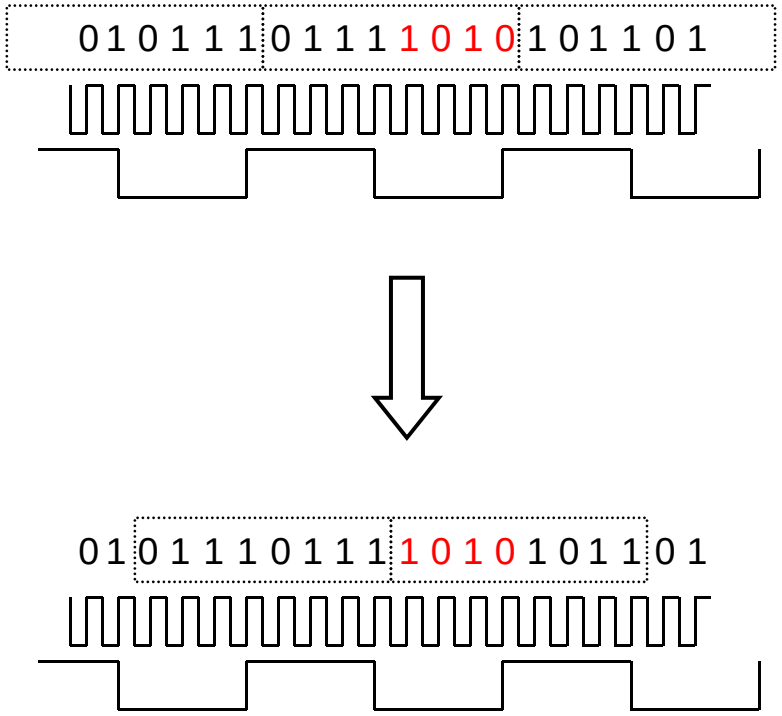
GBT receive data path

Virtex-4 RocketIO MGT



Simplified block diagram of the transceiver module

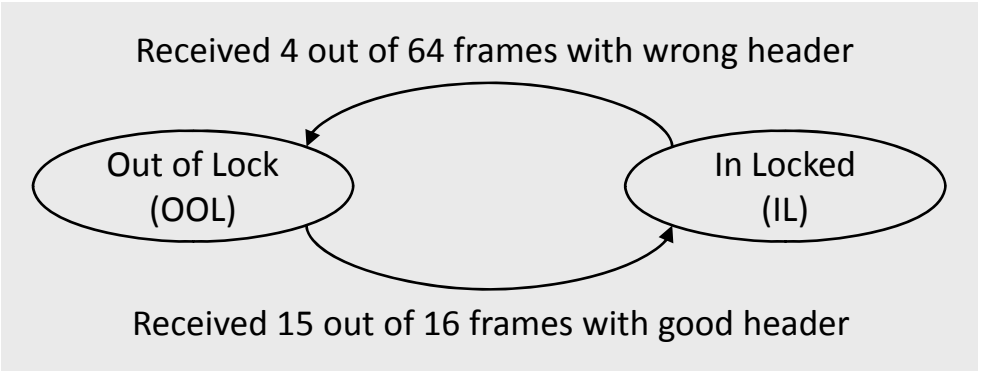
Word alignment



received data

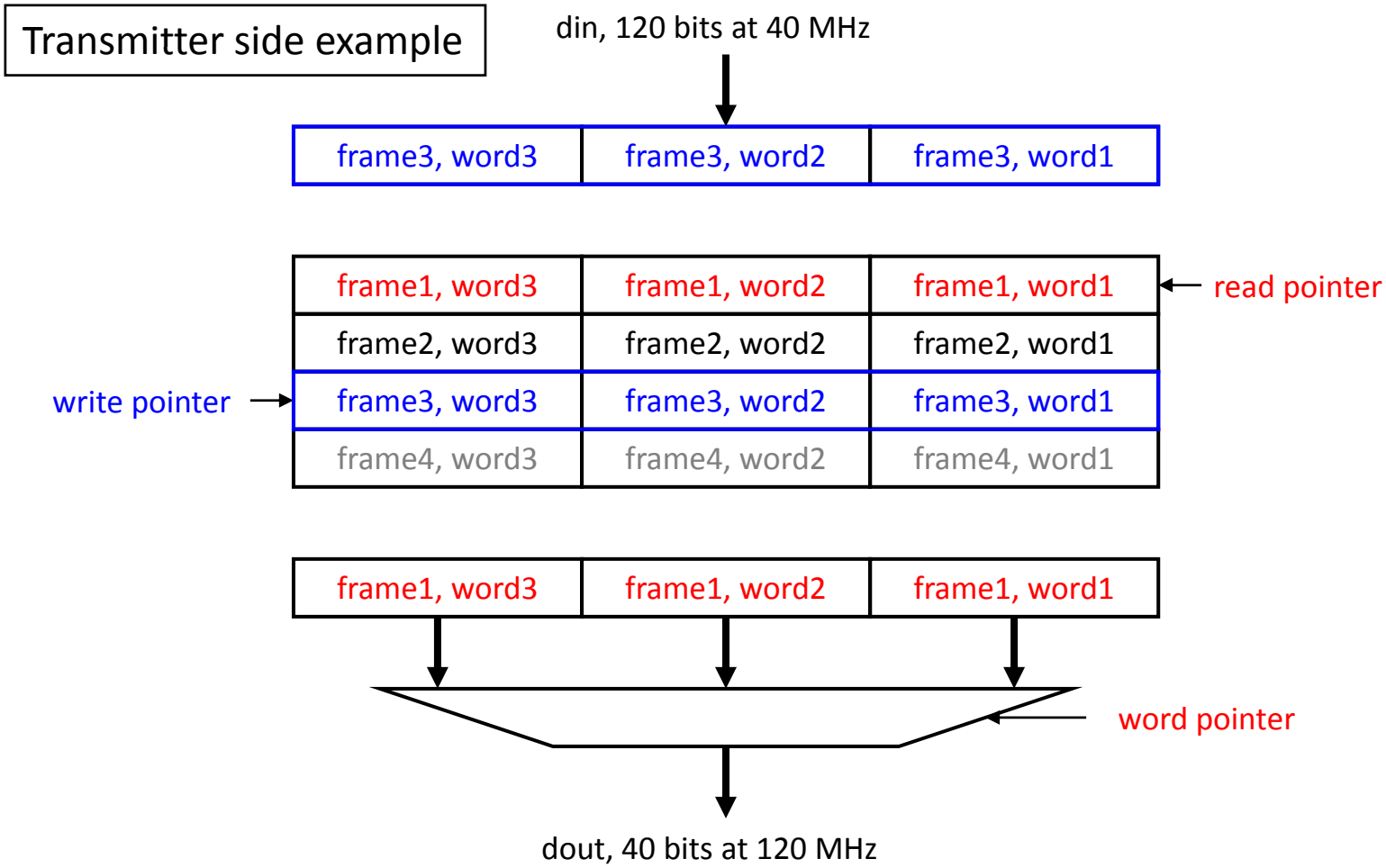
recovered bit clock

word clock

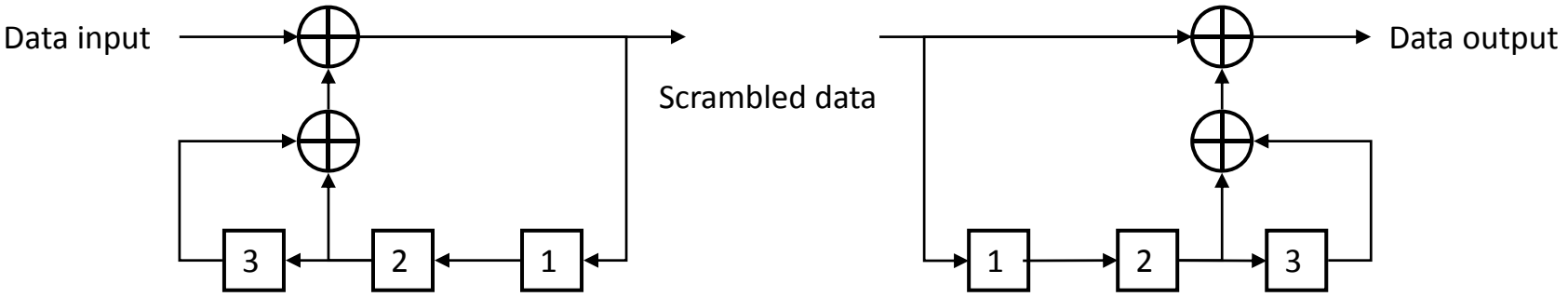


During the alignment, we slide the sampling window with a Barrel shifter. The process is controlled by a state-machine.

Gearbox


Transmitter side example
din, 120 bits at 40 MHz
frame3, word3
frame3, word2
frame3, word1
frame1, word3
frame1, word2
frame1, word1
read pointer
frame2, word3
frame2, word2
frame2, word1
write pointer
frame3, word3
frame3, word2
frame3, word1
frame4, word3
frame4, word2
frame4, word1
frame1, word3
frame1, word2
frame1, word1
word pointer
dout, 40 bits at 120 MHz

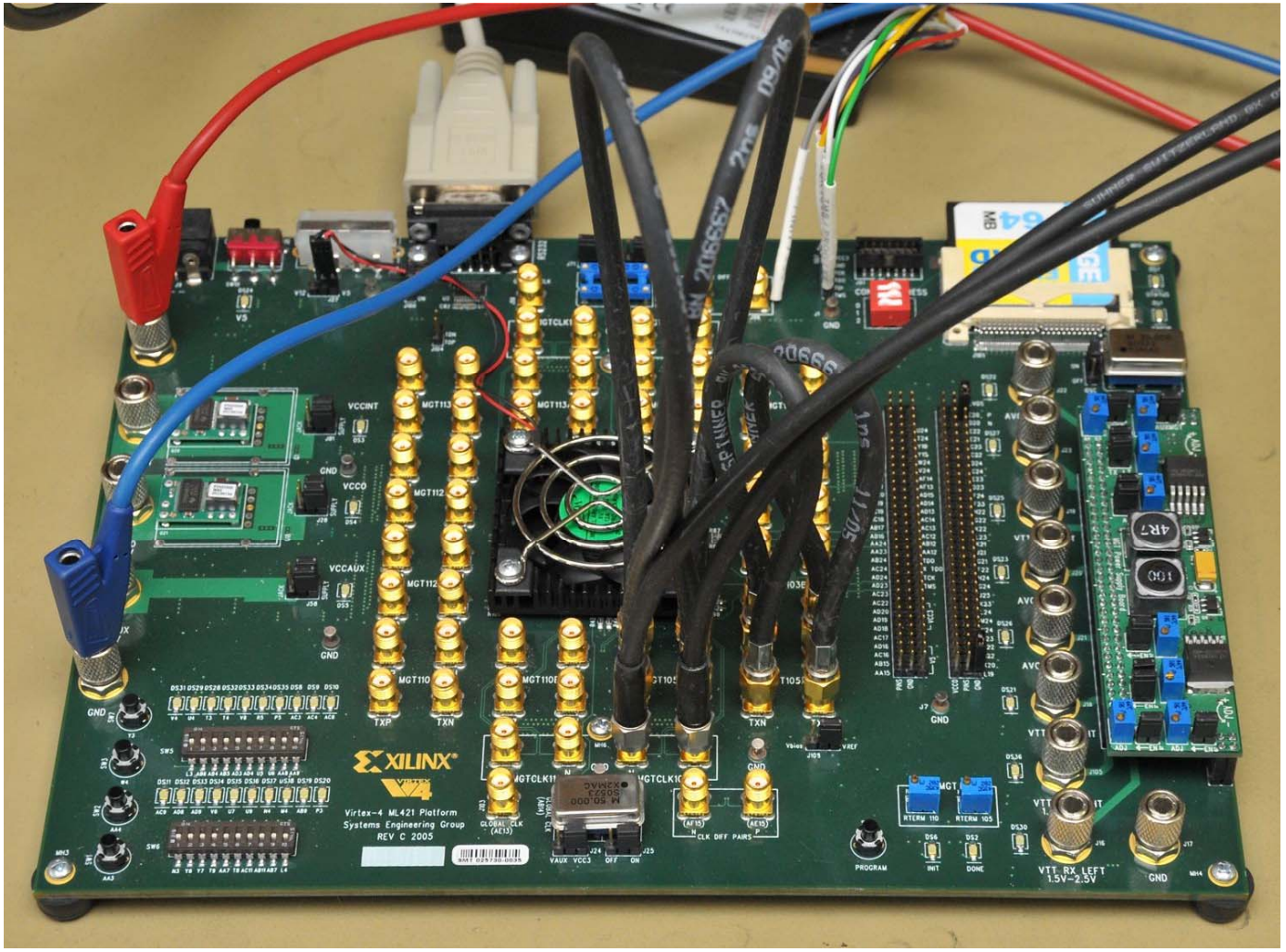
Scrambling/Descrambling



- Self-synchronizing (multiplicative) scrambler
- Defined by the polynomial of its LFSR (X^3+X^2+1 above)
  - should be a maximum sequence length polynomial and have the fewest taps possible
- GBT uses 21-bit scramblers ($X^{21}+X^{19}+1$)
- Can be implemented in parallel form (registers + XORs)
  - fewer taps result in simpler logic, hence higher speed

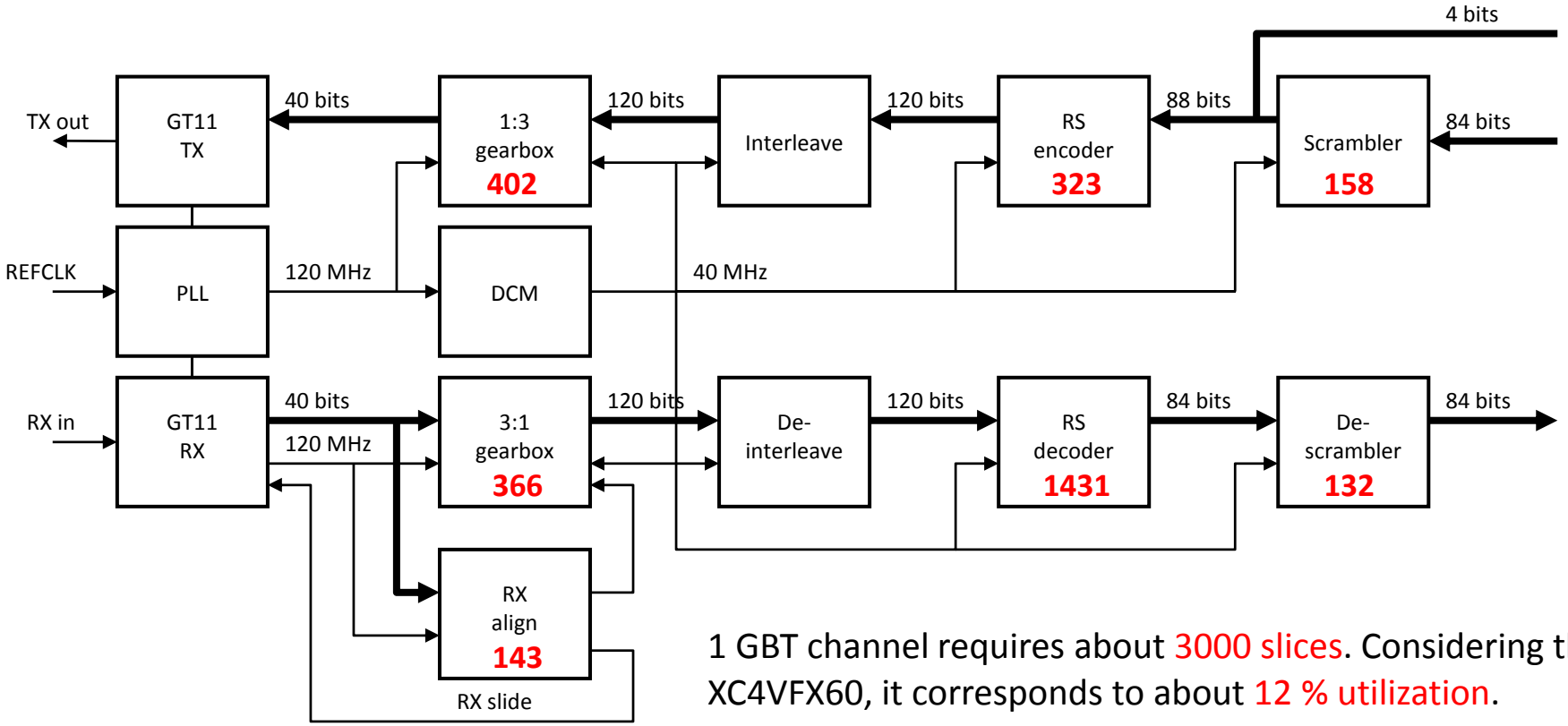
ML421 board

XC4VFX60 device:
- 12 MGTs
- 25,280 slices
- 128 DSP48 blocks
- 4,276,224 bits memory



Resource usage

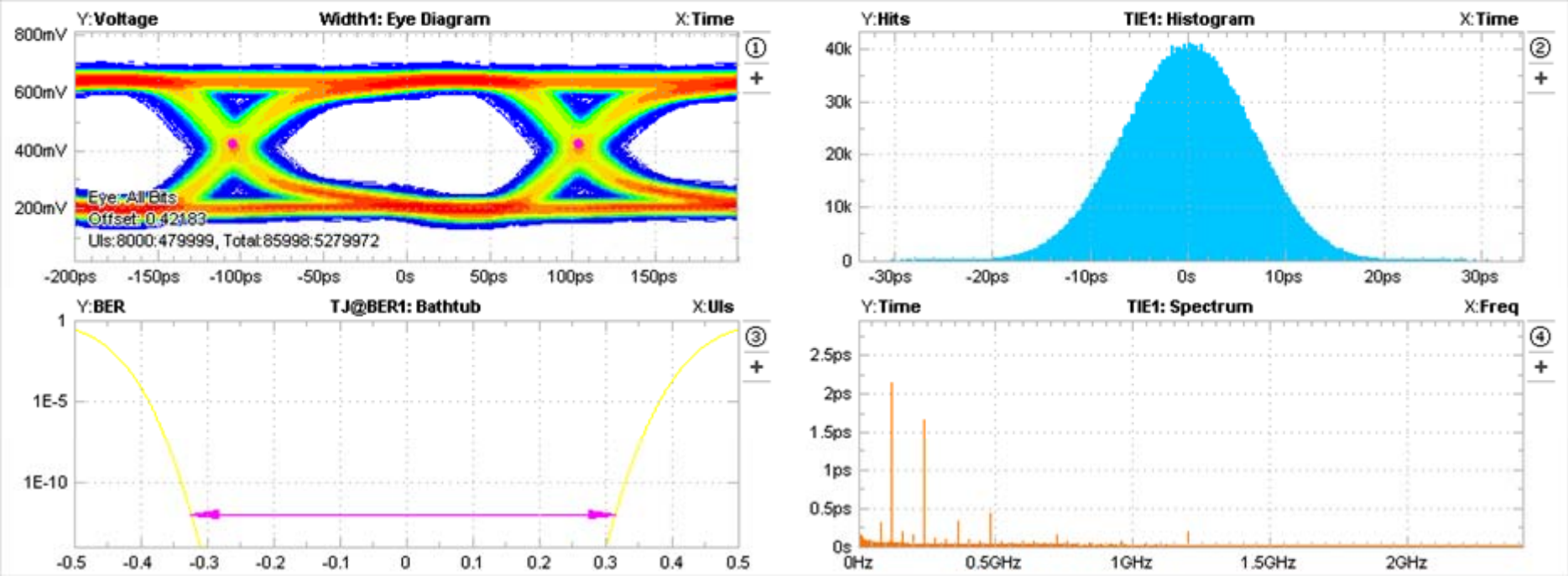
GBT transmit data path



1 GBT channel requires about 3000 slices. Considering the XC4VFX60, it corresponds to about 12 % utilization.

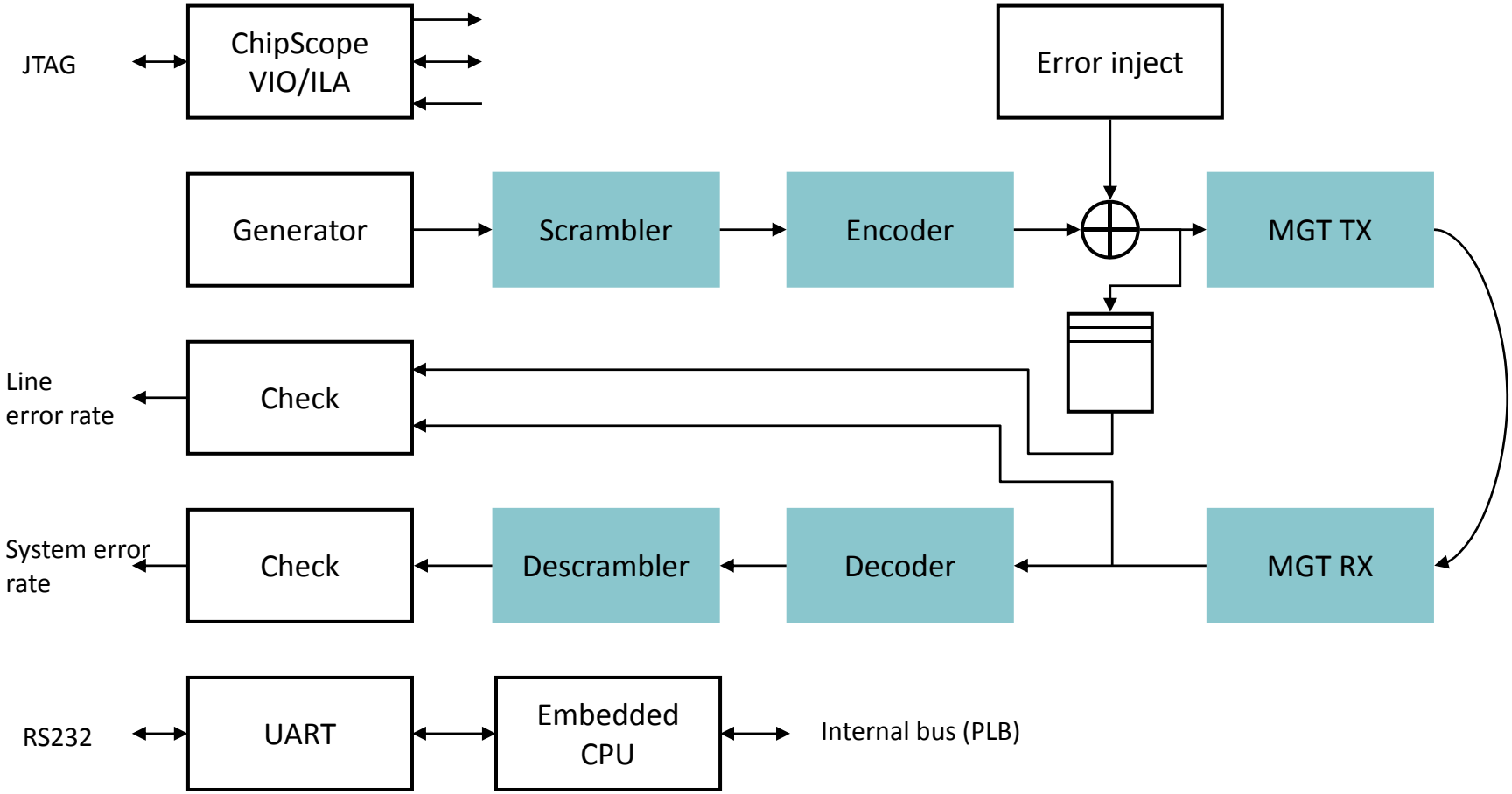
GBT receive data path

MGT performance at 4.8 Gbps

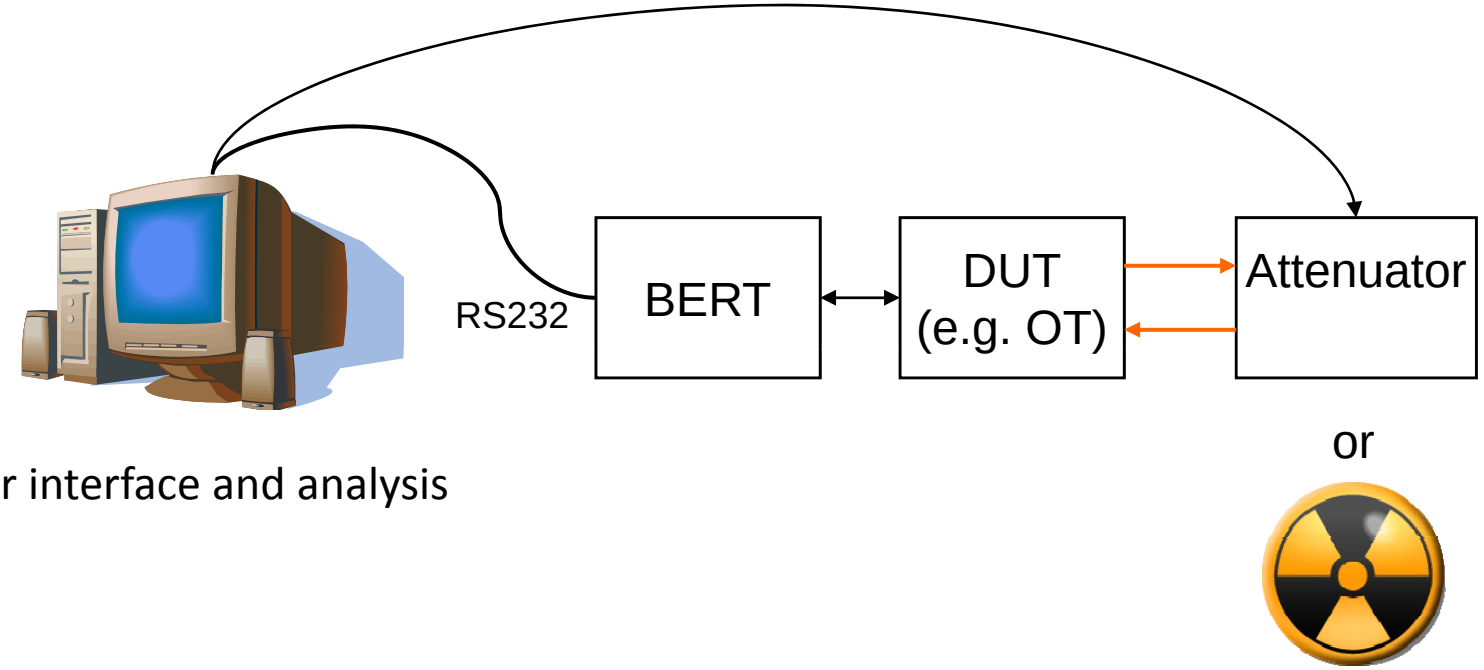


Jitter decomposition: Tj@BER10E-12 = 74ps, RJ = 3.9ps, DJ = 19.6ps

Application: BER tester

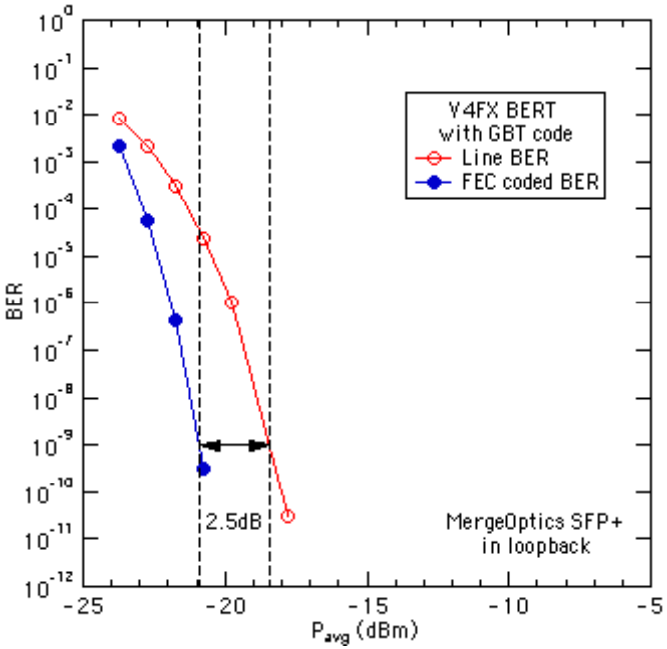


BER test system

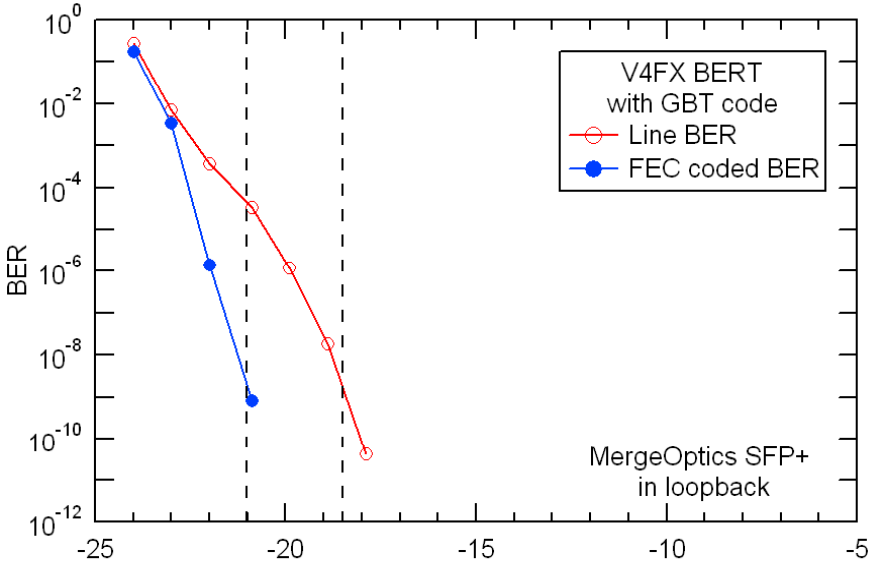


User interface and analysis

BER test result



Alignment is disabled



Alignment is enabled

Conclusion

- We gained lot of experience implementing the GBT protocol on the ML421 platform (Xilinx Virtex 4 FX)
  - The full data path has been tested
- The embedded transceivers are compatible with the GBT protocol
- BER testing can be performed using either the ChipScope or the UART
  - We need to develop the user interface for the second method (e.g LabView)