A Super-TFC for a Super-LHCb

- *Top-down approach* -

TFC Team: Federico Alessio
Zbigniew Guzik
Richard Jacobsson

General Reflections

Assumptions:

- Project in the cradle

- 40 MHz readout with 25ns bunch spacing

- Keep and maintain old TFC (?)

- Minimum MEP packing factor (?) (5-10 with InfiniBand?)

- (whatever is related to an upgrade is preceded by an )

Overall requirements:

1. Partitioning of the detector in sub-systems
2. Intelligent throttle based on some local trigger conditions within S-ROBs
3. Destination assignment with load balancing of the farm
4. ODIN data bank
5. Calibration commands, reset commands for synchronization
6. Clock control (phase, low jitter) and reception/distribution (“synchronicity”)

Reflections on Current TFC

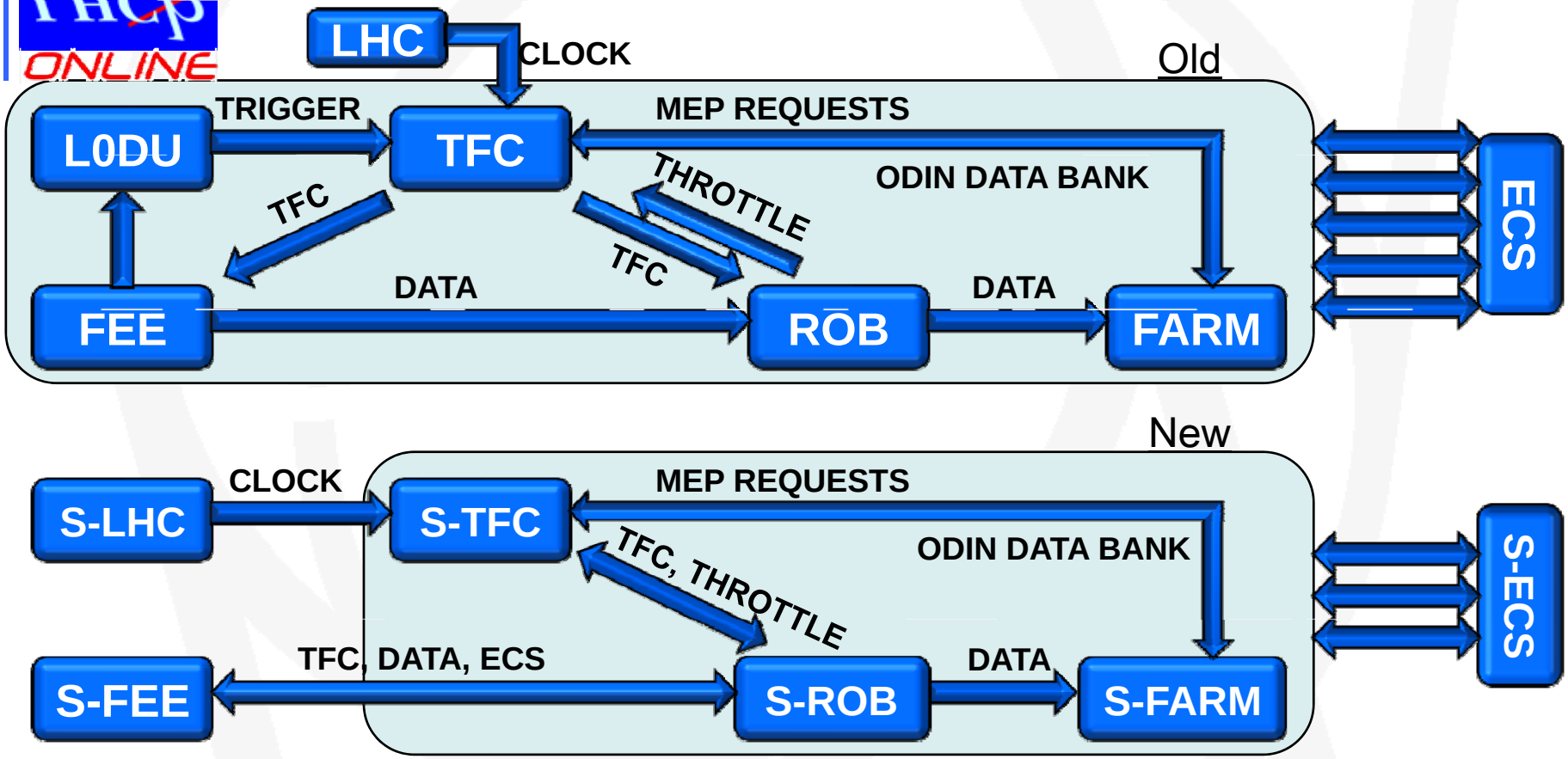
What is questionable?

1. A pool of identical ODINs
2. “Discrete” partitioning electronics → Switches THOR and MUNIN
3. A lot of “inter-board” connections based on single ended signaling over LEMOs
4. Separate network for TFC and Throttle based on different technologies
5. Dedicated (and separate) TFC links to FEE and ROBs

Single ODIN Resource usage:

- ~25k logical elements
- 40/80 MHz clock speed
- Memory usage (L2 cache-like) 2.4 MByte
- Control resources (~400 logical/functional parameters) organized in ~100 32-bit registers
- Monitoring resources readout via subscription mechanism, ~100 32-bit registers (packing of monitored data by “TFC server”)
- ODIN data bank 40 Bytes of data words

Old vs New

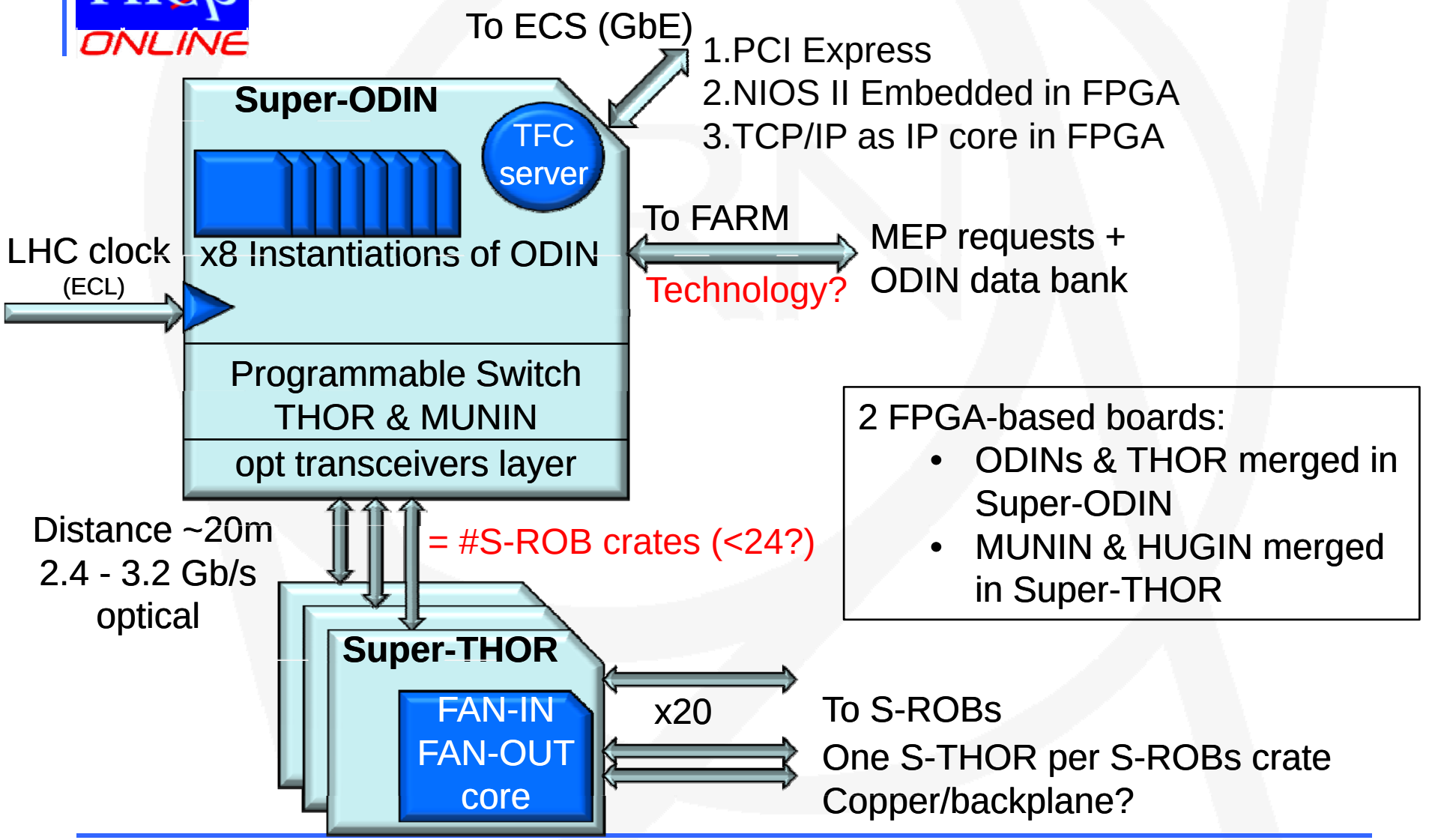


Obvious conclusions:

- Many fewer optical TFC links (TFC distribution rides on GBT to FEE)

- Shared serial link for TFC and Throttle signals (bidirectional)

New: TFC wise



2 FPGA-based boards:

- ODINs & THOR merged in Super-ODIN
- MUNIN & HUGIN merged in Super-THOR

New: TFC protocol (1)

Super-ODIN ←→ Super-THOR link

- Current idea is TFC control fully synchronous protocol with 48+header bits/event(@40MHz)
  → 2.4 - 3.2 Gb/s
  1. All TFC information encoded in 48 bits words sent every event
  2. A minimum MEP factor could reduce this by having two different word lengths
  3. Even though RS-encoding mainly for radiation environment, also used on TFC links for maximum reliability (header ~16 bits)
- Throttle("trigger") protocol
  1. Must be synchronous (currently asynchronous)
     → Both protocol will require alignment
  2. Word length of 20 yes/no bits/event for a S-ROB crate + id + header

- Currently looking at how a subset of TFC control protocol can be incorporated on GBT link for FEE

New: TFC protocol (2)

Super-THOR ←→ Super-ROB link

- Copper or backplane technology
- TFC synchronous control protocol same as S-ODIN←→ S-THOR
  → One GX transmitter with external transmitter 20x-fan-out (PHYs)
- Throttle("trigger") protocol simplified using 20x SERDES interfaces <1.6 Gb/s
- In practice 20 HI-CAT bidirectional links

Super-ODIN

Board with one big central FPGA (Altera Stratix IV GX or alt. Stratix II GX for R&D)

- Instantiate a set of ODINs cores to guarantee partitioning control for sub-detectors
- TFC switches become a programmable patch fabric: a layer in FPGA
  → no need of complex routing, no need of “discrete” boards
- #logical elements for TFC functionalities should be less than current ODIN
- More I/O interfaces based on bidirectional transceivers
  → depend on #S-ROBs crates
- No direct links to FEE
- Common server that talks directly to each instantiation:
  → DIM server in NIOS II or even VHDL … ?
- Flexibility to implement (and modify any protocol)
  → GX transceiver as IP cores from Altera
- Control average rate based on “yes/no recommendation” of local trigger logic within potentially each S-ROB
- “Absolute rate” can only be controlled if S-ROB output buffer is deterministic
- Bunch structure (predicted/measured) rate control

Super-THOR

Board with FPGA entirely devoted to fan-out TFC information/fan-in throttle info

- Controlled clock recovery
- Shared network for Throttling (Intelligent) & TFC distribution
- All links bidirectional
  → 1 link to S-ODIN, 2.4 - 3.2 Gb/s, optical
  → 1 link per S-ROB, 20 max per board (full crate)
- Technology for S-ROBs links could be backplane (ex. ATCA) or copper HI-CAT
- Protocol flexible: compatibility with flexibility of S-ODIN
  → We will provide the TFC transceiver block for S-ROBs' FPGA to bridge data to FEE through GBT

- For stand-alone test benches, Super-Thor would do the work of a single ODIN instantiation

Action list & plans

- Simulation framework of entire TFC in preparation
  - → Thanks to Marseille team we have the GBT protocol in simulation
- Soft studies
  - Defining the TFC protocol ontop of GBT
  - Define TFC/throttle protocol between S-ODIN ←→ S-ROBs
  - Both protocols should incorporate latency fidelity and allow alignment
  - Throttle latency → S-ROB buffering
  - Resource usage in S-ODIN and S-THOR
  - InfiniBand destination addressing?
  - Contents of an ODIN data bank
- Hard studies
  - Clock control, latency fidelity, and jitter through GX transceivers
  - TFC_server (DIM) in NIOS II
- We have good chances to get onto Altera Early Access Program for Stratix IV 230 GX
  - → good contact with Field Application Engineer from Altera
  - Alternatively we could use Stratix II GX
  - Idea is to design S-ODIN prototype 2009Q2-Q3 for the hard studies and protocol tests

Environmental Questions

-To which extent is output buffer of S-ROB deterministic?

-What are the jitter requirements for sub-detectors?

-What is the planned protocol for DAQ?