

Monolithic Pixel R&D at LBNL

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An R&D effort of LBNL & University - INFN, Padova
in collaboration with KEK & JPL-NASA

Monolithic Pixel Meeting
CERN, November 25, 2008

Technology/Application Matrix



| | <u>Thin CMOS</u> | <u>SOI</u> | <u>3D</u> |
|-----------------|--|---|--|
| Technology R&D | Sensor Thinning In-pixel CDS Fast r/o Radiation Tolerance on-chip ADC | Proof of principle Back-gating Radiation Tolerance Thinning and Backplane Processing | Technology Characterisation Sensor Integration |
| HEP/LC | Prototype Thin Tracker ILC-compliant Sensor (20 μ m pixel, 25-50MHz column parallel r/o, 5-bit ADC, low power) | Prototype Thin Tracker ILC/CLIC-compliant sensor (10 μ m digital pixel, >50MHz column parallel sparsified r/o, time stamping) | |
| Imaging Spinoff | Fast Nanoimaging in TEM | Beam Monitoring Solar and Earth Observation Fast Nanoimaging in TEM | |

Prototype Monolithic Pixel Chips



Thin CMOS

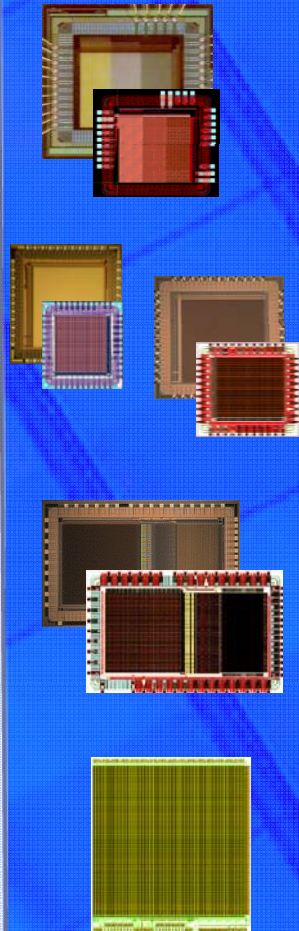
AMS 0.35 μ m-OPTO

- **LDRD-1** (2005)
10, 20, 40 μ m 3T pixels

- **LDRD-2** (2006)
(+ **LDRD-2RH**(2007))
20 μ m pixels, in-pixel CDS
(+ RadHard pixels)

- **LDRD-3** (2007)
20 μ m pixels, in-pixel CDS
on-chip 5-bit ADCs

- **TEAM Imager** (2009)
1kx1k 9 μ m pixels, analog



SOI

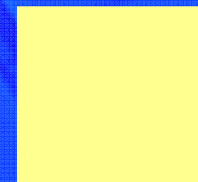
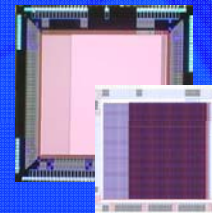
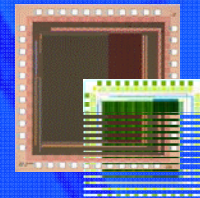
OKI 0.15 μ m FD-SOI

- **LDRD-SOI-1** (2007)
10 μ m pixels,
analog & binary pixels

OKI 0.20 μ m FD-SOI

- **LDRD-SOI-2** (2008)
20 μ m pixels, in pixel CDS
fast binary pixels

- **LDRD-SOI-3** (2009)
~10 μ m pixels, 4x4 mm²
imager w/ fast readout



Main R&D Objectives



Monolithic Pixel R&D originated with ILC application, nowadays HEP R&D leveraged with on-site spin-off projects funded over 2-3 FYs:

Back-thinning of CMOS pixel sensors and application to ILC/CLIC tracking and vertexing

Demonstrator chip for ILC/CLIC Vertex Tracker

Thin CMOS Imager for Dynamic Transmission Electron Microscopy

Demonstration of SOI technology and development of Fast SOI Imager for low energy electrons and photons

Back-thinning of CMOS pixel sensors and application to LC tracking and vertexing



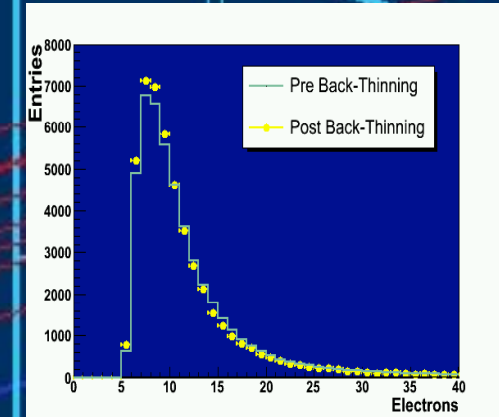
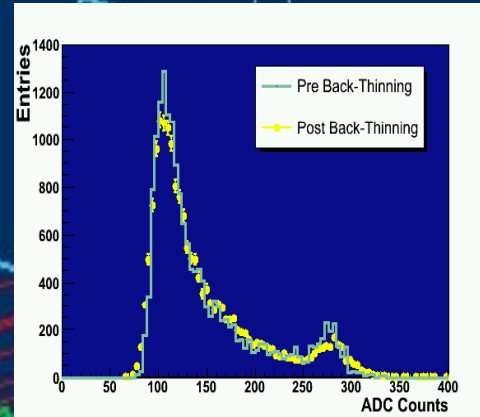
Thinning of MIMOSA-5 diced chips

Backthinning yield ~ 90 %:

“50 μm ” = $50 \mu\text{m}$,

“40 μm ” = $40 \mu\text{m}$;

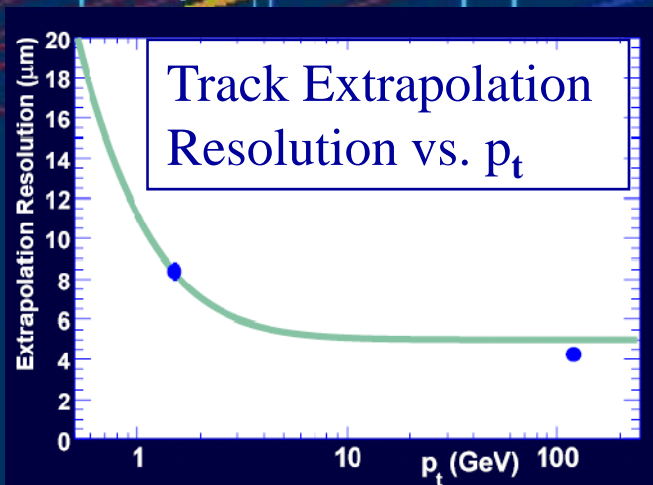
chips fully characterised before/after:



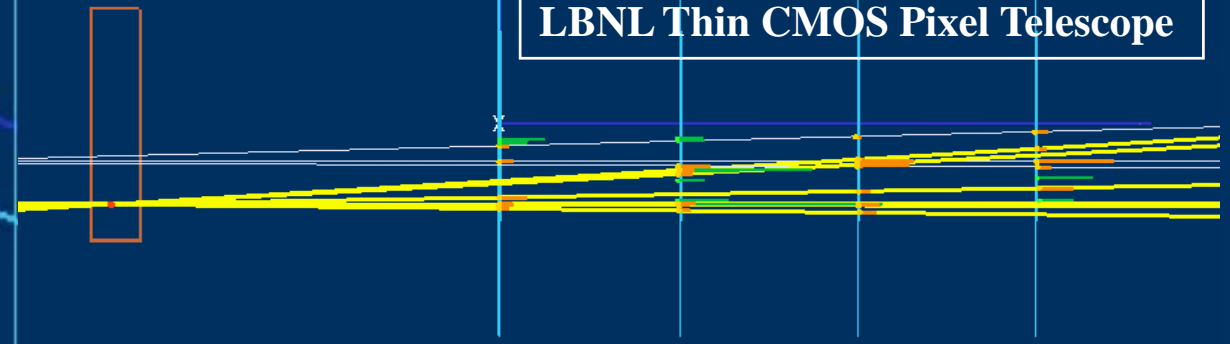
NIM A579 (2007)

Thin Pixel Prototype Telescope

4 layers of 50 μm thin MIMOSA-5, 15 mm layer distance,
tracking results at ALS 1.5 GeV e^- beam and MBTF 120 GeV p beam



FNAL MBTF T966 Data
120 GeV p on Cu target
LBNL Thin CMOS Pixel Telescope



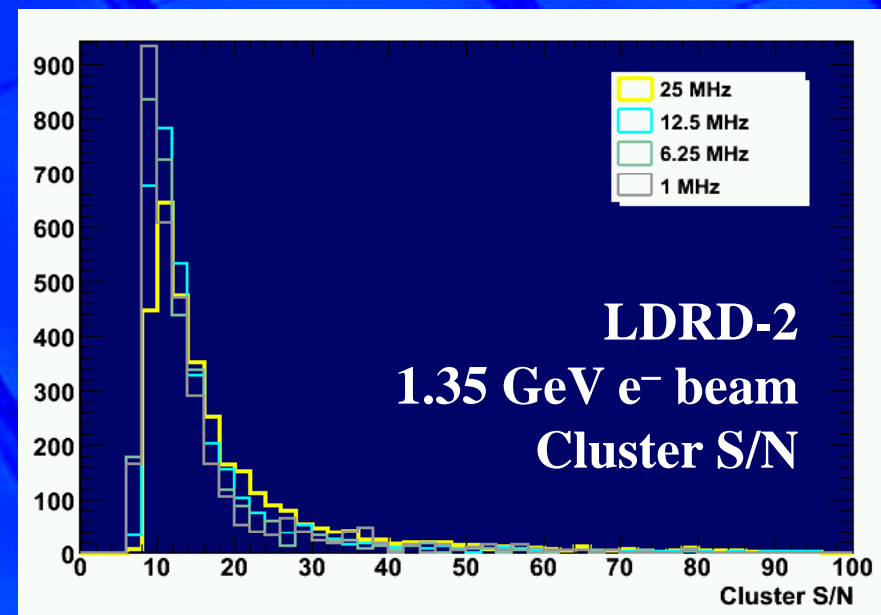
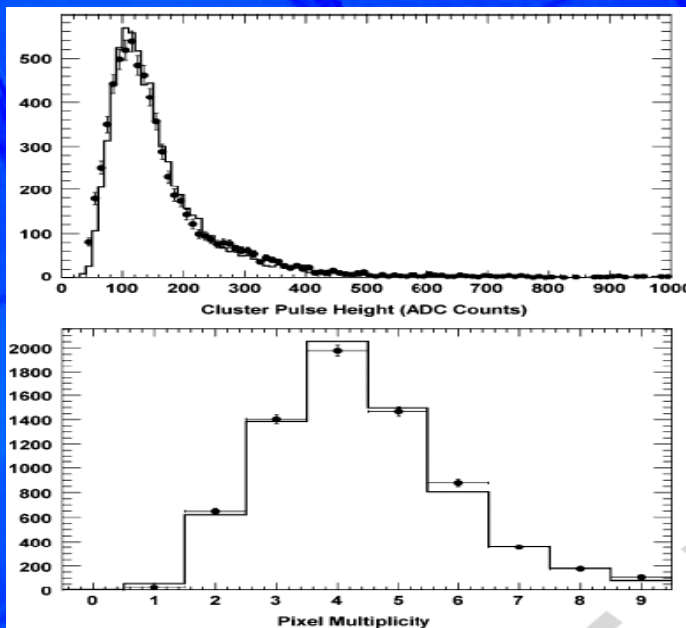
Demonstrator chip for LC Vertex Tracker



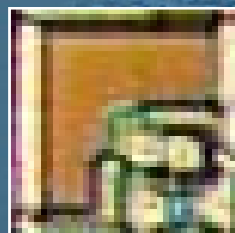
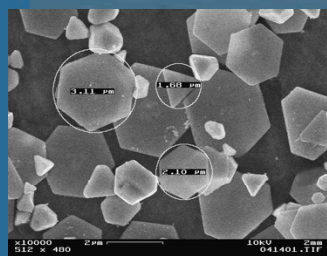
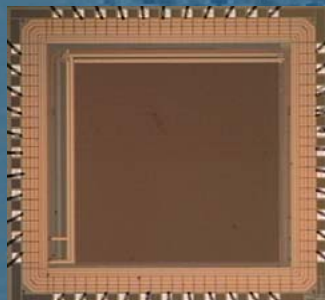
LDRD-2 chip with 20 μ m pixel, in-pixel charge storage for CDS,
25 MHz r/o tested on ALS and MBTF and irradiated at LBNL 88-inch cyclotron

Cluster S/N = 12-13 for r/o from 1 MHz to 25 MHz;

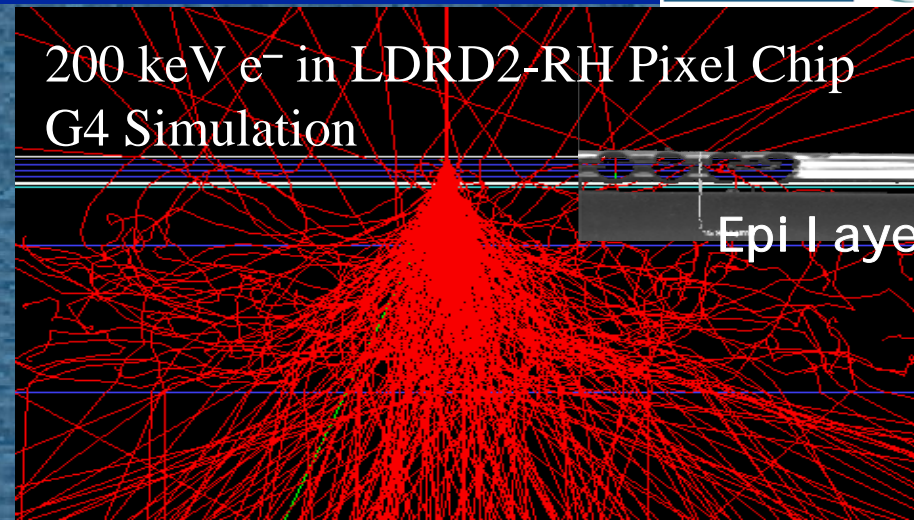
Chip performs well up to several hundreds kRads from 200 KeV electrons
and 10¹³ n cm⁻²



Thin CMOS Imager for Electron Microscopy

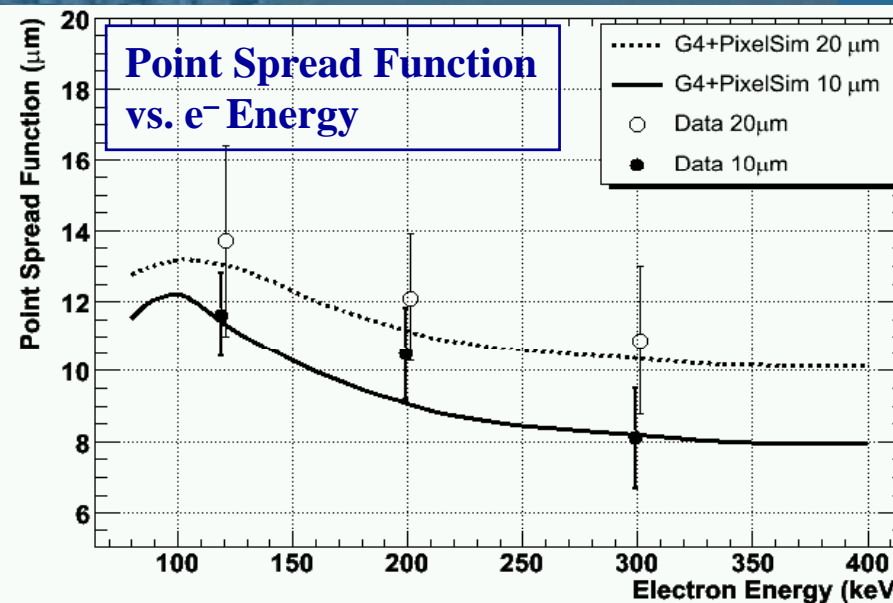


200 keV e⁻ in LDRD2-RH Pixel Chip
G4 Simulation



LBNL program to develop large surface (1→4 cm²), rad-hard CMOS imager with fast readout (up to 400 frames s⁻¹) for deployment at TEAM microscope;

- Single e⁻ sensitivity;
- < 10 μm Point Spread Function;
- Radiation tolerant to > 1 MRad.



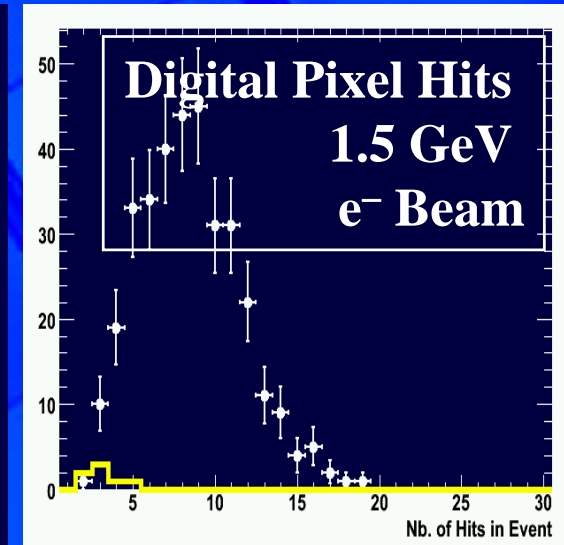
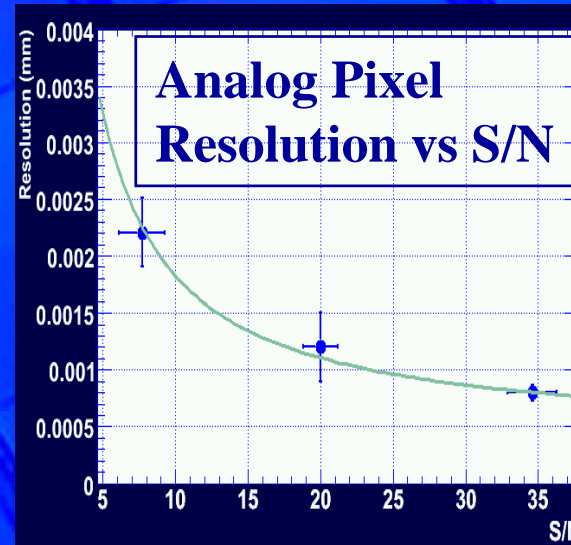
Demonstration of SOI technology and development of fast SOI imager for low energy electrons and photons



First demonstrator with 3T analog and simple digital (10 μm)

NIM A583 (2007)

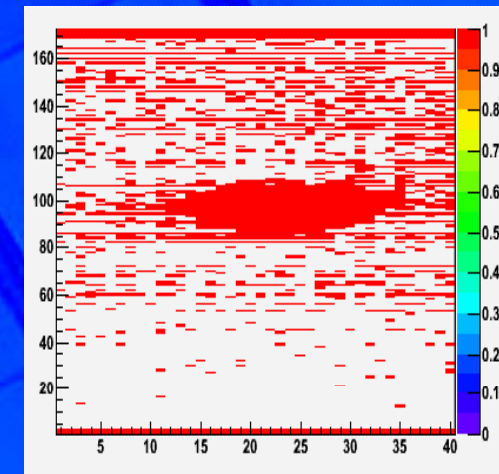
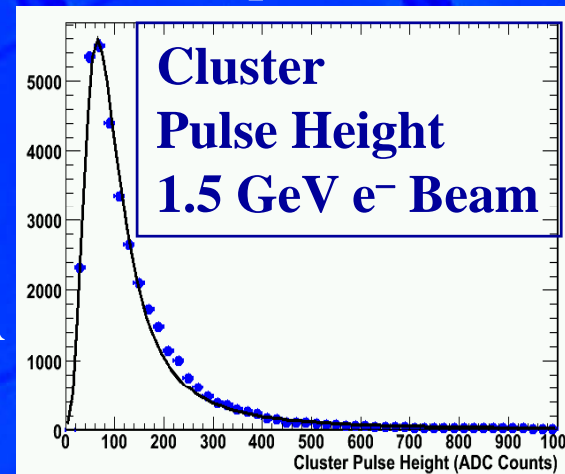
and to appear on NIM A (2009)



Fast Analog Pixel and Digital Pixel with in-pixel CDS and current threshold

Analog Readout at 50 MHz,
<S/N> for 1.5 GeV e⁻ Beam = 15
Digital pixel fully functional

Collaborative R&D with JPL-NASA
on thinning and backplane
post-processing



Planned Activities for FY2009-2010



- Submission, characterisation and deployment of 1kx1k TEAM imager, design of 2kx2k final imager (LBNL);
- Beam telescope based on thinned 1kx1k TEAM sensors and test at MBTF (LBNL+INFN Padova+Purdue U(?));

- Backside post-processing of thin SOI sensors for low energy radiation (LBNL+JPL-NASA);
- Development of fast SOI imager and test at LOASIS and other facilities (LBNL+JPL-NASA+INFN Padova+IPNL);
- Characterisation of radiation tolerance of OKI-SOI process (LBNL+KEK+INFN Padova);

- Submission and characterisation of ZyCube 3D process (LBNL+KEK)