Column Parallel CCD and Raw Charge Storage Pixels by LCFI

Andrei Nomerotski, University of Oxford

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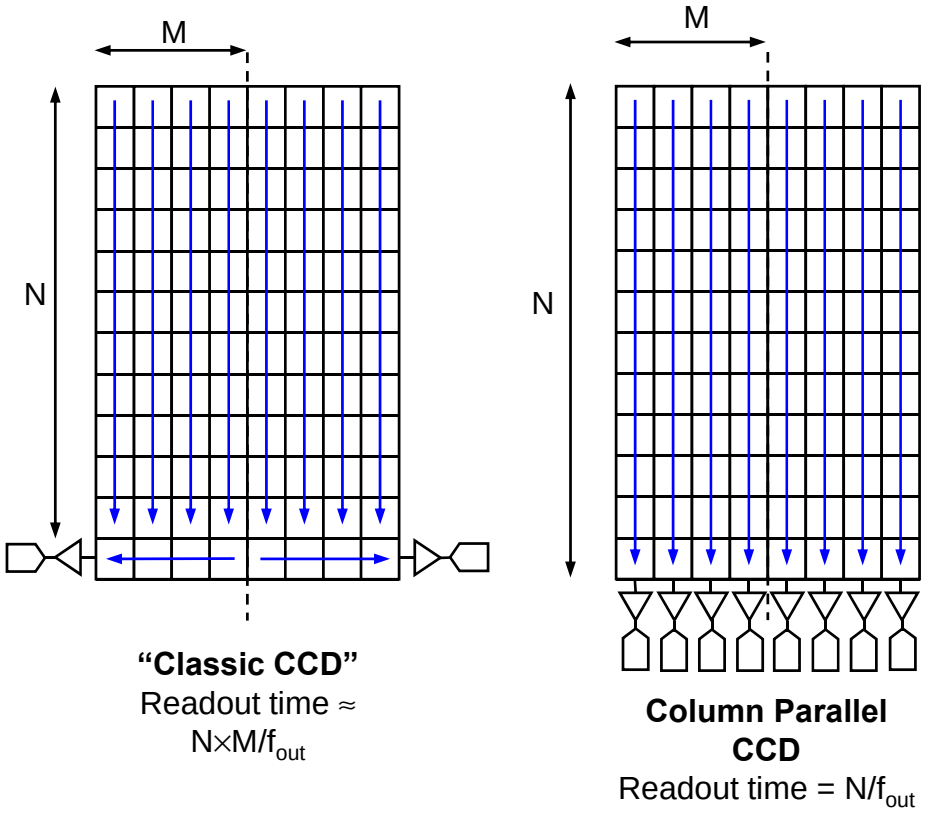
CPCCD Sensors: CPC2

Column Parallel CCDs

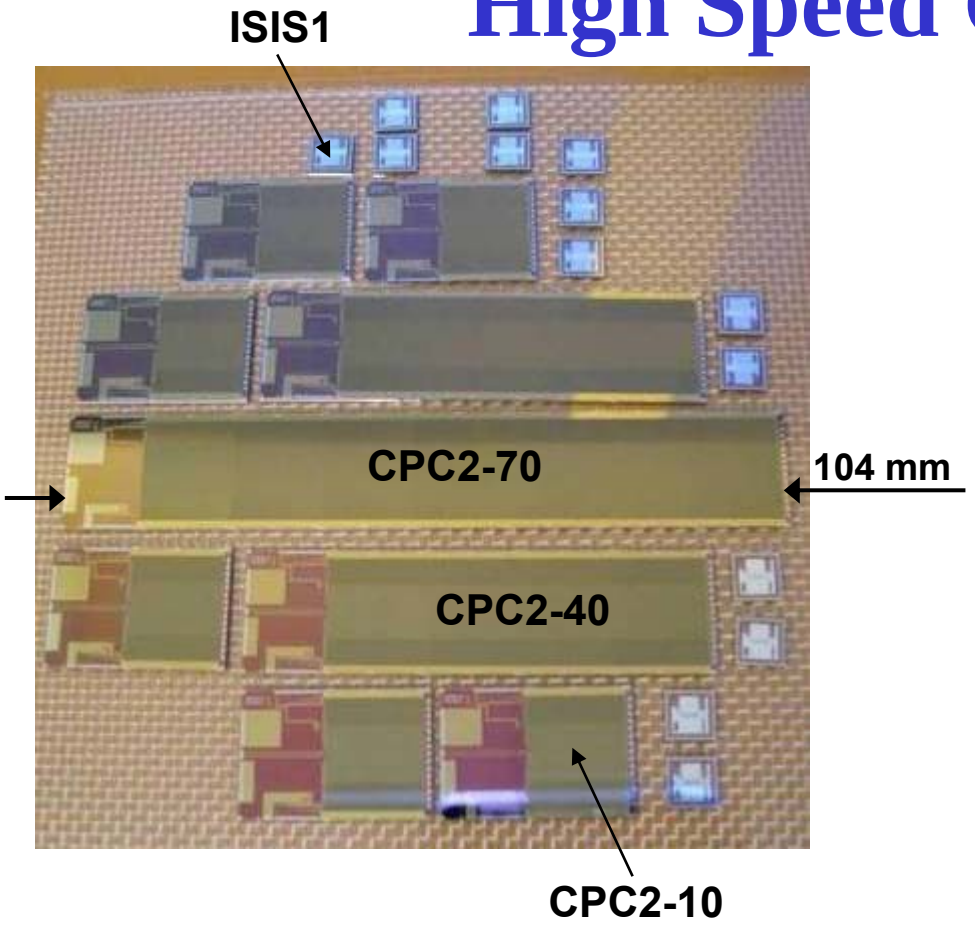
- **Every column has its own amplifier and ADC**
- **All of the image area is clocked, complicated by the large gate capacitance**



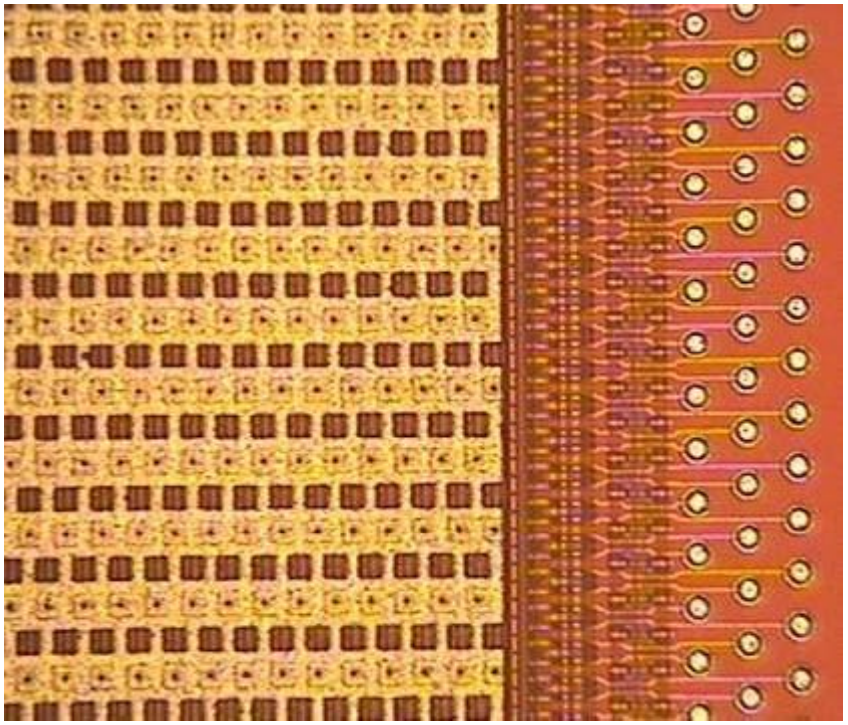
"Classic CCD"
Readout time ≈ $N \times M / f_{out}$

Column Parallel CCD
Readout time = N / f_{out}

High Speed CPCCD



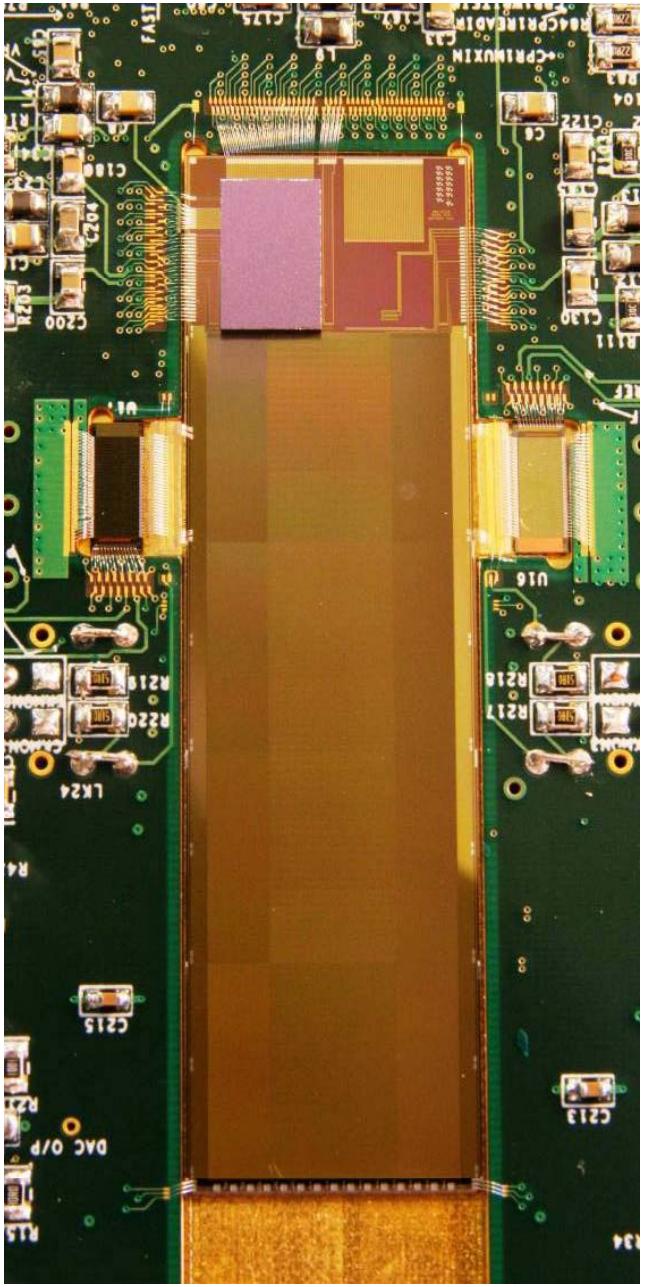
Busline-free CPC2



- High speed devices with 2-level metal clock distribution
  - Whole image area serves as a distributed busline
- Designed to reach 50 MHz operation

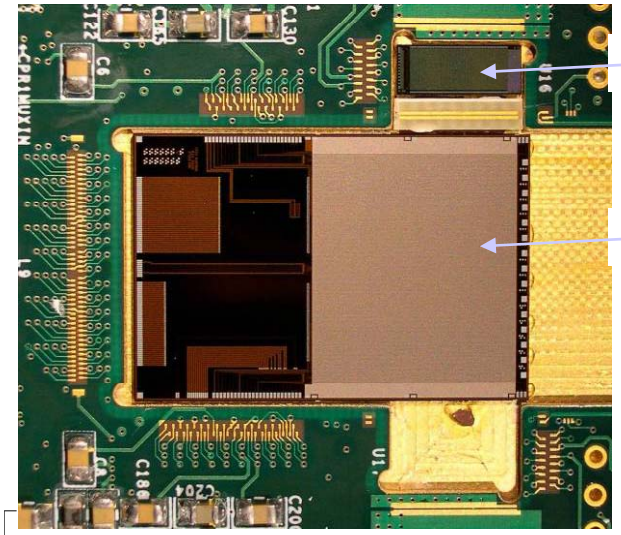
Tests of CPC2

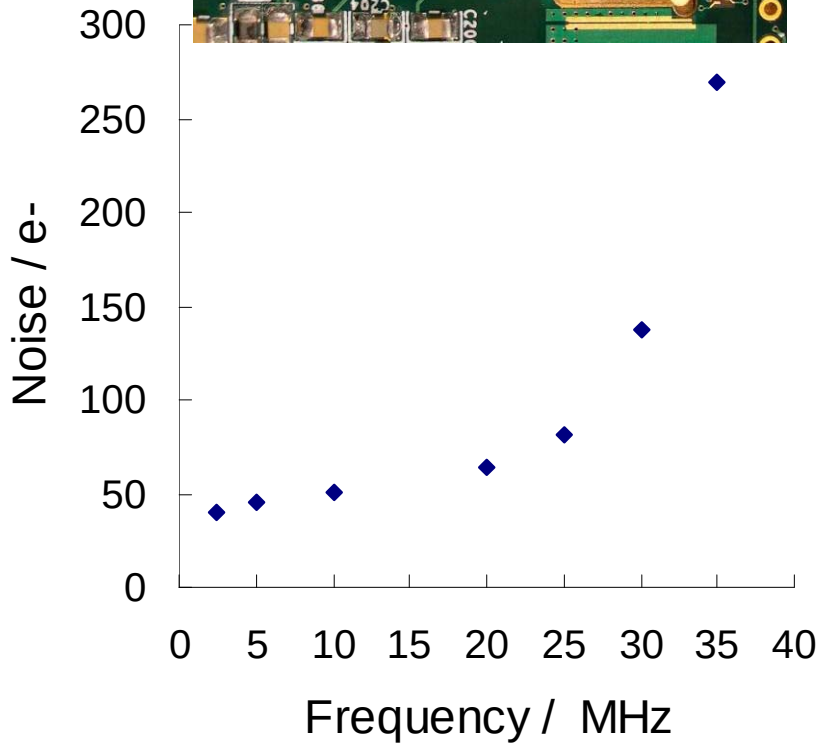
- Bump-bonded CPC2/CPR2 driven by two CPD1 clock driver chips
  - CPR2 – readout ASIC
- Works up to 9 MHz



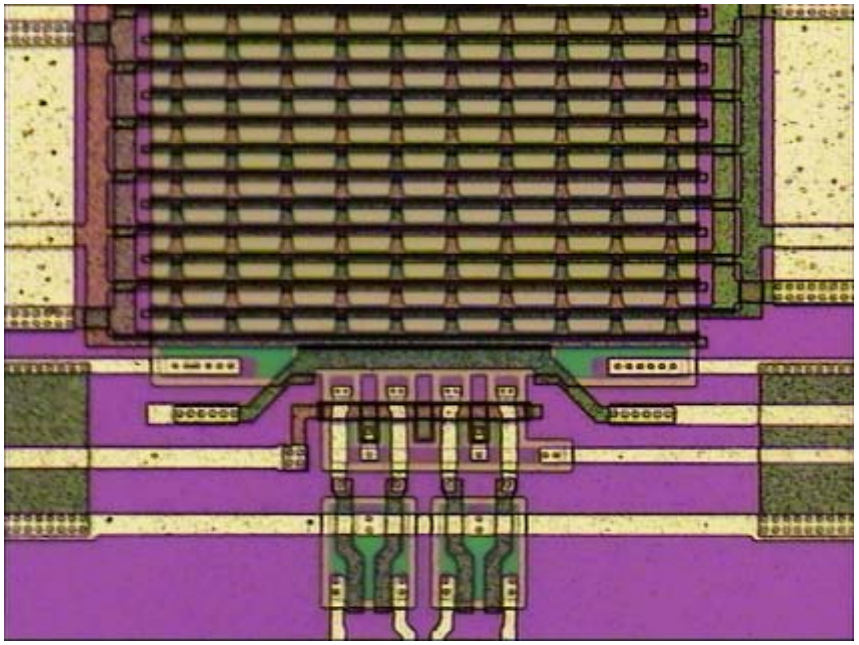
Maximum Frequency

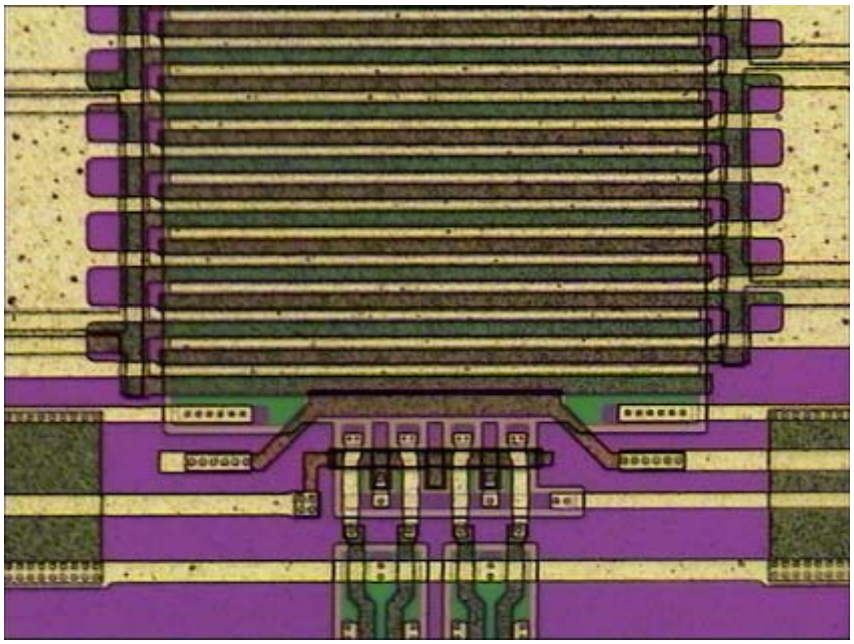
- Low noise operation up to 30 MHz for CPC2-10
  - 50 MHz within reach
  - Limited by substrate bounce effects
- Operated at up to 45 MHz





Low Capacitance CPCCDs

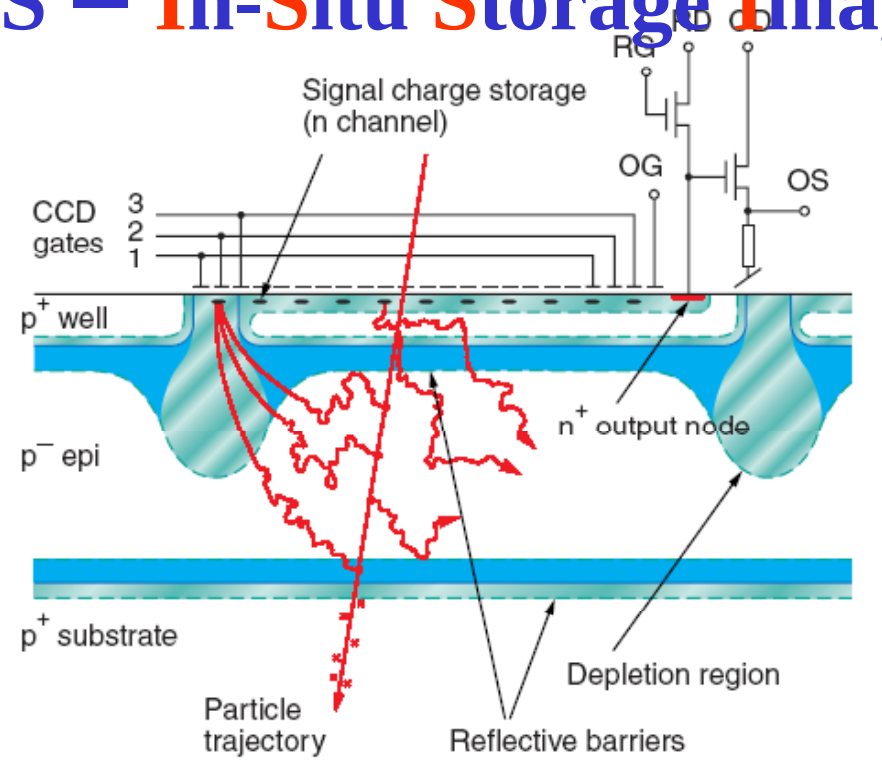




- Small CPCCD to test several ideas to reduce the capacitance and required clock voltage
- Under test

Raw Charge Storage Pixels: ISIS

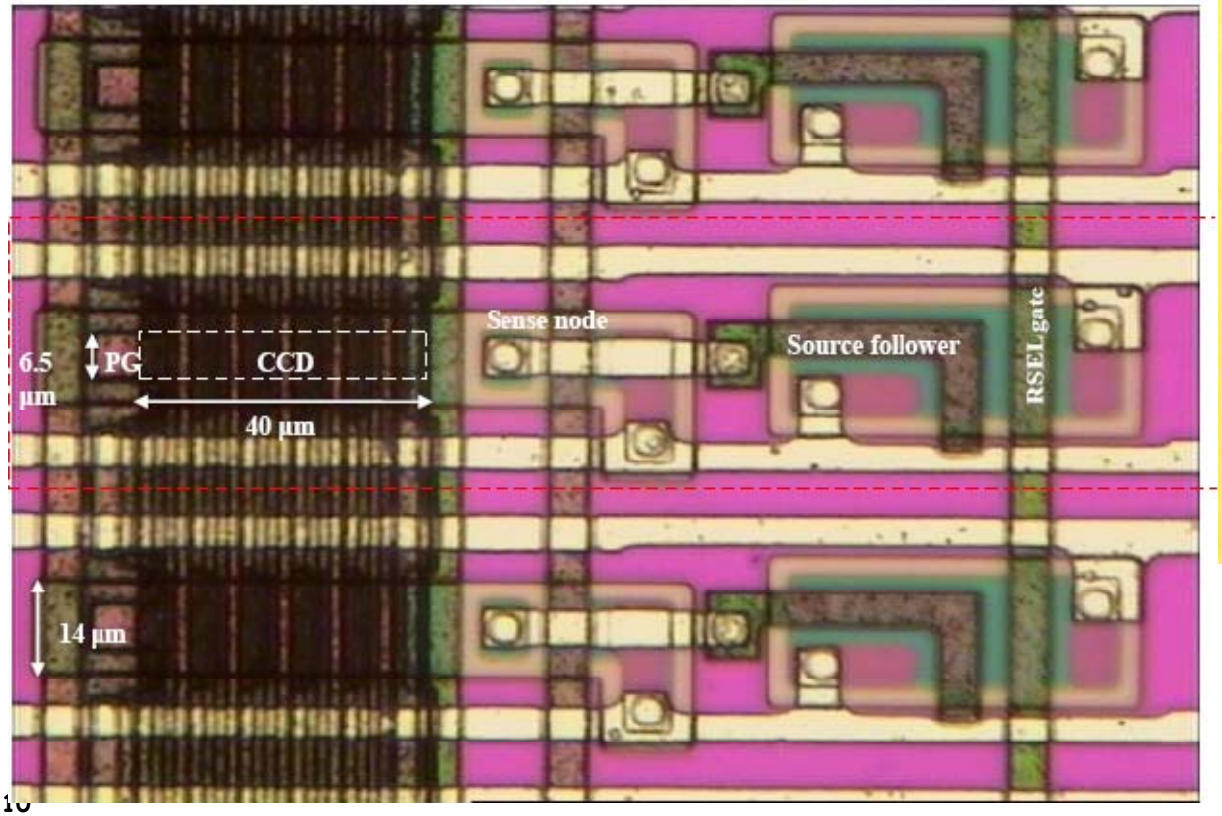
ISIS – In-Situ Storage Image Sensor

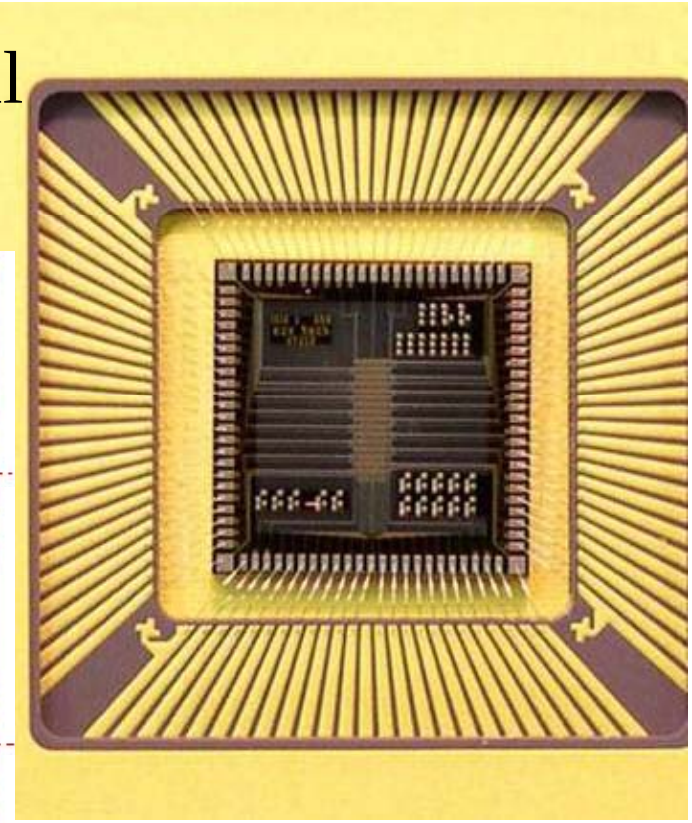


- Each pixel has internal memory implemented as CCD register
  - Charge collected under a photogate
  - Charge is transferred to 20-pixel storage CCD in situ
  - Conversion to voltage and readout in the 200 ms-long quiet period after collisions
- Visible light imagers based on the ISIS principle are available off-the-shelf (ex. DALSA, 100 MHz camera with 16 storage cells)

The ISIS1

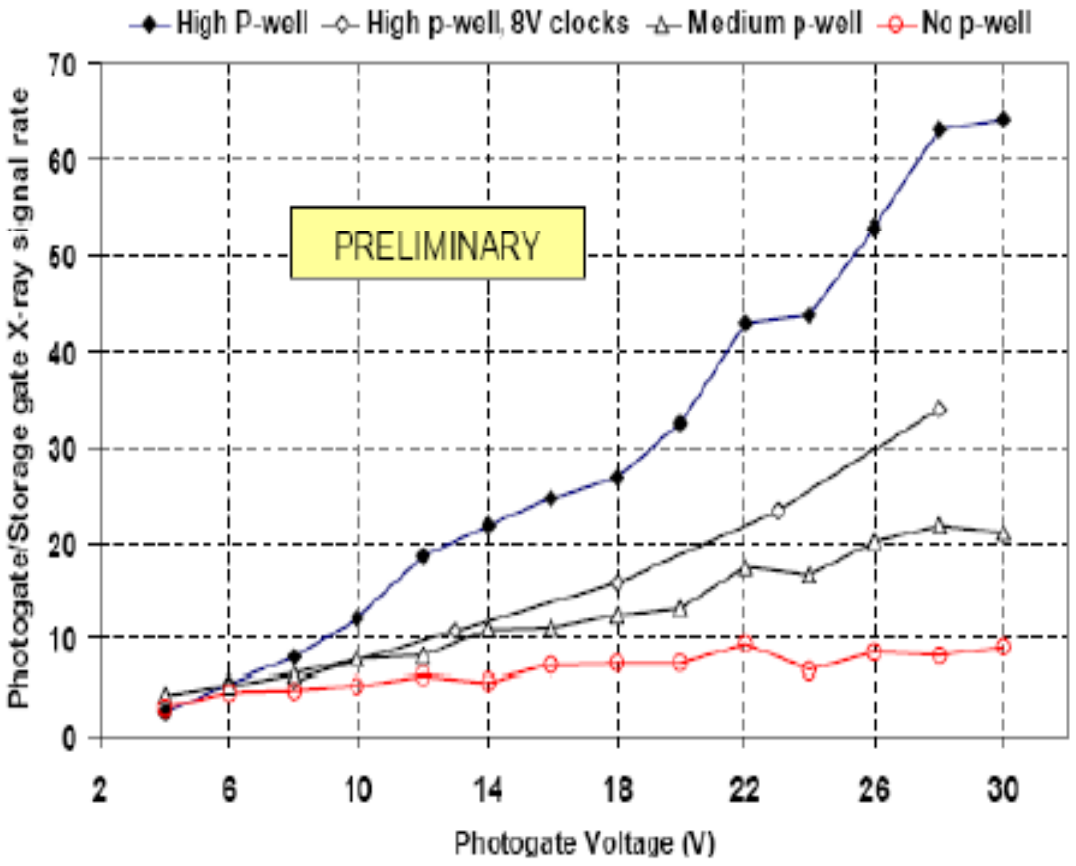
- 16x16 pixels, each 40x160 μm^2
- Five storage cells for pixel
- Two variants : with and without p-well
- Produced by e2V in UK





ISIS1 with p-well

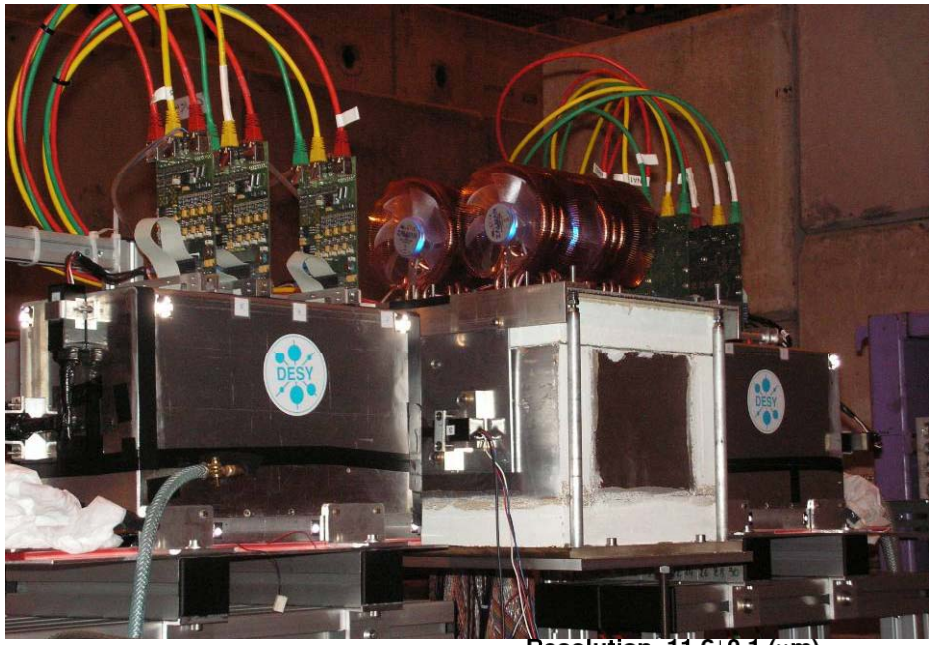
- High p-well doping protect storage register
- Look at ratio R of charge collected at photogate to charge collected at storage pixel
  - From ^{55}Fe (1640 e-)

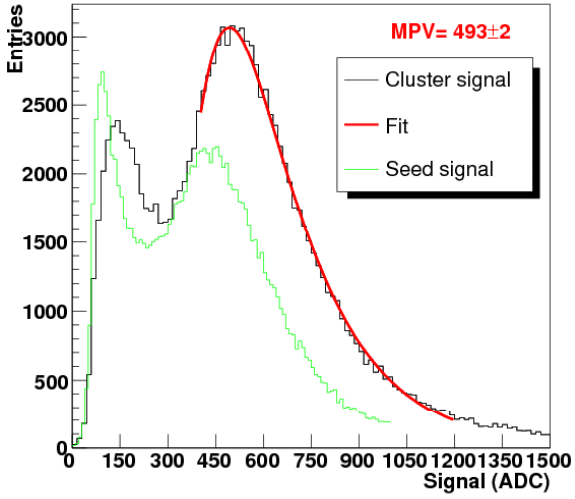


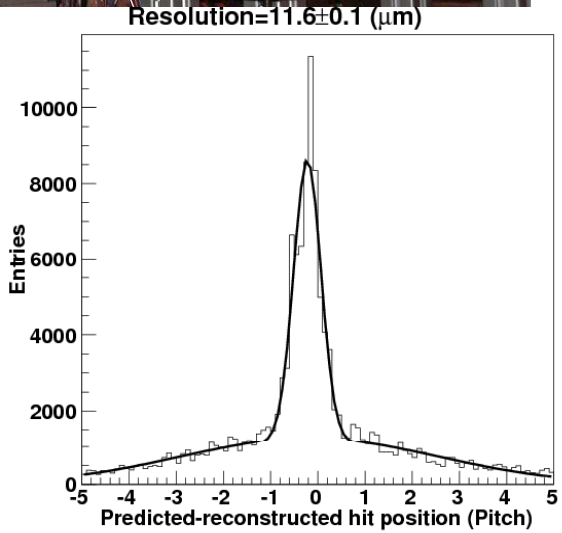
- Demonstrated that p+ well protection works

ISIS1 Testbeams

- Active area 0.56 x 2.22 mm^2
  - Accurate alignment required
- Tests performed at DESY and CERN in 2007 and 2008
- Limited efficiency due to large cell dimensions as expected
- Resolution 12 micron



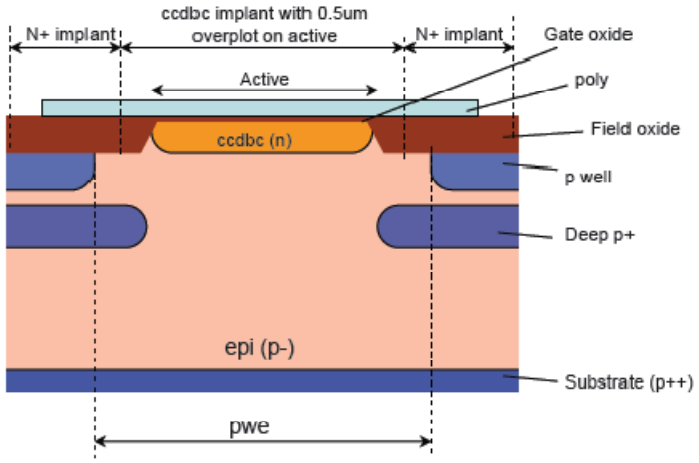


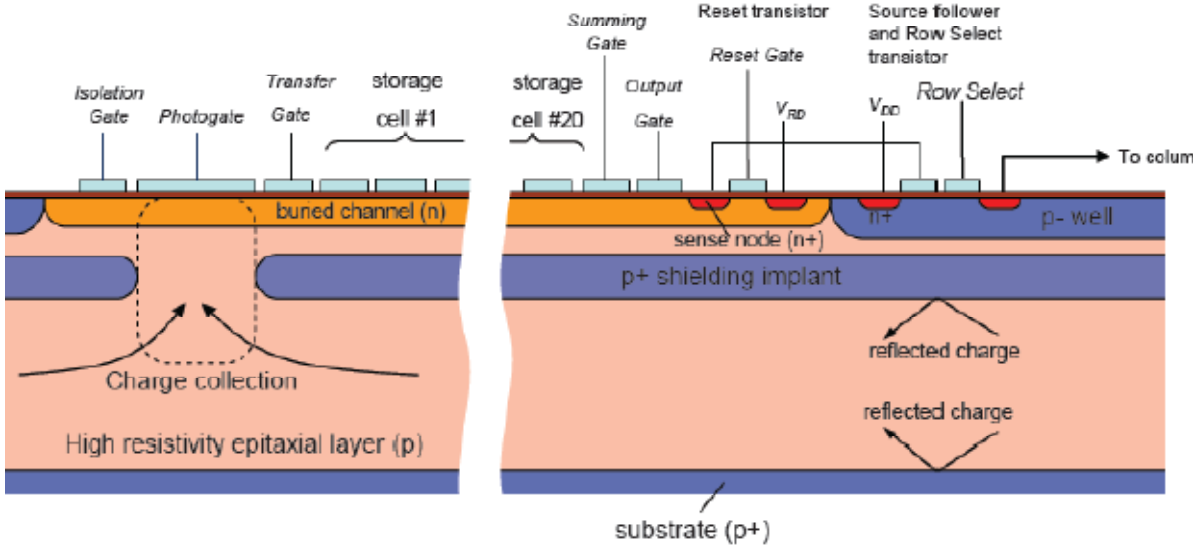


Next generation ISIS: ISIS2

- ISIS2 manufactured by Jazz Semiconductor

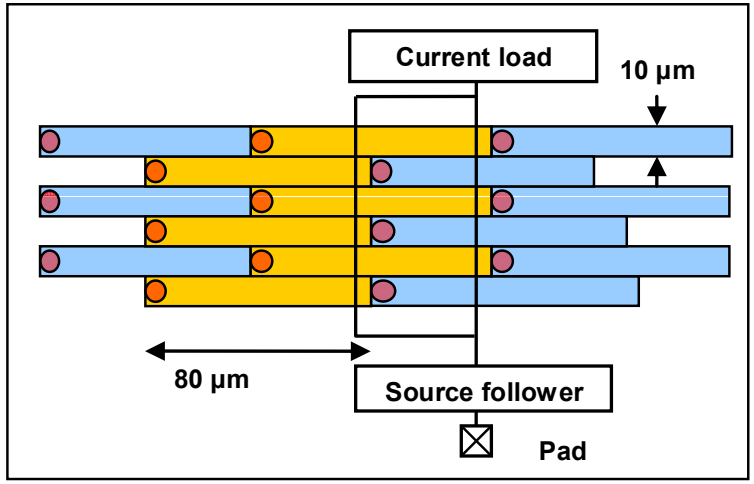
- Process: 0.18 μm with dual gate oxide
  - p++ wafers with 25 μm epi layer ρ > 100 Ohm cm
- Process enhancement for LCFI: buried channel and deep p+ implant
  - Buried channel is necessary for raw charge storage
  - Deep p+ protects buried channel from parasitic charge collection
- Cross sections :

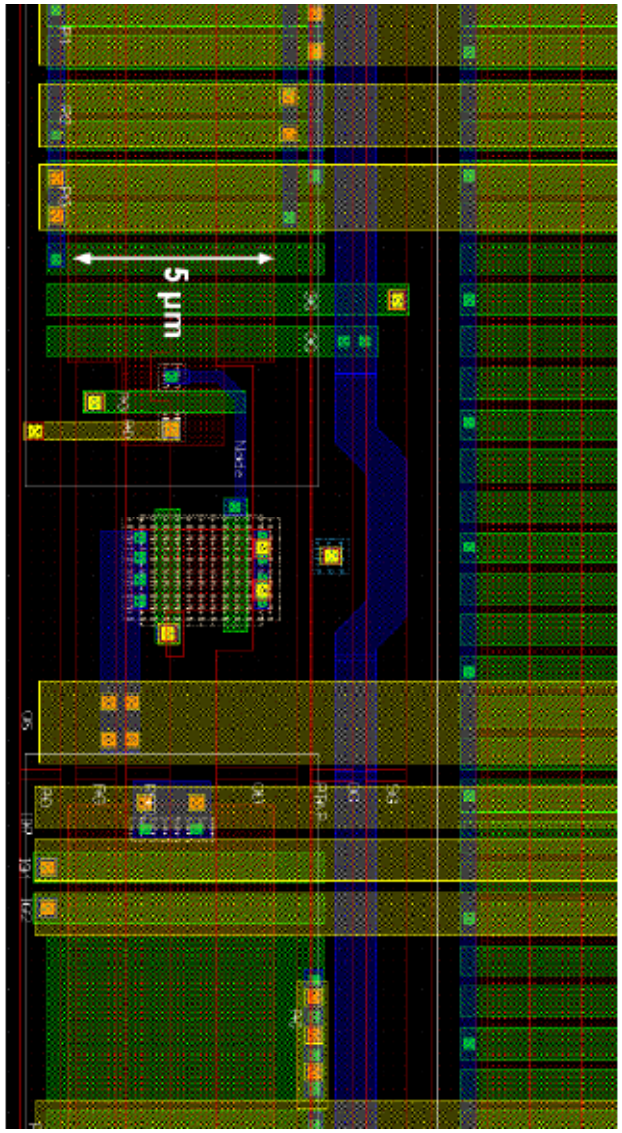




ISIS2 Design (1)

- Pixels 80 x 10 μm^2
- Imaging pixels 40 x 20 μm^2
- Buried channel 5 µm wide
- CCD gates: doped polysilicon, non-overlapping
- Logic, source followers use 5V custom logic gates, 3 metal layers

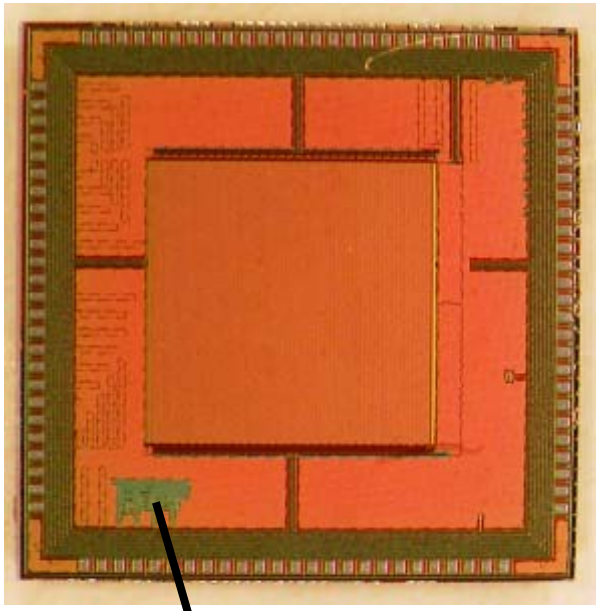


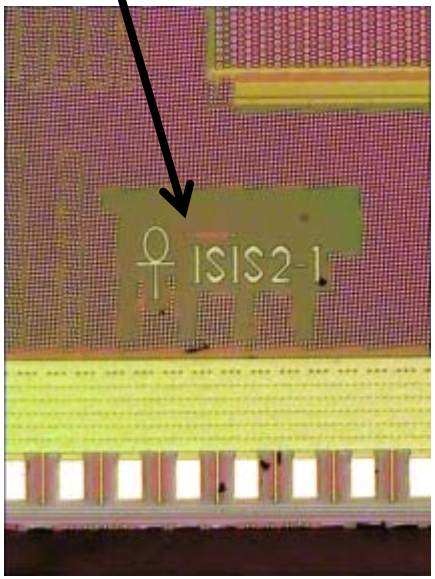


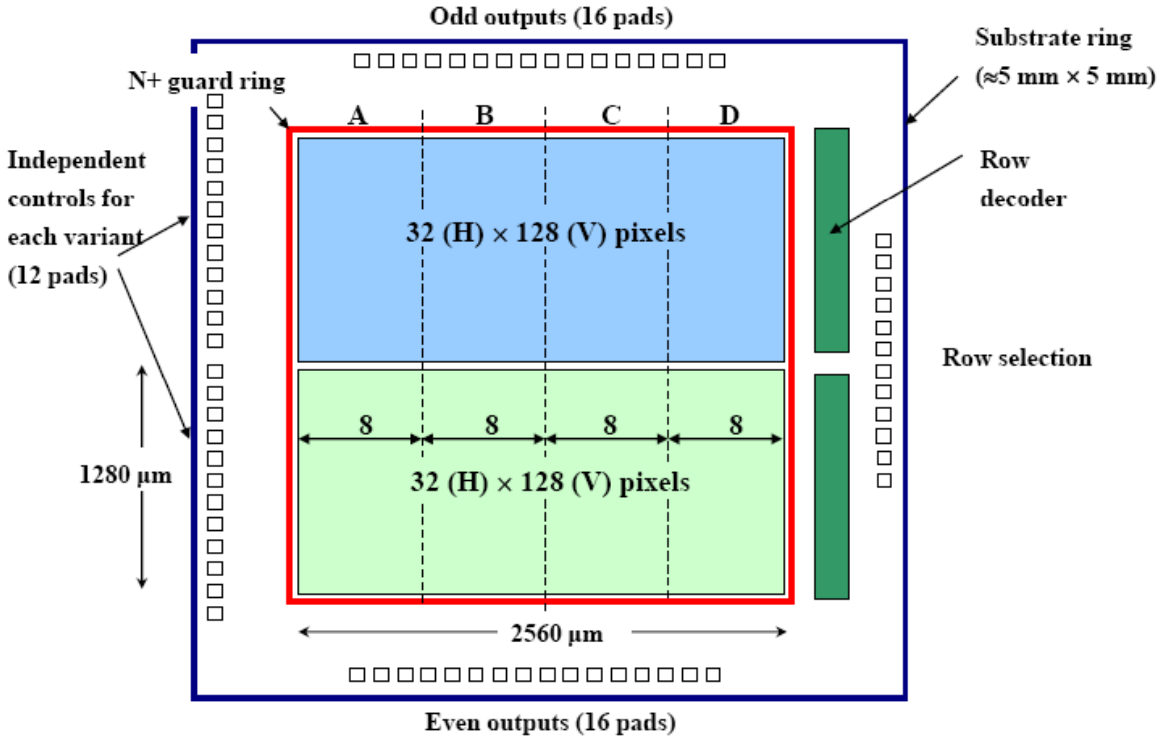
ISIS2 Design (2)

- One chip will have several variants of ISIS2
  - Each has independent control
- Row select and decoder edge logic
- Area 1 cm^2 (four 5x5 mm^2 tiles)

- Submitted in May 2008, delivered in November 2008, tests started







Summary

- CPCCD concept demonstrated
  - Operation at 45 MHz, low noise operation at 30 MHz
  - Operation with readout chip CPR2 at 9 MHz
- Raw charge storage concept demonstrated
  - Proof of concept ISIS1 tested in beam
  - Started testing of ISIS2 based on 0.18 um CMOS process
- Future : New proposal SPIDER (Silicon Pixel DEtector R&D)
  - Continue the ISIS program