Status and perspectives of Deep N-Well 130 nm CMOS MAPS

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for the SLIM5, VIPIX and P-ILC Italian collaborations

CMOS MAPS R&D in Italy so far

- 130nm Deep NWell MAPS design for SuperB
  - → the APSEL series chips with sparsified readout and time stamping
  - → Funding by INFN (SLIM5) and Italian Ministry of University and Research (PRIN)

- 130nm DNW CMOS MAPS for the ILC Vertex Detector
  - → smaller pitch and power dissipation, different readout architecture
  - → funding by INFN (ILC collaboration)

- 180nm and 130nm bulk CMOS MAPS
  - → Various readout architectures, small pixels
  - → funding by INFN (Perugia and Roma3 groups)

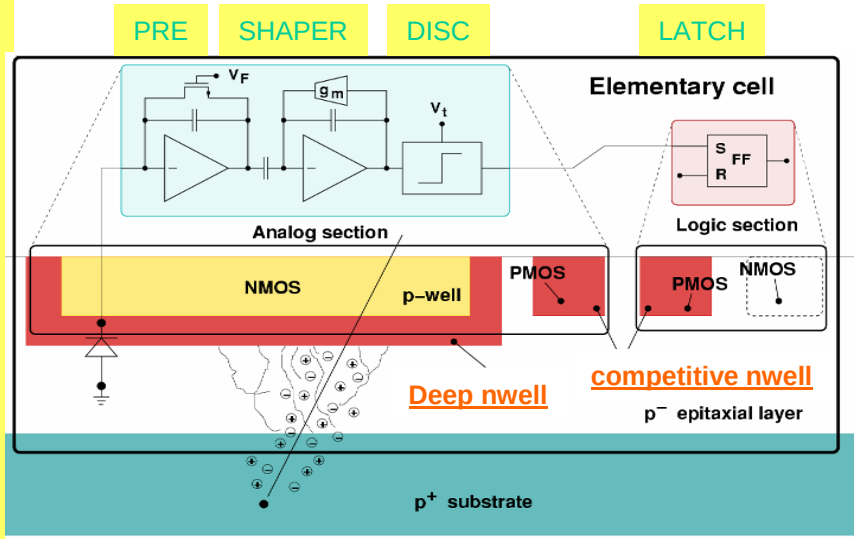
Deep NWell 130nm CMOS MAPS

- Rad-hard MAPS with data sparsification and high rate capability (self-triggering pixel design, in-pixel comparator, in-pixel time stamping and sparsification logic)
  - Deep N-Well (DNW) as collecting electrode
  - Classical pixel analog processing with charge-sensitive preamplifier

    Gain independent of the sensor capacitance collecting electrode can be extended and include NMOS of the analog section

  - Area of the "competitive" nwells housing PMOSFETs inside the pixel kept to a minimum. Fill factor = DNW/total n-well area ~90% in the prototype test structures
- **Pros:** With 100-nm scale CMOS, integration of advanced analog and digital functions at the pixel level (as in hybrid pixels), rad-hard electronics
- **Cons:** possible limitations in pixel pitch (go to more scaled CMOS, but higher cost, only binary readout) and detection efficiency (pixel layout critical, deep P-well option?)

SLIM5, ILC – INFN & Italian Universities

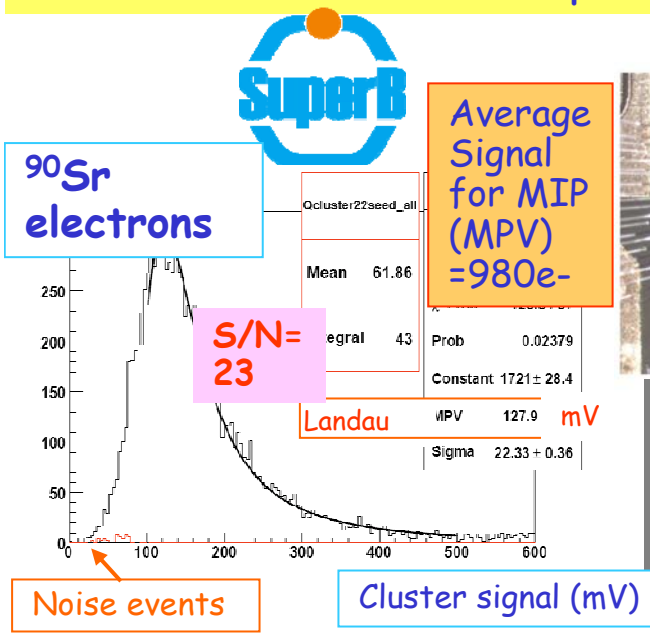


- 2004-2006: Proof of principle achieved with the first prototypes in a 130 nm triple well CMOS process
- 2007-2009: Full size MAPS sensors and detector modules, beam tests

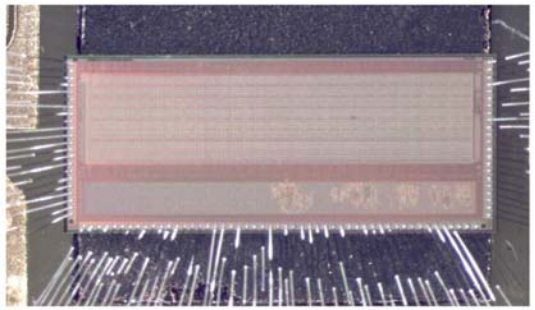
Experimental results and plans

•Performed successful tests of a **first generation of Deep N-Well CMOS MAPS with in-pixel sparsification and time stamping**.

•**Sensors with different sparsified readout architectures and pixel pitches** are being optimized for operation at a **Super B-Factory** (large background, equivalent to a continuous beam operation) and at **ILC** (intertrain readout).



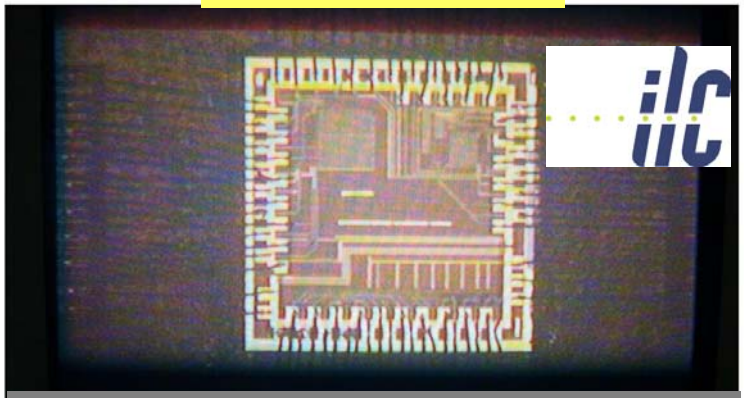
APSEL4D



32x128 matrix.
Data Driven, continuously operating sparsified readout
Beam test Sep. 2008

50x50 um pitch

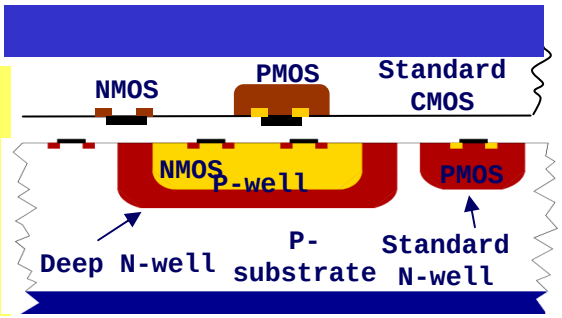
SDR0



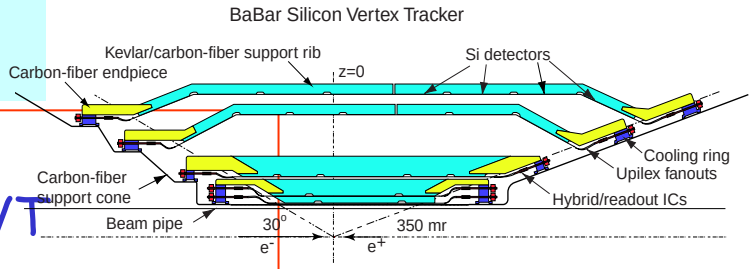
16x16 matrix, Intertrain sparsified readout

25x25 um pitch

•**DNW MAPS are evolving towards vertical integration.**
A design with a 2 tier structure (sensor&analog tier + digital tier) is pursued to improve performance (smaller pitch, higher efficiency, increased pixel functionalities)



SuperB Layer 0 Options

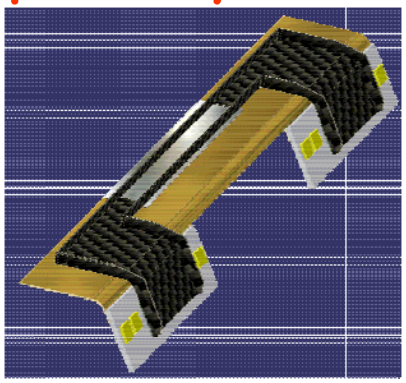


- The BaBar SVT technology is adequate for R > 3cm: use design similar to BaBar SVT
- For SuperB Layer0, R = 1.5 cm
- Layer0 is subject to large background and needs to be extremely thin: > 5MHz/cm^2, 1MRad/yr, < 0.5%X0

The beam test was focused on two options for the SuperB Layer0:

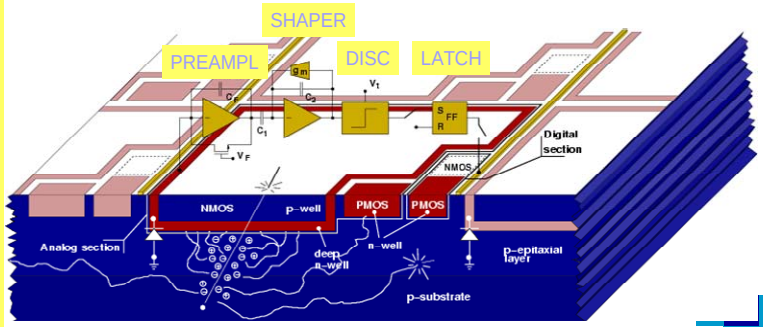
Striplets option: mature technology, not so robust against background.

- Marginal with background rate higher than ~ 5 MHz/cm^2
- Moderate R&D needed on module interconnection/mechanics/FE chip (FSSR2)

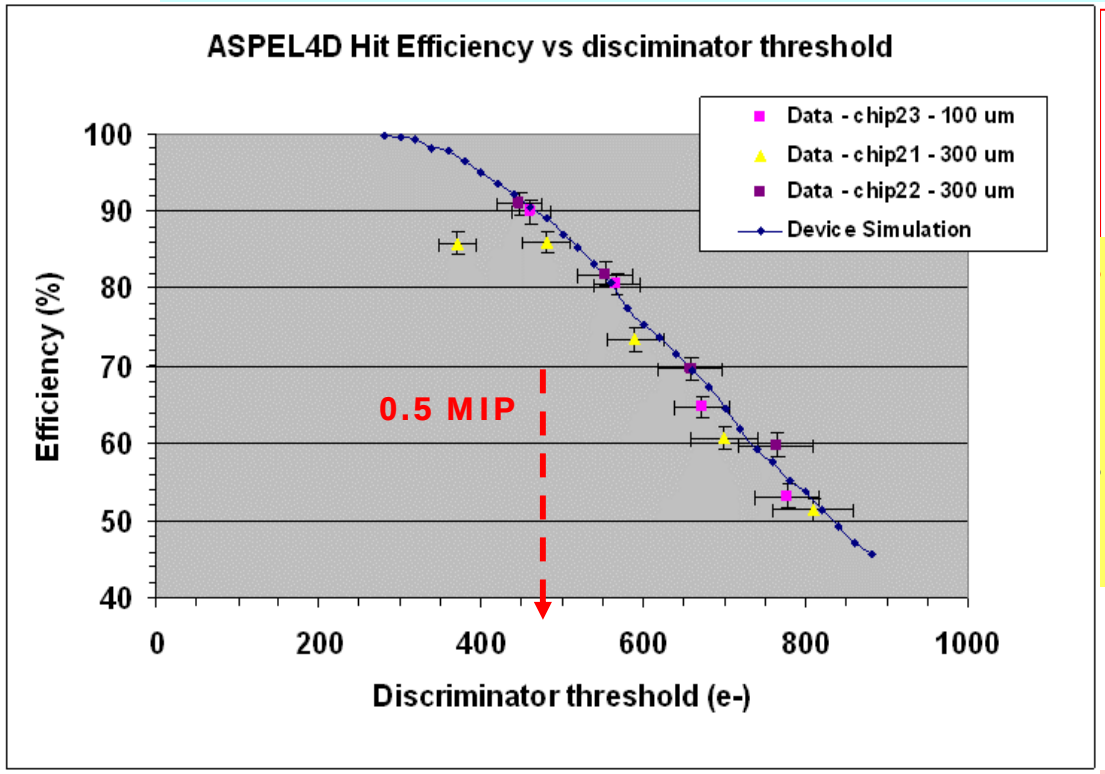


CMOS MAPS option

- new & challenging technology:
- can provide the required thickness
- existing devices are too slow
- Extensive R&D ongoing (SLIM5-Collaboration) on 3-well devices 50x50um^2



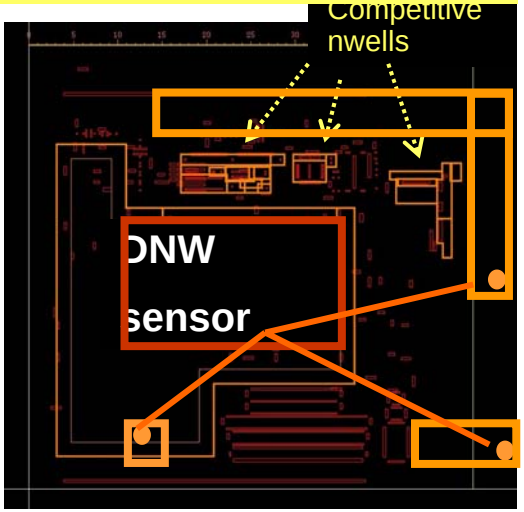
DNW MAPS Hit Efficiency measured in a beam test (APSEL4D)



Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

MAPS hit efficiency up to 90 % with threshold @ 450 e- (~ 4σ_noise+2σ_thr_disp)

300 and 100 μm thick chips give similar results

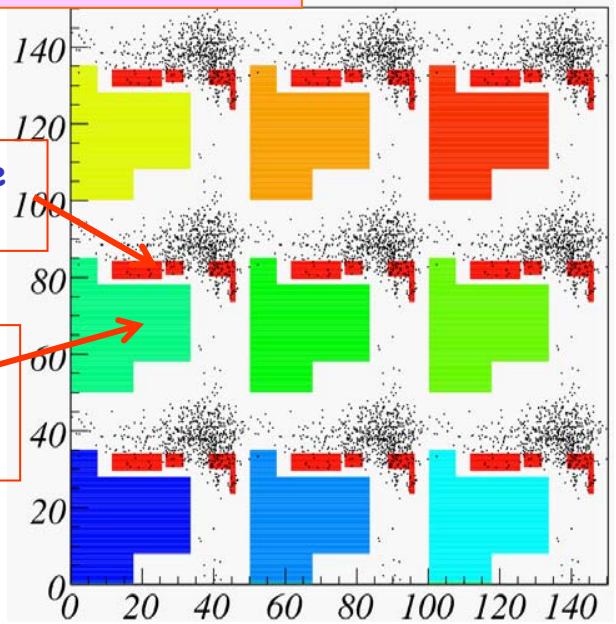


- Competitive N-wells (PMOS) in pixel cell can steal charge reducing the hit efficiency
  - Fill factor DNW/total N-well area ~ 90 % in present design
- Room for improvements with a different design of the sensor (multiple collecting electrodes around competitive N-wells)

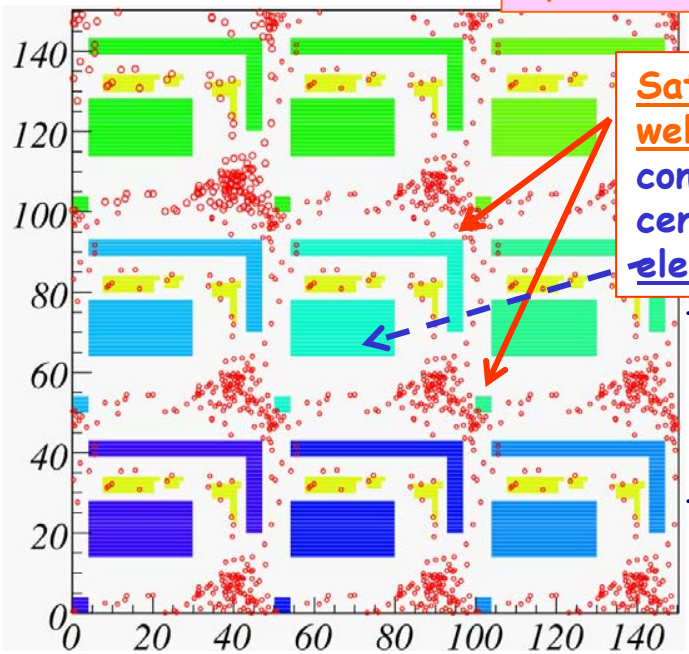
Detection efficiency and charge collection

- Beam test results of APSEL4D show a ~90% efficiency, which agrees very well with TCAD simulations
- With APSEL4D sensor geometry (left), Efficiency ~ 93.5% from simulation (pixel threshold @ 250 e- = 5xNoise)
- Inefficient regions shown with dots (pixel signal < 250 e-)
- Optimized cell with satellite N-wells (right) Efficiency ~ 99.5%

3x3 MATRIX
T sensor geometry



3x3 MATRIX
optimized sensor



- Locate low efficiency region inside pixel cell
- Add ad hoc "satellite" collecting electrodes

The way forward

- Next generation of DNW MAPS has to provide devices that approach actual experiment specifications more closely

  Several issues have to be addressed to meet ILC Vertex Detector specifications (pixel pitch, detection efficiency):

  - Binary readout: ILC VTX demands a **pixel pitch** < 20 μm to achieve required single point resolution < 5 μm.
  - **Detection efficiency** does not meet requirements (> 99 %) because of competitive n-wells (PMOS) decreasing the fill factor
  - Capability of **handling multiple pixel hits** has to be included without degrading efficiency and pitch

- Two different ways to approach this goal:

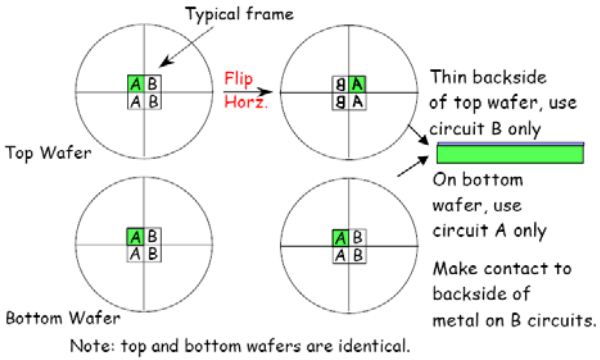
1) **A gradual performance improvement**
   ⇒ better sensor layout, optimize interconnections and pixel cell
   ⇒ SuperB Layer0 test module
2) **A technology leap**
   ⇒ Vertical integration

3D vertical integration and DNW MAPS

Use vertical integration technology to interconnect two 130nm CMOS layers

Overcome limitations typically associated to "conventional" and DNW CMOS MAPS:

- Reduced pixel pitch
- 100 % fill factor (few or no PMOS in the sensor layer, no competitive N-wells)
- Better S/N vs power dissipation (smaller sensor capacitance)
- Increased pixel functionalities

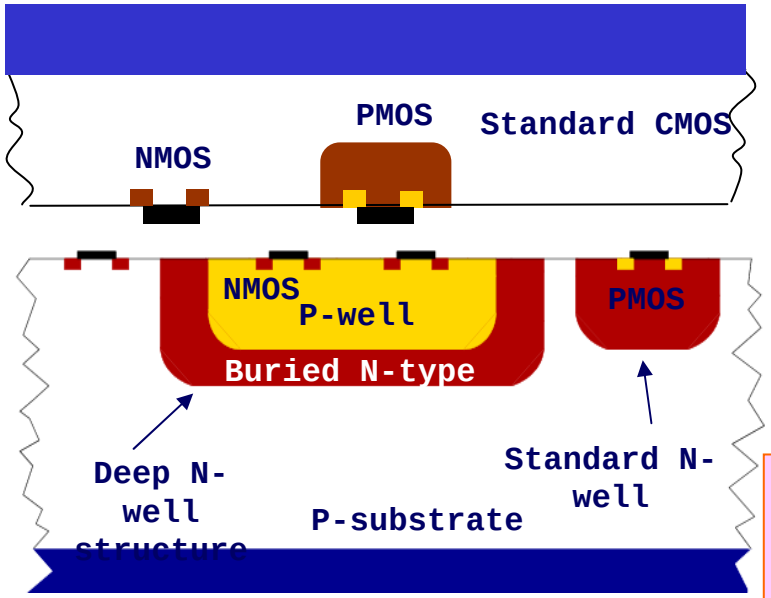


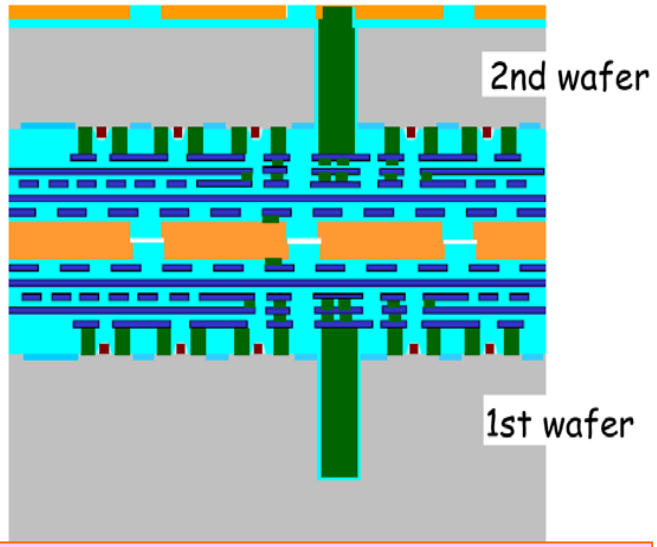
Face to Face Bonding

Mostly digital CMOS tier

Tier interconnection and vias

Analog and sensor CMOS (mostly NMOS) tier





Tezzaron/Chartered technology (Fermilab MPW run)

The Italian VIPIX collaboration

- "Pixel systems for thin charged particle trackers based on vertical integration technologies" - VIPIX (INFN Pisa, Pavia, Bologna, Trieste, Trento, Perugia, Roma3, Torino)

- Members of the CMOS-3DIT Consortium (FNAL-IN2P3-INFN)

1. **Interconnection between 2 (or more) CMOS layers**,
   a) one layer with a MAPS (DNW) device and analog front-end, and the other layer(s) with the digital readout
   b) 2 layers with CMOS MAPS

2. **Interconnection between a CMOS readout electronics chip (2D or 3D) and a fully-depleted high resistivity sensor**
   a) with bump bonding (standard, but low pitch may be needed)
   b) with a vertical integration technique (low material budget, more advanced)

Conclusions

- After several years of R&D, Deep N-Well monolithic active pixel sensors are reaching a good maturity level, but there is room for substantial improvements

- The performance of DNW MAPS needs to be upgraded if they have to fulfill specifications of experiments at ILC or SuperB

- DNW MAPS can benefit from technological advances such as vertical integration