Activities related to monolithic and vertically integrated pixel detector at CERN

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Outline

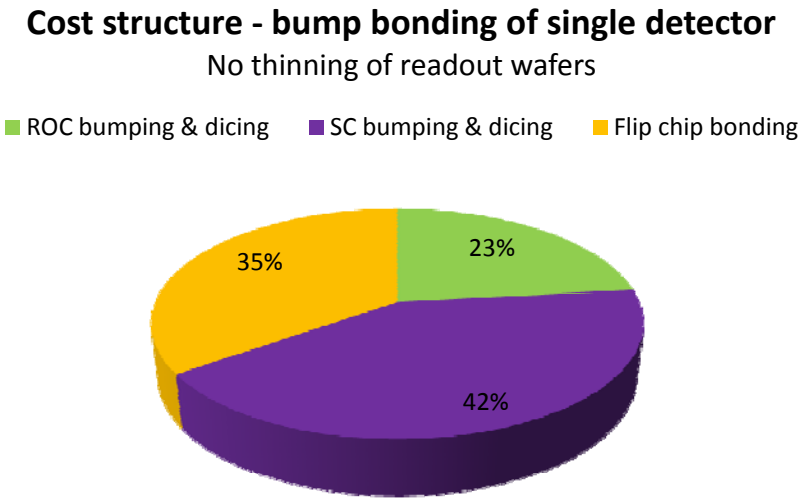
- Low cost bump bonding
- CERN MPW service
- 3D activities in or around Medipix
- A new approach to monolithic active pixel design
- Summary

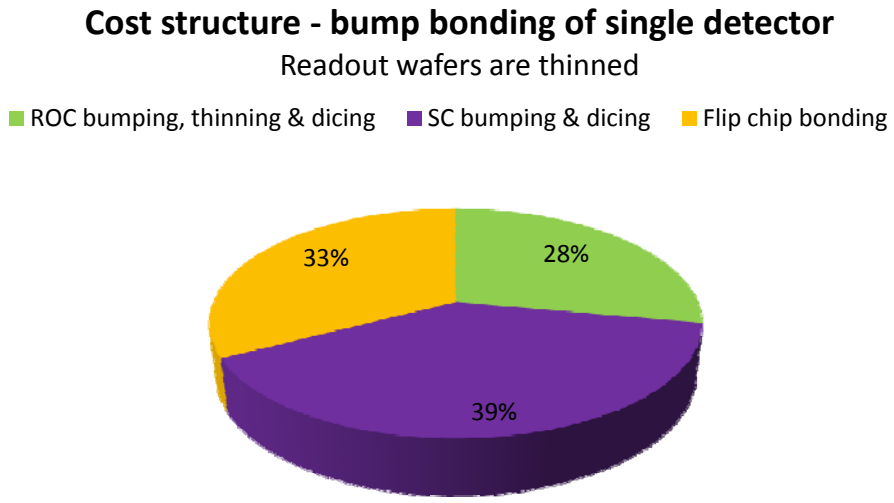
Low cost bump bonding

- Solder bump bonding costs approx € 200 per assembly at present
- This dominates the cost of hybrid pixel systems and has limited their reach at LHC vertex detectors
- A cost analysis has been carried out and potentially interesting new approaches identified

Cost distribution of bump and flip-chip bonding

- Here's an estimation how the costs have been shared between readout chip (ROC) bumping, sensor chip (SC) bumping and flip chip bonding.
- Readout chips are cheapest because they are typically single chips on big (8") wafers → many good chips from each bumped wafer.
- Sensor bumping is the dominating cost-issue at the moment. Use of ladder shaped sensor chips (e.g. multiple ROC's placed on single sensor unit) makes the situation even worse due to higher material loss (bumping yield).





Sami Vaehaenen

Cost reduction

- The goal of the project is to significantly reduce the share of the bump bonding of the total detector building cost. There are 2 solutions available:
  - Move the detector assembly into real production facilities and modification of existing bumping processes.
  - Creation of new bumping process with less work (batch process).
- Present day systems use ladder assemblies consisting of 4-16 chips per ladder.
- Cost analysis indicates the single chip assemblies are much more cost effective

Under Bump metalisation

- ENIG - Electroless (chemical) deposition of nickel and gold – promises low cost bump (or UBM) deposition
- Advantage
  - Price
  - Mask free process
- Challenges
  - Compatibility with module wire bonding
  - Pin hole free passivation required
  - Pitch

Solder deposition

Pitch (μm)	<30	50	100	>=150
Possible Approaches (ordered by cost, lowest first)	Photoresist lift-off + evaporation sputtering of metals (indium) (no low cost process exists)	Electroplating C4NP?	Electroplating C4NP Stencil printing	Electroplating C4NP Stencil printing

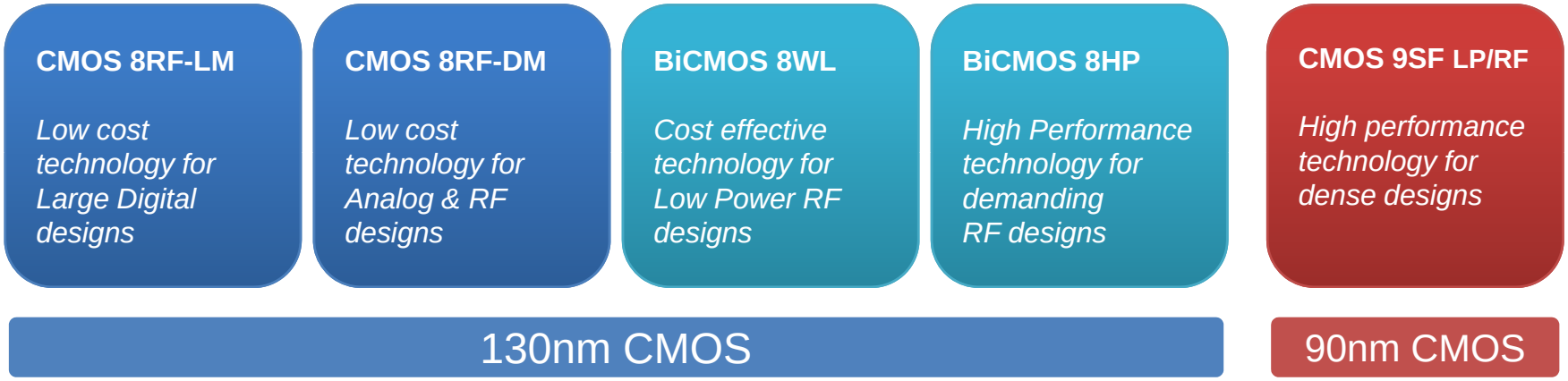
Flip chip bonding

- Solder bump flip chip
  - Most reliable technology, good electrical conductivity between chips, elastic solder bumps relax stresses between the chips.
- Anisotropic conductive films (ACF)
  - Film material which include conductive particles (< 15 vol-%). Particles create a conductive path in Z direction once compressed between elevated pads.
  - Suitable film providers: Sony and Btech (aligned Ni fibres)
- Anisotropic conductive adhesives (ACA)
  - Same as AFC, except in paste form. Requires stencil printing.
- Isotropic conductive adhesives (ICA)
  - Contain typically silver flakes in polymer matrix 30-80 Vol-%. Shrinks during curing and creates conductive polymer “bumps”. Requires stencil printing.
- Z-bond using Anisotropic conductive adhesives (ACA)
  - Magnetically aligned Ni/Au particles during curing, special ACA’s needed.

Low cost bumping summary

- Cost analysis indicates saving if single chip assemblies used
- ENIG is a maskless bumping process which might be usable for UBM (and solder deposition)
- Select solder deposition process according to pitch
- New solutions to flip chip exist but may not be appropriate for the finest pitches

CERN MPW Services
Overview of Technologies



- 130 (CMOS and BiCMOS) and 90 nm contract available since 6/2007.
- Future technologies can be negotiated with the same manufacturer, once the necessity arise.

CMOS8RF Technology Features

Standard Features

- **130 nm lithography, twin-well on 1-2 Ω-cm non-epi P- substrate, low K dielectric**
- **Thin Oxide (22Å gate) FETs (1.2 /1.5V)**
- **Thin Oxide MOS Varactors**
- **Forward bias diodes**
- **N-well resistor**
- **5 to 8 levels of metal**
  - Thin and thick Cu metal (~0.3/0.55 μm)
  - Last metal options:
    LM: Cu 0.55μm DM: 3 μm Cu + 4 μm Al
- **Vertical Natural Capacitor**
- **Spiral inductors, RF Transmission lines**
  - Series & Symmetrical inductors in DM wiring option only
- **Electrically programmable fuses**
- **Wire bond or solder bump (C4) terminals**

Optional Features

- **Triple-well NFETs**
- **Thin Oxide Low power FETS**
- **Thin Oxide Low-Vt FETs**
- **Thick Oxide (52Å) 2.5V FETS**
- **Thick Oxide (52Å) 3.3V FETS**
- **Thin and thick Oxide Zero-Vt NFETs**
- **Thick Oxide MOS Varactors**
- **Hyperabrupt Varactor**
- **Polysilicon and diffused resistors**
- **TaN metal resistor**
- **Single and dual-layer MIM capacitor (DM option only)**

Access to Technology Data

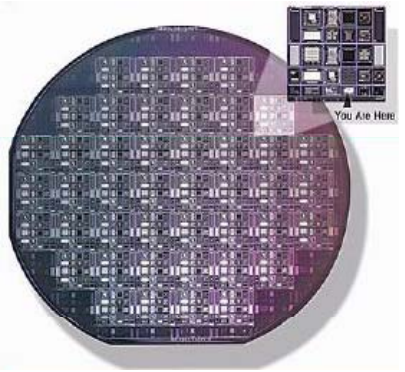
- What you need to start designing.

- Distributed by CERN

Technology	Process	Distributable
CMOS8RF-LM	130nm	IBM PDK, Digital Kit
CMOS8RF-DM	130nm	IBM PDK
BiCMOS8WL	130nm (SiGe)	IBM PDK
BiCMOS8HP	130nm (SiGe)	IBM PDK
CMOS9SF	90nm	IBM PDK

- IBM PDK : Physical Design Kit for Analog and full custom design.
- Digital Kit : Design Kit that supports Digital design.

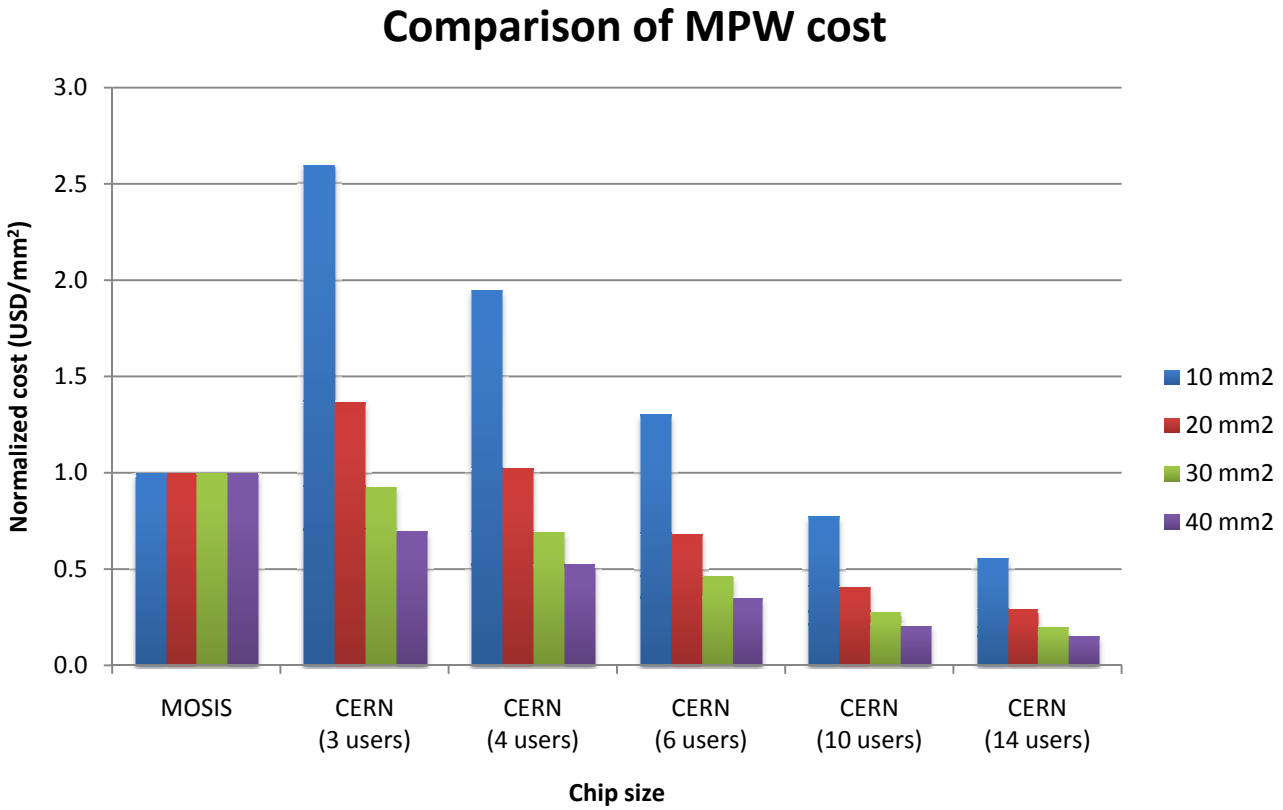
Access to Foundry Services



- Technologies:
  - IBM CMOS6SF (0.25µm), legacy designs
  - IBM CMOS8RF (130nm), mainstream process
  - IBM CMOS8WL & 8HP (SiGe 130nm)
  - IBM CMOS9SF (90nm), option for high performance designs

- MPW services:
  - CERN offers to organize MPW runs to help in keeping low the cost of fabricating prototypes and of small-volume production by enabling multiple participants to share production overhead costs
  - CERN has developed working relationships with MPW provider MOSIS as an alternate means to access silicon for prototyping.

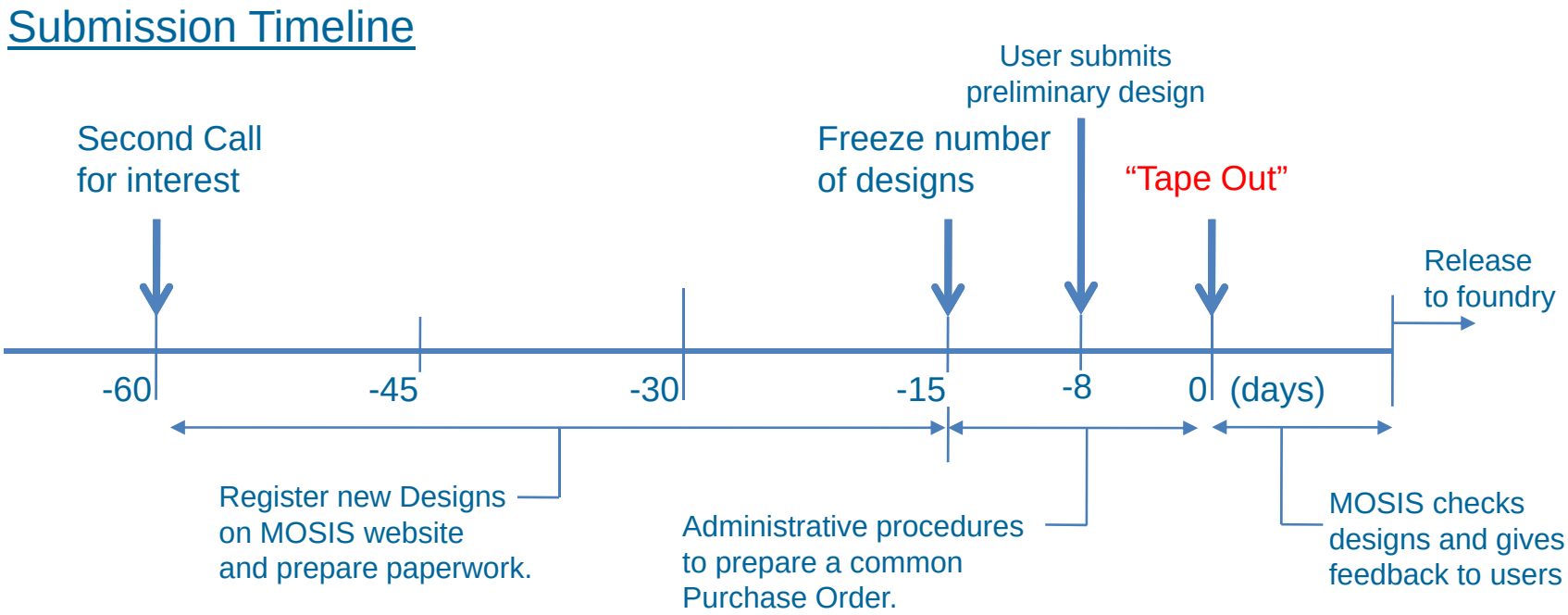
130nm MPW Pricing



- At present the level of demand is below threshold for CERN-organized MPW
  - Last MPW had 3 users sharing 20 mm^2 silicon area. (Submitted to MOSIS for fabrication.)

Fabricating through MOSIS

- Our alternate path for prototyping



- Turn Around Time: ~70 calendar days from release to foundry
- Number of prototypes: 40 pieces

Foundry Service Wrap-Up

- Centralized foundry services.
  - Provide access to advanced technologies by sharing expenses.
  - Provide standardized common design flows.
  - Provide access to shared tools and common IP blocks.
  - Organize common Training and Information sessions.

- Availability of foundry and technology services is modulated by user's demand.

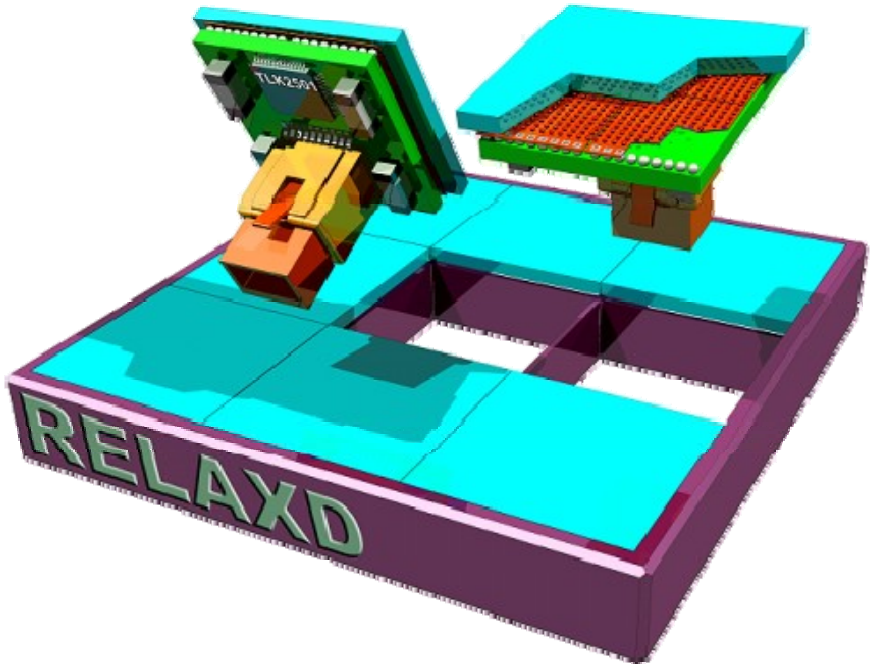
- Your feedback is welcomed. Please contact:
  - Organizational issues, contracts etc.:
    - Alessandro.Marchioro@cern.ch
  - Technology specific:
    - Kostas.Kloukinas@cern.ch
  - Access to design kits and installation:
    - Bert.van.Koningsved@cern.ch

Medpix2/3 Activities

- Timepix is a Medipix2-like chip with identical bump bond pitch and similar wire bonding layout
- However wire bonding pads have been designed for compatibility with back end TSV processing (full M1 pads)
- Wafers are available for prototyping with TSV’s

RelaxD Project

- Partners: PANalytical, Nikhef, IMEC, Canberra
- Aim to produce 4-side buttable quad assembly
- Uses Timepix wafers



RelaxD Project Status

- High speed serial R/O is almost done (Nikhef/PANalytical)
- 4-side buttable Si tile has been designed(IMEC)
- Important TSV processing issues have been addressed (IMEC)

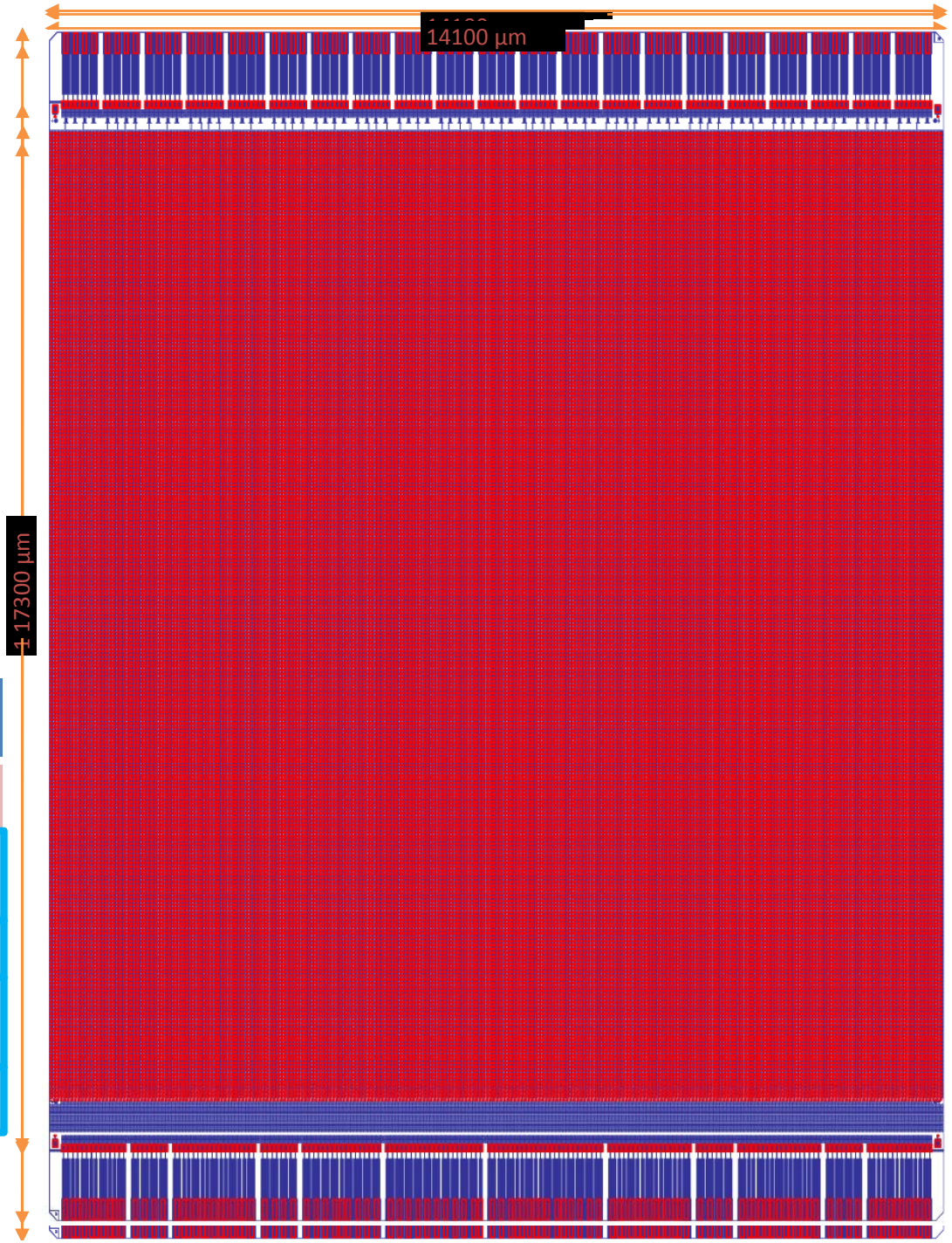
Medipix3

- Project aims at developing new readout chip providing simultaneously high spatial and energy resolution
- Uses 0.13μm CMOS
- A number of extra features have been incorporated including space for TSV landing pads and a novel dicing scheme

Mpix3 chip

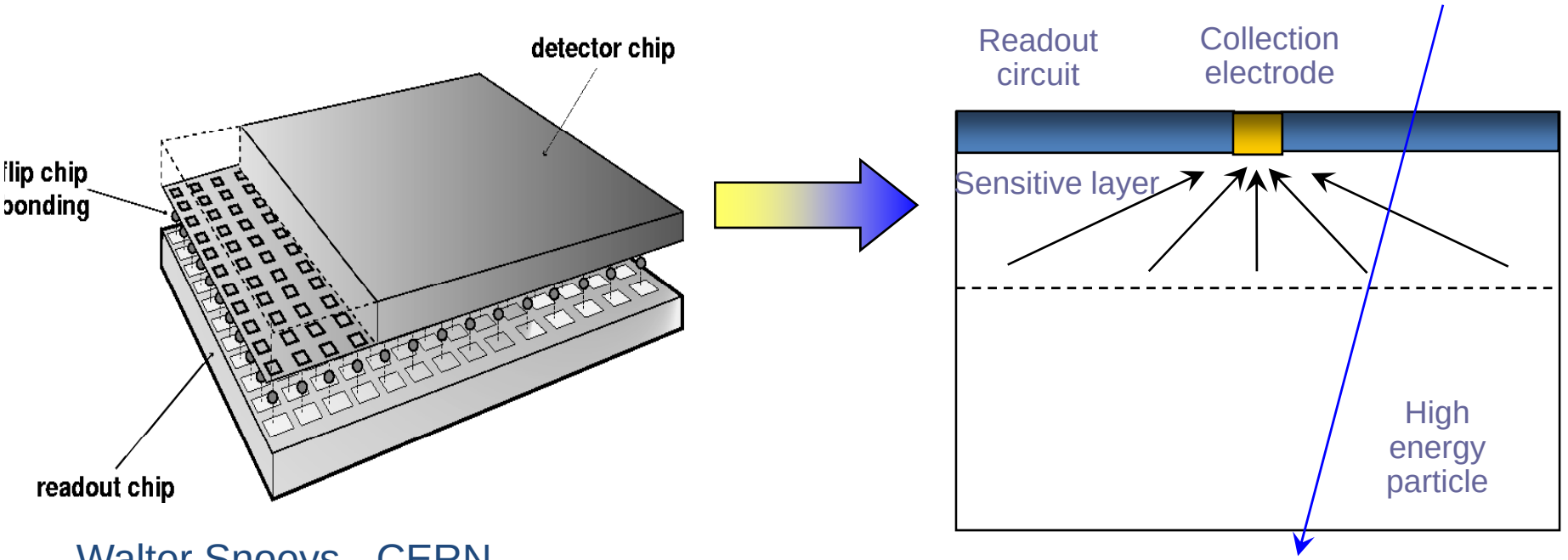
- Top Metal (MA) and passivation opening (DV) displayed
- Multiple dicing cuts depending on:
  - Top power connection
  - WB or TSV bonding

	X [µm]	Y [µm]	Active Area
Medipix2 and Timepix	14111	16120	87.1%
Medipix3 top and bottom WB	14100	17300	81.2%
Medipix3 bottom WB	14100	~15900	88.4%
Medipix3 top and bottom TVS	14100	~15300	91.9%
Medipix3 bottom TVS	14100	~14900	94.3%



A monolithic detector in standard very deep submicron CMOS technology

- Silicon detector development and its associated electronics are part of the R&D activities of the CERN PH department. This implies the study of advanced standard CMOS technologies (130 nm and beyond) .
- This R&D comprises the development of a monolithic detector integrating a matrix of detecting diodes and their readout circuitry in the same piece of silicon: feedback from foundry that substrate sufficiently lowly doped is available, 10 micron depletion no problem, strong perspectives to obtain more
- Traditionally monolithic detectors on very high resistivity substrate need non-standard processing, or are MAPS based with serial readout not necessarily compatible with future colliders, and with collection by diffusion very much affected by radiation damage



Monolithic now possible in very deep submicron standard CMOS !

- Cost per unit area in production less than that of traditional silicon
- Standard volume production (~ 20 square meter a day)
- Detector-readout connection automatically realized
- Low capacitance allows very favorable power – signal-to-noise ratios
- Very deep submicron allows power and speed advantages
- Allows innovative readout circuits
- Collection by drift will allow increased radiation tolerance

Very interesting for the LHC upgrades or any future linear collider

Significant investment dominated by engineering run submissions (90 nm or beyond !)

- Aiming for 10 mW per square cm or less with ~100x100 micron elements
- Significant advantages beyond 130 nm (lower parasitics due to low k dielectrics)
- 2-3 year project to put full prototype on the table and a few MCHF dominated by the submissions

Summary

- A number of relevant technologies have been presented
- Low cost bump bonding should help increase the reach of hybrid pixels and may be useful in vertically integrated module building
- CERN offers access to a number of deep sub micron CMOS processes via MPW service
- The Medipix2 and Medipix3 Collaborations are exploring ways of developing 4-side buttable tiles using back end TSV. This could be very useful in HEP and photon science
- A new concept for a monolithic CMOS detector has been presented