Parallel Algorithms for GEM Detectors Systems Postprocessing

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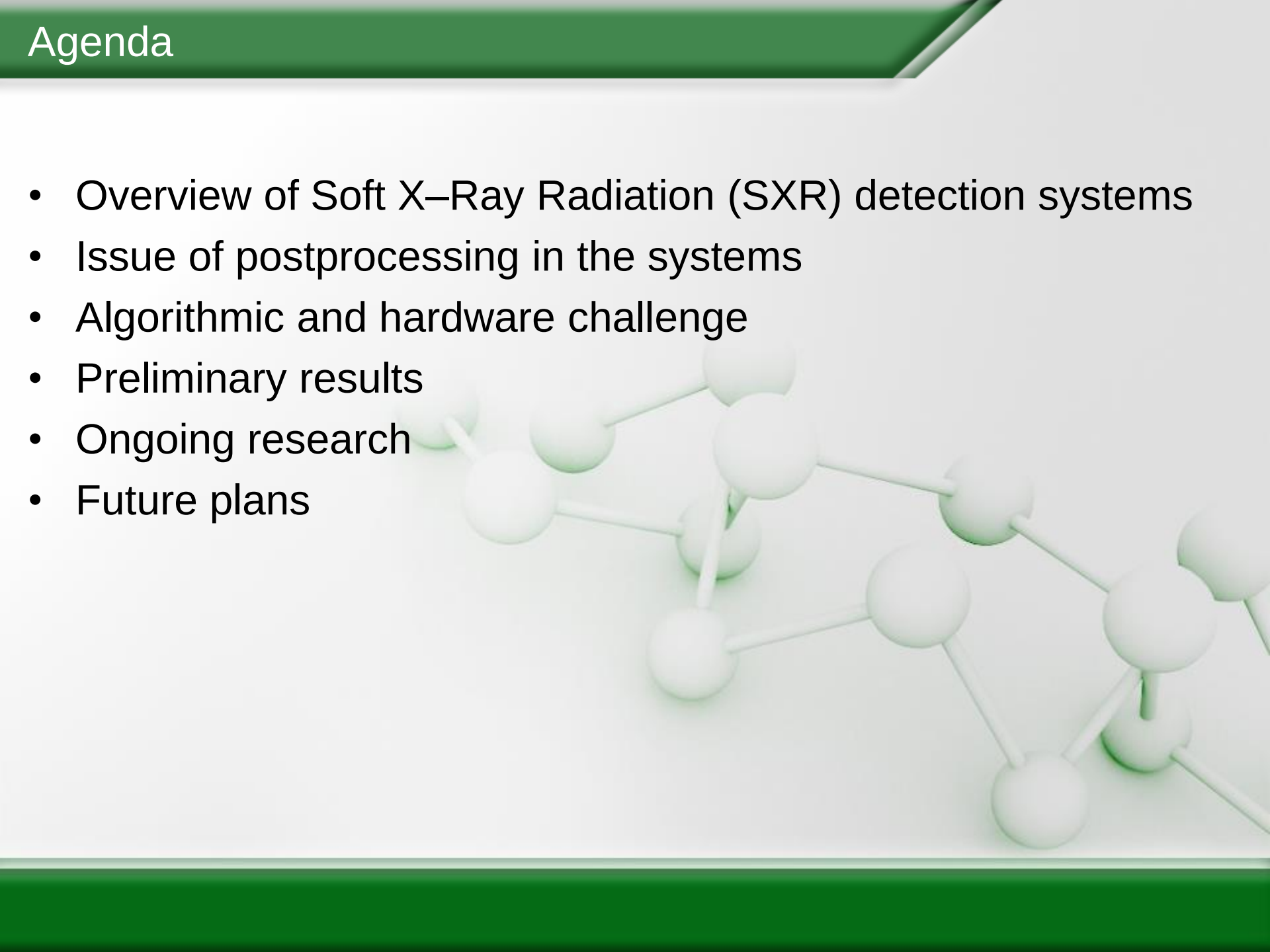
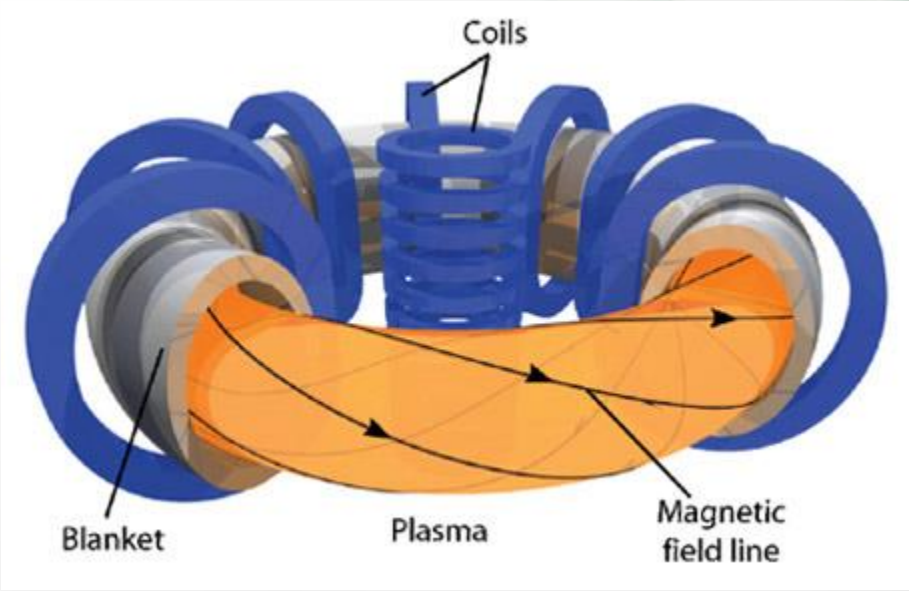
Agenda

- Overview of Soft X–Ray Radiation (SXR) detection systems
- Issue of postprocessing in the systems
- Algorithmic and hardware challenge
- Preliminary results
- Ongoing research
- Future plans



Tokamaks

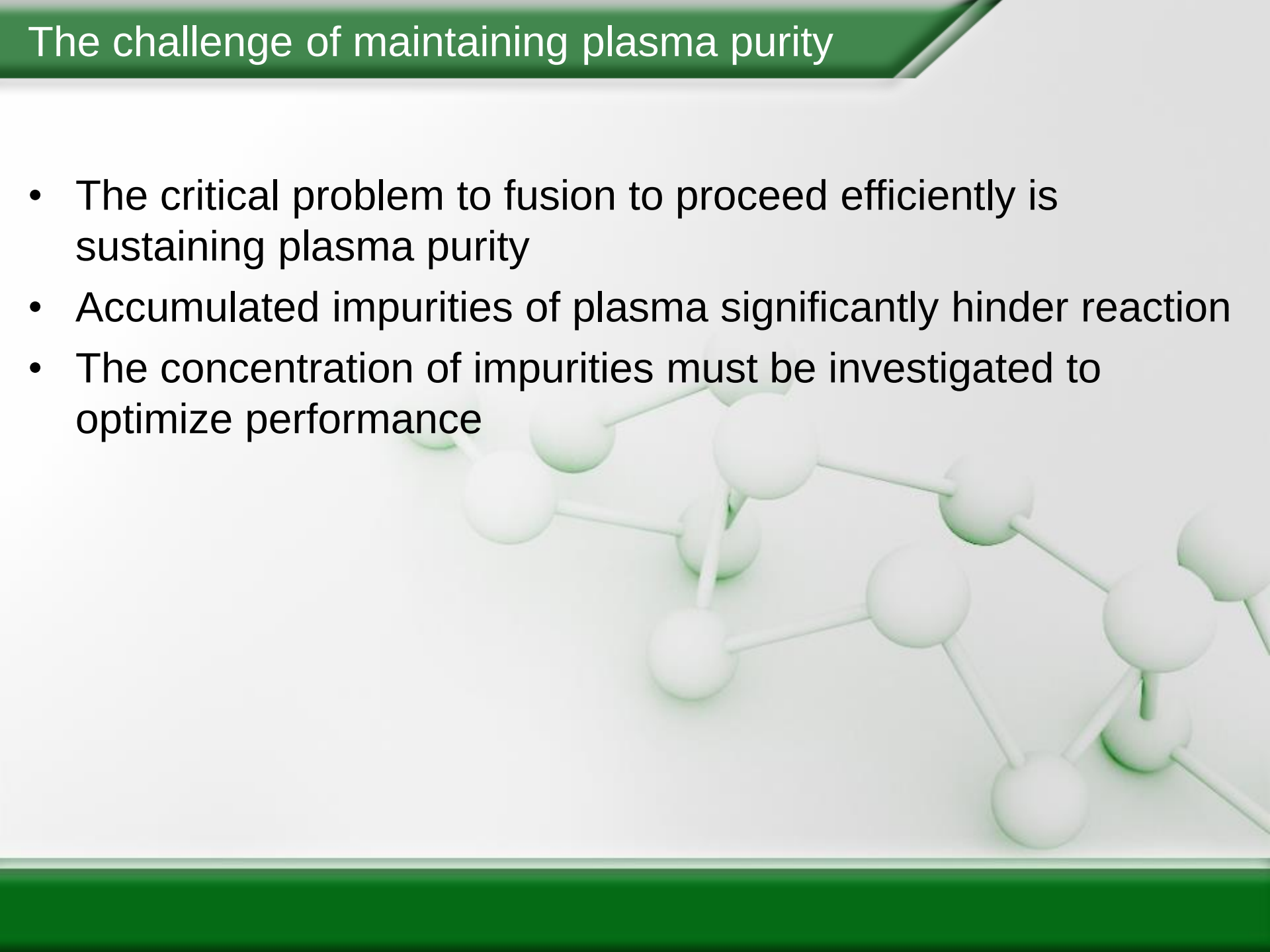
- Rus. **To**roidalnaja **Ka**miera s **Ma**gnitnymi **K**atuszkami
- Fusion reactor responsible for accelerating and maintaining plasma within magnetic boundaries to allow fusion reaction



Source: fusionforenergy.europa.eu

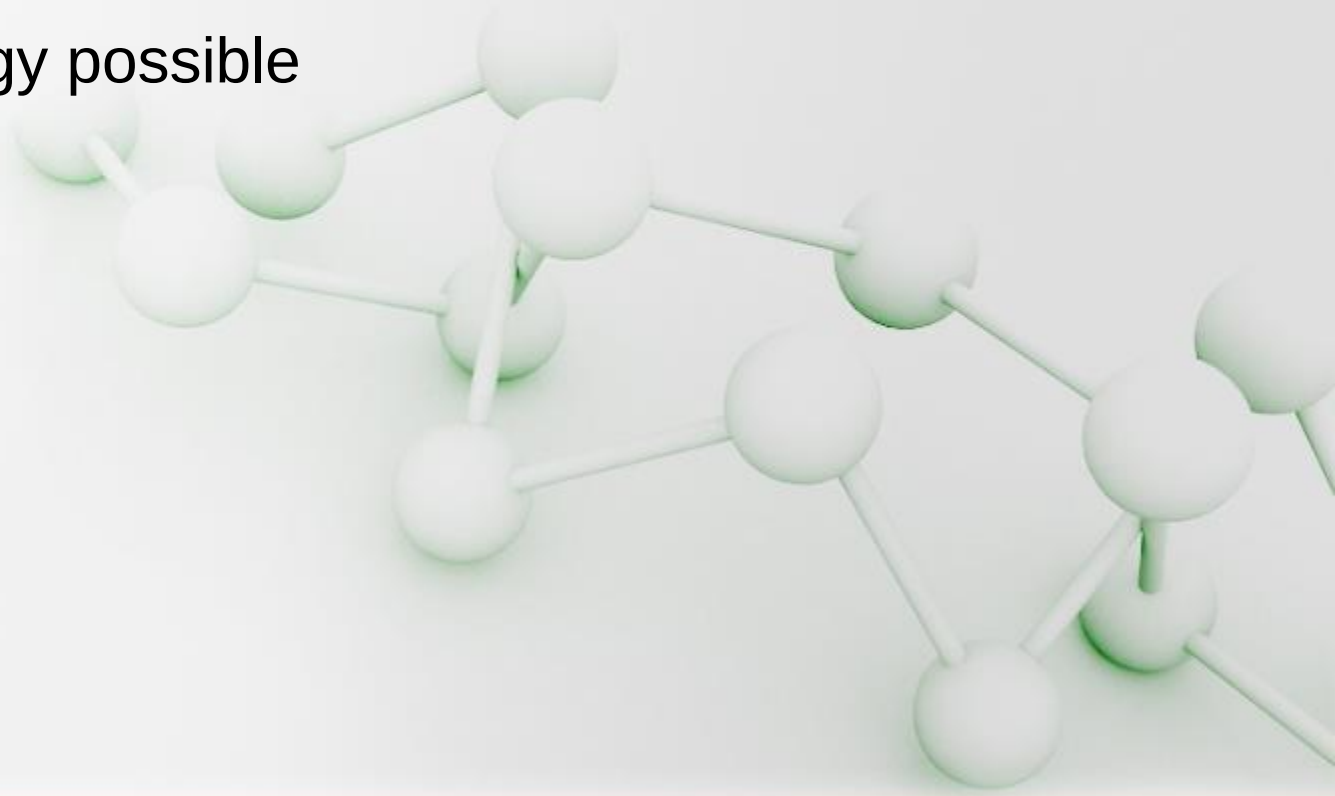
The challenge of maintaining plasma purity

- The critical problem to fusion to proceed efficiently is sustaining plasma purity
- Accumulated impurities of plasma significantly hinder reaction
- The concentration of impurities must be investigated to optimize performance



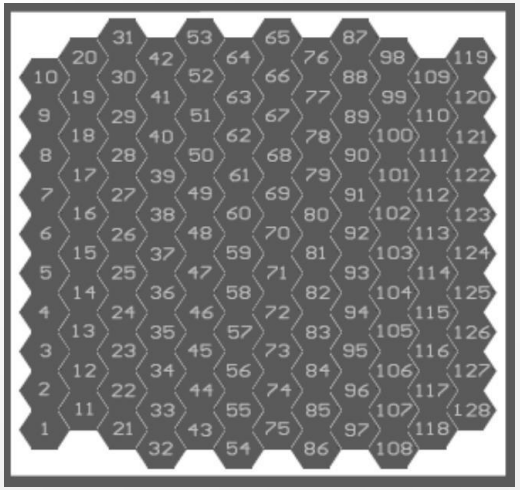
Why the SXR detection ?

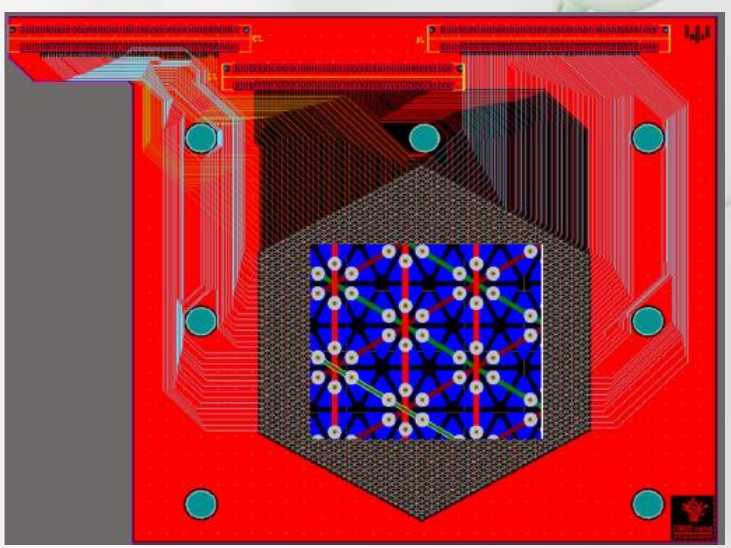
- Local impurities can be measured through SXR measurement
- Also: information about photon temperature, shape of plasma and magnetic axis
- Magnetic topology possible

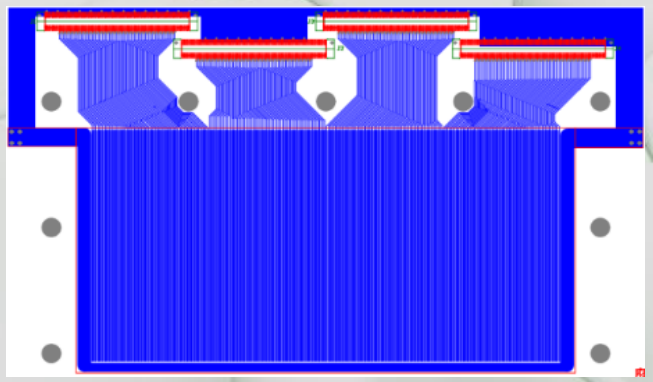


GEM detector

- GEM - Gas Electron Multiplier
- Impervious to neutrons in tokamak
- High spatial and time resolution
- Possible two-dimensional detection
- Manifold detection topologies possible

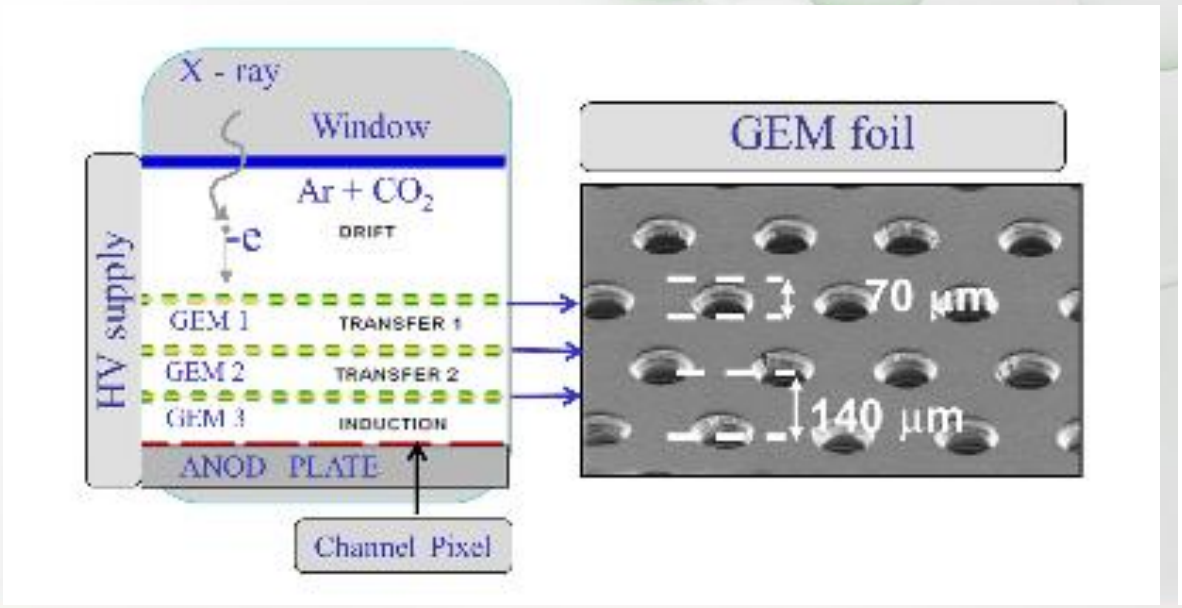


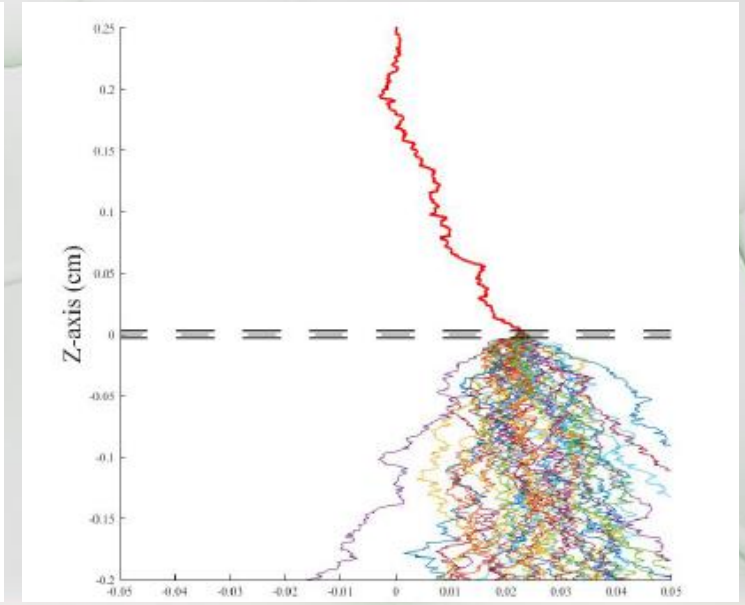




GEM detector – principle of work

- Generation of electron as a result of radiation absorption
- Multiplication in gas
- The cloud falls on the anode plate
- Henceforth electrical signal- amplification and A/D conversion



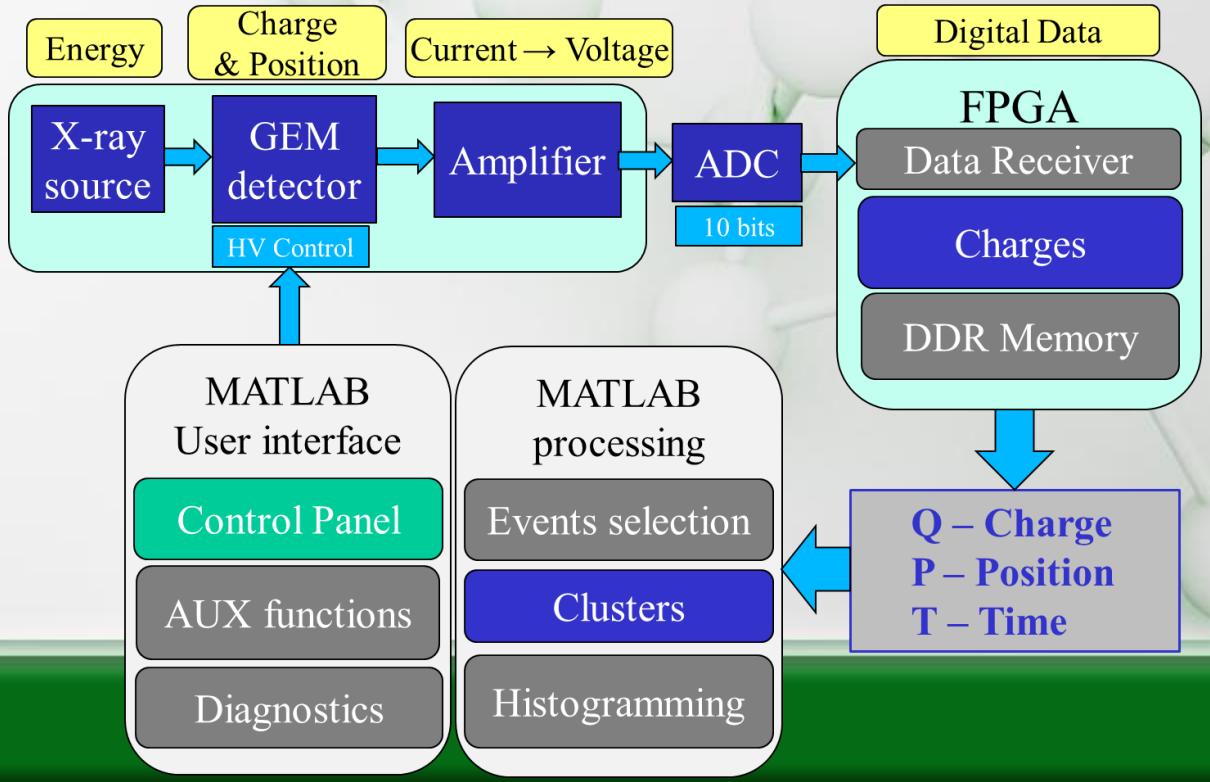


Systems with GEM detectors

- Tremendous amounts of data and throughput– hundreds of Gbits/s
- Achieving highest spatial and temporal resolution with hardware constraints
- The preprocessing phase done by FPGAs

Legacy system

- Data saved to disk
- Preprocessing online in FPGAs, postprocessing offline in MATLAB
- The MATLAB algorithms hard or impossible to implement in FPGAs

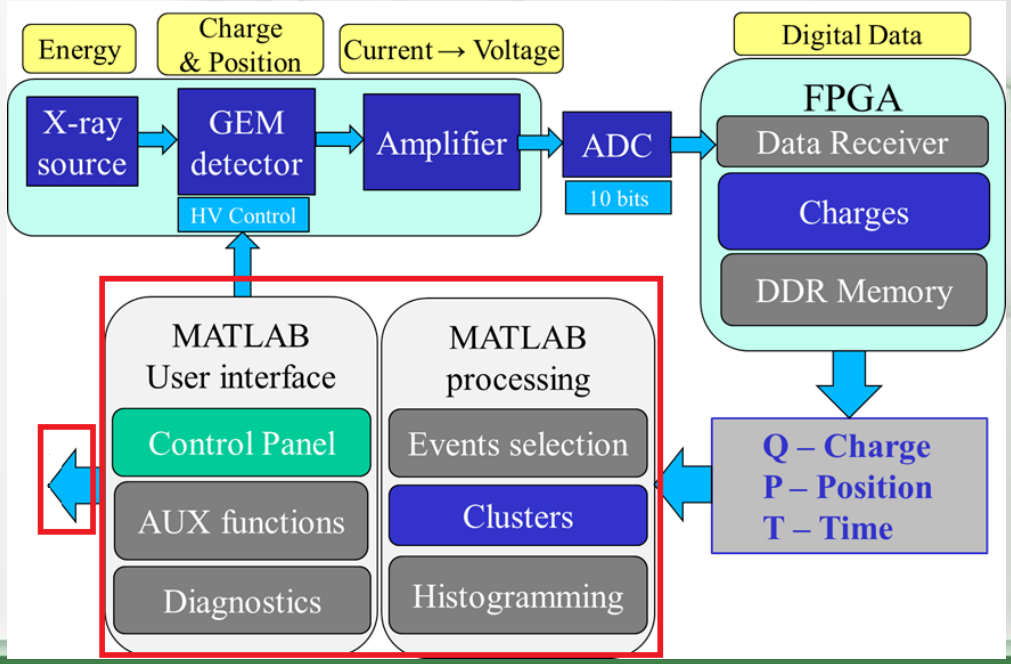


The development of system

- For 512 channels real-time processing of above 500Gbit/s of data – increase of resolution and throughput
- Increase of functionality – further processing of data on-line (so-called postprocessing)
- Postprocessing of data of reduced though significant throughput (several GB/s) after preprocessing

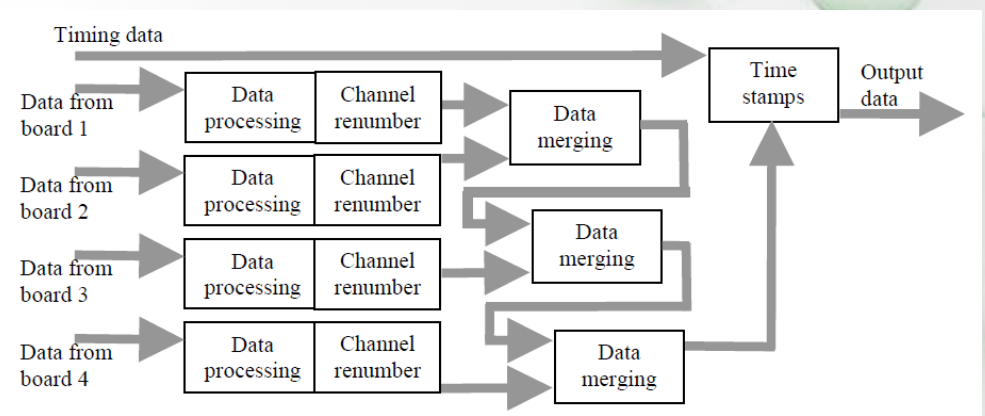
Postprocessing- the primary objective

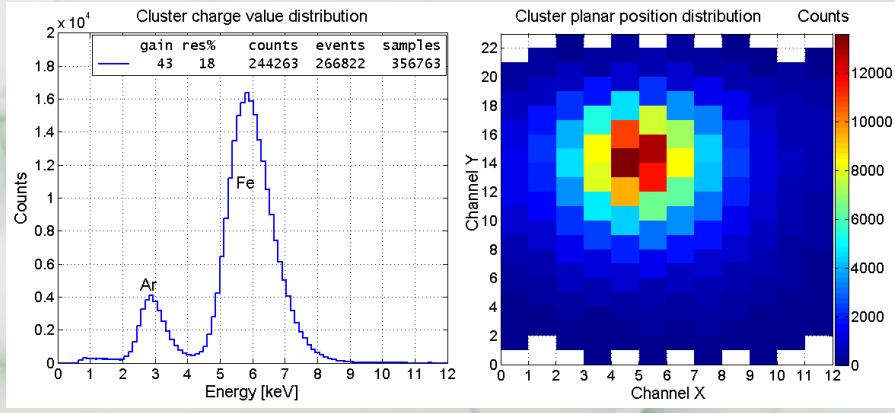
- Optimizing data analysis
- Development of platform to implement and to test the both algorithms
- Finding an alternative for FPGAs
- Introducing loopback to plasma control mechanisms in tokamaks



Posprocessing- algorithmic challenge

- Merging and sorting of data from different boards
- Subsequent histogramming of collected data with cluster and event detection
- Reconstruction of 2D charge distribution in the detector
- Planned 3D reconstruction



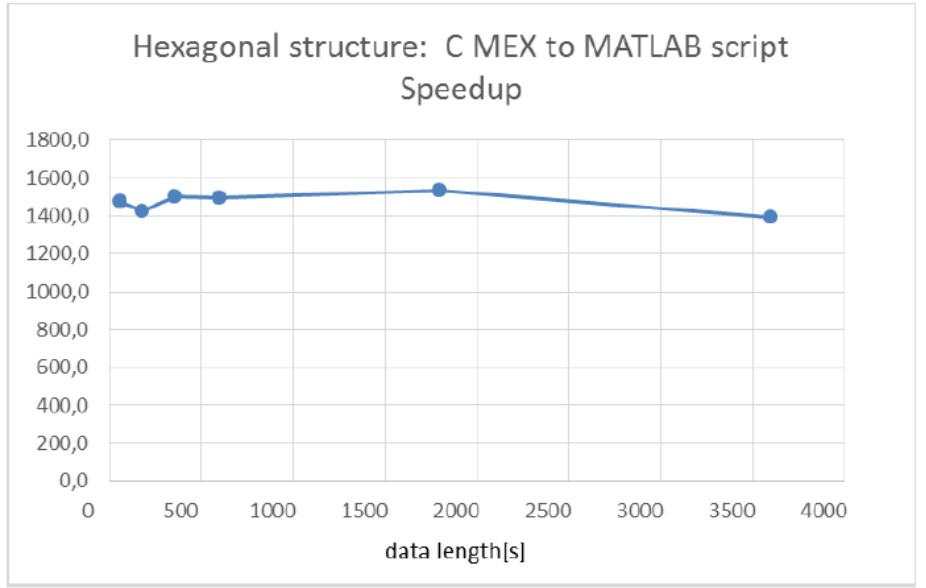


Postprocessing- hardware challenge

- The necessity of investigating architectural capabilities of available high-end electronics
- GPU(CUDA)
- MIC Intel Xeon Phi + CPU Intel Xeon
- DSP
- FPGA

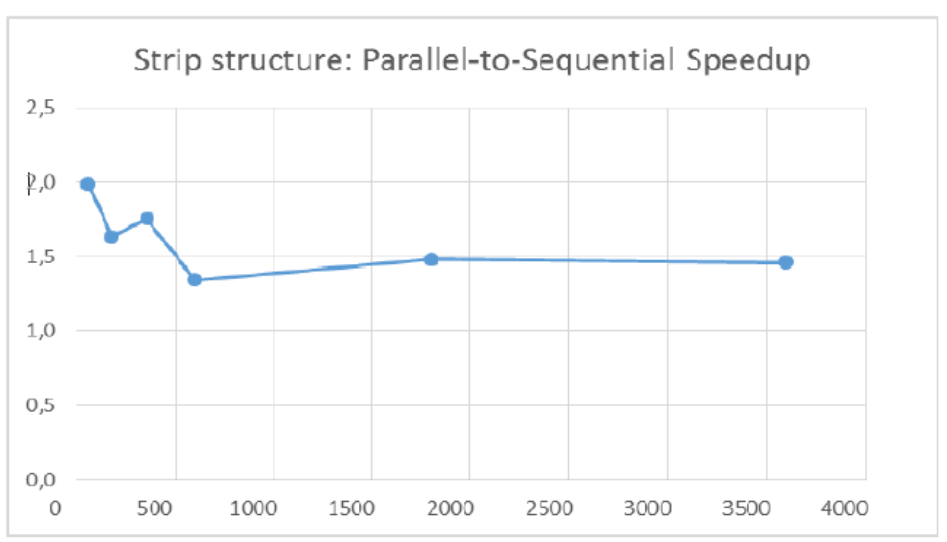
Preliminary results

- Basic goal- achieving speedup on MATLAB algorithms with offline data
- Achieved by implementing algorithms in C accessible via MATLAB mex API
- Redesigning algorithms while retaining their functionality
- Up to 1000 x speedup achieved



Preliminary results cont'd

- Preliminary parallelization led to further speedup on dual-core CPU
- Format of data and patterns of memory access strongly influence performance
- Conclusion – attempt to optimize via manipulating the data format and parallelizing seems legitimate



Ongoing research

- Reverse- engineering the collected data to format at a stage of PCIe transfer to PC
- Study of known methods to parallelize the given algorithms
- Finding parallel patterns
- Necessary implementation of crucial parts of algorithms and scrutinizing the influence of various forms of data representation and parallelization

Ongoing research cond'd

- Investigating achieved speedup on Intel Xeon, Intel Xeon Phi and NVIDIA GPU
- Major problem – Computation-to data transfers ratio, data of variable length, memory access patterns
- Investigating and assessing which technology will allow to achieve highest speedup
- Necessary deep insight into architecture and justifying the reason of achieved speedups
- The collected information crucial for further studies

Future plans

- Basing on the achieved speedups, propose a platform for further development of algorithms
- Implement more elaborate algorithms, e.g. 3-d reconstruction
- Pinpointing algorithm and hardware features that led to such decisions
- Developing a heuristics to choose appropriate hardware for given algorithms
- Develop a loopback to the tokamak

Thank you for your attention