A novel digital magnet power supply approach

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Abstract

Programmable logic and integrated technologies, as SoC, FPGA and DSP, have became mature enough to be employed in high performance magnet power supply applications. The use of a configurable mixed current and voltage digital control, combined with adaptable complex algorithms for protections (e.g. quench in superconducting magnets) and auxiliary integration (e.g. transverse flux density in a dipole gap) allows obtaining the perfect fit for each specific magnet application. An entire series of power supplies, coming from a background of particle accelerator applications, has been developed for both bipolar and monopolar operation with high bandwidth (fast fields as in corrector magnets and steerers) and high adaptability with a user-friendly interface and an embedded Linux OS that allows users to implement their own applications directly on the power supply. The use of 24-bit Analog-to-Digital converters and state-of-the-art PWM generation (with possible application of dithering techniques to reach 65-ps resolution) enables to obtain fields actuations in the ppm-level range. Some power converters, for specific applications (usually dipoles or superconducting), are equipped with closed-loop zero flux transducers that feeds their signals to temperature-stabilized electronics to reach current temperature coefficient values of 1 ppm/K.

Conclusions

- control of different types of power topologies - i.e. **different magnet types** with different requirements
- **remote optimization** of the current dynamic behaviour using the digital control loop - i.e. no oscillations or slow response
- fast connectivity (Gigabit Ethernet + SFP/SFP+): optimized for **single module or** for **large installations**
- **extreme high-stability** at 1 ppm/°C with matched 0-FLUCS DCCTs + temperature stabilization
- easy **software development**/integration directly on the power unit using the embedded **Linux OS** - Yocto Project
- **paralleling** of modules via SFP/SFP+ optical links
- **remote configuration** of waveforms, triggers, interlocks and **protections** configurations for the specific application
- implementation of **different control schemes** - e.g. IIR filters, adaptive algorithms, etc.

Platform

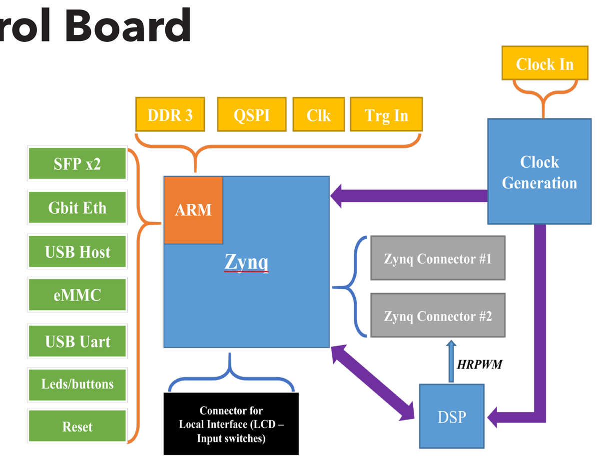
Control Board

Digital **Control Board** including:
- FPGA (Zynq)
- DSP (Texas Instruments)

Interfaces included are the following:
- 10/100/1000 Ethernet
- 2 x SFP+ (6.5 Gbps/channel)
- USB Host
- eMMC
- display and encoder control

FPGA is used for digital output control algorithms and **DSP** for High-Resolution PWM generation.

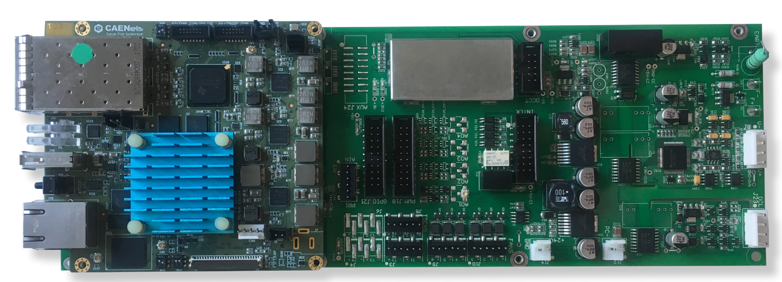
Linux OS (Yocto Project) is embedded in the ARM.



Carrier Board

The digital Control Board is plugged onto the **Carrier Board** with two 100-pin high-speed FCI connectors. The Carrier Board is provided with:

- 2 x 24-bit@100 ksps ADCs for current and voltage readout (T-stabilized)
- DC-Link, Temperature and Auxiliary analog readings (16-bit@100 ksps)
- I/O signals for interfacing with external protections (e.g. quench)
- interlocks and status signals
- connector for future expansions.



The Carrier Board also embeds the power section to supply the active DCCT transducer with low-noise power at ±15V in order to have a direct, accurate, stable and precise current readout.

Power Stage Control

The on-board FPGA performs all the control loop algorithms at a hardware-level to maximize speed and computing power.

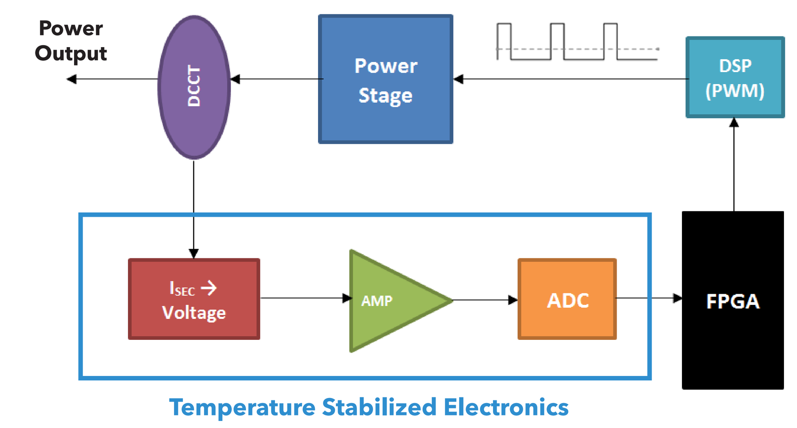
The DSP is used as a multi-channel PWM generator with a 65-ps PWM resolution. For bipolar stages (H-Bridge topologies), this resolution can be halved.

The equivalent setting resolution for a 15-kHz switching monopolar power stage can be computed as:

$$Resolution = log_2\left(\frac{1}{T_{PWM} \cdot f_S}\right) = log_2\left(\frac{1}{65 \cdot 10^{-12} \cdot 15 \cdot 10^3}\right) \cong 20\ bit$$

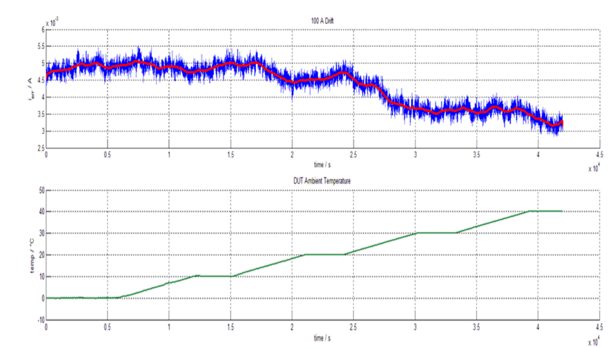
This resolution can be increased to **21 bit** for bipolar stages.

Current Sensing



0-FLUCS DC Current Transformer

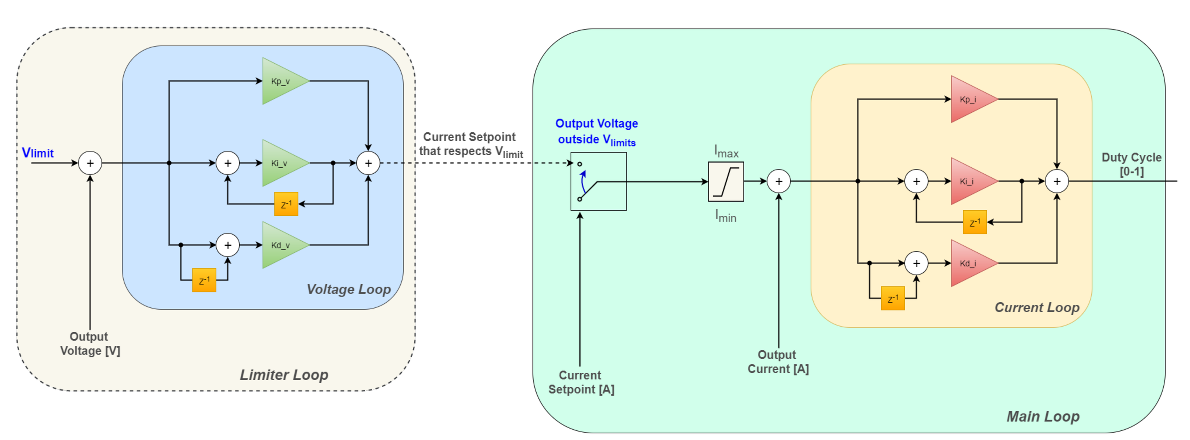
The current sensing is made using a proprietary closed-loop zero flux **DCCT** (DC Current Transformer) and fed to the ADC via a temperature-stabilized signal conditioning section to reach a **TC < 1 ppm/°C**.



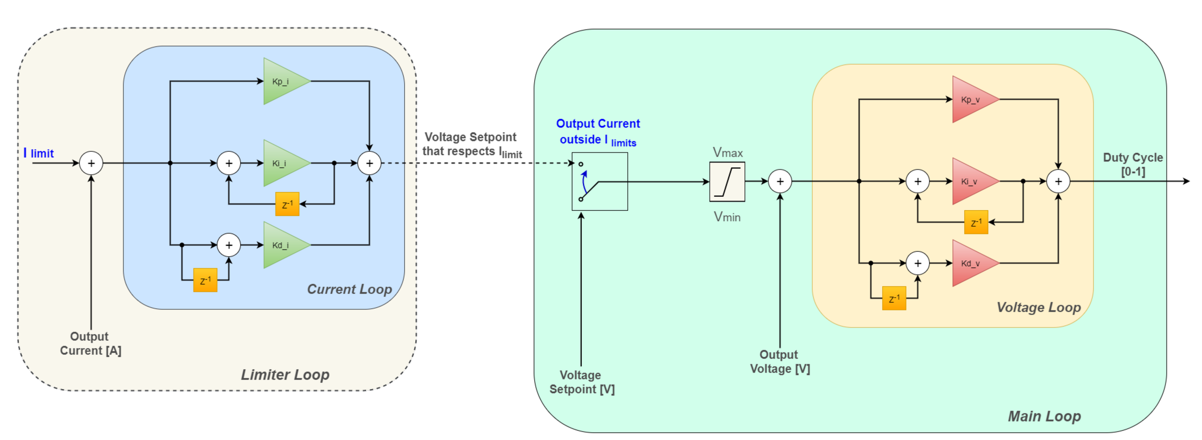
Output Control Loop

The on-board programmable logic allows for **complex algorithms** to be performed on the current and voltage output values.
A lot of different feedback control loops have been implemented but standard ones are modified versions of Proportional Integral Derivative (PID).
Two examples are hereafter shown:

Constant Current (CC) Output Control



Constant Voltage (CV) Output Control

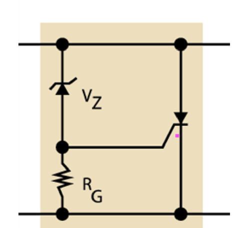


Application Example: *a user can implement a slower closed loop directly on the Linux OS by using the readings of the magnetic field from a Hall probe fed to the auxiliary input of the carrier board.*

Additional Features

Crowbar

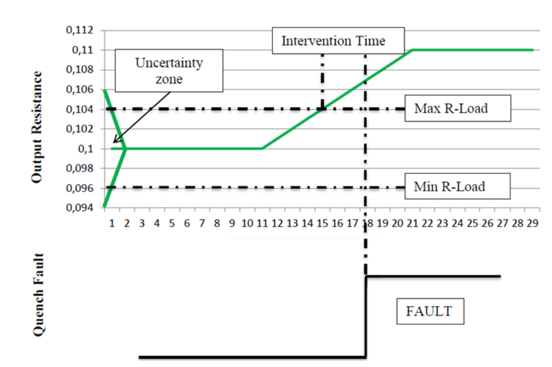
Active circuits to protect against back-energy are designed for monopolar and bipolar power supplies.



A specific circuit that remains active for **> 10 min after an AC mains failure** has been integrated also for superconducting magnets.

Quench

A quench protection procedure is **running on the FPGA** and it is configurable.



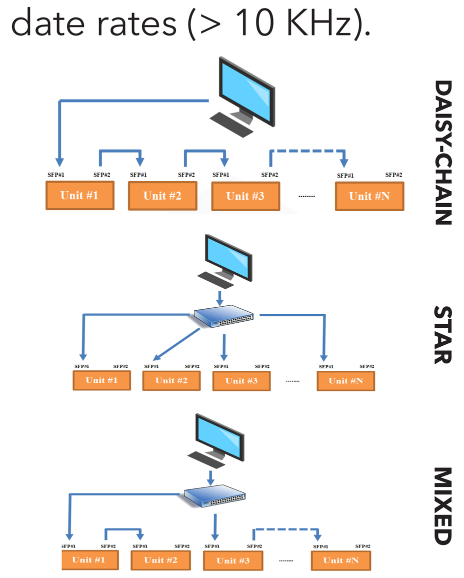
Auxiliary Inputs

External analog control input (e.g. to use the power supply as an **amplifier**) is provided by using another ADC at 16-bit 100 ksps.

An external input can also be used to read, for example, the **magnetic field** generated by the magnet - e.g. Hall probe. A slow loop can be closed on the field value.

Fast Connections

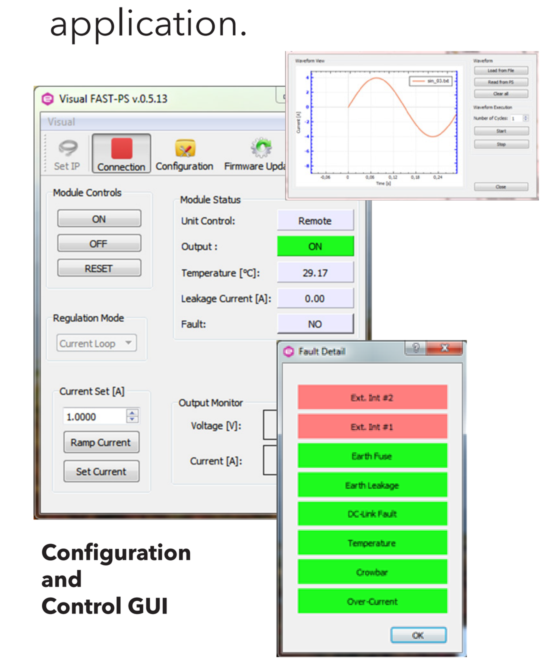
Two 6.5 Gbps SFP+ links are provided for fast update rates (> 10 KHz).



Paralleling is also performed using the SFP+.

Remote Configuration

Interlocks and protections can be configured remotely to match the application.



Configuration and Control GUI