CLIC DR Kickers Inductive Adders – Status Update

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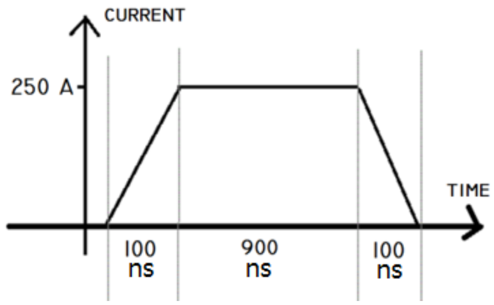
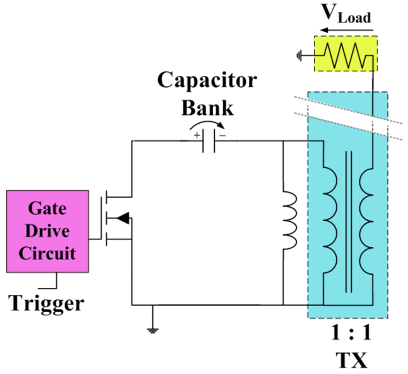
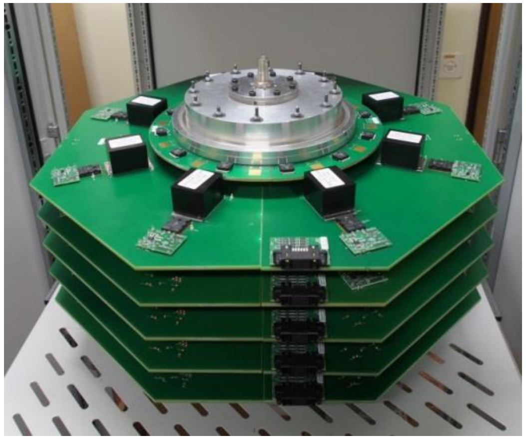
Overview

- **Background**
  - CLIC Layout with Damping Ring (DR) kickers
  - Specifications for CLIC DR Extraction Kicker System
  - Challenges and Issues
- **Inductive Adder Design**
  - Schematic
  - Improving the Pulse Stability
- **3.5 kV Prototype Inductive Adders**
  - Specifications for the First Prototype Inductive Adders
  - 3.5 kV Pulses without Modulation
  - Passive and Active Droop Compensation
  - Active Compensation of Droop and Ripple
  - Evaluation of Magnetic Core Material for 12.5 kV Prototypes
- **12.5 kV Prototype Inductive Adders**
  - Initial Measurements on Magnetic Cores
- **Summary and Future Work**

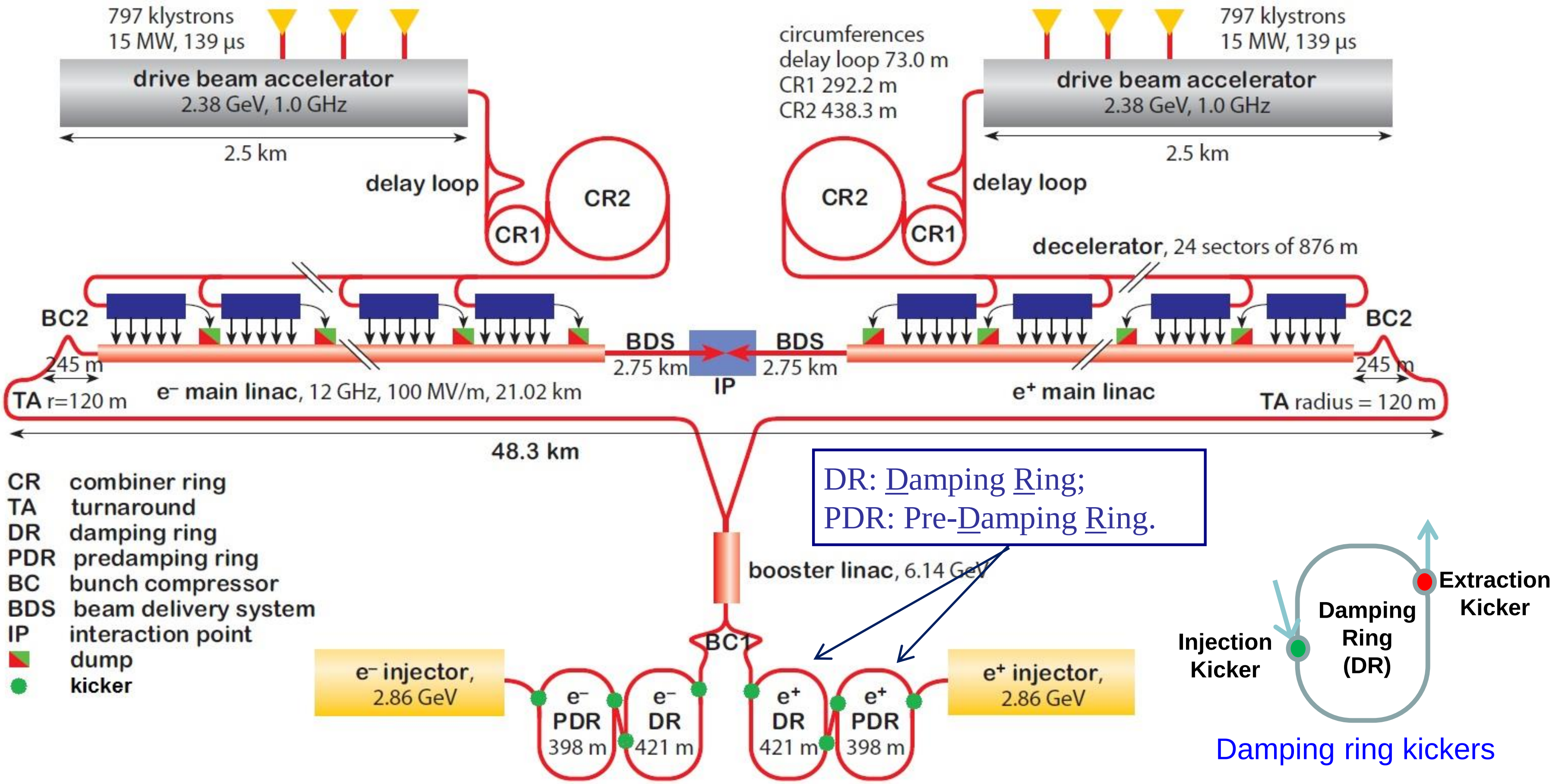


Ideal stripline current for 1 GHz option





CLIC General Layout



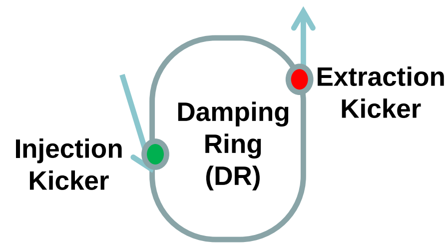
PDR & DR Kickers (●):

- One injection and extraction system per ring and per beam (8 systems);
- Damping rings reduce beam emittance; hence kickers must be high stability (low ripple);
- Low beam coupling impedance and good field homogeneity are required (talk by C. Belver-Aguilar).

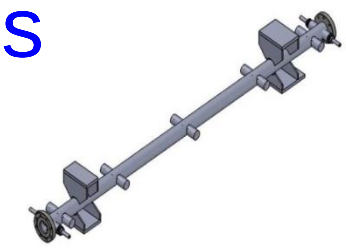
Specifications for the CLIC DR Extraction Kicker Systems

	CLIC DR (1 GHz | 2 GHz)
Pulse voltage (kV) (per Stripline)	**±12.5**
Stripline pulse current [50 Ω load] (A)	**±250**
Repetition rate (Hz)	**50**
Pulse flat-top duration (ns)	**~160 | ~900**
Flat-top repeatability	**$\pm 1\times10^{-4}$ (±0.01 %)**
Flat-top stability [inc. droop], per Kicker SYSTEM (Inj.) (Ext.)	**$\pm 2\times10^{-3}$ (±0.2 %) $\pm 2\times10^{-4}$ (±0.02 %)**
Field rise time (ns)	**1000**
Field fall time (ns)	**1000**
Beam energy (GeV)	2.86
Total kick deflection angle (mrad)	1.5 (0.09 deg)
Aperture (mm)	20
Effective length (m)	1.7
Field inhomogeneity (%) [3.5mm radius] [1mm radius]	±0.1 (Inj.) ±0.01(Ext.)

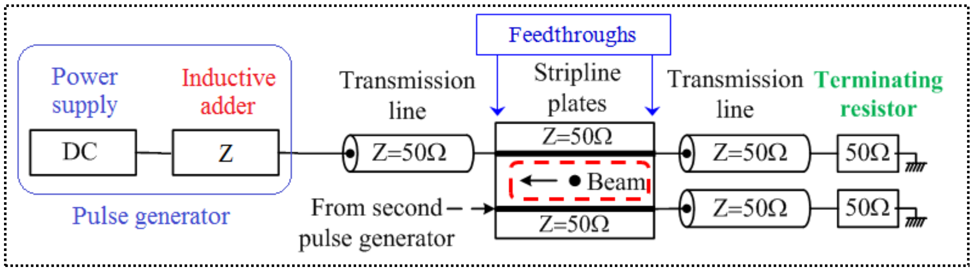
- **NOTE:**
  - **For rise/fall times, ≤ 100 ns desired!**
  - **Close to 0 V intra-pulse (off-time) voltage required!**



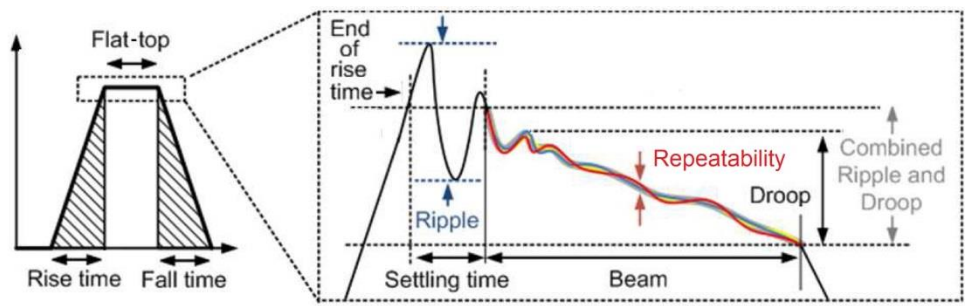
Damping ring kickers



Drawing of the CLIC DR extraction kicker
(Courtesy of C. Belver-Aguilar)

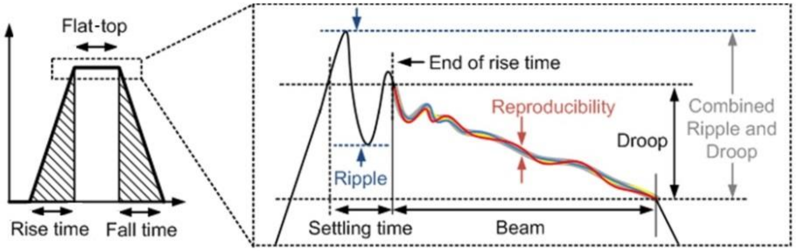


Schematic of a kicker system

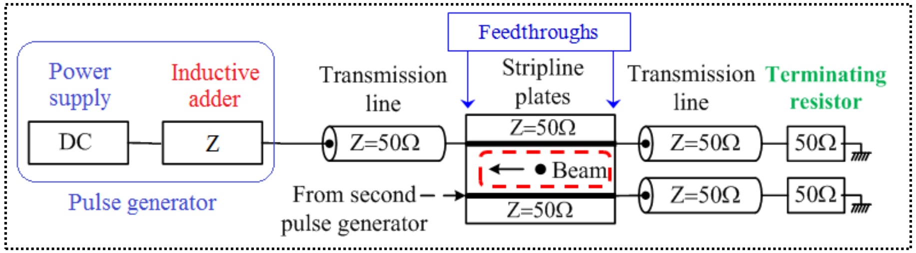


CLIC DR kicker pulse definition

Challenges and Issues

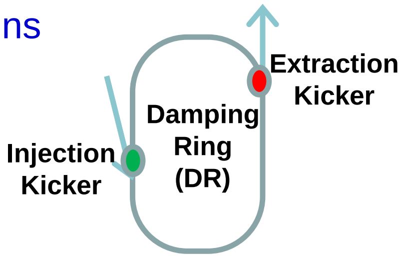


CLIC DR kicker pulse definition



Schematic of a kicker system

- **±0.02 % (± 2.5 V)** requirement for the **flat-top stability** of ±12.5 kV, 160 to ~900 ns pulse is an extremely demanding specification!
  - **An order of magnitude better than in any existing kicker systems!**
  - **Compensation of droop and ripple of the output voltage is required.**



- Adequate impedance matching to minimize duration of settling time:
  - Impedance (and field homogeneity) of the stripline kicker has been optimized: unfortunately the impedance cannot be 50 Ω for both power-off (even) and power-on (odd) operation modes!
  - Odd-mode impedance of the striplines is ~41 Ω (see talk by C. Belver-Aguilar), which causes settling time to be ~100 ns. Therefore **the pulse flat-top duration is at least ~260 ns** (2 GHz option)
- Suitable high precision measurements of the pulse in the laboratory: **better relative precision than ±2.5 V in 12.5 kV required!**

Inductive Adder

- ➢ Many primary "layers", each with solid-state switches
- ➢ The output voltage is approximately the sum of the voltages of the primary constant voltage layers

+ Control electronics referenced to ground

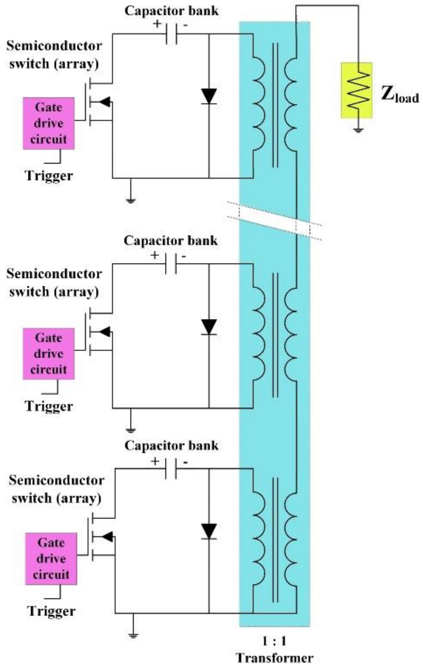
+ No electronics referenced to high voltage despite the high voltage output of the adder

+ The output voltage can be modulated during the pulse with an analogue modulation layer

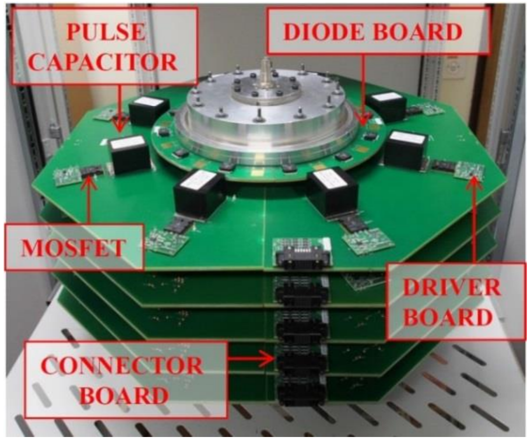
+ Modularity: the same design can potentially be used for kickers with different specifications (CLIC PDR & DR kicker modulators)

+ Redundancy and machine safety: if one switch or layer fails, the adder still gives full voltage or a significant portion of the required output pulse

+ Possibility to generate positive or negative output pulses with the same adder: the polarity of the pulse can be changed by grounding the other end of the output of the adder



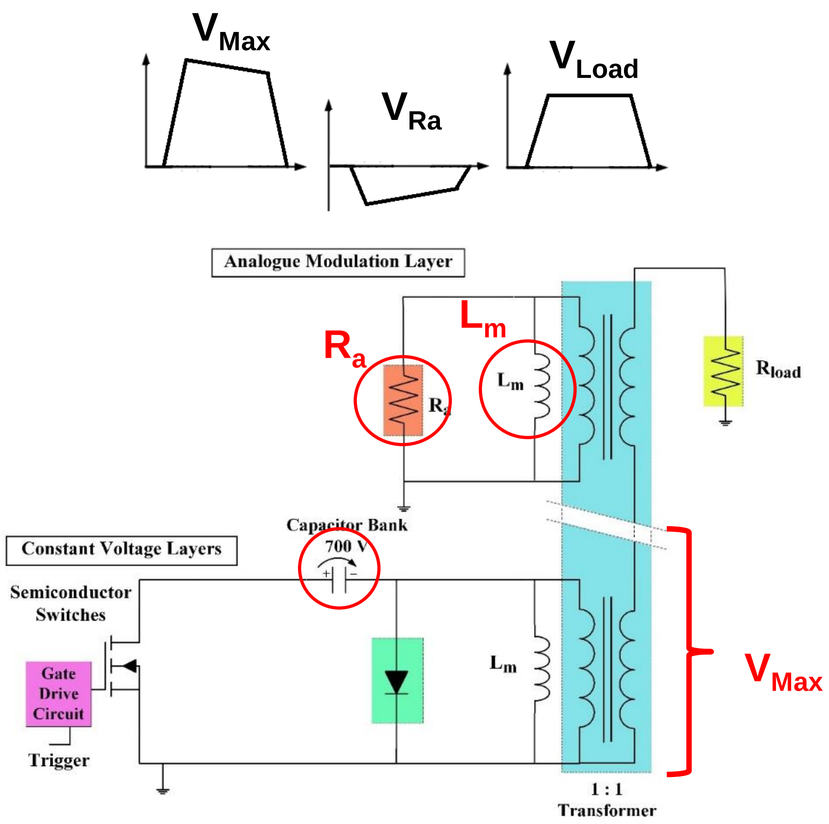
Schematic of an inductive adder



A prototype inductive adder

Improving the Pulse Stability

- Droop and ripple of the output pulse of an inductive adder can be compensated with an analogue modulation layer
- In the analogue modulation layer, resistor R_a is effectively in series with the load
- The load voltage is the difference of the voltage across the analogue modulation layer and the sum of the voltages across other layers
- Two modes:
  - **Passive mode:** During the pulse, current through $\boldsymbol{L_m}$ increases, which causes current through $\boldsymbol{R_a}$ to decrease. Therefore, voltage over $\boldsymbol{R_a}$ decreases, which can compensate for a reduction (droop) in the primary voltage of the other layers.



Passive analogue modulation

Improving the Pulse Stability

- Droop and ripple of the output pulse of an inductive adder can be compensated with an analogue modulation layer
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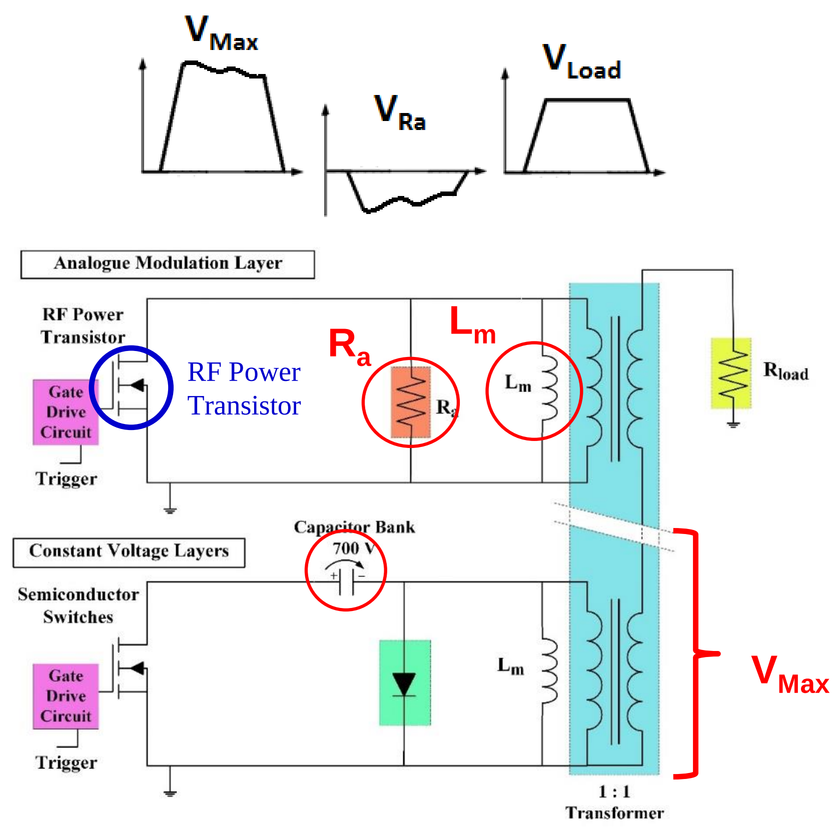
- The load voltage is the difference of the voltage across the analogue modulation layer and the sum of the voltages across other layers
- Two modes:
    - **Passive mode:** During the pulse, current through L_m increases, which causes current through R_a to decrease. Therefore, voltage over R_a decreases, which can compensate for a reduction (droop) in the primary voltage of the other layers.
    - **Active mode:** A linear RF power transistor is connected in parallel with resistor R_a. The voltage across R_a can be controlled by controlling the current through the RF power transistor.



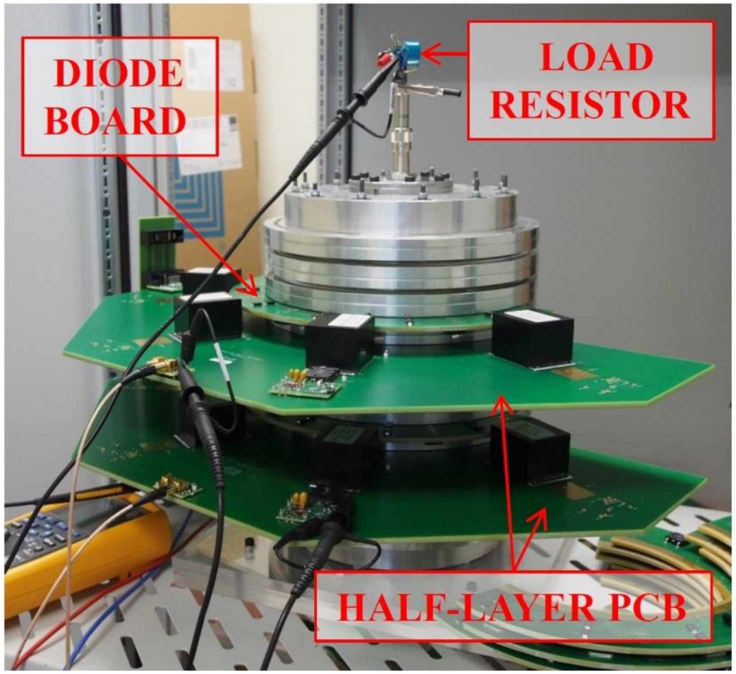
Active analogue modulation

Two 5-Layer Prototype Inductive Adders

- The purpose of the prototype inductive adder has been:
  - To verify theoretical models, which have been used to predict the operation of an inductive adder with extremely high flat-top stability
  - To verify experimentally design steps for an inductive adder with high flat-top stability
  - To test both passive and active analogue modulation
  - To approach the required ±0.02 % flat-top stability for the output pulse, as specified for the CLIC DR extraction kicker modulator

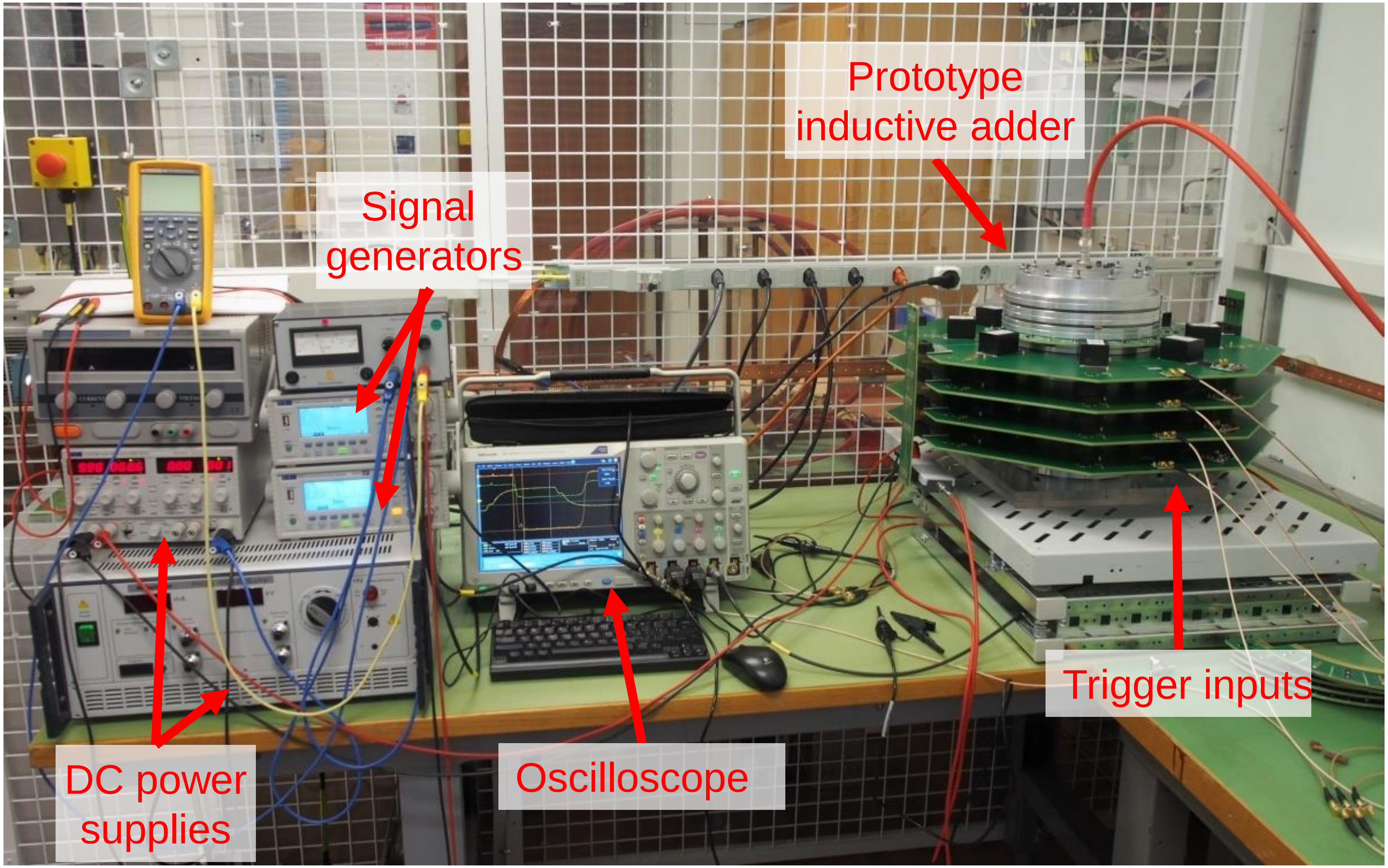
Design Parameter	Prototype Inductive Adder	CLIC DR Extraction Kicker Modulator
Output Voltage (kV)	**3.5**	12.5
Output Current [50 Ω load] (A)	**70 (250)**	250
Voltage per layer	**700**	700
Number of layers	**5**	20
Pulse flat-top duration (ns)	**160 – 350*** (900)	160 – 900
Pulse rise time [0.1-99.9 %] (ns)	**100**	< 1000
Pulse fall time [0.1-99.9 %] (ns)	**100**	< 1000
Flat-top stability (for 160 ns)	**±0.02 %**	±0.02 %
Repetition rate (Hz)	**50**	50

* limited by transformer cores, design value 900 ns



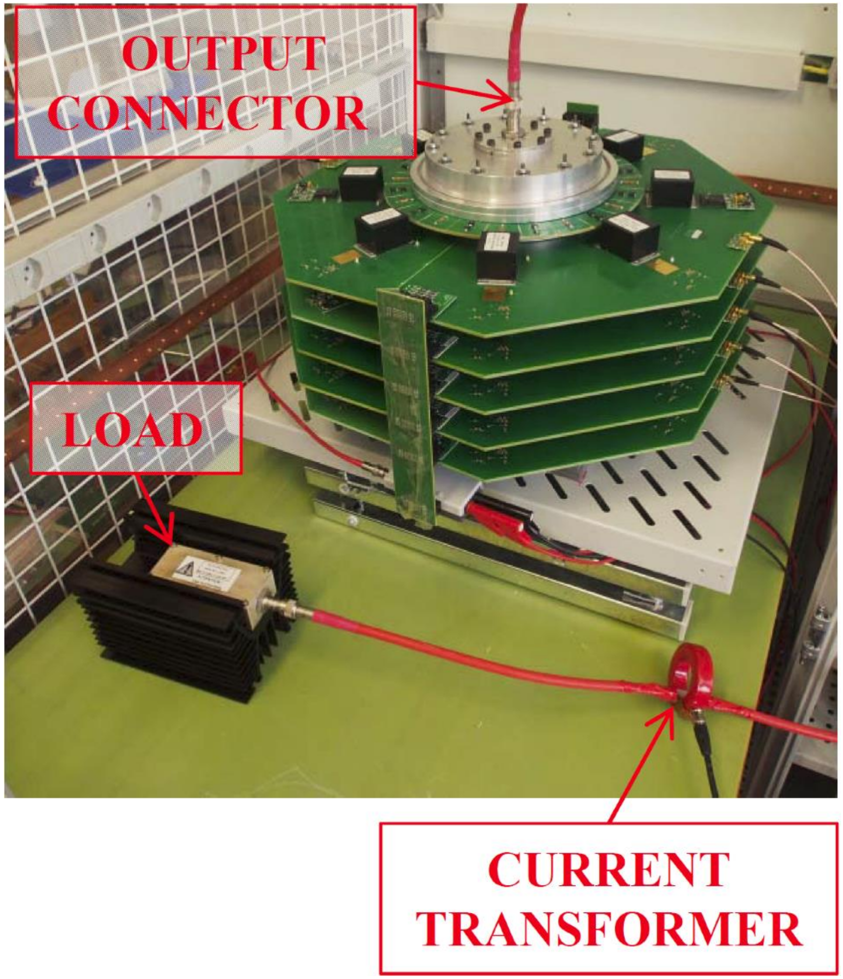
The prototype inductive adder with two half-layers inserted

Measurements on the 5-Layer Prototype Inductive Adder

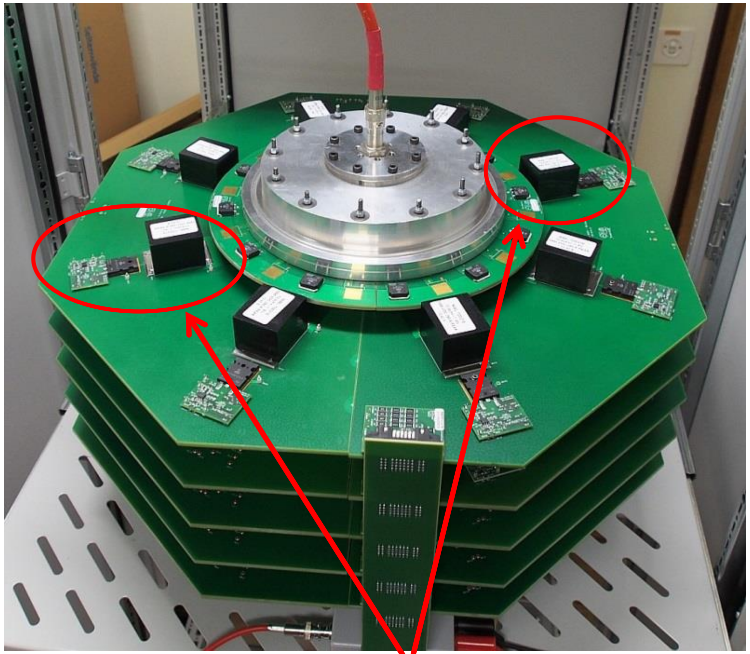


The prototype inductive adder with the measurement setup

Measurements on the 5-Layer Prototype Inductive Adder



The prototype inductive adder with a current transformer and a load



In initial measurements, only one branch per half-layer PCB was powered!
2 branches per layer.

Measurements: 3.5 kV Output Pulse - No Modulation

- **Setup for the measurement:**
  - The prototype adder with 5 layers
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) charged initially to 750 V
  - 50 Ω, 18 kV load by Diconex
  - No modulation applied.
- **Output pulse parameters**
  - Output voltage: 3.5 kV
  - Rise time (0.1...99.99 %) 160 ns
  - Droop: ~3.4 % (120 V) for 170 ns flat-top duration
  - Small intra-pulse voltage (~10 V).

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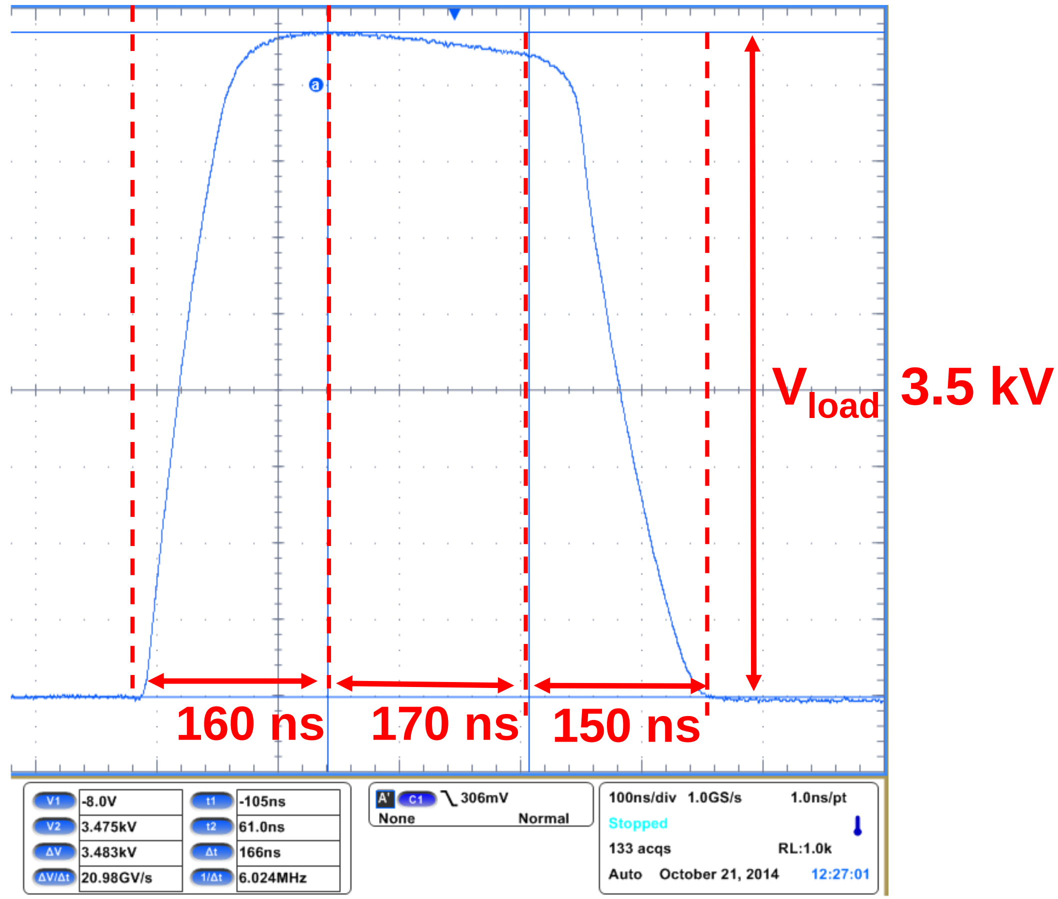
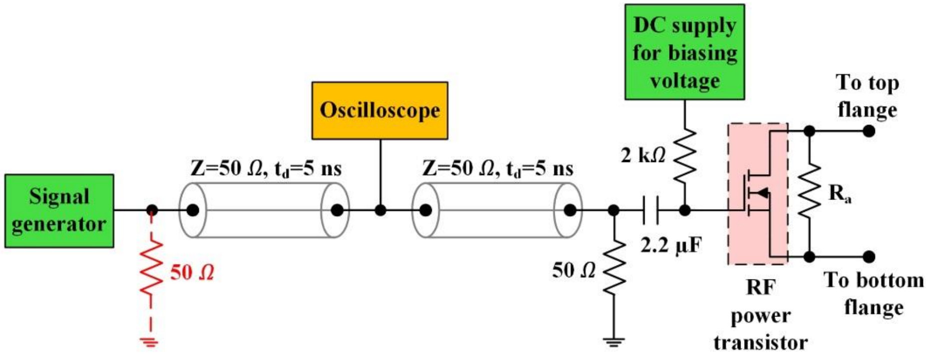
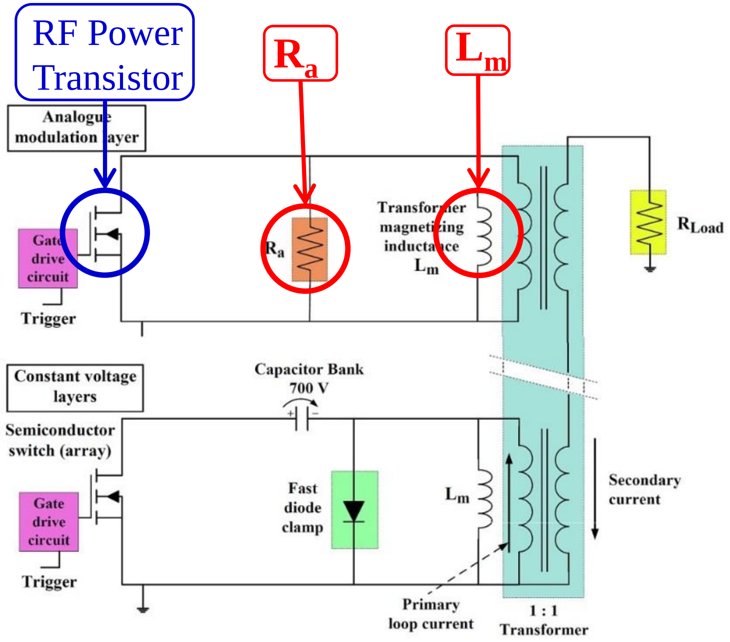
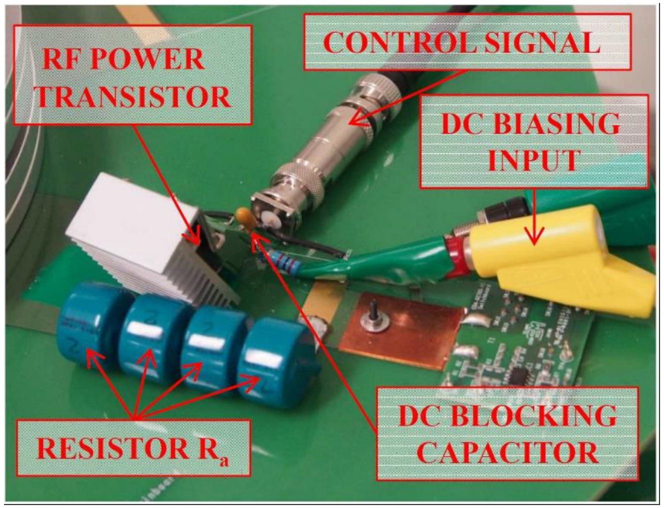


Measurements: Passive Compensation of Droop and Active Compensation of Droop and Ripple

- **Setup for the measurement:**
  - The prototype adder with 4 constant voltage layers and an analogue modulation layer
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 μF/layer) charged initially to 350...553 V.
  - Passive or active analogue modulation applied

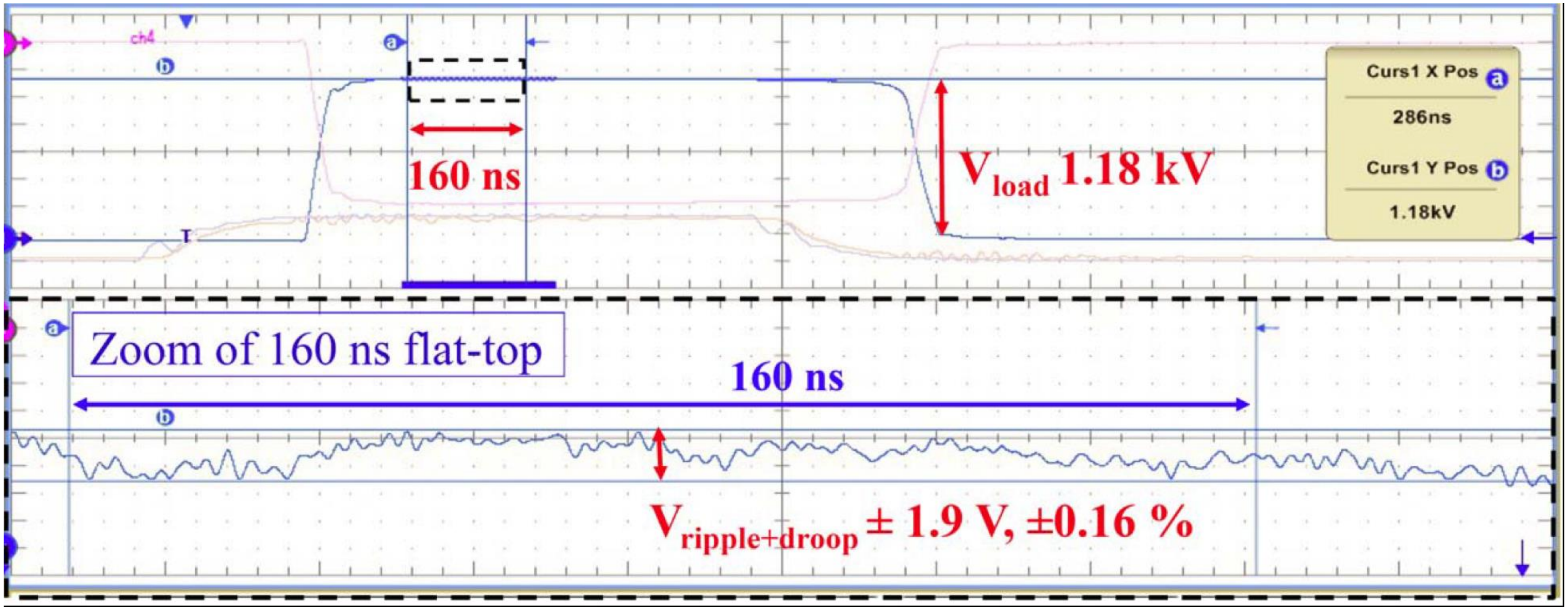






Schematic and layout of the active analogue modulation layer

Measurements: Passive Droop Compensation

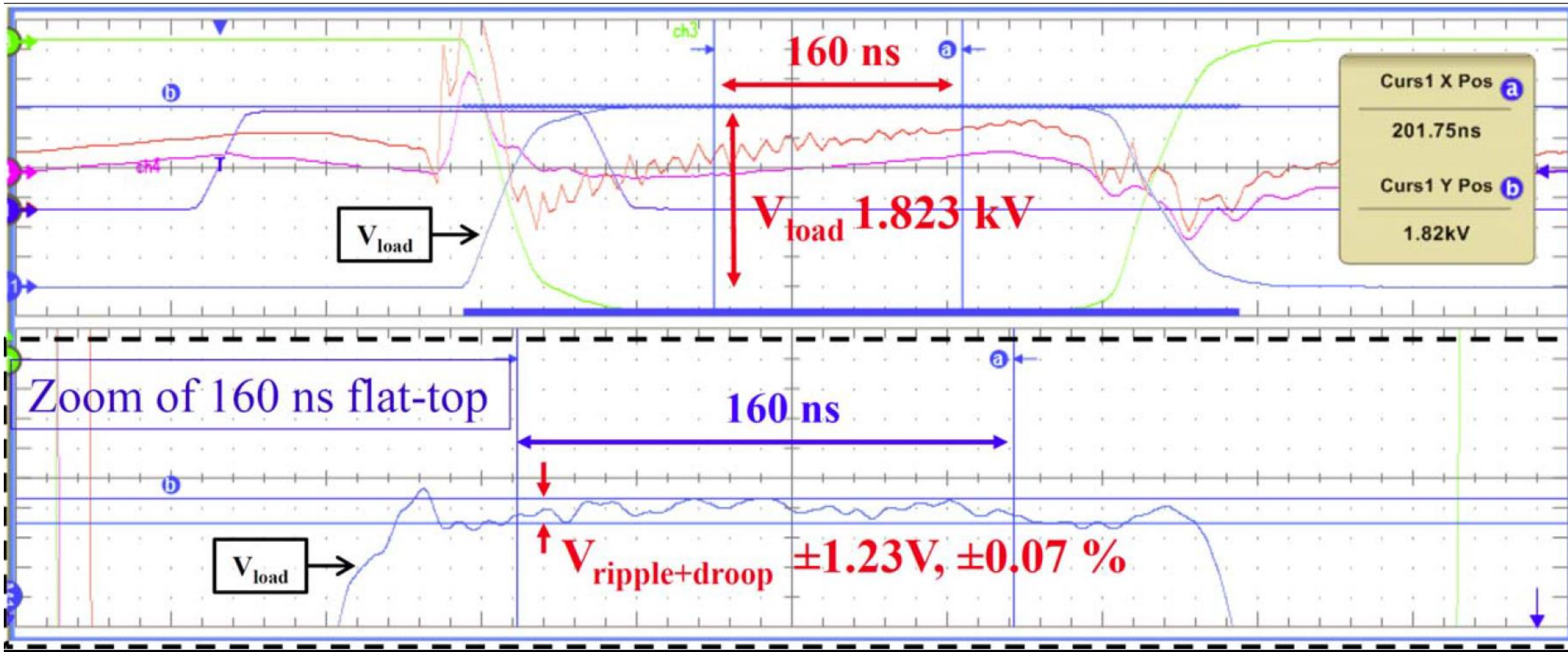


- **Setup for the measurement:**
  - 4 constant voltage layers and a passive analogue modulation layer
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) initially charged to 350 V (R_a = 7.9 Ω)

Notes:

- **Tektronix scope used (DPO 5034) has a nominal vertical resolution of 8 bits (< ±0.4%) – can be improved with oversampling and averaging**
- **The curve is an average of 1000 measured pulses**
- **The optimal combination of R_a & L_m depends on the output voltage!**

Measurements: Active Droop Compensation

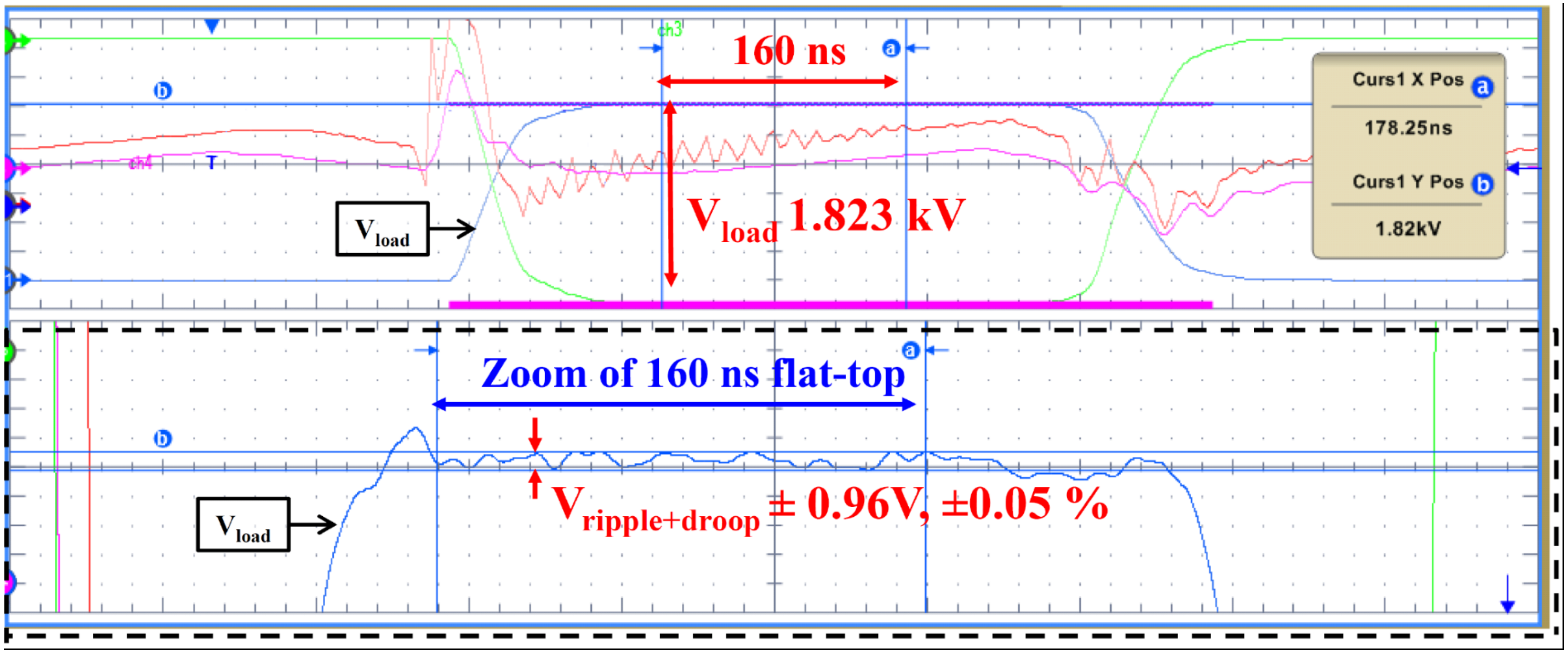


- **Setup for the measurement:**
  - 4 constant voltage layers and a passive analogue modulation layer
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) initially charged to 551 V (R_a = 7.9 Ω)
  - Active droop compensation with piece-wise linear ramp function

Notes:

- **The curve is average of 1000 measured pulses**
- **Repeat of the measurement with averaging of 4000 pulses resulted in ±1.17 V (±0.06 %)!**

Measurements: Active Ripple Compensation



- **Setup for the measurement:**
  - 4 constant voltage layers and a passive analogue modulation layer
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) initially charged to 551 V (R_a = 7.9 Ω)
  - Active droop and ripple compensation

Notes:

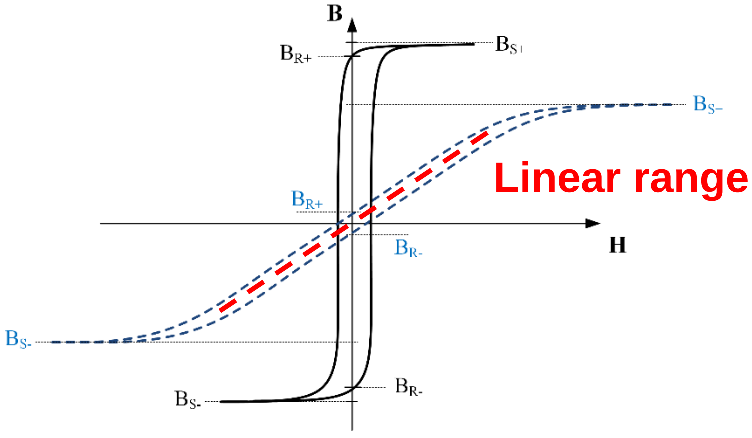
- **The curve is an average of 1000 measured pulses**
- **Repeat of the measurement with averaging of 4000 pulses resulted in ±1.02 V (±0.06 %)!**

Summary of the Measurements with 3.5 kV prototypes

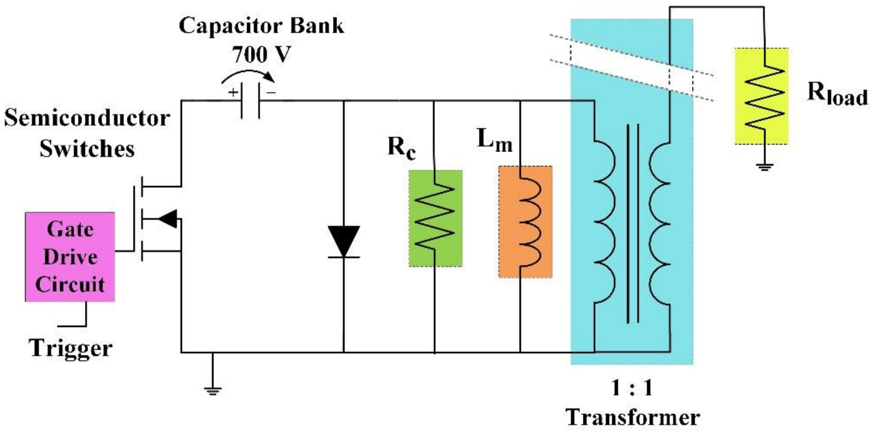
- The required absolute stability (in absolute numbers) was achieved for all damping ring kicker systems (≤ ±2.5 V). Hence, the pulse power modulators for the kicker systems for the CLIC damping rings are very probably feasible.
- The required relative stability (relative to the pulse voltage or current) was not reached for the DR extraction kicker systems (≤ ±0.02 %).
- The required resolution for the direct electrical measurement of the pulse waveform is very close to the limit of the measuremen set-up (Bergoz CT-E.01 current transformer & 8-bit Tektronix oscilloscope DPO 5034)
- Hardware limitations:
  - Maximum voltage up to 3.5 kV
  - Maximum pulse duration up to 350 ns flat-top at 700 V per layer (restricted by cross-sectional area of available magnetic cores)
  - 2 branches powered per layer (increased the amplitude of the droop to be compensated)
  - No amplifier between an RF power transistor and signal generator in the active analogue modulation layer (low gain)

Evaluation of Magnetic Core Material for 12.5 kV Prototypes

- Different core materials were evaluated for 12.5 kV prototypes with 3.5 kV prototype adders
- Based on measurements with 3.5 kV prototypes, the requirements for magnetic cores for inductive adders with extremely high flat-top stability are the following:
  - High magnetizing inductance L_m
  - Large linear flux swing of B-H loop (constant permeability)
  - Low remanent field (no biasing required)
  - Relatively low losses (high core loss resistance R_c)
  - Sufficient insulation between ribbon layers, to prevent break-downs with a high magnetization rate

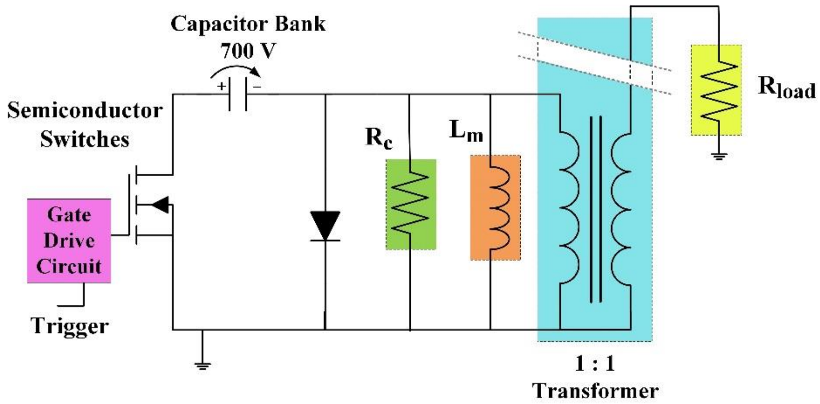


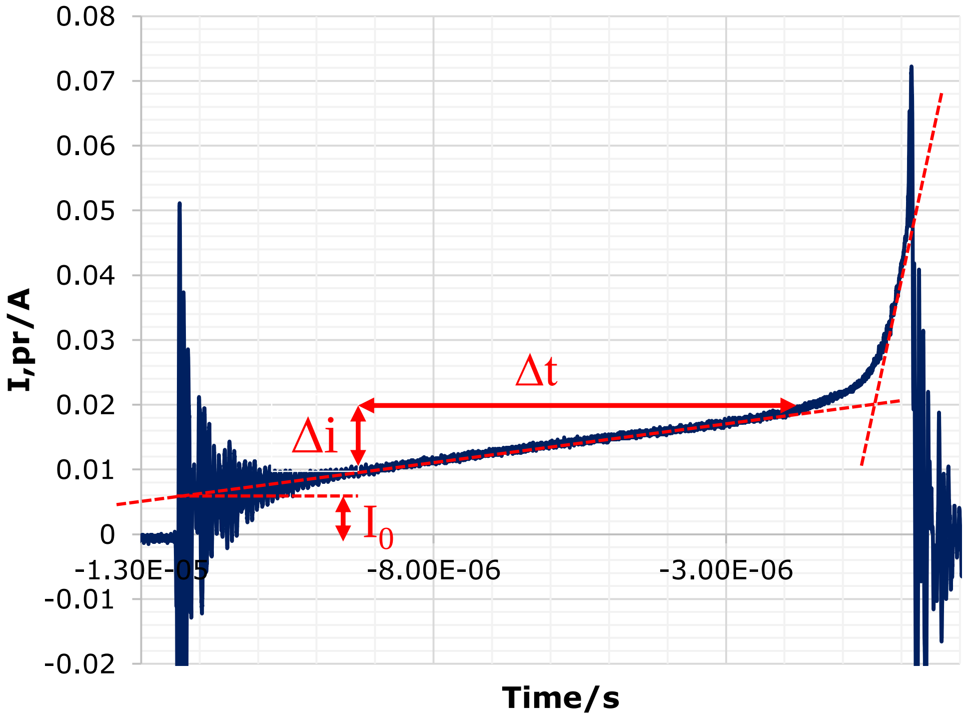
Examples of square-loop (black) and linear (blue) B-H curves

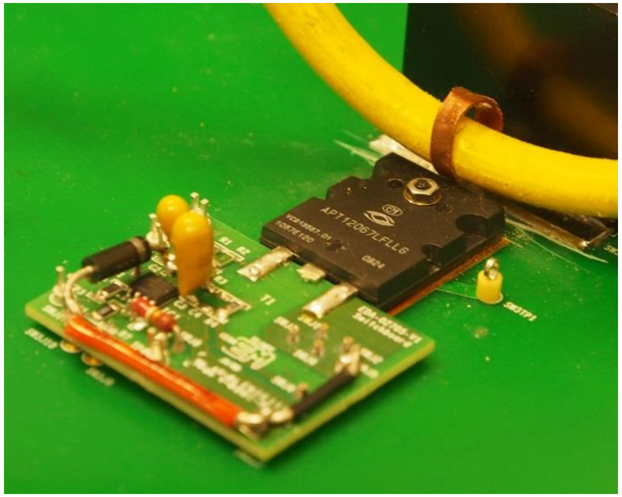


Evaluation of Magnetic Core Material for 12.5 kV Prototypes

- Core materials were evaluated by measuring primary current (***I,pr***) of a single layer with a Rogowski coil current transducer.
- Numerical estimates for R_c and L_m:
  - $R_c \approx V_{Rc} / I_0$
  - $L_m \approx (V_{Lm} \times \Delta t) / \Delta i_{Lm}$



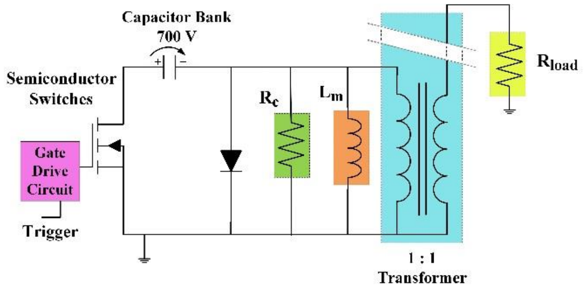


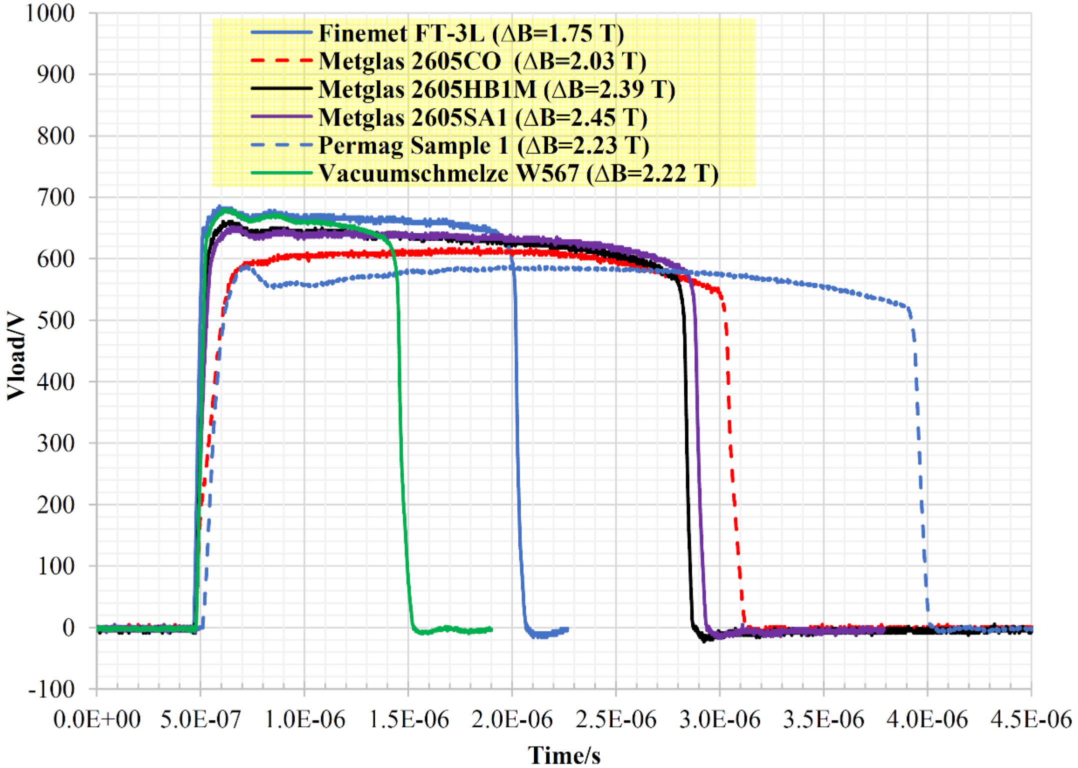


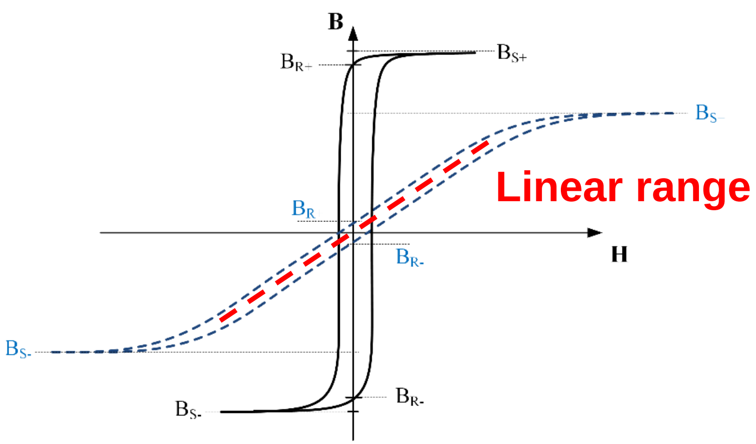
Measurement set-up for magnetizing current

Evaluation of Magnetic Core Material for 12.5 kV Prototypes – with Biasing

- Set-up for measurement:
  - Output voltage of an inductive adder with single layer powered (700 V)
  - Biasing (8 A, DC) applied, to use most of the flux swing range
- Biasing circuit (large inductor) causes ripple for the pulse flat-top and off-time voltage, which is not acceptable for CLIC DR kicker system.

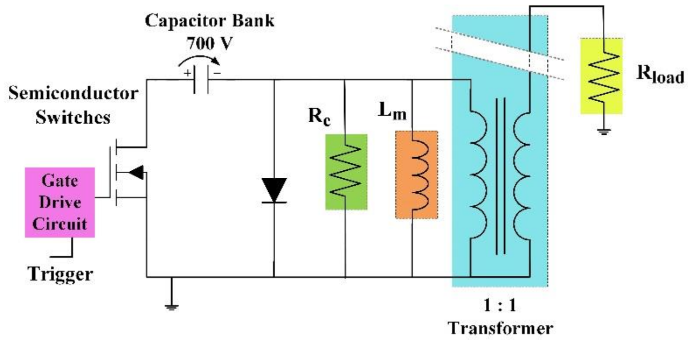


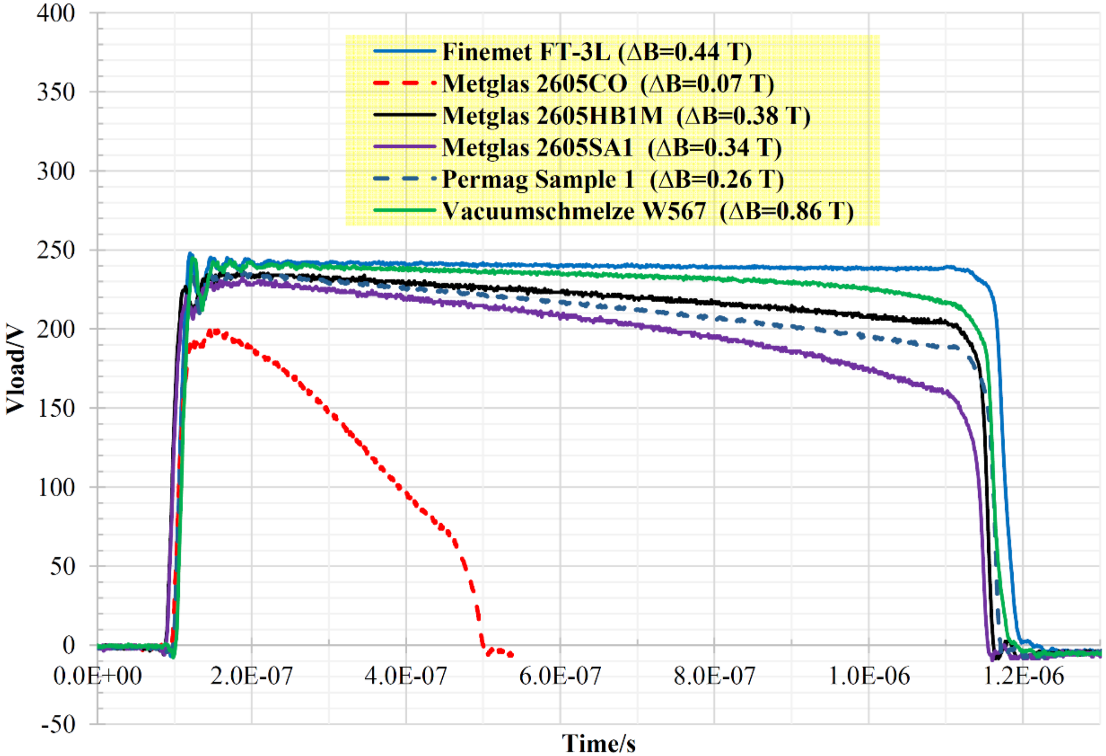




Evaluation of Magnetic Core Material for 12.5 kV Prototypes – No Biasing

- Setup for Measurement:
  - Output voltage of an inductive adder with a single layer powered (250 V)
  - No biasing applied
- Best candidates without biasing: Vacuumschmelze Vitroperm 500 F and Finemet FT-3L.
  - Lowest remanent field.
  - Lowest losses
- Limitations of Vacuumschmelze cores:
  - Not available in custom sizes and insulation
  - ”Standard” insulation between ribbon layers is not adequate for this application.
- **Finemet FT-3L chosen for 12.5 kV prototypes.**



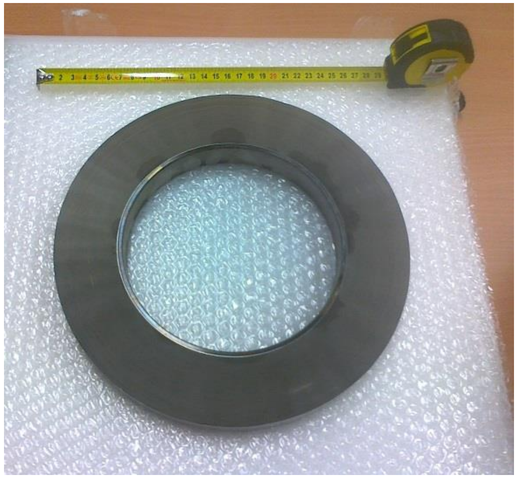


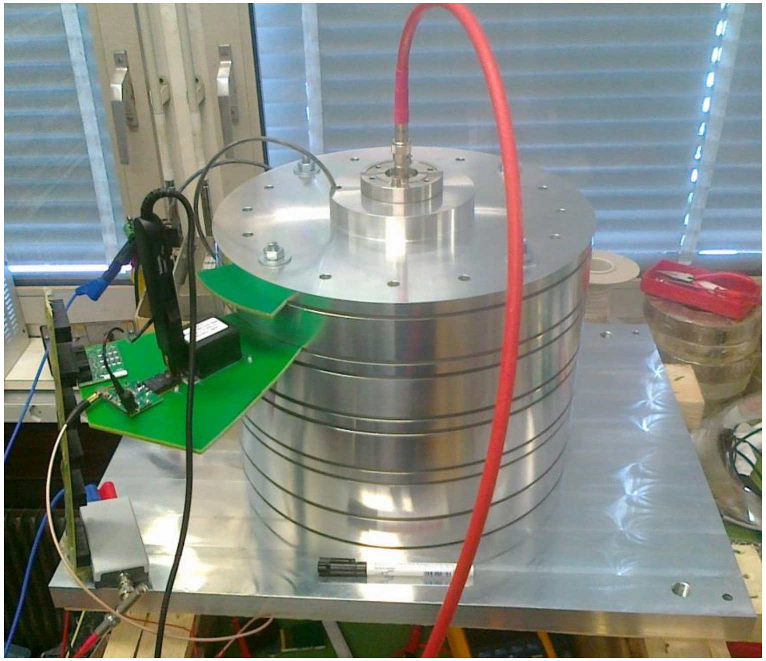
Evaluation of Magnetic Core Material for 12.5 kV Prototypes

Core	V_c (V)	I_b (A)	$I_{Lm,max}$ (A)	T_p (µs)	R_c (Ω)	L_m (µH) Max | Min	$\mu_r \times 10^3$ Max | Min
Finemet FT-3L	700	0	100	0.9	25.0	110 | 0.9	58 | 0.5
	700	8	100	1.7	25.1	40 | 1.9	21 | 1.0
Vacuumschmelze W567	700	0	100	0.6	25.3	4.9 | 0.8	4.8 | 0.8
	700	8	100	1.1	24.8	16| 1.4	16 | 1.4
Metglas 2605CO	700	1	100	3.3	6.2	n/a | 40	n/a | 17
	700	8	100	3.5	6.3	n/a | 39	n/a | 17
Metglas 2605HB1M	700	1	100	1.1	8.4	13 | 7.4	6.3 | 3.7
	700	8	100	2.4	8.6	29 | 10	15 | 5.0
Metglas 2605SA1	700	1	100	2.1	8.4	n/a | 5.2	n/a | 2.6
	700	8	100	2.6	8.3	36 | 3.3	18 | 1.6
Permag Sample 1	700	1	100	0.5	10.5	7.4 | 3.8	2.6 | 1.4
	700	8	100	3.8	10.6	n/a | 11	n/a | 3.9

Next Prototypes: 12.5 kV Inductive Adders

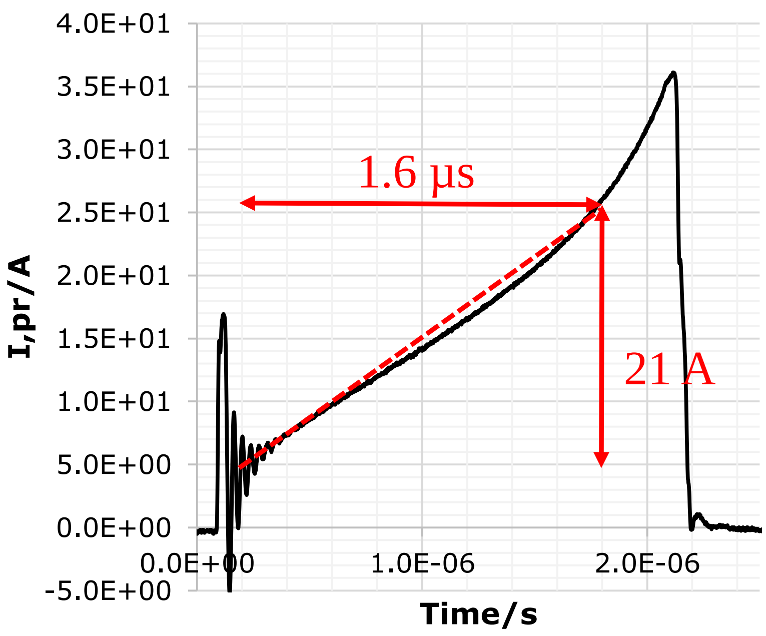
- The design for the first of two full-power, 12.5 kV, 250 A, inductive adders has been completed:
  - Air insulated, nominal output impedance 50 *Ω*
  - Mechanical parts for the first 5 cells (layers) received
  - 4 layers assembled for testing magnetic cores
  - Layout designs of PCBs finished (by Cern DEM) and the PCBs layouts have been sent to production (today!)
  - Magnetic cores (Hitachi Finemet FT-3L) ordered in 2015 and partly received (50 %)
- Hardware upgrades:
  - Maximum voltage up to 12.5 kV (20 layers)
  - Maximum pulse duration up to 1 µs flat-top at 700 V per layer (excluding rise/fall times and settling time of 100 ns)
  - RF amplifier (Tabor A10160) for feeding the RF power transistor in the active analogue modulation layer (1 A,peak, up to 45 MHz)
  - 8 branches per layer (soldering pads for 24 branches)
  - Fault detection and protection in the PCBs (short-circuit, saturation of a magnetic core)

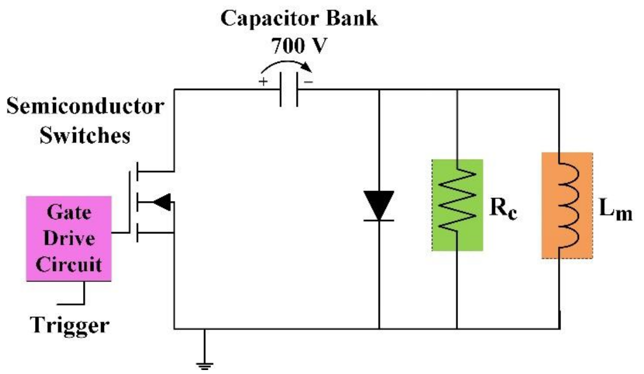




Initial Measurements on Magnetic Cores for 12.5 kV Prototypes

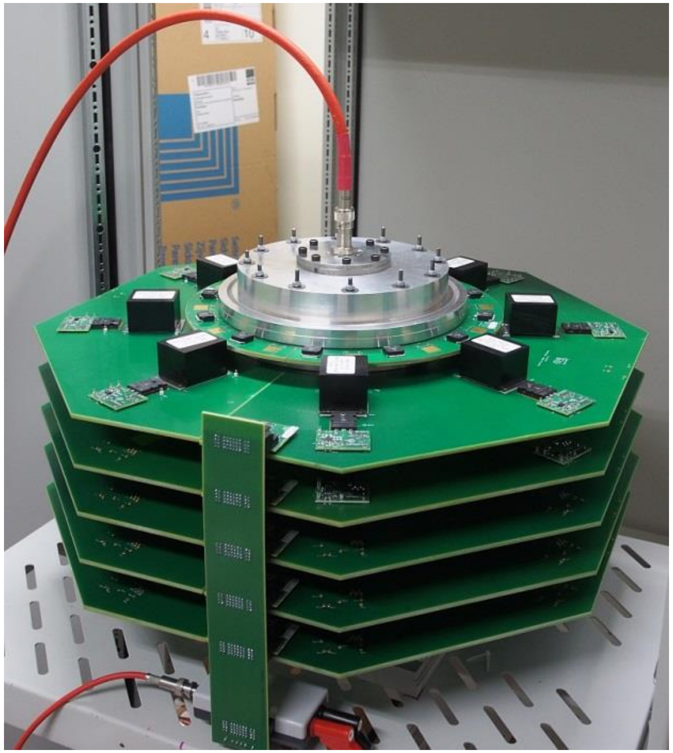
- First full-size Finemet FT-3L cores for the two 12.5 kV prototypes have been evaluated
- According to initial measurements, the cores fulfil the specifications:
  - 2 cores per layer, effective cross-sectional area in total at least 14.7 cm^2
  - Magnetizing inductance L_m ~ 50 µH for 1.6 µs at 700 V ($\mu_{r,core}$ ~ 35,000)
  - Core loss resistance $R_c > 140\ \Omega$
  - Maximum usable B-H flux swing ~0.9 T without biasing (from remnant field to the end of ”linear” part of the B-H curve)
  - ”Safe” pulse flat-top duration at least 1.1 µs (with ~100 % margin) at 700 V
- 12.5 kV prototypes can be used as a testbench for future projects at CERN (e.g. FCC):
  - Maximum pulse duration (at 700 V/layer) can be extended up to ~3 µs by biasing the magnetic cores (compromises the pulse flat-top stability)
  - Maximum current capability of primary PCBs can be extended up to a few kA by powering 24 branches (depending on the semiconductor switches)
  - Soldering pads for 1.6 kV Leclanche prototype pulse capacitors. In the previous designs, only 1.2 kV NWL capacitors used (from USA).





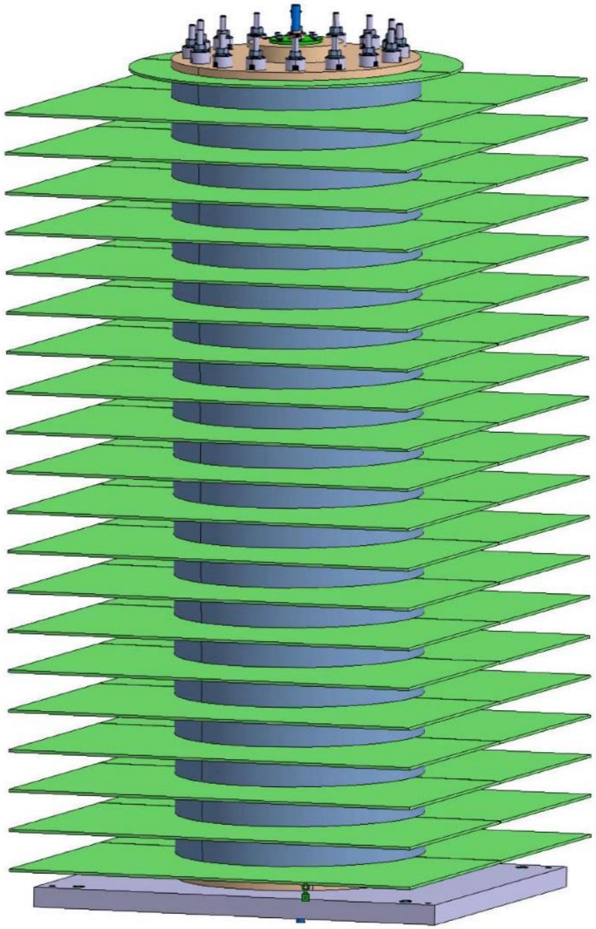
Summary

- Two 5-layer, 3.5 kV prototype inductive adders have been built and tested at CERN
- Both passive and active analogue modulation methods tested to improve the flat-top stability of the output pulses
- The best measured flat-top stability for 160 ns pulse flat-top has been ±0.05 % (±0.96 V) at 1.8 kV, which was reached by applying active droop and ripple compensation.
- **The pulse power modulators for CLIC DR kicker systems are very probably feasible with inductive adder technology.**
- The design of the first full-size, 12.5 kV, 250 A, CLIC DR kicker prototype inductive adder is being finished. The main components and mechanical parts have been received and PCBs have been ordered.
- The initial measurements have commenced with full-size inductive adder cells to evaluate the magnetic cores.
- The evaluated Finemet FT-3L for 12.5 kV prototypes cores fulfil the specifications.



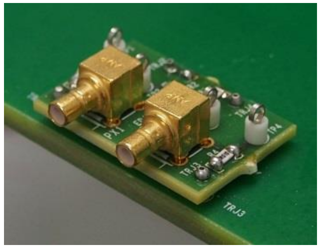
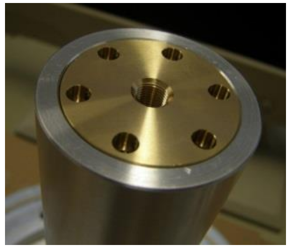
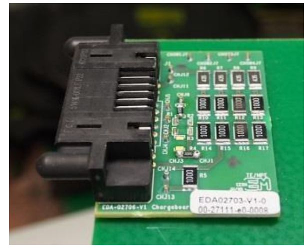
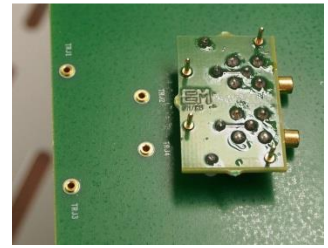
Future Work

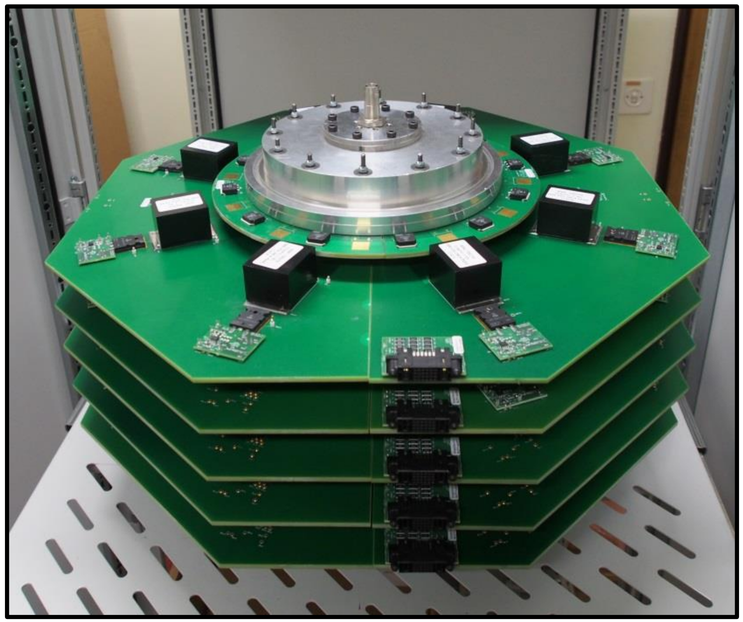
- Assembly and testing of the first 20-layer, 12.5 kV, 250 A, prototype inductive adder
- Improve the precision of the active analogue modulation, to meet ±0.02 % requirement for the combined droop and ripple:
  - Measurements with pulse flat-top duration up to 900 ns
  - Active analogue modulation layer with improved precision of ripple compensation (an RF amplifier between the RF MOSFET and a signal generator)
  - Measurements with a 16-bit oscilloscope
- Measurements of two 12.5 kV inductive adders with a stripline kicker installed in a beamline in an accelerator test facility
- Other possible applications for inductive adder technology at CERN:
  - FCC kicker systems (20 kV, 3.6 kA, 2.5 μs)
  - PS KFA kicker system (40 kV, 1.5 kA, 2.6 μs)

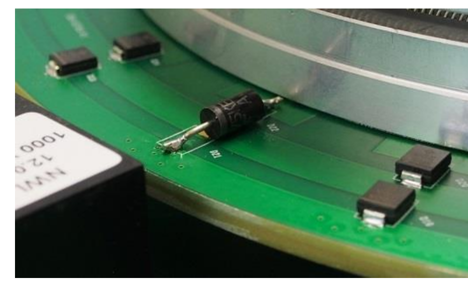
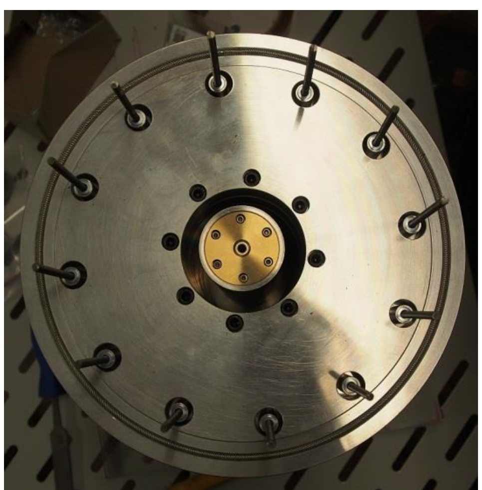


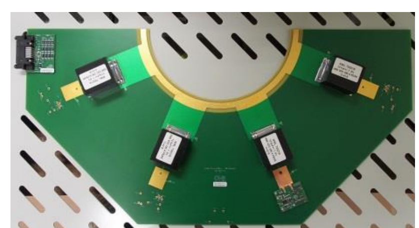
3D model of a 20-layer inductive adder at CERN (Courtesy of P. Faure)

Questions & Comments?

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3. Holma J., Barnes M.J., Belver-Aguilar C.: ”Measurements on a Prototype Inductive Adders with Ultra-flat-top Output Pulses for CLIC Kicker Systems”, Proc. IPAC’14, Dresden, Germany, June 15-20, 2014.

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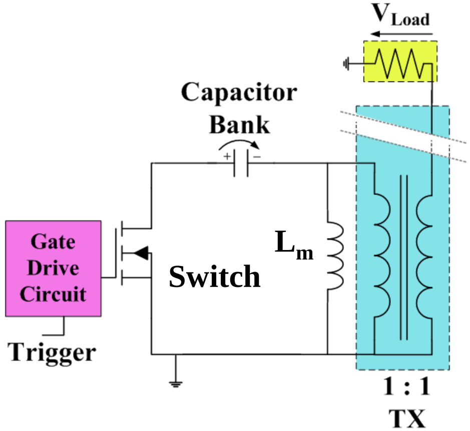
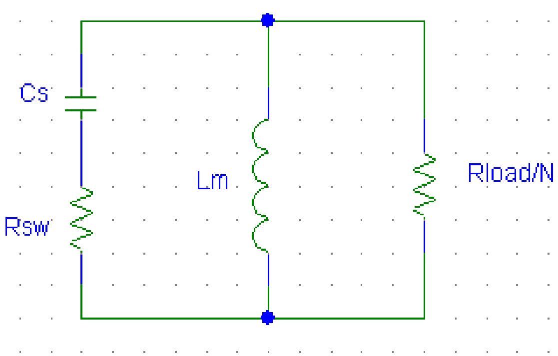
Spare Slides

Contributors to the Droop of the Output Waveform of an Inductive Adder

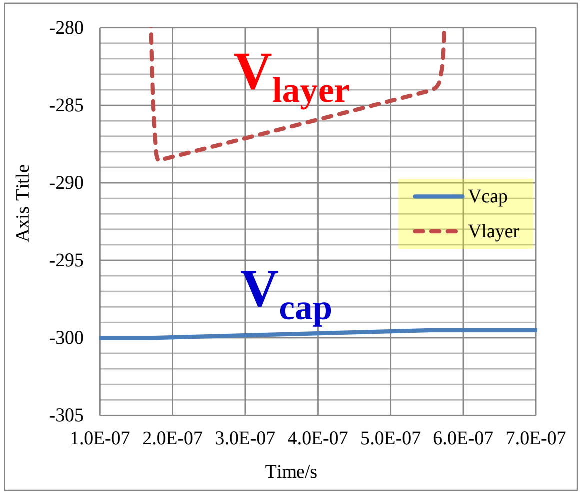
- The droop of the output pulse of an inductive adder is caused by:
  - The small voltage droop of the storage capacitor (**C_s**) as it supplies charge during the pulse
  - The resistive losses in the primary switch and in the primary circuit (**R_{sw}**), which depends on the current through the magnetizing inductance (**L_m**).
- **Only the voltage droop of the capacitors can be compensated by adding more capacitance per layer!**
- **The only methods to effectively decrease the droop, caused by a combination of resistive losses and magnetizing inductance of the transformer core, is to apply either passive or active analogue modulation (or both) for the output pulse.**
- **These methods are necessary to reach very low droop (<< 1 %).**



Simplified schematic of a constant voltage layer of an inductive adder



Simplified model of a layer of an inductive adder during the pulse



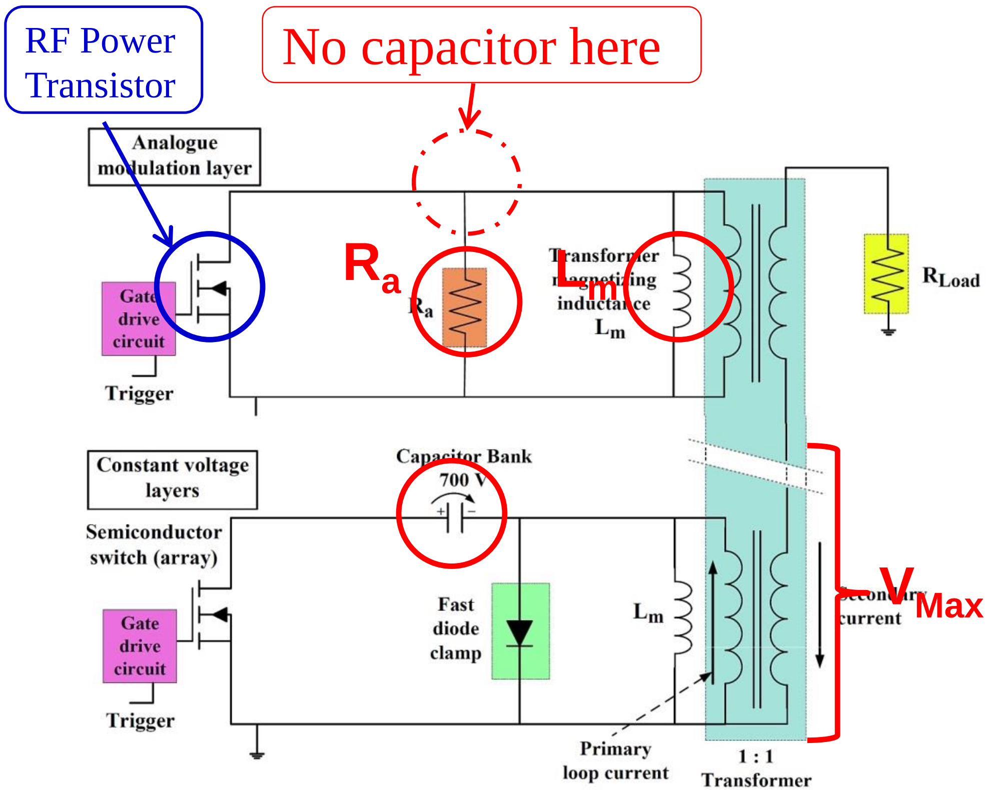
Capacitor voltage V_{cap} and voltage of a layer V_{layer} during a pulse. C_s = 24 uF, Rsw = 0.34 Ω and R_{load}/N = 10 Ω.

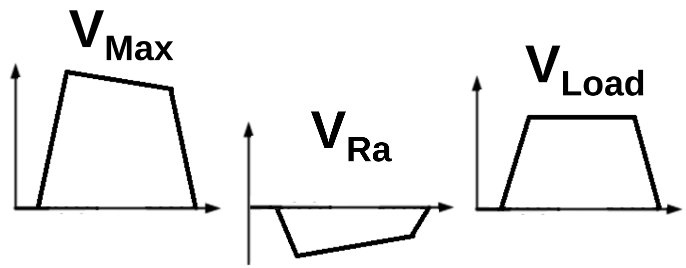
Compensation of Droop and Ripple

- In analogue modulation layer, there is no storage capacitor but there is resistor R_a
- Resistor R_a is effectively in series with the load
- Load voltage during the flat-top:

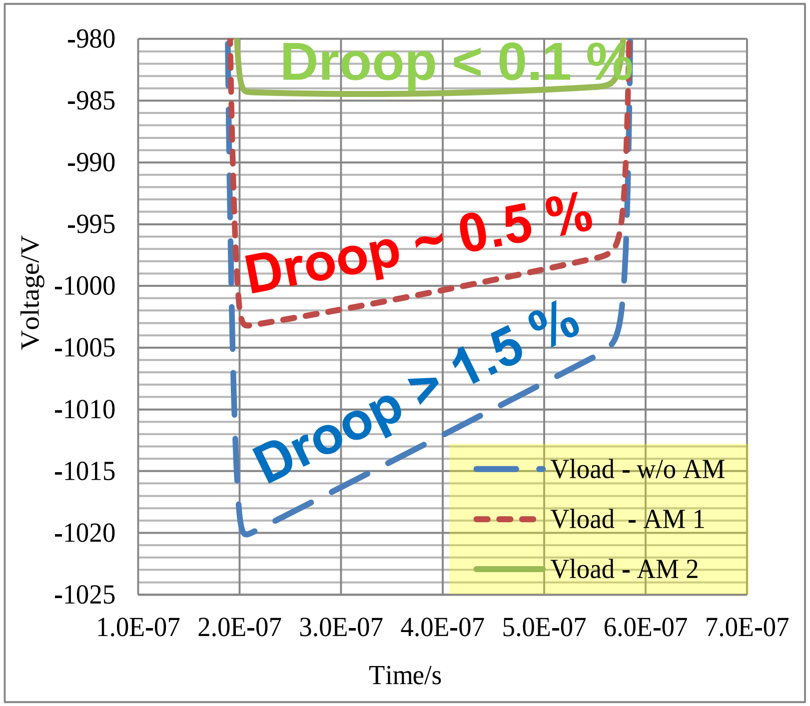
$$V_{Load} \approx \frac{R_{Load}}{R_{Load} + R_a} V_{Max}$$

- $\mathbf{V_{Max}}$ is the sum of the voltages over the layers except the analogue modulation layer: $\mathbf{V_{Load} \leq V_{Max}}$**!**
- Resistor R_a is in parallel with magnetizing inductance L_m
- Compensation modes:
  - **PASSIVE MODE**: During the pulse, current through L_m increases, which causes current through R_a to decrease. Therefore, voltage over R_a decreases, which causes V_{Load} to increase. This voltage change is reverse in comparison with voltage droop caused by storage capacictors in other layers.
  - **ACTIVE MODE:** A linear RF power transistor provides a shunt path for the current through resistor R_a. Therefore, the voltage over R_a can be controlled by controlling the current through the RF power transistor.

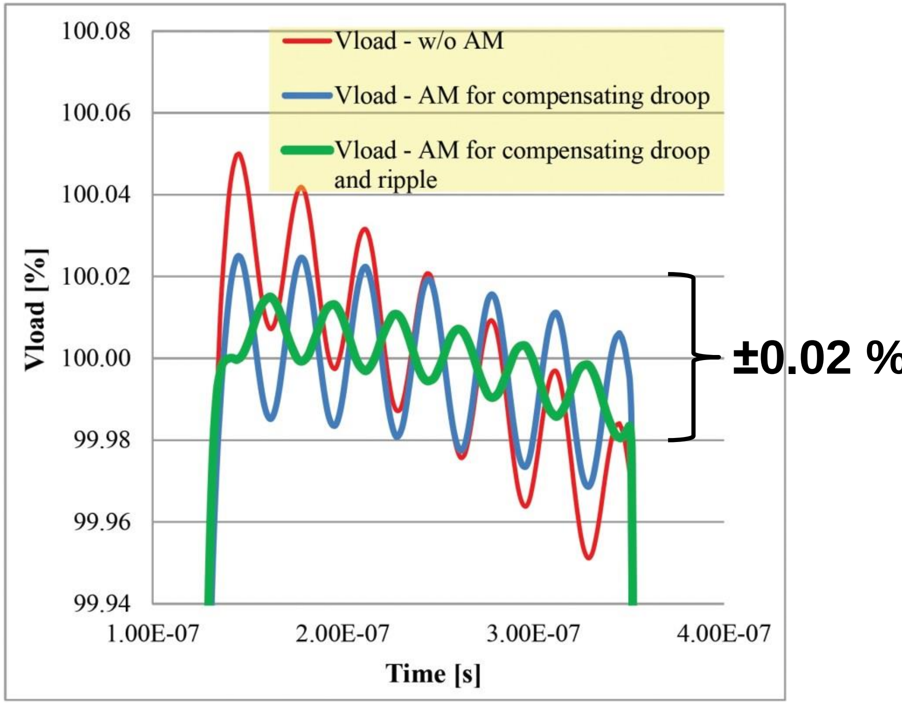




Compensation of Droop and Ripple



Simulated droop compensation with passive analogue modulation

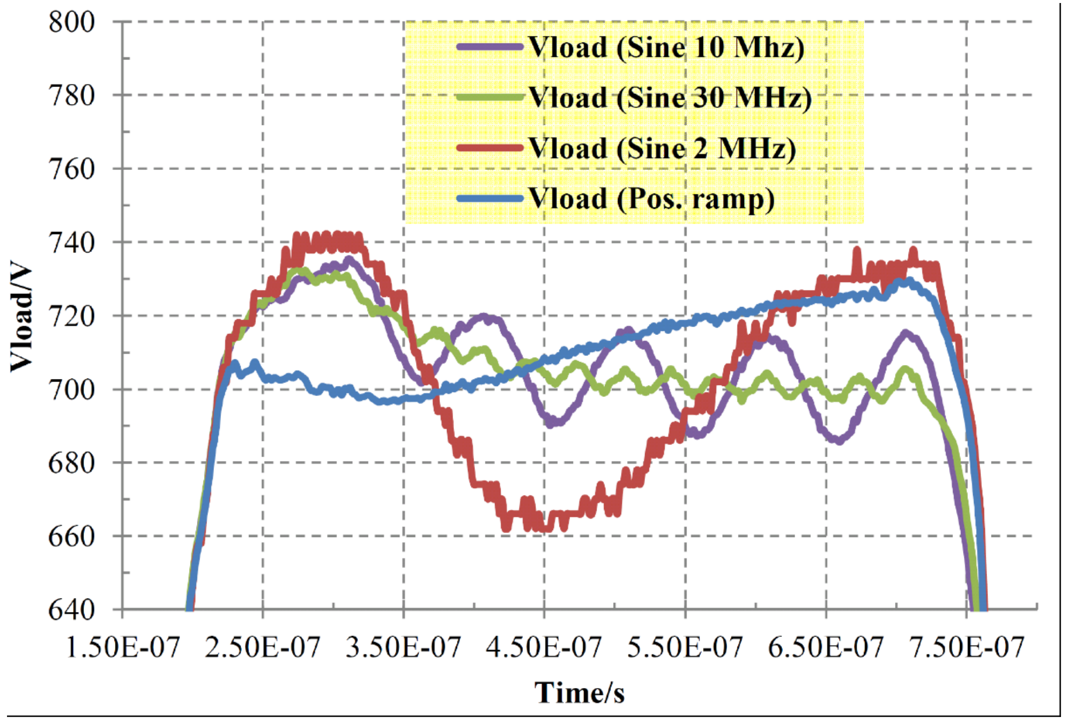


Simulated droop and ripple compensation with active analogue modulation

- **Passive analogue modulation – partial droop compensation**
- **Active analogue modulation – partial droop and ripple compensation**

➢ **For the CLIC DR kicker modulator, both PASSIVE and ACTIVE modulation methods will be applied!**

Measurements: Active Ripple Generation



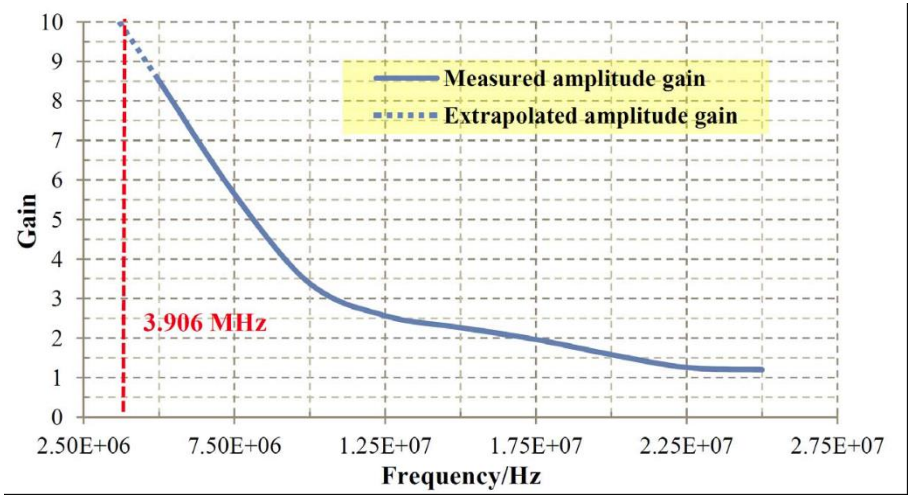
- **Setup for the measurement:**
  - 4 constant voltage layers and a passive analogue modulation layer
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) initially charged to 200 V (R_a = 7.9 Ω)
  - Active ripple generation with **a positive ramp (blue)** and **2 MHz (red)**, **10 MHz (purple)** and **30 MHz (green)** sine waves.

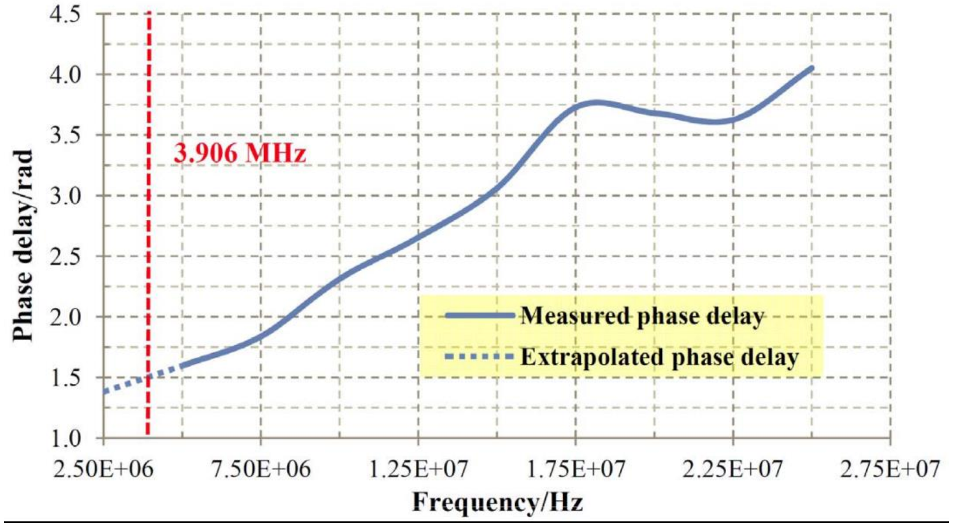
Note:

- **Modulation range: ~10 % of the maximum output voltage**

Measurements: Active Ripple Compensation

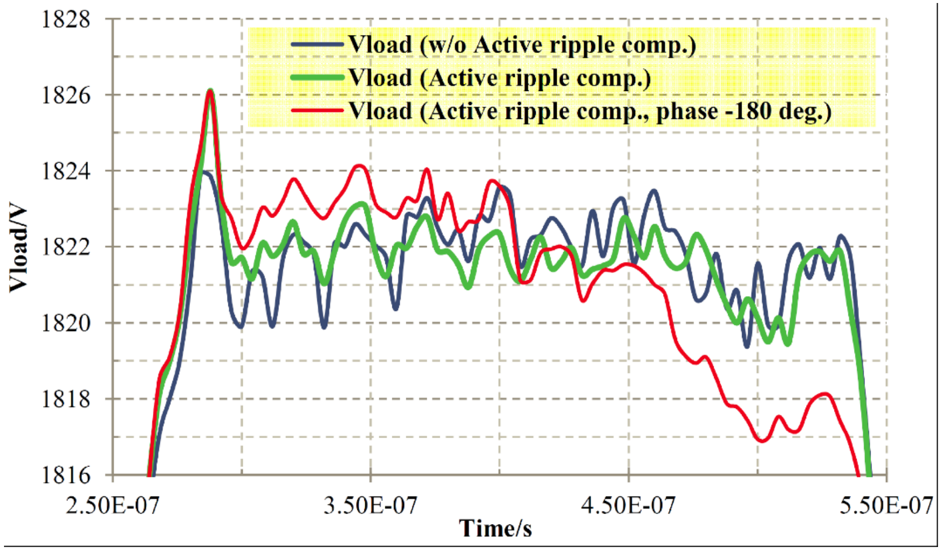
- **Setup for the measurement:**
  - The prototype adder with 5 layers
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) charged initially to 551 V
  - Active analogue modulation layer
  - Modulation signal: a ramp + a sine wave with a frequency of 5...25 MHz.
- **Steps for active ripple compensation**
  - Gain and phase responses for the injected compensation signal from the signal generator to the load voltage were measured
  - Correction factor were defined for compensation signal
  - Load voltage was measured
  - Fast Fourier Transformor (FFT) was applied to define the most significant ripple components
  - A compensation signal, consisting of ramp to compensate the droop and a a sine wave to compensate the most significant ripple component was created.
  - The compensation signal was applied and the load voltage was measured.

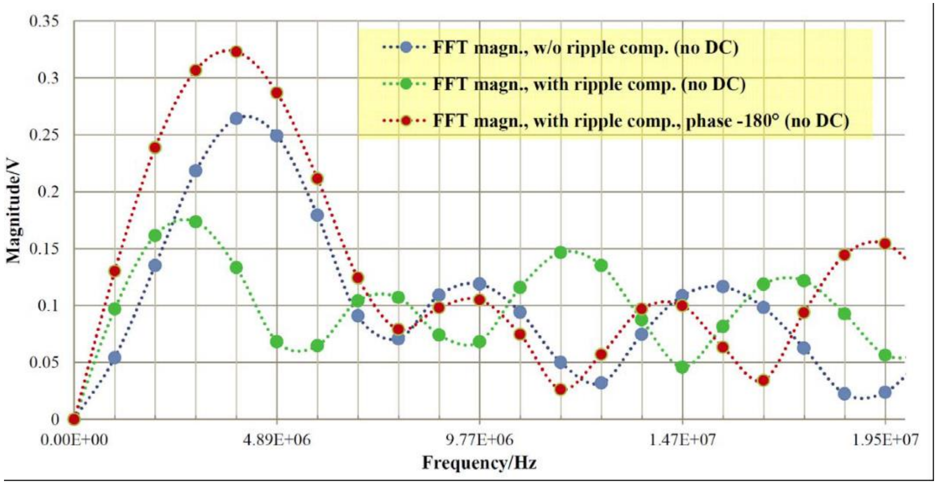




Demonstration of Active Ripple Compensation in Time and Frequency Domains

- **Time domain**
  - Original waveform: load voltage with ramp compensation applied (blue)
  - Compensated waveform (green): the droop and the most significant ripple frequency has been compensated
  - A ripple component deliberately amplified (red): the most significant ripple component has been amplified (phase shift of the ripple component -180 degrees in comparison with the green curve)
- **Frequency domain**
  - Magnitudes of FFTs of the original load voltage (blue), ripple compensation applied (green) and a ripple component amplified (red).
  - FFT of original waveform: load voltage with ramp compensation applied (blue)
  - FFT of compensated waveform (green): the droop and the most significant ripple frequency has been compensated
  - FFT of a the waveform in which a ripple component has been amplified (red): phase shift of a ripple component -180 degrees in comparison with the green curve





Evaluation of Accuracy of the Measurements

- **The effective bit length of a 8-bit ADC is 6-7 bits.**
- **The effective bith length of the oscilloscope can be increased with the following means**
  - Oversampling (OS)
  - Ensemble averaging (EA)
  - **Both these methods were applied**
- **Accuracy of the measurements**
  - **Active droop compensation:**
    - The best measurements: **±0.06 % (± 1.17 V)**
    - The effective number of bits of the ADC: **6** (effective length of bits) + **1** (OS,4x) + **6** (EA,4k) = **13**
    - Absolute precision: **0.37 V** (in the range of 3 kV)
  - **Active droop and ripple compensation:**
    - The best measurements :**±0.05 % (± 0.96 V)**
    - The effective number of bits: **6** + **1** (OS,4x) + **5** (EA,1k) = **12**
    - Absolute precision: **0.73 V** (in range of 3 kV).
    - With EA of 4k, the numbers were ±0.06 % (± 1.02 V), 13 bits and 0.37 V.

Mod. method	PM (d)	AM (d)	AM (d&r)
ΔU_{d+r} (%)	±0.16	**±0.07 (1k)** **±0.06 (4k)**	**±0.05 (1k)** **±0.06 (4k)**
ΔU_{d+r} (V)	±1.9	**±1.23 (1k)** **±1.17 (4k)**	**±0.96 (1k)** **±1.02 (4k)**
$Res_{Enh,OS}$ (bits)	0	1 1	1 1
Averaging (n)	100	1000 4000	1000 4000
$Res_{Enh,EA}$ (bits)	3.3	5 (1k) 6 (4k)	5 (1k) 6 (4k)
$V_{r,ADC}$ (V)	2000	3000 (1k) 3000 (4k)	3000 (1k) 3000 (1k)
Res_{Rel} (%)	0.16	0.024 (1k) 0.012 (4k)	0.024 (1k) 0.012 (4k)
Res_{Abs} (V)	3.2	**0.73** **0.37**	**0.73** **0.37**

ΔU_{d+r} = combined droop and ripple (flat-top instability), $Res_{Enh,OS}$ = resolution enhancement by oversampling (averaging of samples), $Res_{Enh,EA}$ = resolution enhancement by ensemble averaging (averaging of pulses), V_r = voltage range of a measurement channel, Res_{Rel} = relative accuracy, Res_{Abs} = absolute accuracy