CTF3 Phase Feed-forward Amplifier:
Experience, Issues and Prospects

C.Perry - Oxford/JAI

18 Jan 2016

Concept

- proposal for a CTF3 phase feed-forward amplifier was made around Sep 2011
- based on the new SiC FETs - at that time:

'commercial devices are reaching mainstream availability'

- aim to achieve useful power from a manageably simple system
- target 20kW peak per amplifier module (+/-700V to each side of a 100 ohm kicker)
- combining 4 modules would get 80kW (double the voltage)

- this would be a factor of 4 up from what looked possible with Si MOSFETS
- and a factor of 10 from a conservative Si MOSFET design

Problems

- power FETs not generally designed or specified for fast linear use
    - all intended for switching use (even RF types)
    - the occasional linear uses are normally slow (eg audio)
- all have very high transconductance
    - convenient, but very liable to cause instability
- the SiC parts are not available in 'RF' packages
    - packages have high lead inductances: ~10nH vs ~1nH for RF packages
    - impairs high frequency response, and aggravates instability
    - manufacturers are concentrating entirely on motor drive/power conversion markets
    - the Siemens/Infineon work with RF parts *c.2010* has not led to commercialization

Limitations:
- allowable output at high frequencies can be reduced
    - voltages across device gate resistance risks gate breakdown
    - improving in newer devices
- transient thermal effects reduce peak power as'on' time extends beyond ~2us
    - not required for CTF3
    - getting *worse*(!) in newer devices (as they reduced die size)

==> Building fast, broadband linear amplifiers with power FETs is not standard practice, is rather uncertain, and is subject to intractable instabilities

It is always going to be somewhat experimental, especially as they are pushed towards their limits

CTF3 requirements

In 2011 phase measurement showed (all at 12GHz):
- large amplitude slow components, under 3MHz, about 60 deg pk to pk
    - with additional fluctuations shot to shot
- oscillatory 'ripples' of ~20MHz, 15 deg pk to pk
- broadband noise to a higher frequency, but at low level

- correction was given as 20 deg for 1mrad, from 2.8kV differential into 100ohm kicker

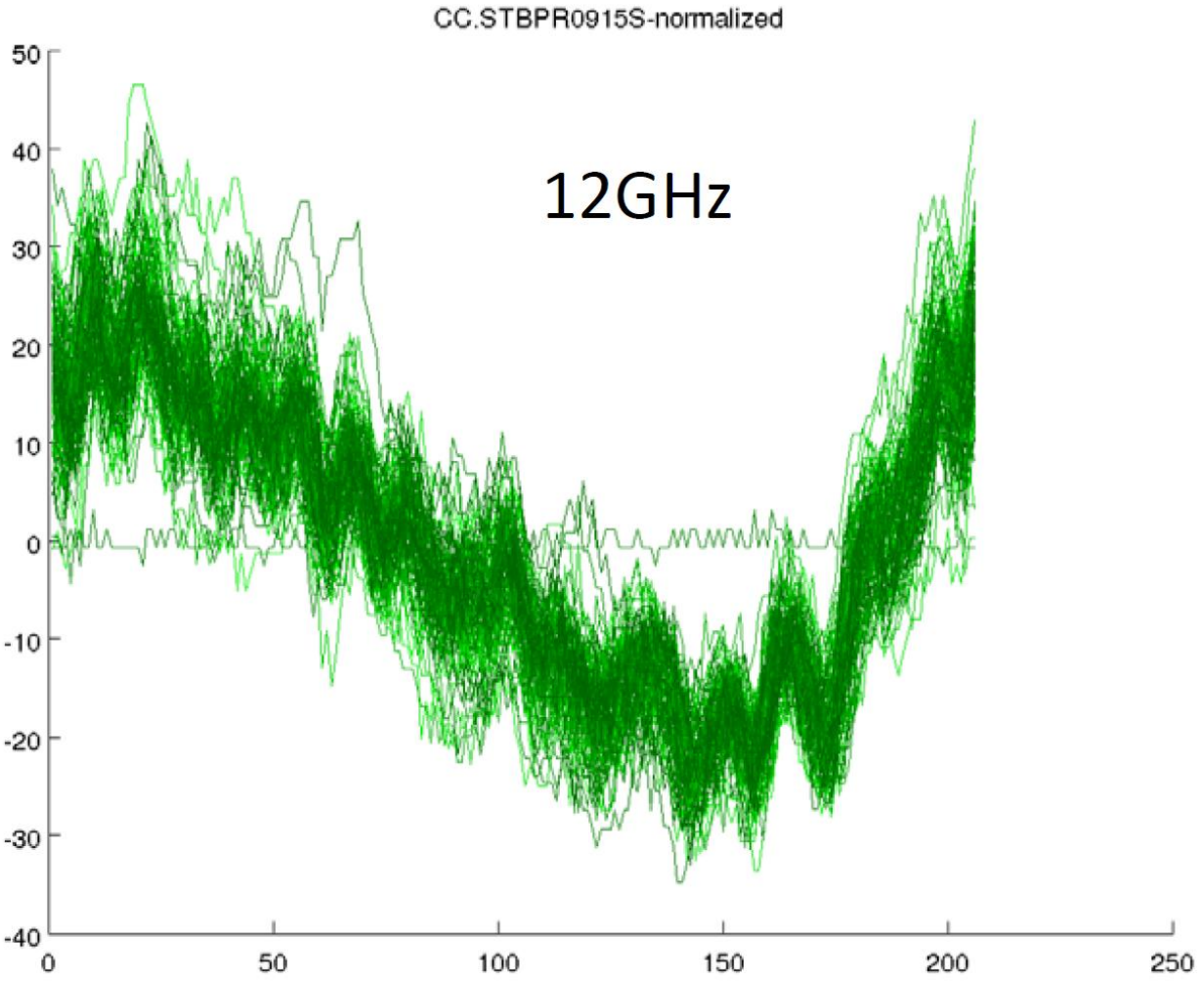
- assumed it would get better as machine was tuned for phase performance...

Target was:
- +/-1400V differential, ie +/-700V each side (or 20kW peak)
- > 1/4 of that drive available at 20MHz
- bandwidth at lower drive to be > 40MHz
    - aiming for 60MHz (CLIC nominal requirement)
- full drive for > 1.3us duration

Latency was not explicitly considered:
- does not directly affect system performance
- machine layout is the governing factor
    - neither CTF3 nor CLIC proposal needed low latency
- wide bandwidth normally gives low latency
    - ~ 1 or 2 cycles at high frequency limit

the sort of phase data we had in 2011....

(from Emmanouil Ikarios)



System Design

- partitioned between control module and amplifier module
    - amplifier module has just the high-level circuitry and essential support
    - control module has signal processing, timing, and power supply
        - can support 2 or 4 amplifier modules

- single amplifier module configuration (for two kickers):
    - 3U subrack
    - 1 control module
    - 2 amplifier modules
    - 1 2:1 custom drive cable assembly
    - 2 terminator modules
    - external 24V 'lump in the cord' power supply (~50W)

- combined amplifier module configuration would be (for each kicker):
    - 3U subrack
    - 1 control module
    - 4 amplifier modules
    - 1 4:1 custom drive cable assembly
    - 1 combining module
    - 1 terminator module mounted separately
    - external 24V power supply (~75W)

single module system....

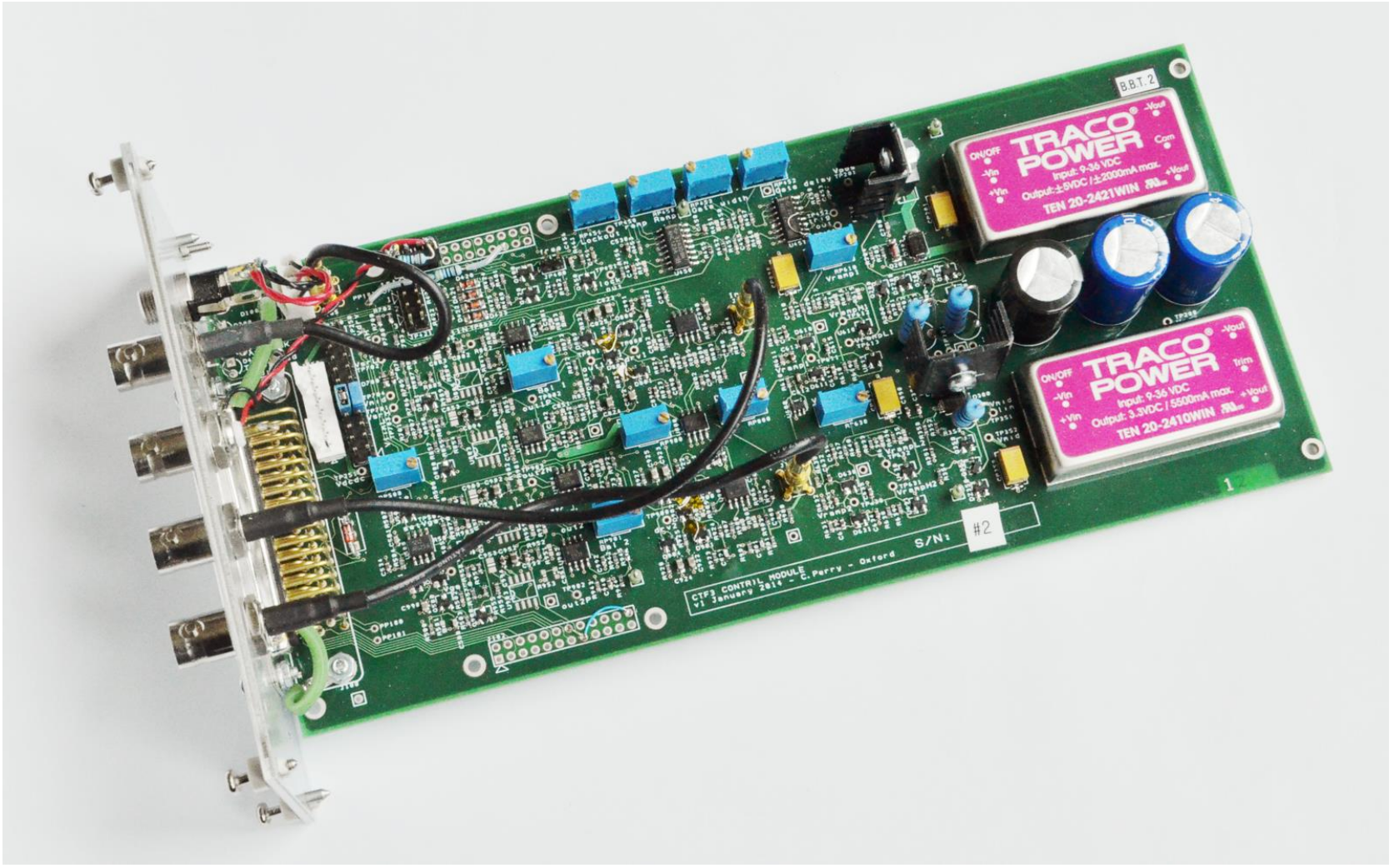
Early days - no panel labelling!

amplifer module....

First assembly of Version 1

... and control module

Much simpler - nothing on the back!



Control Module

Control module provides:

- power rails
  - 22V, 8.5V, -3.3V

- timing
  - ramping on and off (version 1: 3.0us; version 2: 1.0us)
  - on duration (version 1: 4.6us; version 2: 1.6us)
  - active signal duration (version 1: 3.2us; version 2: 1.3us)
  - lockout to prevent excessively rapid triggering

- fault protection: blocks triggering if an amplifier module reports problems

- signal conditioning
  - limiting to maximum acceptable drive
  - limiting slew rate
  - conversion to differential drive to amplifier module
  - adding the common-mode ramping voltage

- support for multiple amplifier modules
  - 2 amplifier modules used for separate drive signals
    - timing is common to both modules (offset needed between channels is small)
  - 4 amplifier modules used for the same drive signal

Amplifier Module

- mechanical:
    - single 220x100mm pcb housed in 220 deep 3U 60mm wide extruded module case
- power supply:
    - runs off 24V (and derived low voltages) from control module
    - total power ~15W
    - output stage runs off ~550V
        - generated locally by 6W DC/DC converter on pcb
        - power during pulse supplied by 10uF of capacitance
    - output bias voltages are generated from the hv rail
- signal input:
    - separate antiphase inputs to the 2 sides
    - both are ramped up together from 0 to 1V to turn on the output stage
        - no separate control signal is used
- input section:
    - boost inputs to suit the driver stages
    - provide trim for gains and offset to set operating point and balance amplifier
    - protects against excessive amplifier on-time under fault conditions
- driver stage:
    - needs wide swing, low output impedance
    - 10 TI THS3061 op-amps off 27V drive each side (partial fit in version 1)

Amplifer Module: Output Stage

- linear class-A push-pull into a transformer

- each side a cascode of a low voltage Si FET driving a high voltage SiC FET
    - reason: high parasitic inductances of (non-RF) SiC package
    - this prevents adequate high frequency response from a simple common-source stage
    - in cascode fast (but low voltage) Si FET forces current through the upper SiC FET

- Si MOSFET Ixys (formerly Directed Energy Inc) DE150-201N09A
    - 200V, 100W class device, rated to 54A pulsed current (see below...)
    - low inductance RF package
    - version 2: used as parallel pairs

- SiC MOSFET from Cree (now Wolfspeed...)
    - version 1: CMF10120D
        - 1200V, 100W class device, rated to 50A pulsed current
    - version 2: C2M01600120D
        - 1200V, 100W class device, rated to 40A pulsed current
        - used as parallel pairs
        - next generation part: faster, lower gate resistance
    - both in standard TO-247 leaded package

Amplifier Module: Transformer

- simple transmission line transformer

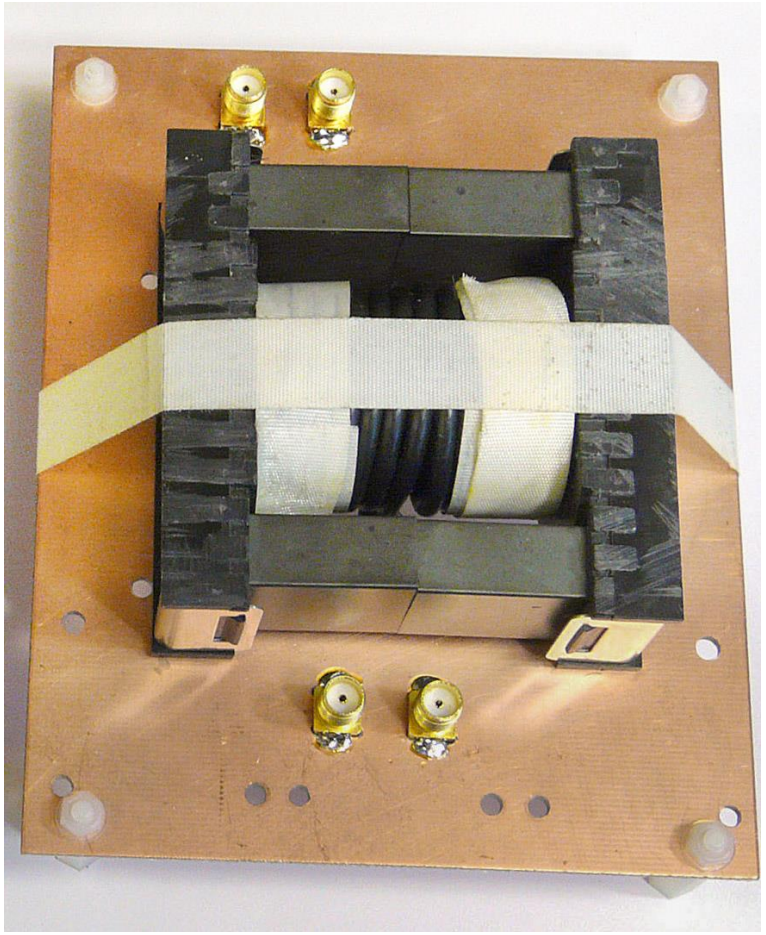
- two winding each of ~60cm of RG405 size insulated 50 ohm conformable coax
    - a balance of size, voltage rating, and losses
    - ...and ease of termination without melting insulation!
- ferrite core of MnZn (low frequency) ferrite, permeability ~4000
    - determines low frequency response of a TL transformer, but not high
- pcb designed for a pair of 'E' type cores (ETD59)
    - allows a toroidal core to be used as alternative

- each side of amplifier swings +/350V
    - a winding connects between the two sides
    - it shifts the balanced +/-700 input to +/-700V relative to ground
    - second winding is connected in parallel
    - wired to give a second output, but in opposite phase
- the +/-350V +/-28A at each input becomes +/-700V +/-14A at each output
    - each output drives 50 ohm load (1.4kV peak across 100 ohm differential = 20kW)

- transformer is simple and gives very good HF response (limit is winding losses), but...
    - no DC isolation: needs blocking capacitors on the outputs
    - not particularly low impedances to common-mode inputs (leading to stability issues)

prototype transformers....

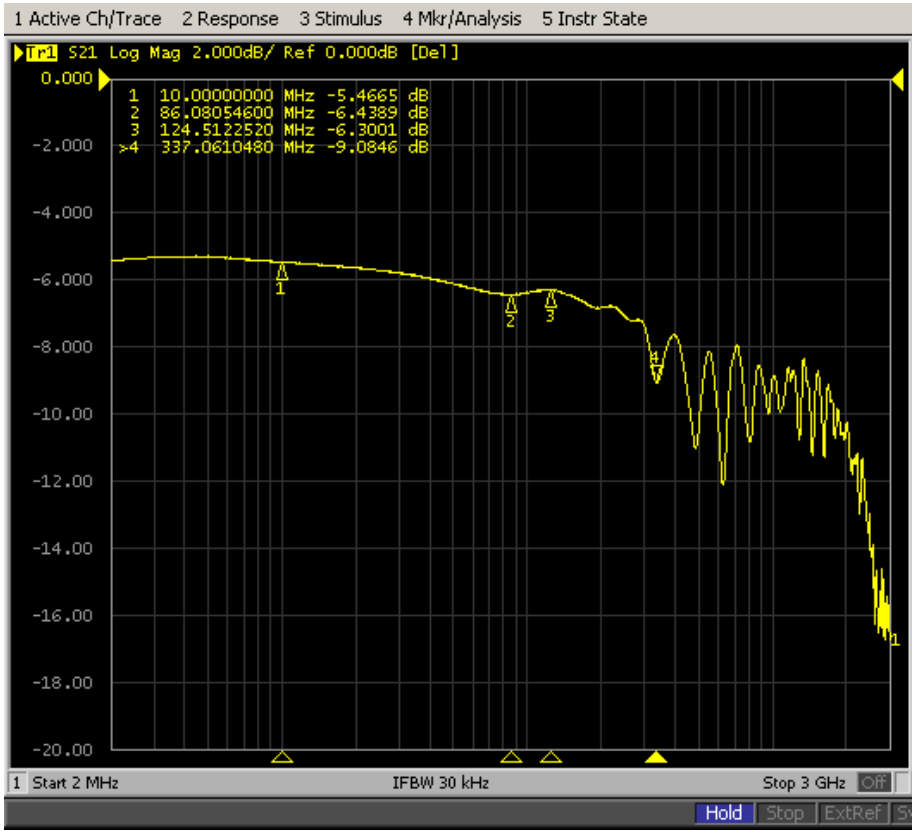
E-core - as used Version 1



Toroidal - as used Version 2

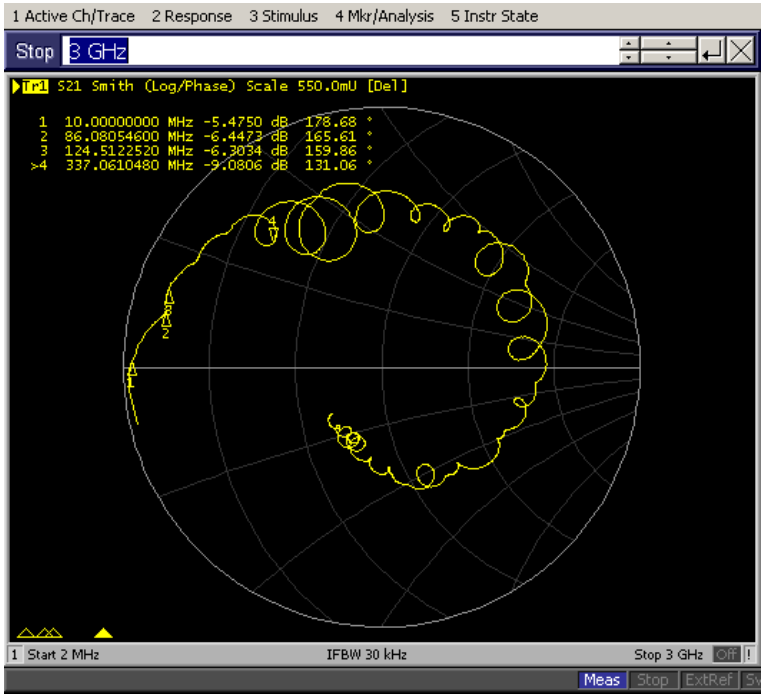
E-core transformer...

OK to 300MHz...



(first dip at 337MHz)

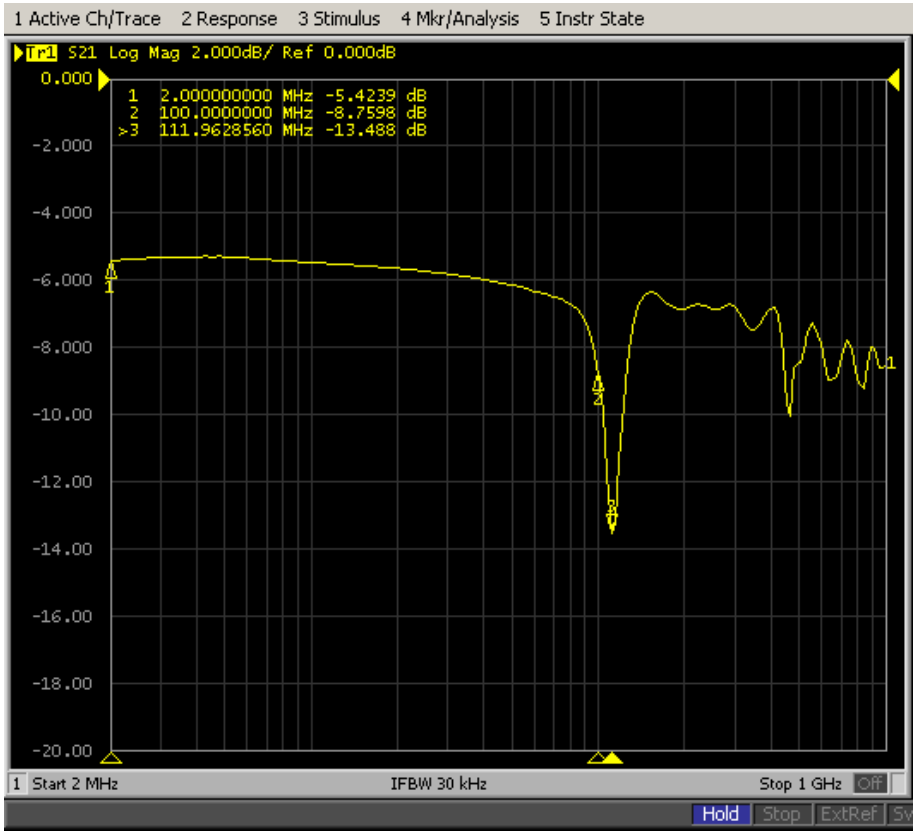
... with a pretty Smith Chart!



... and with interleaved winding

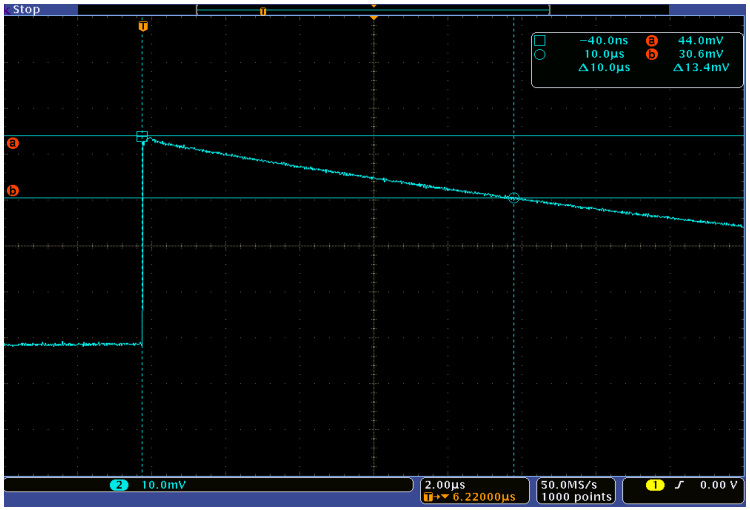
- *To reduce common-mode inductance*
  - *no undue harmful effects*
- *Used in Version 2 but on toroid*

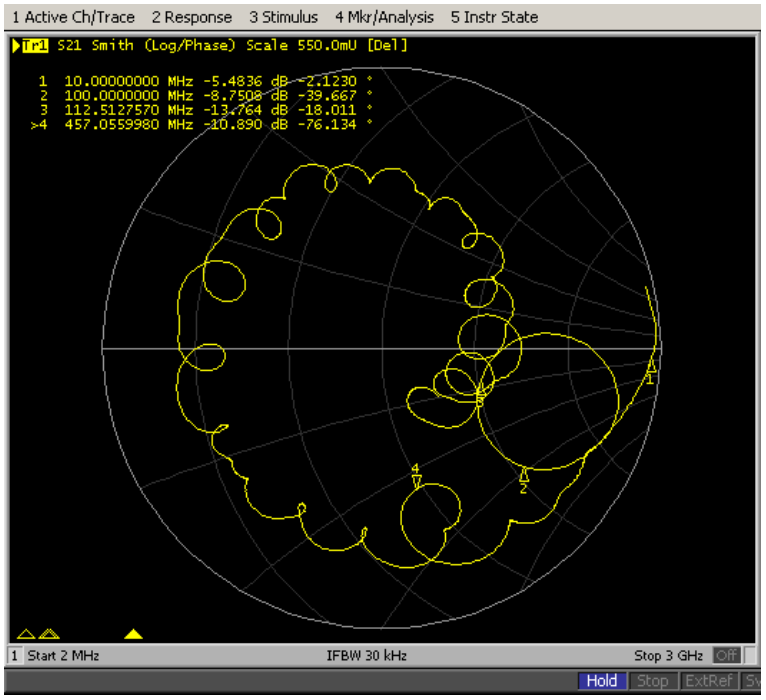
Still OK to 100MHz...



(deep dip at 112 MHz)

Check that droop is ok (3%/us)





... a not so pretty Smith Chart!

Minor Hardware

Terminators:

- 50 ohm terminators able to take the maximum system output energy: 20kW for 1.3us
- monitoring output at about -40dB
- good to 180MHz (S11 < -20db)
- dual units (ie one unit terminates both cables from a kicker)
- mount in 3U subrack

Connnection between modules:

- custom 'Y' harness with D connectors
- 2 short 75 coaxial signal cables in each branch
- plus power and monitor wiring

Kicker Connections:

- TNC (like BNC, but threaded) on amplifier modules
  - compact, secure & adequate voltage rating for 1 module
  - a 4:1 combiner module would have been 8xTNC in, 2xN out
  - for single amplifier module, use with adapter to N
- N on kicker cables and terminators
  - robust and adequate voltage rating for 4 modules combined

First Version

Built as designed, with 'E core' transformer and single FETs.

System performance:

- output: ~+/-350V

- risetime/bw: 8ns/45MHz small signal (to 20% max output)

- slew rate: for half max output: ~15ns (10% to 90%)
  for max output: ~40ns (10% to 90%)

- droop: 6% over 1.3us

Latency was not checked

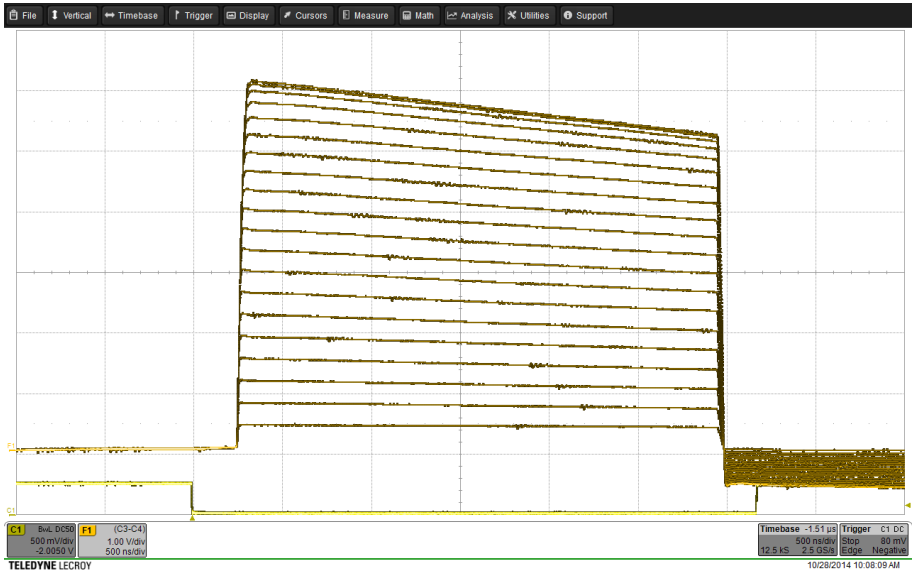
There is hardware droop correction, but it was not enabled

version 1 response....

Driven by control module...to saturation

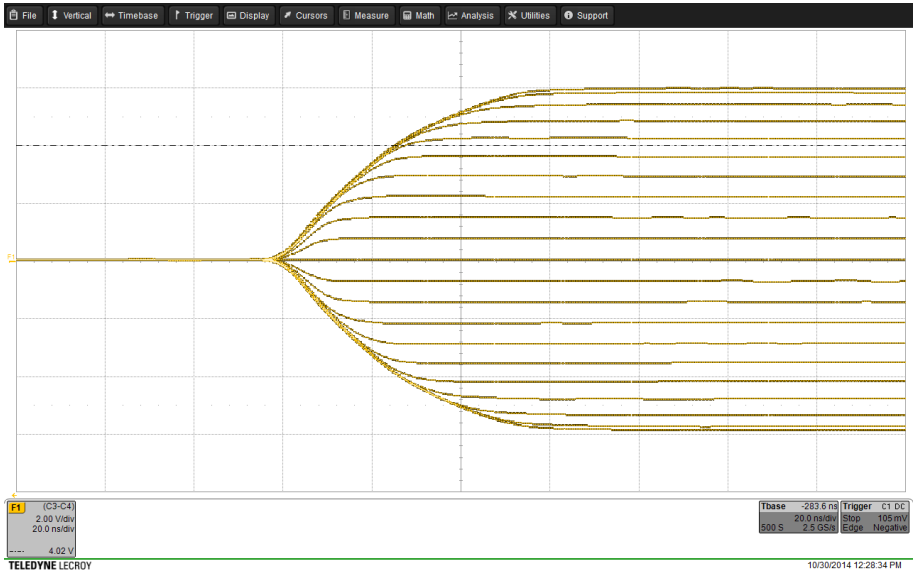
Overall response - 2.5us pulse

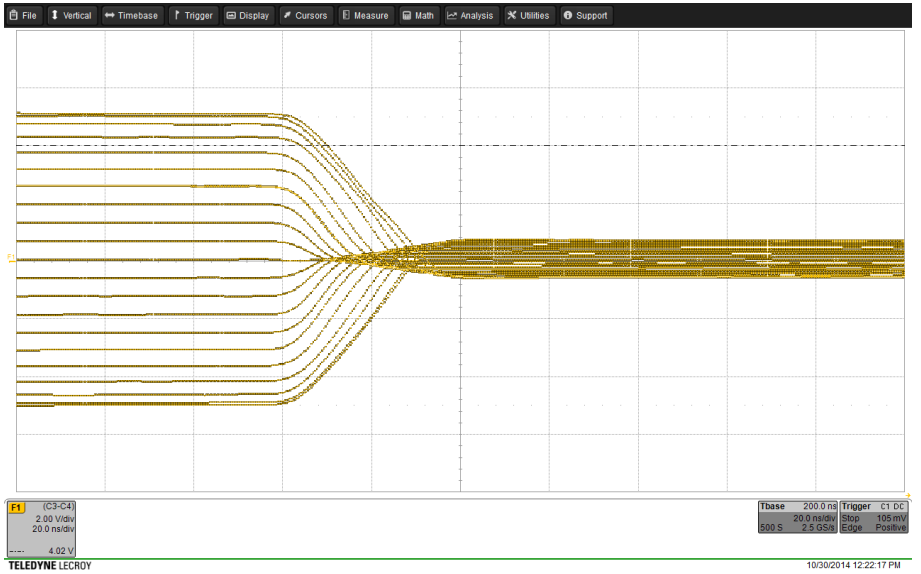
(500ns/div)



Effects of slew-rate limiting - slower response at large amplitudes

leading edge... *(20ns/div)* *...and trailing edge*

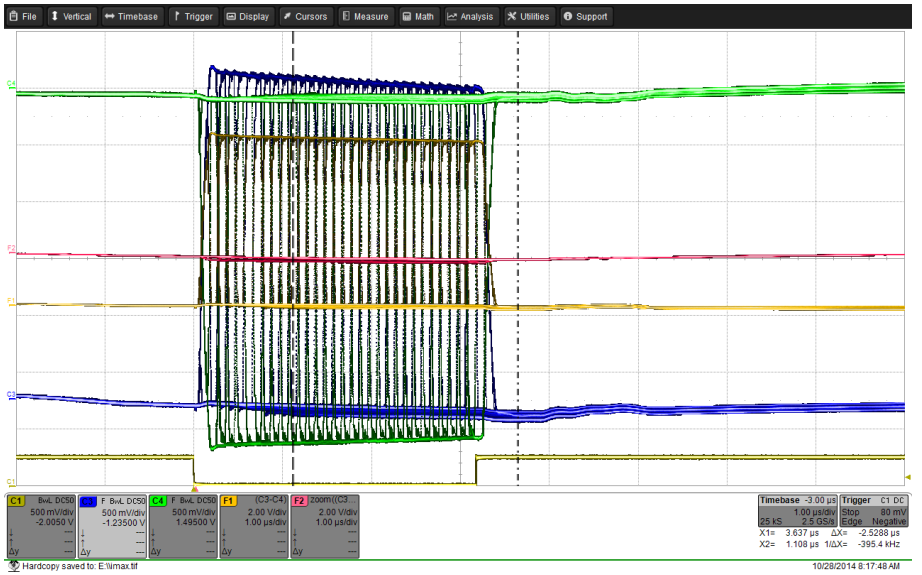




... and curiosities

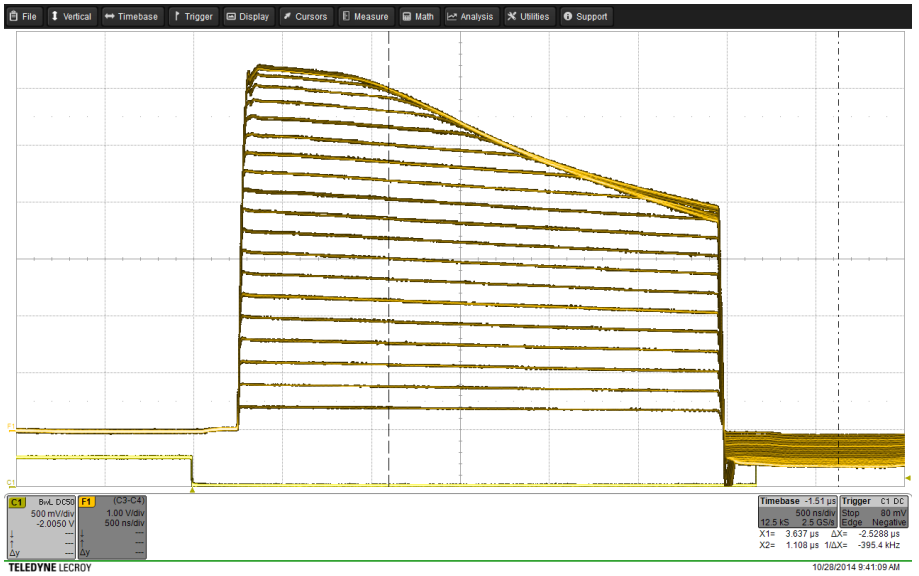
Short pulse at different delays - showing drop in gain of amplifier due to transient heating of FETs

(green and blue are outputs)



(1us/div)

What happens with inadequate high voltage and output coupling capacitance...



(500ns/div)

First Version: Main Issue

ISSUE: got only half the output expected

- could have got a *bit* more than we did: it needed more time to set up optimally

ANSWER: change in Si MOSFET spec just before buying the parts...

- headline data:

WAS:	**15A**	**0.3ohm**	**200W**
BECAME:	**9A**	**0.2ohm**	**75W**

- maximum drain current rating (NB not actually usable to these currents):

WAS:	**90A**
BECAME:	**54A**

- I had never seen seen the spec of an estabished device reduced in this way
- apparently, it was a completely new device
  - presumably designed to be roughly equivalent in its intended applications
  - but otherwise only vaguely similar

Sent to CTF3 as urgently wanted, but forced to go to a second version using parallelled FETs

what they did to my FETs....

DE150-201N09A
RF Power MOSFET

nt Mode

Ξ Applications

ıs	Maximum Ratings	
	200	V
; R_{GS} = 1 MΩ	200	V
	±20	V
	±30	V
	15.0	A
dth limited by T_{JM}	90	A
	3.0	A
	7.5	mJ
IA/µs, $V_{DD} \le V_{DSS}$, 2Ω	-	...

WAS...

V_{DSS}	=	200 V
I_{D25}	=	15 A
$R_{DS(on)}$	≤	0.2 Ω
P_{DC}	=	200 W

Note the RF package of this device...

...IS

IXYS

N-Channel Enhancement Mode
Low Q_g and R_g
High dv/dt
Nanosecond Switching
Ideal for Class C, D, & E Applications

DE150-201N09A
RF Power MOSFET

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	200	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	200	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_c = 25°C	9	A
I_{DM}	T_c = 25°C, pulse width limited by T_{JM}	54	A
I_{AR}	T_c = 25°C	9.0	A
E_{AR}	T_c = 25°C	7.5	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100A/µs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 0.2Ω	5	V/ns

V_{DSS}	=	200 V
I_{D25}	=	9 A
$R_{DS(on)}$	≤	0.3 Ω
P_{DC}	=	75 W

First Version: Other Issues

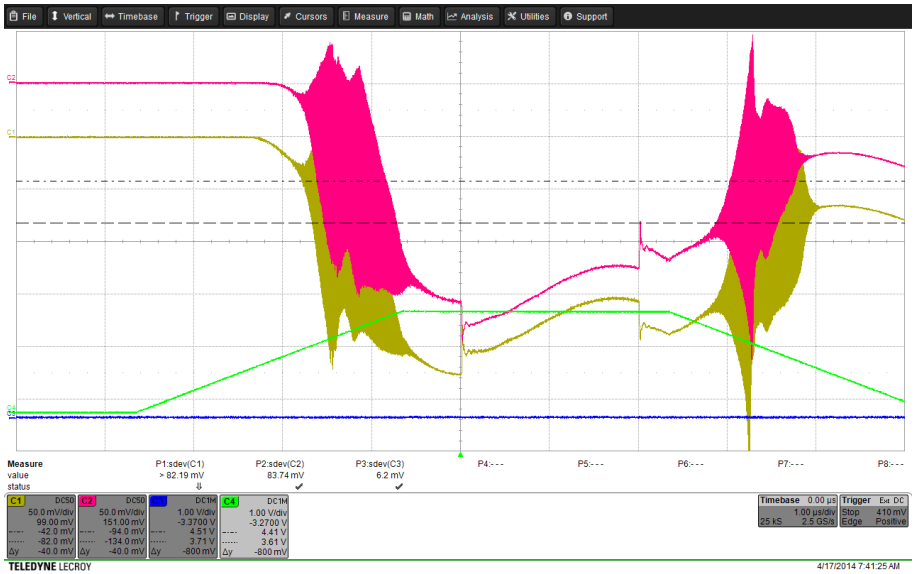
- instability, in particular common mode
    - around 10MHz
    - supressed by adding damping resistors across transformer
        - highest value giving stability was found
        - then value reduced to half to ensure a margin
- also occasional at 200 to 300MHz
    - seemed of little consequence, and more or less went away

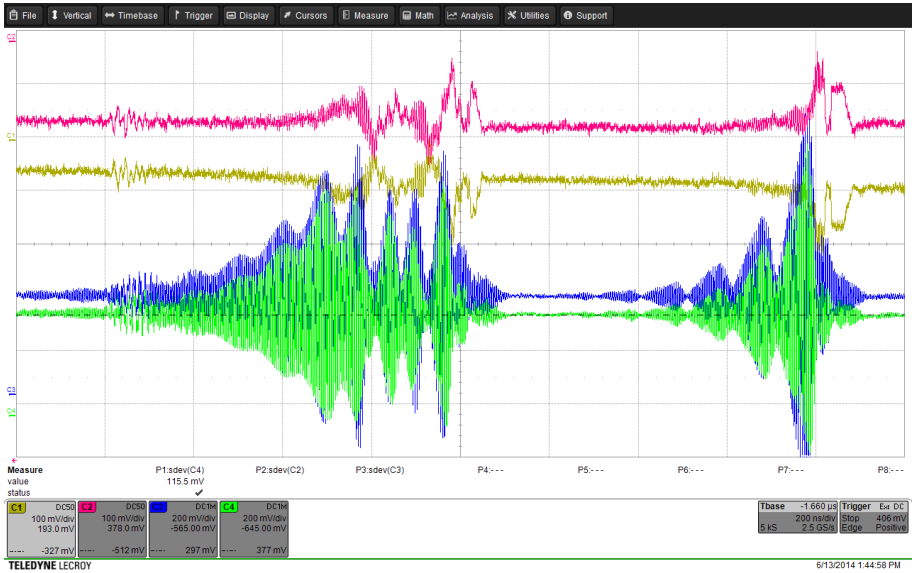
- ceramic output capacitors (and on hv rail) lost a lot of capacitance under voltage
- the 1000V X7R dielectric caps were about 20% of nominal at 600V...
    - commonplace with other types, but a surprise for X7R
    - observation, and manufacturer's data (when you dig it out - not in datasheets) agree
- reduces available swing (and output) towards end of pulse
    - in effect, wastes some of the supply voltage...
- fix was to stack capacitors on the pcb
    - 2 or 3 on top of each other
    - sufficient, given low output of module

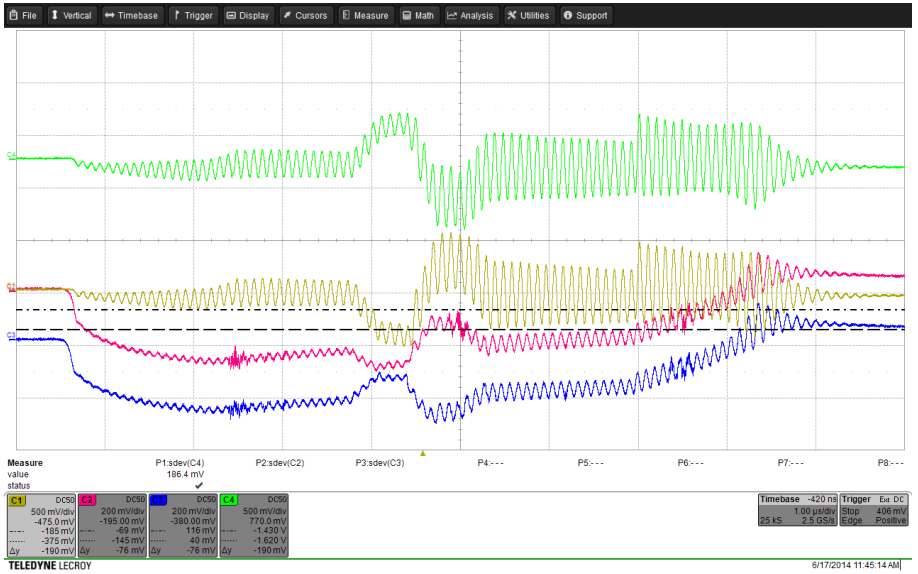
- transformer leakage inductance was a bit high
    - gave unwanted swings on output from unintended common-mode drive to output stage
    - didn't matter too much, because of the reduced output possible...

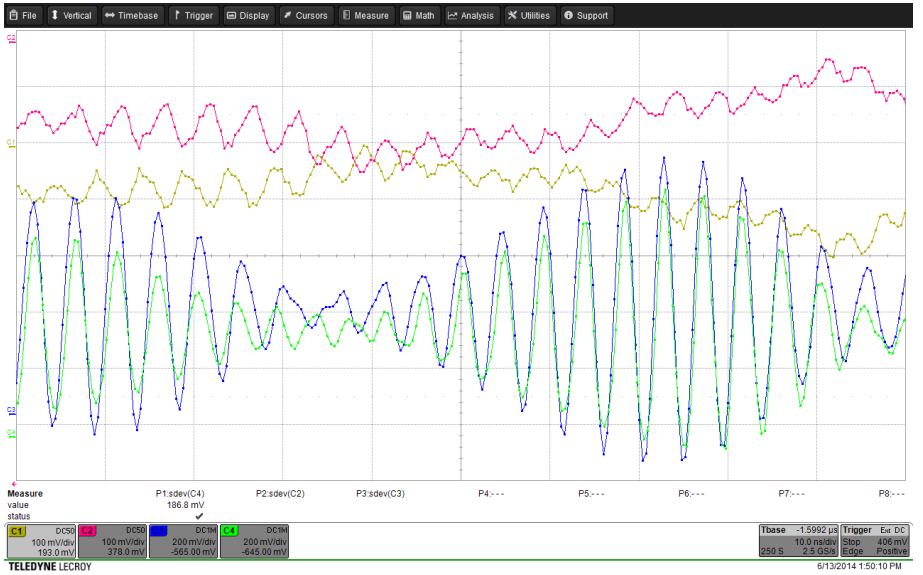
version 1 horrors...

A gallery of unpleasantnesses observed during development...









FET Tests

- extensive tests were made of the FETs and alternative types

- showed parallelled Si FETs were essential to get the target output

- showed that the SiC FET was *probably* enough for full output, but a bit marginal
    - ok when cold, but would be limiting at the end of a maximal length pulse

- transient thermal heating tests clarified (and resolved inconsistencies in) device data sheets
    - looked just ok
    - would force reduced output to be safe, for pulse lengths longer than ~2us
    - needed to adjust control module to ramp current up and down faster

- as expected, high temperature performance of the SiC devices looked exceptional
    - transient temperature taken safely well above datasheet maximum
    - but not tested to destruction!

- there is an expectation of some thermally-induced non-linear behaviour
    - not likely to be significant (or even detectable) in the context of CTF3
    - but would have to be characterized and allowed for in a CLIC amplifier

Second Version

- had to change to parallelled Si MOSFETs to get current

- decided to also change SiC FETs to a next generation device, and parallel pairs
    - this was to improve HF performance
        - and it reduced the amount of drive limitation needed at high frequencies
    - parallelling (smaller) devices reduced the impact of package lead inductance

- also changed the transformer
- found how to wind one on a toroidal core (63mm diameter)
    - not entirely easy: the conformable coax is rather stiff and springy
- decided to use try this construction
- conclusion: there was not a lot to choose, electrically or mechanically, between the two

- loss of capacitance of ceramic output caps was compensated by adding film caps
    - needed to avoid loss of output by end of pulse
    - also some on hv

- pcb had made provision for parallelling pairs of output FETs (being cautious!)
- but not all the stability issues involved had been considered
- modification to the pcb and various kludges in assembly allowed for most of these

Second Version (...cont)

- control module needed slight changes
    - timing had to be changed to guard against transient overheating
        - this needed a few component changes
        - it was outside the range of the trimmer adjustments
    - slew rate limitation was also reduced
- other deficiencies were tolerated: it would have needed a revised pcb to make improvements

- some protection circuits in the amplifier and control modules were enabled
    - it was clear the amplifier would be more vulnerable to faults

Only limited tests of amplifier module were done - urgently wanted at CTF3!

- output: ~+/-700V (ie design target)

- risetime/bw: 7.5ns/47MHz small signal (with 20% overshoot)

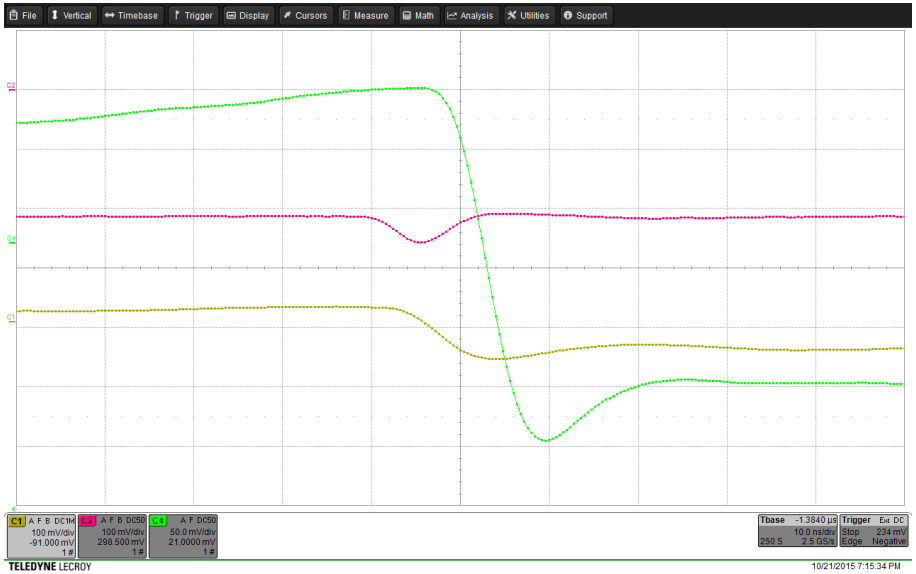
- slew rate: closely followed a 25ns risetime input giving swing from 0 to 650V

In system should give <30ns from zero to maximum output (10% to 90%), and less overshoot

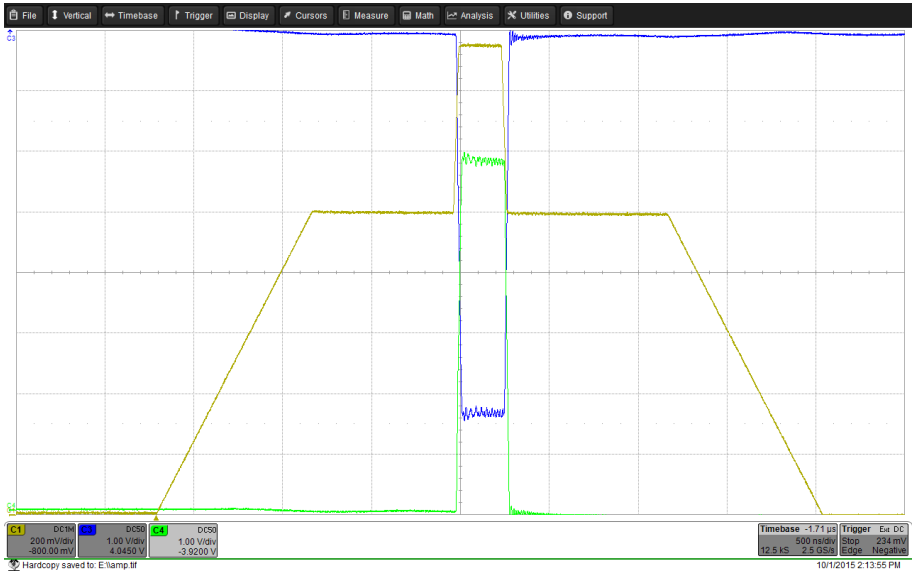
version 2 response...

A few shots grabbed as evidence that it was working...

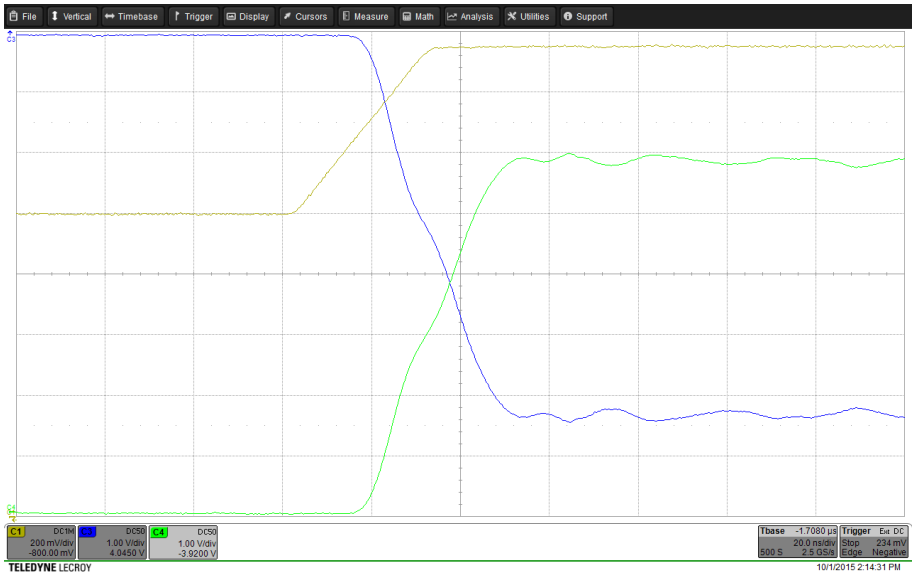
Small signal step response
(test signal not flat-topped)
7.5ns risetime



Full design output: *(10ns/div)*
700V into each side of load



Following a 30ns ramp to max output *(20ns/div)*



Second Version: Instability

- major problems with instability (despite precautions in parallelling devices)

- general issues:
    - the risk of achieving only marginal stability with no ill effect on performance
        - ok, but risk of changes (or a new build) giving marginal instability instead
    - changes to improve one mode often made another worse
    - difficulty of trying to patch stabilizing components onto the pcbs
        - and even worse, to keep changing them...

- worst: common mode instability
    - damping as used in the first version was not sufficient
        - reduced transformer leakage inductance made instability worse
        - new transformer still better than original for other reasons
        - something halfway between might have been best, but too hard to change...
    - supression required adding negative common-mode feedback
    - from the drain voltage monitoring networks to after the gain-setting trimmers
    - phase compensation required, and empirically adjusted
    - had to slightly impair this stabilization to avoid aggravating another instability
    - particularly messy to do, needing ~12 components plus patch wires adding to board

- oscillation at reduced supply voltage
    - around 70MHz
    - not directly affecting operation, but a worrying sign of marginal stability
    - mitigated (sufficiently?) by adding 4 damping resistors across inductors

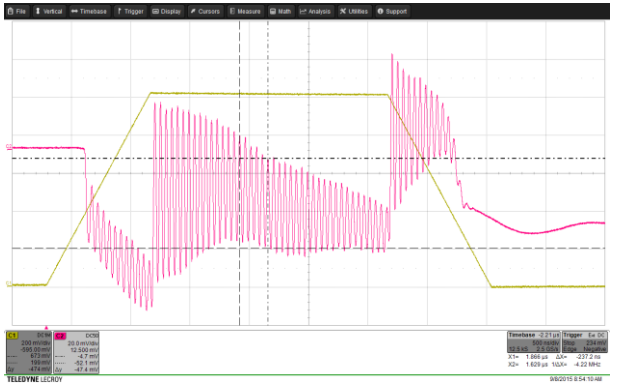
Second Version: Instability (...cont)

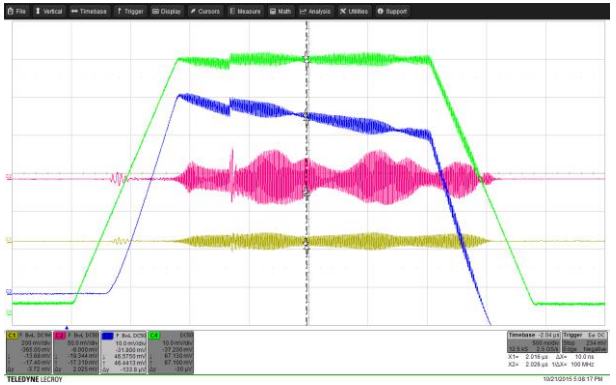
- apparent low-level, lightly damped ringing
    - appeared to have two independent sources of fractionally different frequencies
    - visible as 'beats' in the tail after a fast step signal
    - never properly understood
    - level was insignificant
    - never became high level, or broke into oscillation
    - but no great confidence that it would not
- high frequency instability
    - occasionally seen (~200MHz) at low level
    - other changes seemed to supress this
- instability at low currents
    - severe instability occured at reduced operating currents
    - gave bursts of instability while ramping up to or down from operating current
    - high level, and unpleasant, though not directly harmful
    - other changes more or less entirely supressed this
- low level instability when driven near to maximum output (95%+)
    - never properly understood
    - slightly reducing quiescent current supressed this...
    - no certainty that this will not recur, with time or temperature..

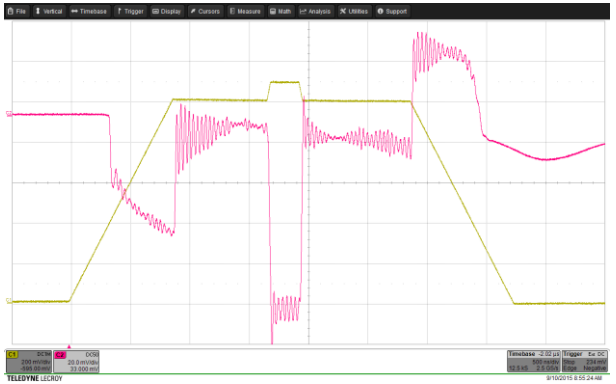
It has worked satisfactorily, but is clearly not in a suitable state for operational use, or even limited quantity production

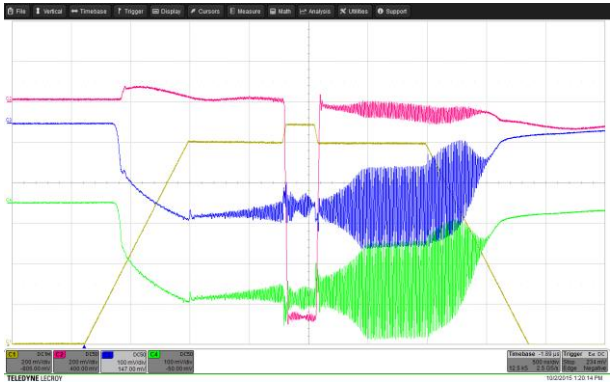
version 2 horrors...

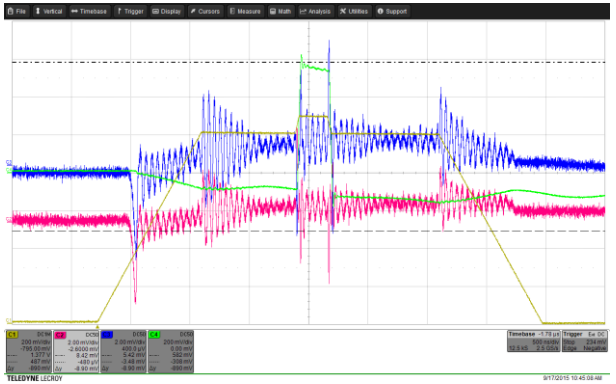
More unpleasantnesses during development...

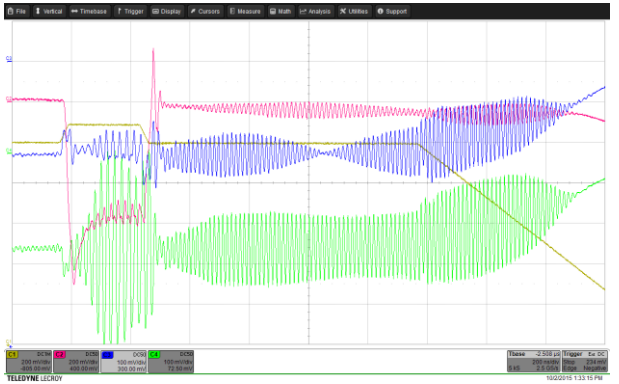






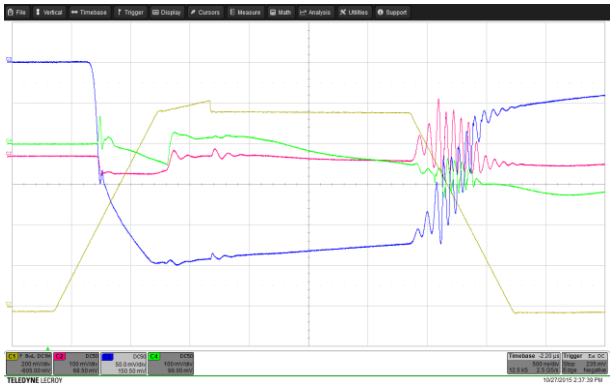


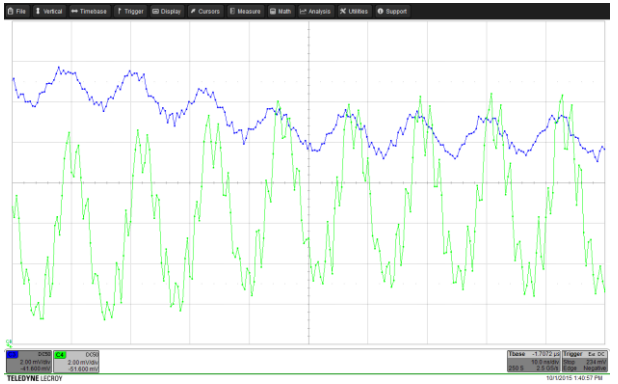


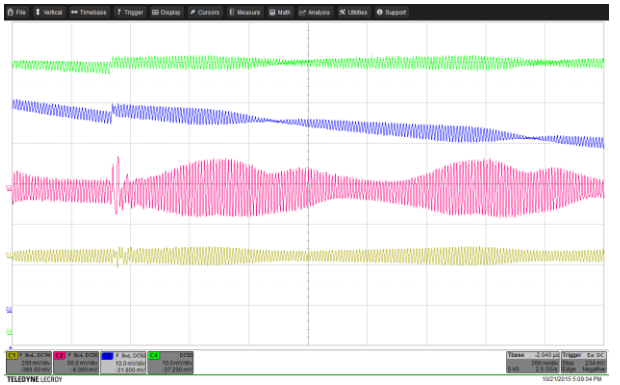


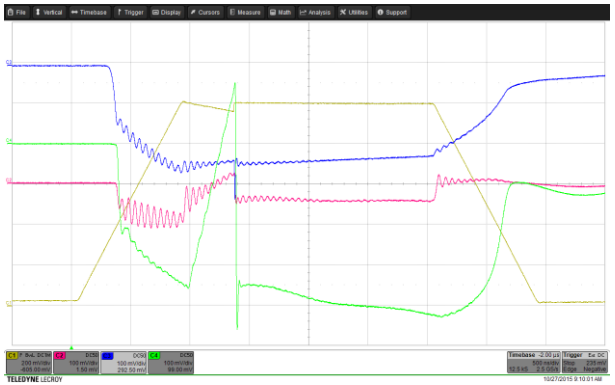
... and yet more

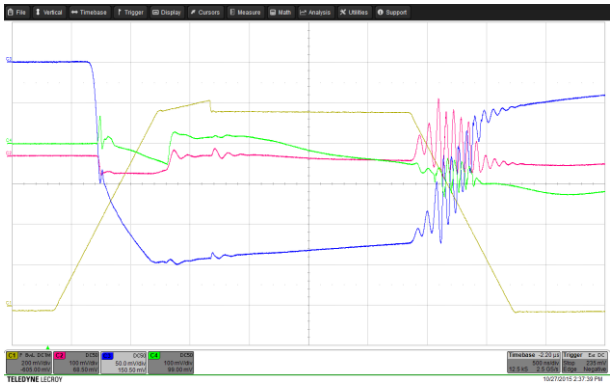
Still more unpleasantnesses...

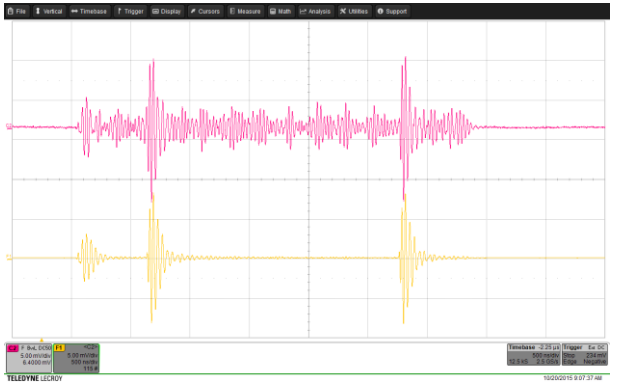


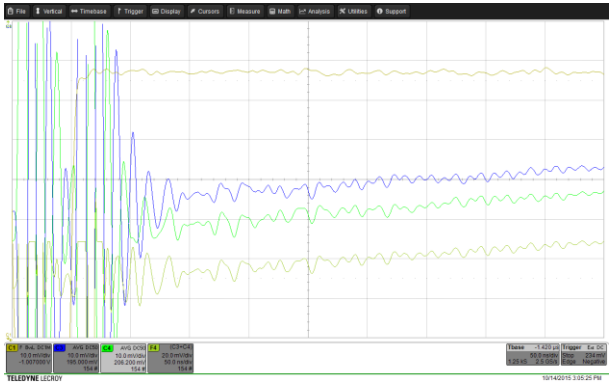


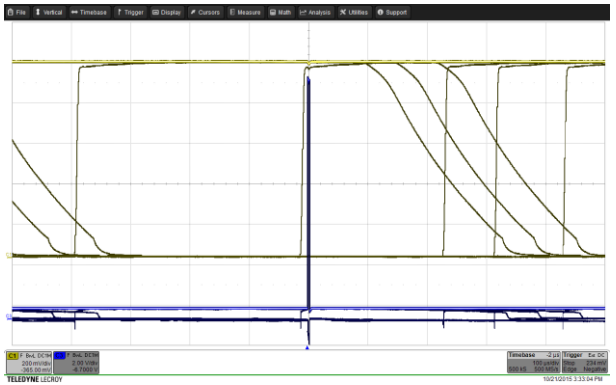


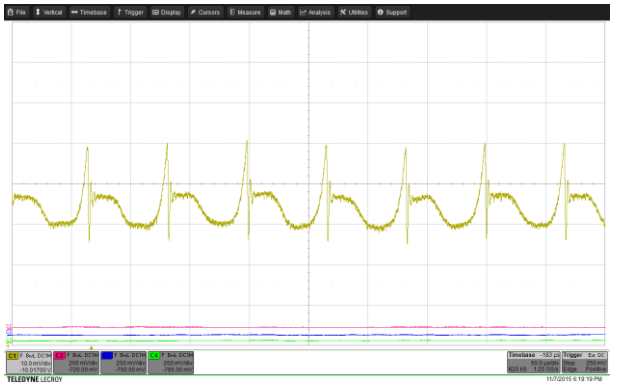












Prospects

- we have demonstrated that:

present commercial SiC FETs can make an amplifier module appropriate for CLIC

- but we have not demonstrated an acceptable degree of stability

- difficulties largely come from the lead inductances of inappropriate packages
    - no manufacture appears intesested in putting these sort of devices in RF packages
    - they are all concentrating on the very lucrative motor control/power conversion markets

- bare die are available, and their use ought to improve stability

- simulations suggest this should work - but the simulations are not very trustworthy...

Prospects - Going Forward

- it should be possible to adapt the present board to use bare die
    - die would be mounted on a small carrier board
- could also demonstrate a planar output transformer
    - preferred form for CLIC
    - performance sacrifices need to be shown acceptable

- if successful, it would justify proposing such an amplifier module for CLIC:
    - much higher power density and lower cost
        - 20kW peak in 20mm wide 3U high module
        - transformer fitting in this space
    - guess at cost: £300 system cost per module
        - inc racks, combiners, psus etc
        - assumes high volume, 5k+, production
    - qualification: it will still not drive full power at the highest frequencies

- it should take a reasonably modest effort
- be interested to try

- BUT: no guarantees!
    - some unfamiliar (to us) technology
    - possible (albeit unlikely) intractable stability issues