Analog & digital processing of detector signals

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Marie Curie EST Fellow

Project: Electronics, Acquisition and Controls Developments for Physics Experiments (ELACCO)

Supervisor: Jan Kaplon

A little introduction…

- 2005 - I finished my Masters in Nuclear Physics on AGH - University of Science and Technology in Krakow, Poland,
- 2005 - I started my PhD studies on the AGH-UST, Krakow, Poland,
- Since 2006 - I have been a Marie Curie Early Stage Training fellow at CERN.

Why have I applied for MC EST?

- To learn a new field: microelectronics,

My goals:

- To become experienced analog integrated circuit designer,
- To get the experience in experimental physics with particular emphasis on microelectronics,
- To collect materials for PhD thesis.

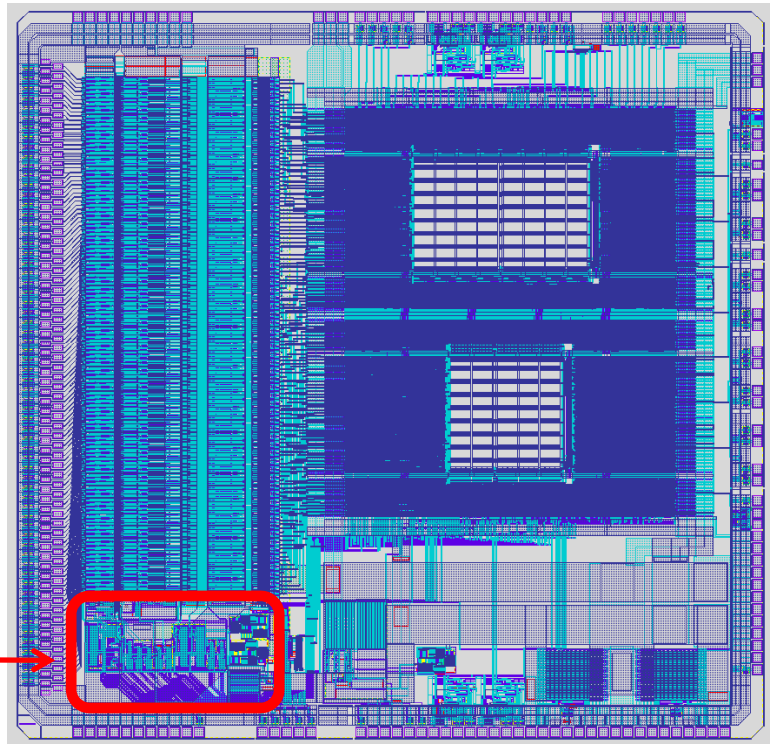
My work at CERN

- Design of the front-end electronics for the position sensitive silicon detectors in the SLHC experiments (ATLAS upgrade program),
- Design of the front-end electronics to read out the amorphous silicon sensors by using the Thin Film on ASIC (TFA) technology,
  - TFA technology is commonly used for solar cells and medical imaging,
  - The goal is to adapt this technology to high energy physics applications .

ATLAS Upgrade program

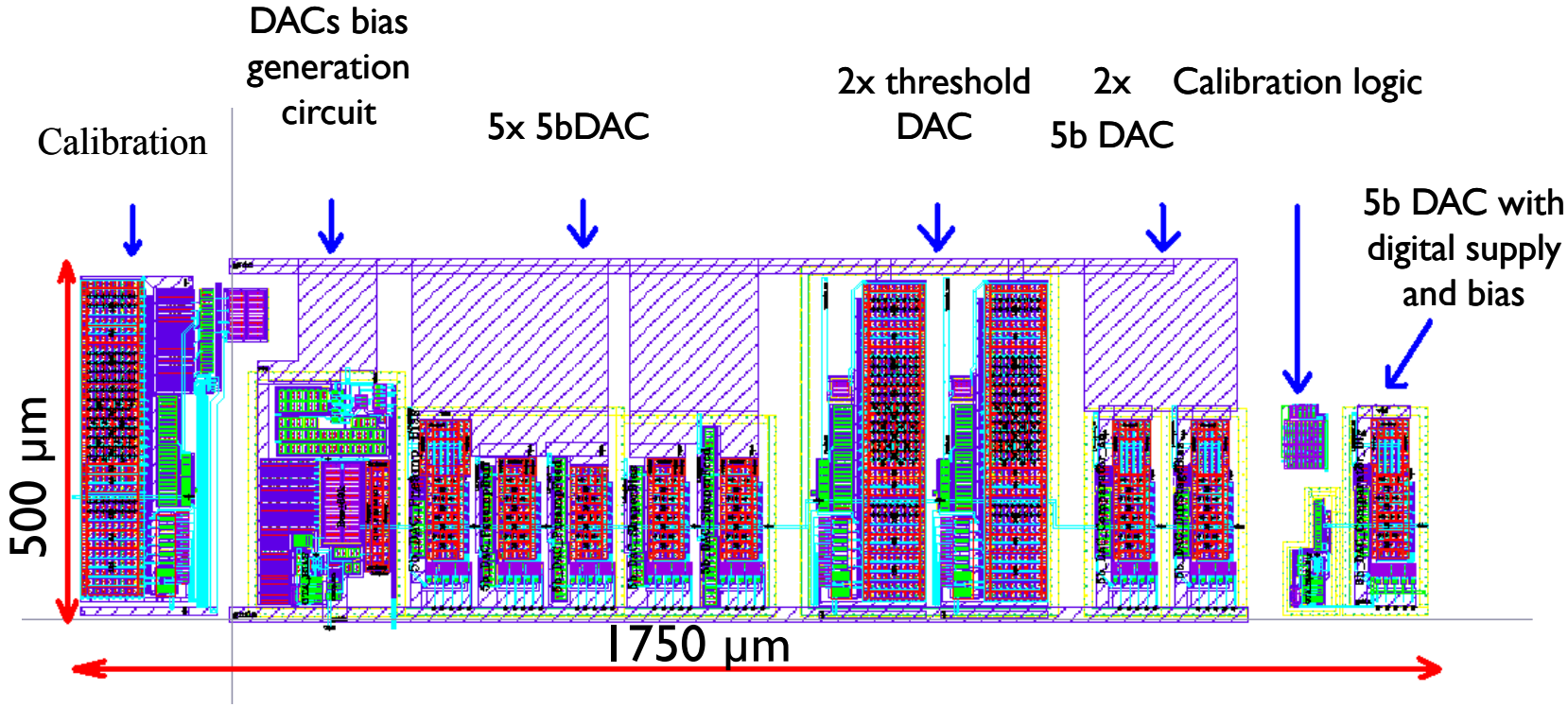
- The readout electronic for upgrade of ATLAS silicon strip detector was optimized, designed, and manufactured in 0.25 μm CMOS process,
- Main ABCN chip parameters:
  - Noise ≤ 750 e- RMS,
  - Gain: 100 mV/fC,
  - Input charges: 0.1-10 fC,
  - 128 channels,
- Designers team involves 10 people,
- My blocks:
  - Calibration circuit,
  - Digital-to-Analog Converters,
- The tests of the prototype chip are in progress.

ABCN chip



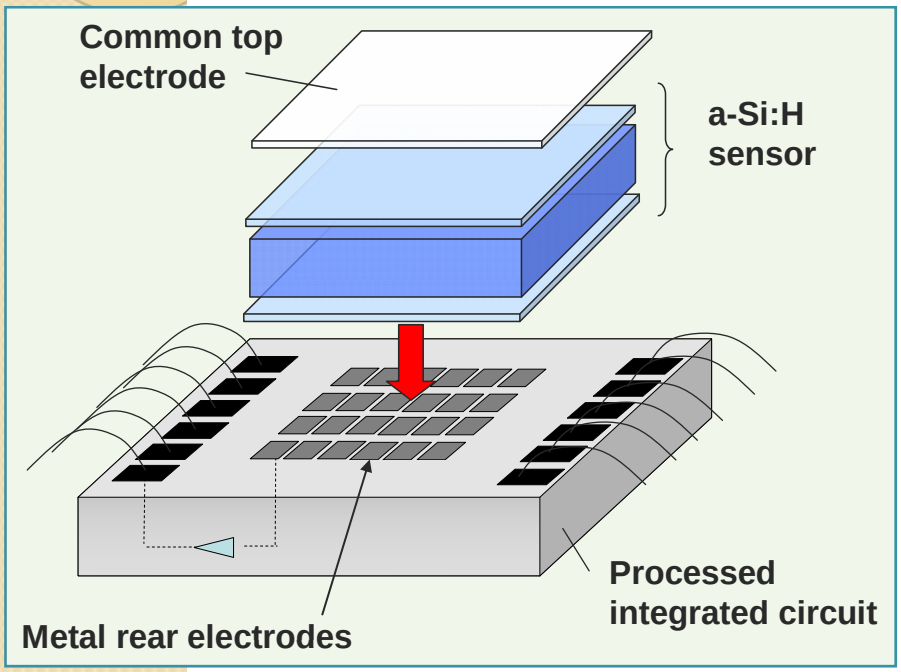
Calibration and DACs layout

Total number of DACs: 8x 5-bit DAC, 3x 8-bit DAC



- 4 calibration lines, each line is connected to every fourth front-end (FE) channels,
- 8 x 5-bit DACs to deliver switchable currents to the FE channels,
- 2 x 8-bit DACs to deliver switchable threshold values for the amplitude discrimination.

TFA – Thin Film on ASIC technology



→A thin film sensor layer is deposited directly on top of the ASIC,

→Sensors (p-i-n diodes) are made of hydrogenated amorphous silicon (a-Si:H),

→Full chip area is covered by the sensor layer,

→It does not require bump bonding,

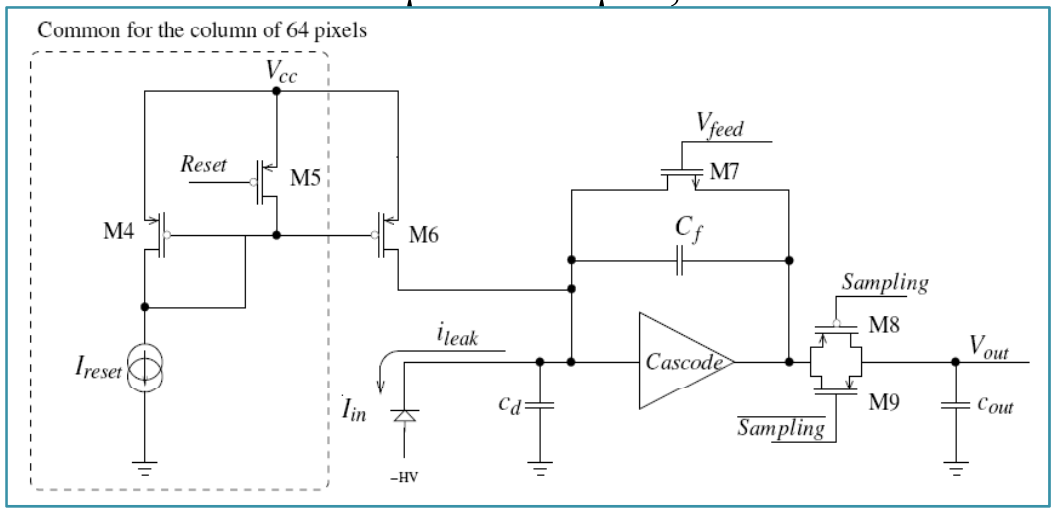
→Low deposition temperature (around 200 ºC) is compatible with post processing on finished electronics wafers,

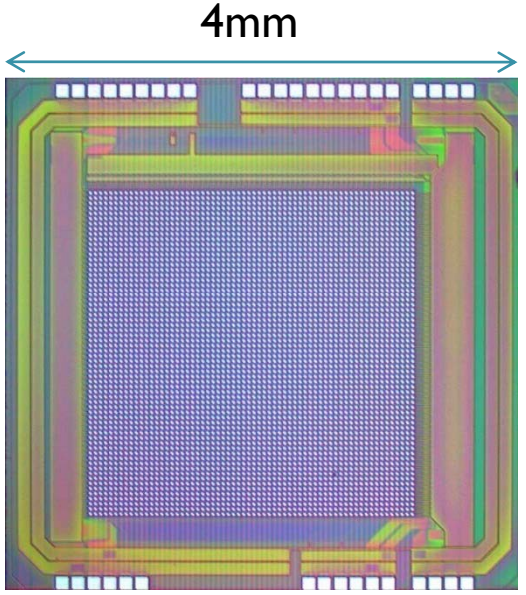
TFA: Applications and requirements

- Tracking detectors for linear colliders (short particle bunch; low repetition rate), imaging,
- Expected charges generated by MIPs: ~40 e-/μm,
- For 10-15 μm thick films of a-Si:H the expected input signals are 400-600 e-,
- Pixel dimension of the demonstrator chip: 40 μm x 40 μm, input capacitance ~40 fF (including detector capacitance),
- Requirements for front end electronics :
  - ✓ High gain (800 mV/fC), ideally in a single stage,
  - ✓ Low noise (< 30 e- ENC), to work with signal to noise ratio (SNR) ~12,
  - ✓ Low power consumption (10μW/pixel).

Amorphous Frame Readout Pixel (AFRP) chip

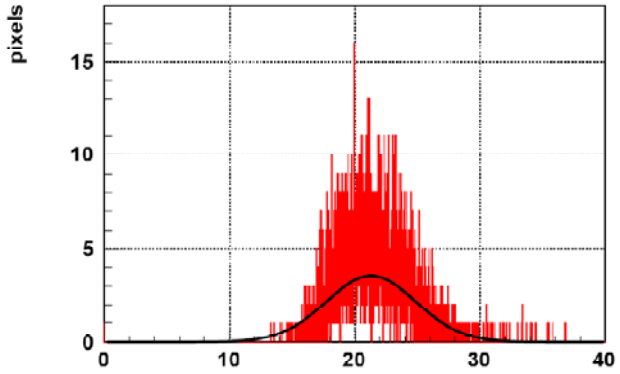
- Detailed noise calculations of the readout electronics,
- Optimisation of the preamplifier parameters,
- Schematic and layout design,
- The chip has been manufactured in 0.25 µm CMOS process,
- Matrix of 64 x 64 pixels,
- Pixel size: 40 µm x 40 µm,

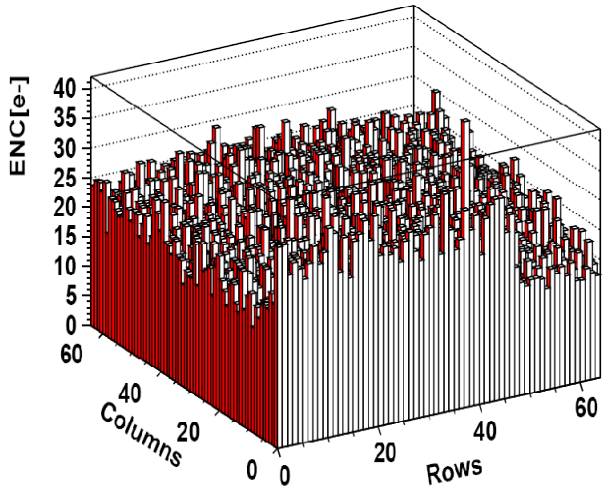




Measurements of the chip

- ✓ Setup:
  - NI PCI-6562 high speed digital input output card,
  - NI 5112 oscilloscope card,
  - Software made in Labview environment,
  - Analyses made in ROOT environment.
- ✓ Results:
  - The ENC averaged over all 4092 pixels is below 25e-,
  - The a-Si sensors will be deposited on the chip in coming weeks, then the final tests of finished TFA devices will be made,
  - It is expected that the 30 e- noise allows to detect MIP from 12 to 15 µm thick a-Si sensors with SNR of about 12.





Attended courses and trainings

- **Low-Noise Analog IC Design**, EPFL, Lausanne, Switzerland, 1 week, 2006
- **Low Power Low Voltage Analog IC Design**, EPFL, Lausanne, Switzerland, 1 week, 2007;
- **Integrated Circuit Front Ends for Nuclear Pulse Processing**, 2007 IEEE Nuclear Science Symposium and Medical Imaging Conference, Honolulu, US, 27.10.2007,
- **X-ray Micro Imaging of Devices, Materials and Organics**, 2008 IEEE Nuclear Science Symposium and Medical Imaging Conference, Dresden, Germany, 22 – 23.10.2008.
- General French course (110 hours),
- Academic Training Lecture Program at CERN.

Attended conferences

- 2007 IEEE Nuclear Science Symposium and Medical Imaging Conference, Honolulu, US, 28. 10 - 3. 11. 2007,
- 2008 IEEE Nuclear Science Symposium and Medical Imaging Conference, Dresden, Germany, 19 – 25. 10. 2008,
- Planned: 2009 SPIE Electronic Imaging Conference, San Jose, CA, USA, 18 - 22. 01. 2009 (http://spie.org/electronic-imaging.xml).

Presentations

- Abstract accepted for oral presentation at 2009 IS&T/SPIE Electronic Imaging Conference, San Jose, USA, 18 – 22.01.2009
  Low noise, low power front end electronics for pixelized TFA sensors,
  http://spie.org/electronic-imaging.xml
- 2008 Nuclear Science Symposium and Medical Imaging Conference, Dresder, Germany, 24.10. 2008
  Design and Noise Analysis of Charge Sensitive Amplifier for Readout of Pixelized Thin Film Amorphous Silicon Sensors,
  http://www.nss-mic.org/2008/NSSMain.asp,
- ATLAS Upgrade Tracker ABCN Final Design Review, CERN, 08.02.2008,
  Digital-To-Analog Converters and Calibration blocks,
  http://indico.cern.ch/conferenceDisplay.py?confId=23490,
- PH-ESE section meeting, CERN, 29.05.2008,
  Noise optimization of a charge sensitive amplifier with soft reset,
- PH-ESE section meeting, CERN, 18.06.2008,
  Overview of my work at CERN,
  http://ph-dep-ese-me.web.cern.ch/ph-dep-ESE-ME/archive2007.htm,

Publications

1. *K. Poltorak, et al.*
   Low noise, low power front end electronics for pixelized TFA sensors
   Abstract submitted for 2009 IS&T/SPIE Electronic Imaging Conference, San Jose, CA, USA (http://spie.org/electronic-imaging.xml)
2. *K. Poltorak, et al.*
   Design and Noise Analysis of Charge Sensitive Amplifier for Readout of Pixelized Thin Film Amorphous Silicon Sensors
   presented at 2008 Nuclear Science Symposium and Medical Imaging Conference, Dresden, Germany (http://www.nss-mic.org/2008/NSSMain.asp)
3. *K. Poltorak, et al.*
   The ABCN front end chip for ATLAS Inner Detector Upgrade,
   presented at TWEPP-08 Topical Workshop on Electronics for Particle Physics,
4. *A. Abdesselam, (K. Poltorak), et al.*
   Engineering for the ATLAS SemiConductor Tracker (SCT) End-cap.
   Journal of Instrumentation, May 2008, Vol. 3, P05003, doi: 10.1088/1748-0221/3/05/P05003; http://www.iop.org/EJ/abstract/1748-0221/3/05/P05002/
5. *A. Abdesselam, (K. Poltorak), et al.*
   The ATLAS semiconductor tracker end-cap module.
   Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 575, Issue 3, 1 June 2007, Pages 353-389, http://www.sciencedirect.com/science/journal/01689002

Thank you for your attention.