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## SILVACO BASED ELECTRO-THERMAL ANALYSIS OF 4H-SIC TIV-JFET STRUCTURE UNDER EXTREMELY HIGH CURRENT DENSITY RESISTIVE SWITCHING

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Electro-thermal analysis of SiC power semiconductor devices is crucial for its suitability in high power pulsed application. The relative stability of the threshold voltage and the absence of surface conduction in a Trenched and Implanted Vertical JFET (TIV-VJFET) structure gives it an inherent advantage over SiC MOSFETs especially in high current density pulsed applications like high voltage DC - DC converters, high voltage laser power supply and other pulsed power circuits. Technology Computer Aided Design (TCAD) modeling of SiC power semiconductor devices provides a simulation-based approach to predict and understand device behavior under extreme electrical conditions. In this research, a 2D model of a 1200 V 4H-SiC TIV-JFET cell structure was designed and simulated using Silvaco ATLAS TCAD software to investigate and understand the effects of extremely high current density pulsed switching on the device characteristics. The JFET cell was designed for an active area of 2 µm<sup>2</sup> and a threshold voltage of -7 V. Physics - based models were included to account for impact ionization, recombination effects, band gap narrowing, mobility and lattice heating. The electro-thermal simulation was performed using a resistive switching circuit at an ambient lattice temperature of 300 K. The circuit was designed for an ON - State drain current density of 5000 A/cm<sup>2</sup>. The device was simulated using a 100 kHz 50% duty cycle gate signal consisting of four switching cycles considering the simulation time bottleneck. The analysis of lattice temperature profile revealed the formation of thermal hot spot in the channel area close to the gate P+ regions in the JFET structure. Further analysis showed an increase in the minority carrier concentration in the vicinity of the gate implants which affected the switching characteristics of the JFET at extremely high current density.

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