Tailoring High-Voltage, High-Current Thyristors for Very High Frequency Switching

Howard Sanders and John Waldron
Silicon Power Corporation
Malvern, PA, USA
howard_sanders@siliconpower.com

Many applications exist requiring high voltage switching in the tens of kilohertz rates with peak currents at the thousands of amps and blocking voltage capabilities greater than several kilovolts. High-voltage, high-current thyristors provide low forward voltage and high peak current rating versus active area but suffer from long recovery times. Optimizing the thyristor for high di/dt capability also allows for tailoring the device to achieve faster recovery. Using these devices we have developed a compact thyristor based switch module capable of achieving greater than 20 kHz pulse rates using only a single low voltage, low power trigger. In present form the module is designed for a maximum blocking voltage of 7.5 kV and a peak current of 3 kA. However, this concept could be easily used to generate higher voltage switches using more devices in series. Also, higher current devices are in development which would increase the peak current rating to 14 kA without a significant increase in the size of the module. This paper will discuss the tailoring of the thyristor, the design of the switch module, and test results showing fast turn-on of greater than 100 kV/µs and 25 kA/µs as well as recovery times of less than 10 µs.

Keywords—thyristor; high-frequency; pulsed-power

I. Background

Several high-voltage, high di/dt, thyristor based switches have been demonstrated. Previously, these switches were used in low frequency applications where the pulse rate was on the order of 120 Hz or less. There are two possible approaches to reducing the time between these events, which we will call the recovery time.

Because thyristors rely on conductivity modulation to achieve low conduction losses, the excess carriers generated during conduction must be extracted before the device can support voltage. Thyristor recovery time can be shortened by supplying a negative bias to the gate relative to the cathode. The negative gate bias diverts carriers otherwise attracted to the cathode to exit the device through the gate. When the excess carriers exit through the gate terminal injection from the top junction ceases and the thyristor begins open base turn-off, similar to the workings of an IGBT. However, most systems require implementing several devices in series. Systems comprising of 10's of devices in series are not uncommon; supplying isolated gate drive power and closely timed gate signals to each level becomes complex and costly. In order to create viable, robust solid state solutions to vacuum tube based technology another path for high frequency applications is required.

As an alternative, the thyristor can be designed and post fabrication tailored to meet a specific application. Instead of actively removing the excess charge created during conduction, the system relies on the natural recombination of carriers at a rate relative to the device's high-level lifetime. To increase the maximum operating frequency of a thyristor requires shortening the charge carrier lifetime of the device. Consequently, the reduction of charge carrier lifetime reduces the common base gain of the lower transistor, increasing the conduction loss of the device. This reduction in lifetime can be implemented in several ways, however, the key to optimizing the device is reducing the charge carrier lifetime in a way to obtain the most favorable recovery time vs. conduction loss tradeoff.

In addition to the conduction loss/frequency capability trade off, the simplicity and power consumption of the gate drive circuit must be considered. In high di/dt application simultaneous triggering of each device in a series stack becomes crucial. Elimination of individual gate drive signals and power supplies for each series level greatly improves the cost, size, simplicity and robustness of the gate drive design.

We demonstrate a prototype device operating at 20kHz. The system was enabled through careful design of the thyristor's vertical doping profile and cellular geometry. These physical design parameters are geared to maximizing the impact of charge carrier lifetime killing on frequency capability while maintaining low conduction losses.

II. Device Design

A. Cell Structure

The thyristor design is based on standard 4-layer NPNP thyristor design using standard IC foundry capabilities to achieve 15 micron cells with 5 micron spacing. [1] This increases the cell density by a factor of 2000 from 50 cells/cm^2 on a standard thyristor to 100,000 cells/cm^2. Fig. 1 shows an example wafer layout and cell structure. A proprietary process is used to increase breakdown voltage which allows for a shallow boron diffusion into the P region as devices do not require a bevel to increase breakdown voltage.

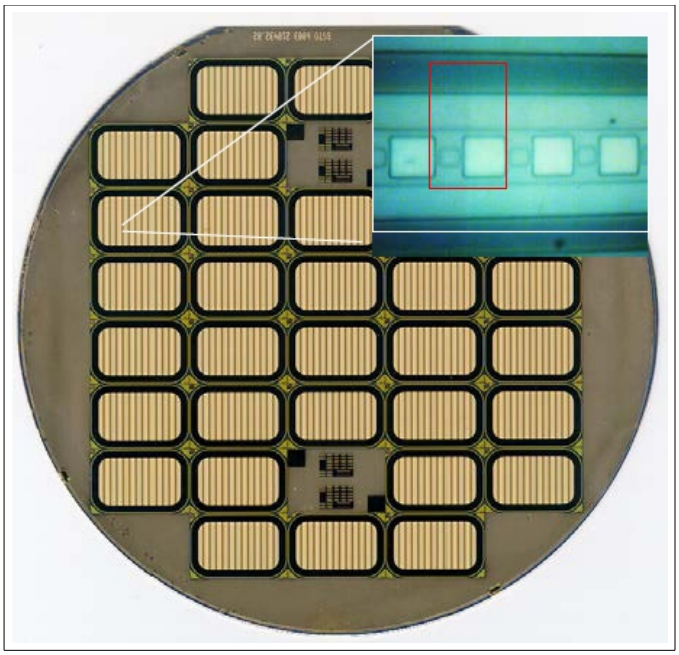


Fig. 1. Example wafer layout and cell structure

The results of this design is a lower forward drop attributed to the thyristors's exceptional upper transistor, measuring 1.7 V at 400 A and 18.5 V at 10 kA. Also, the thryristor achieves a higher di/dt capability attributed to the high cell density with near simultaneous turn-on, with tests achieving greater than 100 kA/µs. With gate-turn-off (GTO) the device achieves higher turn-off capability, up to twice the current of a standard GTO of the same size, again with nearly simultaneous turn-off of the cells.

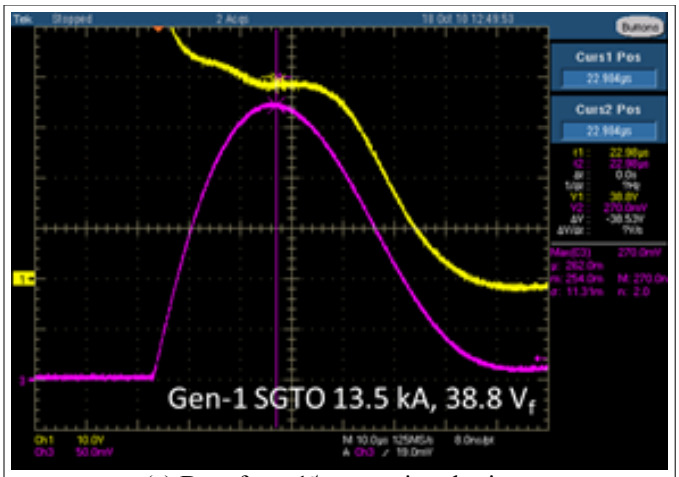
B. 2nd Generation Devices

This design has been further improved in a 2nd Generation device (Gen-2) increasing the capability of the Super-GTO in terms of lower forward voltage drop at higher peak current. This is accomplished by changing the cell design to optimize cathode and gate surface area. Fig 2(a). shows the data for a 1st generation device while Fig. 2(b) shows the data for a 2nd generation device.

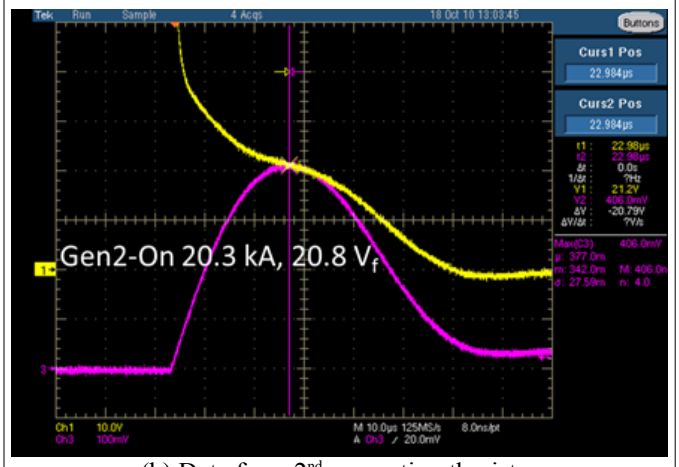
III. Test Results

A. Device Characterization

Four levels of modification, increasing from type B to Type E, were examined against an unmodified device, Type A, for on-state voltage drop. Fig. 3 shows that the on-state voltage drop increased from 2.9 V to 4 V at 400 A. Leakage current increased from 10 nA to 90 nA. Minimum current required to maintain on-state increased from 5 mA to 200 mA.



(a) Data from 1st generation thyristor



(b) Data from 2nd generation thyristor

Fig. 2. Data from 1st and 2nd generation thyristors

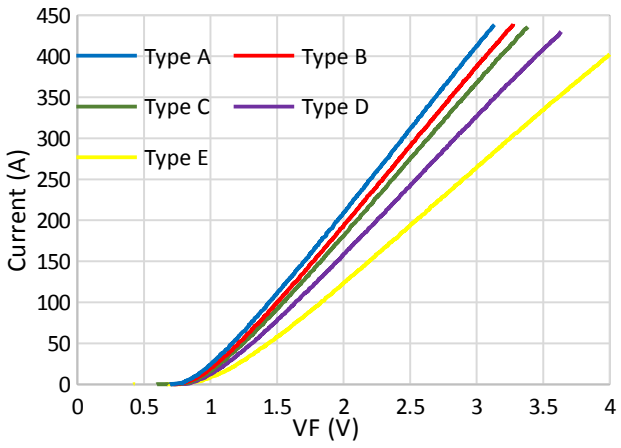


Fig. 3. On-state voltage drop

Under most circumstances it would not be desirable to increase on-state voltage, leakage current, and minimum current required to maintain on-state. However, pulsed power applications are not as dependent on these parameters. Turn-on

losses will be more significant than the on-state losses in the pulsed power time ranges of ≤10 µs. Balancing resistance used in parallel with devices in series will typically cause leakage currents > 100 µA. Higher minimum current required to maintain on-state allows for faster turn-off. Fig. 4 shows the difference in operation of the least and most modified versions in a pulsed-power circuit. The difference is less than 2% in power, a difference below the accuracy of the measurement. The circuit was 1.65 µF charged to 1375 V with 0.75 Ω and 20 nH circuit inductance.

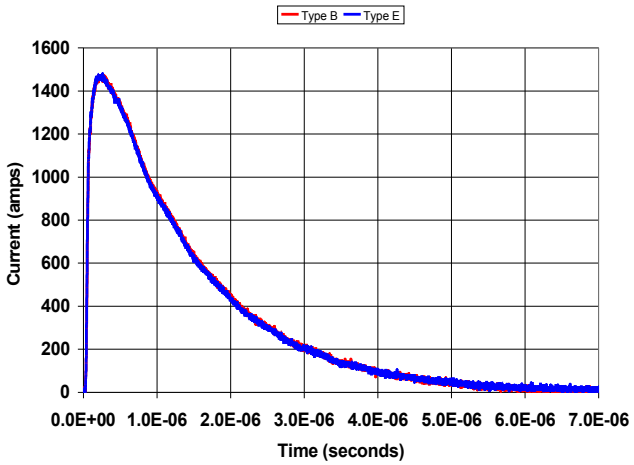


Fig. 4. Effect of on-state voltage drop in a pulsed-power circuit

B. Device Recovery

Fig 5 shows that device recovery improved from over 60 µs to under 10 µs. The advantage of faster recovery is allowing higher pulse repetition rates as well as reduced recovery losses. Fig. 6 shows operation at 20 kHz using a module consisting of multiple type E devices in series. Based on existing triggering techniques [2,3], the triggering can be achieved using a simple 15 V, 1 A pulse with no external power to the module.

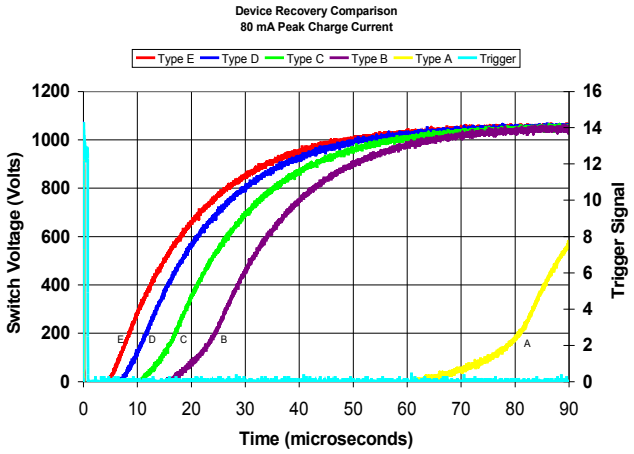


Fig. 5. Device Recovery

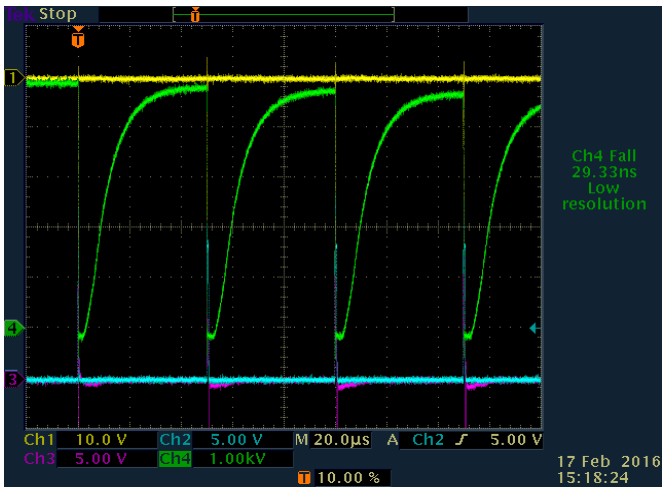


Fig. 6. 20 kHz operation, CH4 is voltage across the switch module; CH1 is load voltage (100:1 probe); CH2 is trigger voltage, and CH3 is load current

Fig. 7(a) shows the turn-on at better than 160 kV/µs or a fall time of less than 20 ns while Fig. 7(b) shows current rise time at over than 30 kA/µs.

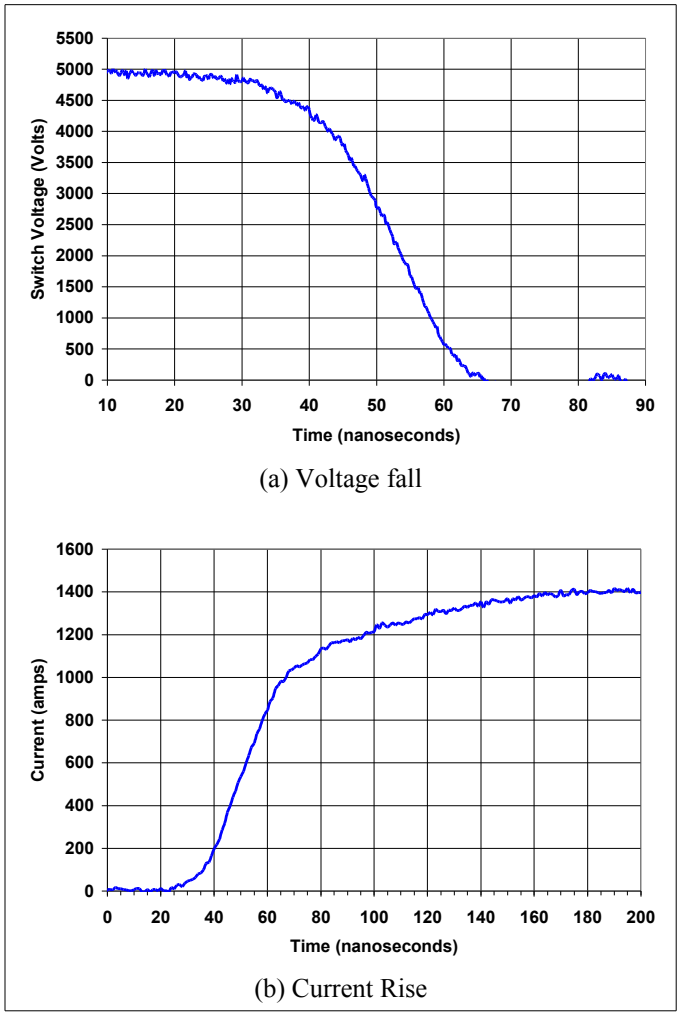


Fig. 7. Module turn-on performance

C. Module Specifications

Table 1 lists the various operation parameters of the module design. Fig. 8 shows the dimensions of the module. The module design as tested used five (5) thyristors in series. Capacitive and resistive voltage dividers are included in the package as well as trigger circuit with thermal interlock.

Switches with higher current rating can be achieved with only a small increase in module size. Switches with higher voltage rating can be achieved using more devices in series. Using these techniques, switches with current ratings to 20 kA and 60 kV have been developed [3] and with tailoring of the thyristor devices can achieve the pulse rates to 20 kHz.

TABLE I. MODULE OPERATIONAL PARAMETERS

Parameter	*Value*	*Unit*
Peak Voltage	7	kV
Peak Forward Current (1 μs)	3	kA
Peak Rate of Current Rise	30	kA/μs
Device Recovery Time (T_j = 25 ºC)	6	μs
Leakage Current (V_{AK} = 5 kV)	100	μA
Capacitance	50	pF

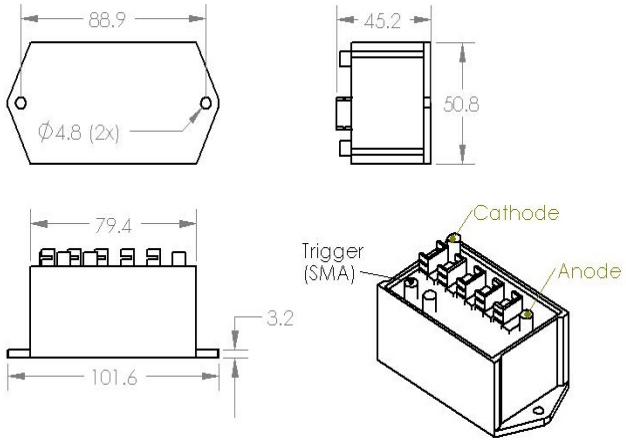


Fig. 8. Module Dimensions (in mm)

IV. CONCLUSION

The tailoring of thyristor devices achieves a device suitable for rate of voltage fall at turn-on of greater than 100 kV/μs as well as rate of current rise at turn-on of greater than 25 kA/μs while achieving a recovery time of less than 10 μs. These parameters make the device suitable for operation at up to 20 kHz. A high voltage switch module with the capability of achieving high-current and high-voltage switching for pulsed power applications has been design, manufactured and tested using these modules.

REFERENCES

[1] Temple, V., et al. "2 nd Generation Si and SiC SGTOs for extreme pulse power and sub-microsecond switching." in *2013 19th IEEE Pulsed Power Conf.*, San Francisco, CA, 2013, pp. 1-6

[2] S. C. Glidden, and H. D. Sanders, "Solid State Spark Gap Replacement Switches," in *Pulsed Power Conf.*, Monterey, CA, 2005, pp. 923-926

[3] H. Sanders, et al., "Thyristor based solid state switches for thyratron replacements." in *Power Modulator and High Voltage Conf.*, San Diego, CA, 2012, pp. 335-338