HV Energy Dosing dc-to-dc Converter in PWM Mode

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***Abstract*— Energy-dosing (ED) topology is effective for capacitor charging and long- flat-top pulse generation. The inherent advantages for these applications are high efficiency and excellent predictability. ED converter power is proportional to the switching frequency f_s. Thus, strict realization of ED is possible only when the output is frequency-regulated. At light loads, f_s might become unacceptably low. Then Pulse Width Modulation (PWM) becomes necessary. This paper develops theory of operation of ED converters in PWM mode. Duty cycle corresponding to a predefined load is calculated, which is sufficient to predict the converter state after any transition. All possible scenarios have been covered and verified with PSpice simulations and experiments with HV converters.**

Keywords—high voltage converter, energy dosing, frequency modulation, pulse width modulation, zero-current switching, prediction

I. Introduction

Energy-dosing (ED) topology was shown to be effective for capacitor charging and long- flat-top pulse generation (see [1]-[3] and their bibliography for examples of implementation and for the theory of operation). The inherent advantages for these applications are zero-current switching and excellent predictability following from the ED principle of operation. As the term ED implies, the output power is proportional to the switching frequency f_s. Thus, strict realization of ED is possible only when the output is frequency-regulated.

The theory of operation of energy-dosing converter (EDC) at what we term as frequency mode (FM) is described in [1]. In this mode, the switching frequency, f_s, in a normalized form, is equal to or lower than

$$f\left(V_{load}, E\right) := \frac{1}{\left[\frac{2}{\pi}\left(\frac{1}{2}\,acos\left(\frac{V_{load}}{V_{load}-E}\right)+\frac{E}{2V_{load}}\cdot\sqrt{1-\frac{2V_{load}}{E}}\right)\right]} \qquad (*)$$

where E is the rail voltage, and both the rail voltage and the load voltage, V_{load}, are referenced to the same side of the transformer. Then Zero-Current Switching (ZCS) is ensured.

On the base of (*), a predictive algorithm enabling forming flat pulses at exceptionally fast transitions and high power was formulated and tested elsewhere [3]; it is limited to FM.

Some low-power operating scenarios cannot be met in FM if the conversion frequency needs to be kept above certain value, e.g., because of the audibility constraints. Such scenarios can be realized with relay (hysteretic) control or Pulse-Width Modulation (PWM). The latter is desirable in view of better output quality, although the transistor losses increase considerably.

This paper extends theory of operation of ED converters into the PWM mode. Full set of equations is derived for calculation of duty cycle corresponding to a predefined load. All possible scenarios have been covered and verified with PSpice simulations and experiments with HV converters. Thus, this paper paves way to implementing prediction similar to that used in FM.

II. EDC in Normal Mode (FM)

We will need the equations for FM mode as a starting point for the PWM analysis. A simplified schematic diagram of an EDC is shown in Fig. 1, and its full and reduced equivalent circuits (EC) and correspondent timing diagrams are shown in elsewhere [2-3]. We neglect here rail/busbar voltage oscillations and the FWD forward drop on the discharged capacitor. Most important, we neglect also all parasitic capacitances including that of the secondary. We assume that the load voltage does not change much during a half-period of the conversion frequency; then the storage capacitor can be represented by a counter EMF equal to the load voltage. These and other assumptions are detailed in [2-3].

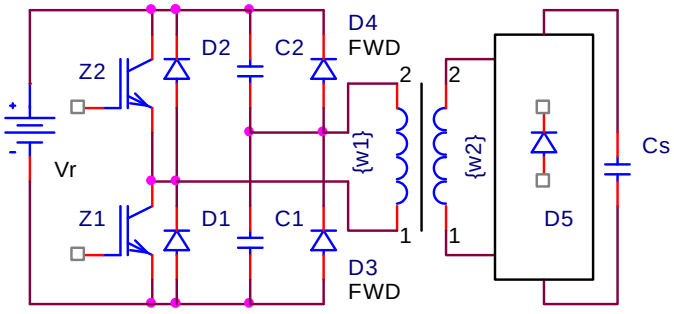

Fig. 1. Half bridge inverter with energy dosing capacitors.

The operation of EDC in FM is described in [1] for both steady-state and charging mode. We will reiterate this analysis to some extent here. All variables and parameters are referenced

to the secondary. Usually, parameters in lowercase are dimensionless, whereas uppercase denotes dimensional parameters. The equivalent circuits (EC) are not reproduced here.

The inductance L current and the resonant capacitor C voltage before t_1 are

$$i_1 = \frac{V_r - V_L}{\rho}\sin\omega t\,, \quad v_1 = (V_r - V_L)\cos\omega t + V_L\,, \tag{1}$$

where $\omega = \frac{1}{\sqrt{LC}}$, $\rho = \sqrt{\frac{L}{C}}$, and V_r, V_L are rail and load voltage, respectively. Moments t_1 and t_2 are given as

$$t_1 = \frac{1}{\omega}acos\left(\frac{v_l}{v_l - 1}\right)\ t_2 = t_1 + \frac{1}{\omega v_l}\sqrt{1 - 2v_l} \tag{2}$$

The winding current at moment t_1 is found from (1) by substituting t_1:

$$i_{1t1} = \frac{V_r}{\rho}\sqrt{1 - 2v_l} \tag{3}$$

Here $v_l = V_L/V_r$ is normalized load voltage. *It can change from zero (short circuit) to ½ (maximum voltage).* Since the load voltage changes little during half-period, it be set as a constant. Thus, it serves as a parameter and not a variable.

With this assumption, the energies transferred to the load in a half- and full period are, respectively

$$W_{hp} = V_L\int_0^{t_2} i\,dt,\ W_p = 2W_{hp}. \tag{4}$$

Obviously, for FM they are

$$W_{hp} = C_d V_{r1}^2,\ P_{pwm} \le P_{FM} = 2W_{hp}f = 2C_d V_r^2 f,$$

where C_d (subscript d stands for capacitive "divider") is the capacitance of the resonant capacitor (C1 and C2), and V_{r1} is the rail voltage measured at the primary side. Power generated in PWM, P_{pwm}, can be only less than that, P_{FM}, in FM.

III. PWM Mode

Our goal is finding duty cycle (DC) corresponding to a predefined load. Contrary to FM, the load cannot be defined in terms of power only; both the power and load voltage have to be specified.

In the following analysis, all variables and parameters are reflected to the secondary side of the transformer.

We assume that at the beginning of a half-period the resonant capacitors are charged to a voltage $V_0 \le V_r$. *No longer is their voltage swing always equal to V_r, as in FM,* which complicates the analysis considerably. We will make use of timing diagrams Fig. 2 and their notation to render the analysis as transparent as possible.

The gate shut-off time is designated as t_c (chopping moment). It can occur any time within $0 < t_c \le t_2$ (t_2 is the time of natural ZCS). There are three possible scenarios:

Case 1. Capacitor voltage v_c does not fall to zero at both t_c and T_{ei} (T_{ei} denotes current zero).

Case 2. Chopping occurs before t_1 (t_1 is moment when v_c falls to zero), but v_c reaches zero before the current does.

Case 3. Chopping occurs after t_1.

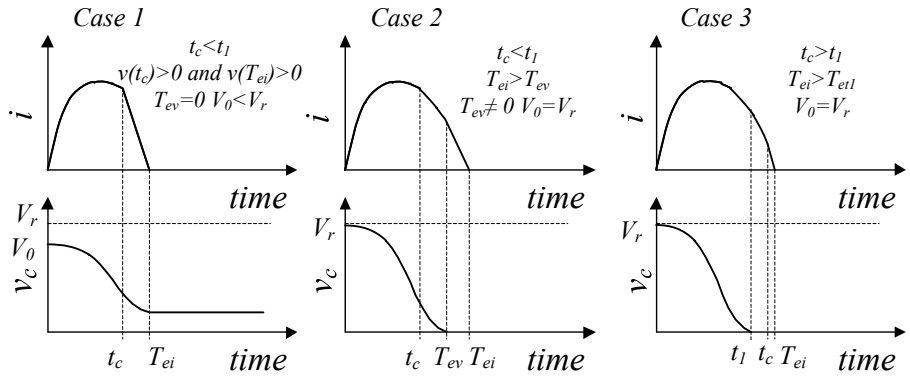

Fig. 2. Timing diagrams of EDC in PWM mode.

We note that diagrams Fig. 3 were derived from experimental observations and circuit simulations.

In steady state, voltage v_c must satisfy the periodicity condition (here and further a Mathcad notation is used):

$$V_r\cdot(1 - v_0) = v_c\left(\frac{T_1(v_l)}{2}, t_c, v_l, v_0\right) \tag{5}$$

where $v_0 = V_0/V_r$, and $T_1/2 = t_2$ is the current pulse duration in FM:

$$T_1(v_l) := \frac{2}{\pi}\left(\frac{1}{2}acos\left(\frac{v_l}{v_l - 1}\right) + \frac{1}{2v_l}\cdot\sqrt{1 - 2v_l}\right)\cdot T\,,\quad T := 2\pi\sqrt{L\cdot C}\,.$$

Thus, for Case 1, $V_r/2 < V_0 < V_r$, and for Cases 2, 3, $V_0 = V_r$.

In PWM mode the output is regulated by changing t_c at a constant conversion frequency. Operating in terms of energy per half-period, rather than power, we rewrite (4) as

$$W_{hp} = \mathrm{V_L} \int_{\mathrm{o}}^{\mathrm{Tei}} \mathrm{idt}, \text{ or}$$

$$w_{hp}(t_c, v_l, v_0) := \frac{V_r \cdot v_l}{W_{hptmax}} \cdot \int_0^{\frac{T_1(v_l)}{2}} i_c(t, t_c, v_l, v_0)\, dt \qquad (6)$$

where $w_{hp}=W_{hp}/W_{hpmax}$ is normalized energy; the quantity

$$W_{hpmax} = C_d V_{r1}^2 \qquad (7)$$

is the maximum energy that can be supplied to the load in a half-period. Assigning

$$W_{hp} = W_{hpt}, \text{ or } w_{hp} = w_{hpt} \qquad (8)$$

and solving system (5), (8) for t_c, v_0, we find t_c, or duty cycle, necessary to provide the *targeted energy* W_{hpt}. The initial state V_0 is for reference only.

Prior to t_c, the operation of an EDC can be described by modified equations (1) recognizing that C can be charged to V_0 rather than V_r. Thus, the inductance L current and the resonant capacitance C voltage before t_1 are given as:

$$i_1 = \frac{V_0 - V_L}{\rho} \sin \omega t\,,\ v_1 = (V_0 - V_L)\cos \omega t + V_L\,, \qquad (9)$$

The winding current at moment t_1 is found from (9) by substituting t_1 from (2):

$$i_{1t1}(v_l, v_0) := \frac{V_r}{\rho} \cdot \sqrt{v_0 \cdot (v_0 - 2v_l)} \qquad (10)$$

After t_c, the EC transforms to that of Fig. 3. (The values are irrelevant.) This EC is actually valid for all the three Cases if we recognize that the current switches to the FWD3 (capacitor clamping diode) after the resonant capacitor C1 has discharged to zero. Full analysis of all possible combinations has been performed. In this short paper, we provide only final equations and their selected solutions.

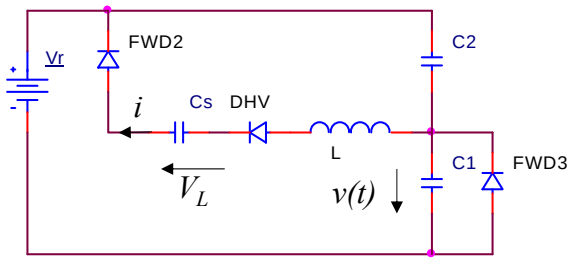

Fig. 3. Equivalent circuit with notation according to Fig. 1 after t_c. (FWD2 is parallel to transistor Z2, DHV stands for HV rectifier.) Current i is split equally between C1 and C2 if FWD3 does not conduct.

Starting from t=0 to the end of half-period, the voltage across the resonant cap v_c and the winding current i_c (all reflected to the secondary) are expressed by

$$v_c(t, t_c, v_l, v_0) := \begin{cases} v_1(t, v_l, v_0) & \text{if } t < t_c \\ \text{if } t > t_c \wedge T_{ev}(t_c, v_l, v_0) = 0 & \\ \quad \begin{cases} v(t - t_c, t_c, v_l, v_0) & \text{if } t < t_c + T_{et}(t_c, v_l, v_0) \\ v(T_{et}(t_c, v_l, v_0), t_c, v_l, v_0) & \text{otherwise} \end{cases} & \\ \text{if } t_c < t_1(v_l, v_0) \wedge t > t_c \wedge T_{ev}(t_c, v_l, v_0) \neq 0 & \\ \quad \begin{cases} v_2(t - t_c, t_c, v_l, v_0) & \text{if } t > t_c \wedge t \le t_c + T_{ev}(t_c, v_l, v_0) \\ 0 & \text{otherwise} \end{cases} & \\ 0 \quad \text{if } t_c > t_1(v_l, v_0) \wedge t > t_c & \end{cases} \qquad (11)$$

$$i_c(t, t_c, v_l, v_0) := \begin{cases} i_1(t, v_l, v_0) & \text{if } t < t_c \\ \text{if } \left(t > t_c \wedge T_{ev}(t_c, v_l, v_0) = 0\right) & \\ \quad \begin{cases} i(t - t_c, t_c, v_l, v_0) & \text{if } t < t_c + T_{et}(t_c, v_l, v_0) \\ 0 & \text{otherwise} \end{cases} & \\ \text{if } t_c < t_1(v_l, v_0) \wedge \left(t > t_c \wedge T_{ev}(t_c, v_l, v_0) \neq 0\right) & \\ \quad \begin{cases} i_{21}(t - t_c, t_c, v_l, v_0) & \text{if } t < t_c + T_{ev}(t_c, v_l, v_0) \\ i_{22}(t - t_c - T_{ev}(t_c, v_l, v_0), t_c, v_l, v_0) & \text{if } t > t_c + T_{ev}(t_c, v_l, v_0) \\ 0 & \text{if } t > T_{e2}(t_c, v_l, v_0) + t_c \end{cases} & \\ \text{if } t_c > t_1(v_l, v_0) \wedge t > t_c & \\ \quad \begin{cases} i_1(t - t_c, v_l, v_0) & \text{if } t > t_1(v_l, v_0) \wedge t < t_c \\ i_{t1}(t - t_c, t_c, v_l, v_0) & \text{if } t < t_c + T_{et1}(t_c, v_l, v_0) \wedge t > t_c \\ 0 & \text{if } t > T_{et1}(t_c, v_l, v_0) + t_c \end{cases} & \end{cases} \qquad (12)$$

Calculations were performed for a hypothetical EDC with the following parameters:

E=480 V, k_{tr}=50, $V_r=Ek_{tr}$, $V_L=V_r/2$, L=6 mH, C_d=2 μH.

Several examples of waveforms derived from System (5), (8) with voltage and current given by (11), (12) for different combinations of w_{hp} and v_l are given in Fig. 4. The V_r value is shown for reference to accentuate the v_c symmetry relative to rail.

We will normalize also the pulsewidth t_c:

$$t_{cn} = \frac{2t_c}{T_1} \qquad (13)$$

The base here is $T_1/2$, which is the current pulse duration in FM. Fig. 5 shows the pulsewidth versus energy per half-period, in both dimensional (for the above EDC) and non-dimensional forms.

We note that both t_c and t_{cn} values corresponding to w_{hpt}=1 were calculated straight from (6), because solution of (5), (8) does not converge well at w_{hpt}=1. Neither does it always converge around v_l=0.5 and very small w_{hpt} values. Using Fig. 5b (or its tabulated version) and basis values for a specific converter, we can calculate the actual pulsewidth (duty cycle).

We will give an example for the converter module described in [3]. Its rated power is 50 kW which can be generated in FM at f_s≈70 kHz at low line. In PWM, the converter operates at f_s=16 kHz. The converter state can be defined in terms of power

that is calculated as $P_{PWM} = 2W_{hp}f_s$. This module has L=1.33 mH, C_d=1.8 μF, k_{tr}=50, and the bases for it are E=480 V, $W_{hpmax}=C_dE^2$=0.415 J.

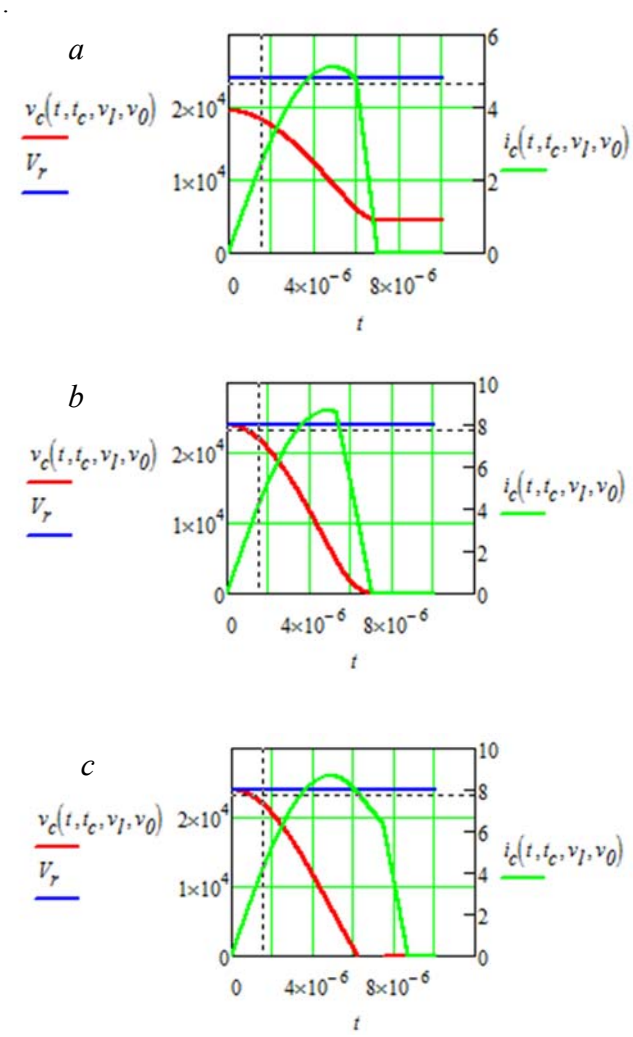

Fig. 4. Current and voltage waveforms (referenced to secondary) illustrating all three cases. Horizontal scale – time, s; vertical – voltages, V. a - Case 1: w_{hpt}=0.5, v_l=0.4, t_1=8.974 μs, t_c=6.02 μs; b - Case 2: w_{hpt}=0.6, v_l=0.3, t_1=6.239 μs, t_c=5.312 μs; c - Case 3: w_{hpt}=0.8, v_l=0.3, t_1=6.239 μs, t_c=7.509 μs.

An example of recalculation for dimensional variables using (13) is shown in Table 1. This information can be used in the following way. If the converter needs to transit abruptly from one state to another, e.g., from a lower voltage to a higher level, *prior* knowledge of DC in PWM mode (or f in FM) allows correct setting of the feedback circuitry, analog or digital, on the point of the transition. Thus, the developed equations, or more correctly, the tabulated results as Look-up-Tables, can serve for prediction of pulsewidth/DC in PWM mode.

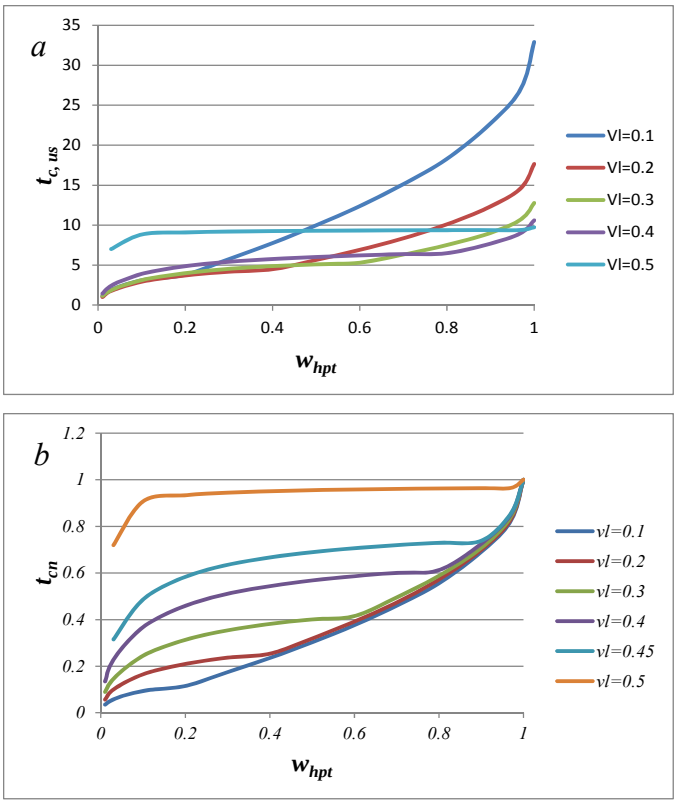

Fig. 5. Pulsewidth dependence on energy per half-period.

TABLE 1. DUTY CYCLE, D, VERSUS POWER WITH LOAD VOLTAGE AS PARAMETER.

	D, %					
P, W	v_l=0.1	v_l=0.2	v_l=0.3	v_l=0.4	v_l=0.45	v_l=0.5
133	0.82	0.71	0.82	1.02		
1328	2.22	2.09	2.24	2.79	3.48	6.31
2656	2.71	2.64	2.86	3.48	4.18	6.49
6640	7.12	4.03	3.66	4.30	4.93	6.64
9296	10.81	5.97	4.52	4.55	5.15	6.68
11952	16.24	8.82	6.46	5.49	5.28	6.71
13280	23.52	12.61	9.13	7.57	7.16	6.96

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